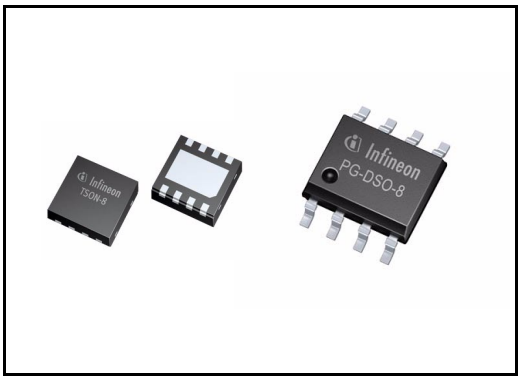
IFX1051

Industrial High Speed CAN-FD Transceiver



1 Overview

Features

- Compliant to ISO 11898-2
- Wide common mode range for electromagnetic immunity (EMI)
- Very low electromagnetic emission (EME)
- Excellent ESD robustness: 10 kV HBM
- Guaranteed loop delay symmetry to support CAN FD data frames up to 2 MBit/s
- Suitable for 12 V and 24 V applications
- V_{IO} input for voltage adaption to the microcontroller supply
- Extended supply range on V_{CC} and V_{IO} supply
- CAN short circuit proof to ground, battery and V_{CC}
- TxD time-out function with very long TxD time-out timing: ≥ 4.5 ms
- Low CAN bus leakage current in power-down state
- Overtemperature protection
- Protected against transients
- Receive-only mode
- Green Product (RoHS compliant)
- Two package variants: PG-DSO-8 and tiny PG-TSON-8

Applications

- Embedded Machine Control and Factory Automation (for example sensors and actuators)
- Building Automation (for example HVAC systems, automatic doors, sun blinds)
- Traffic Lights and Variable Message Signs (VMS)
- Elevator and Escalator applications
- Motor- and Motion-Control (for example renewable power generation: pitch control in wind power or sun-tracking in photovoltaic)
- any kind of CAN-application with the need of higher bandwidth

Description

The IFX1051 is a transceiver designed for HS CAN networks in industrial applications. Acting as interface between the physical bus layer and the CAN protocol controller, the IFX1051 drives the signals to the bus and protects the microcontroller against interferences generated within the network. Based on the high symmetry

of the CANH and CANL signals, the IFX1051 provides a very low level of electromagnetic emission (EME) within a wide frequency range.
The IFX1051 is available in a small, leadless PG-TSON-8 package as well as in a standard PG-DSO-8 package. The packages are RoHS compliant and halogen free and moreover support the solder joint requirements for automated optical inspection (AOI). The IFX1051 is fulfilling or exceeding the requirements of the ISO11898-2.
The IFX1051 provides a digital supply input V_{IO} that allows direct interfacing to 3.3 V microcontrollers and in addition offers a Receive-only mode.

One key feature of the IFX1051 is that it fulfills the enhanced physical layer requirements for CAN FD (CAN with Flexible Data Rate) and supports data rates up to 2 MBit/s. This allows the usage of the IFX1051 in networks using CAN FD protocol next to all industrial CAN applications using the classical protocol. CAN FD based networks offer a considerably increased bandwidth compared to classical CAN protocol because it allows increased data bitrate in combination with increased payload per message and thus making CAN FD a powerful and future-oriented alternative for all existing CAN applications whenever bandwidth limitations become an issue.

On the basis of a very low leakage current on the HS CAN bus interface the IFX1051 provides an excellent passive behavior in power-down state. These and other features make the IFX1051 exceptionally suitable for mixed supply HS CAN networks. In addition the IFX1051 provides excellent ESD immunity together with a very high electromagnetic immunity (EMI). Moreover the IFX1051 is equipped with a TxD time-out functionality which protects the CAN bus from being blocked if the transceiver receives by error a permanent low level signal on TxD from its controller. The implementation of this functionality with a very long delay timing of > 4.5 ms allows at the same time the usage of the device in physically very long bus networks as they can be found in many industrial applications.

The two different operating modes - Normal mode and Receive-only mode, its additional fail-safe features like TxD time-out but as well the CAN FD capability and optimized output slew rates on the CANH and CANL signals make the IFX1051 an ideal choice for large HS CAN networks with demand for high data transmission rates.

The qualification of this product is based on JEDEC JESD47 and may reference existing qualification results of similar products. Such referring is justified by the structural similarity of the products. The product is not qualified and manufactured according to the requirements of Infineon Technologies with regard to automotive and/or transportation applications. Infineon Technologies administrates a comprehensive qualify management system according to the latest version of the ISO9001 and ISO/TS 16949

The most updated certificates of the aforesaid ISO9001 and ISOTS 16949 are available on the Infineon Technologies webpage **http://www.infineon.com/cms/en/product/technology/quality/**

Type	Package	Marking
IFX1051LE	PG-TSON-8	1051LE
IFX1051SJ	PG-DSO-8	1051SJ

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2 Block Diagram

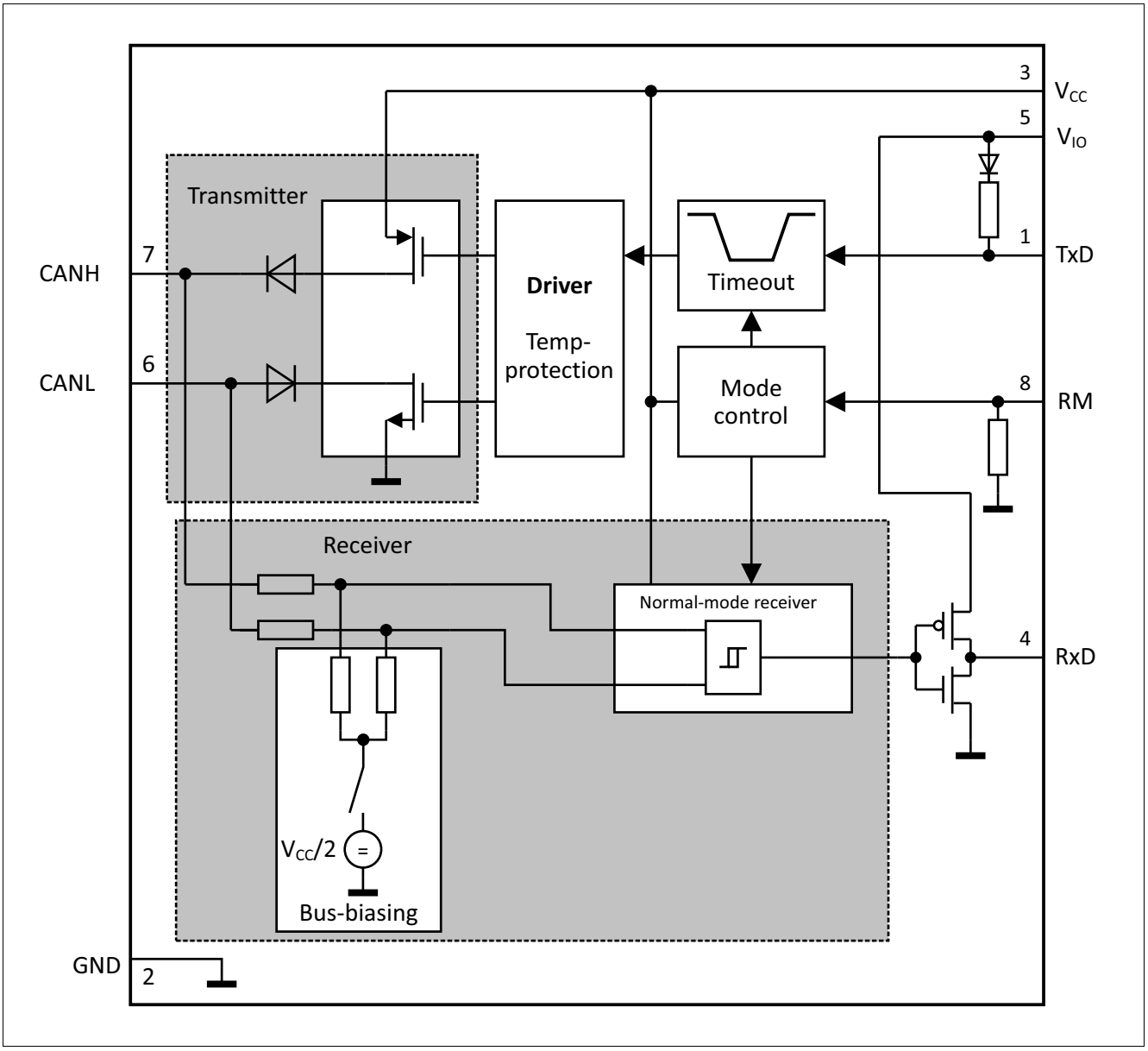


Figure 1 Functional block diagram

3 Pin Configuration

3.1 Pin Assignment

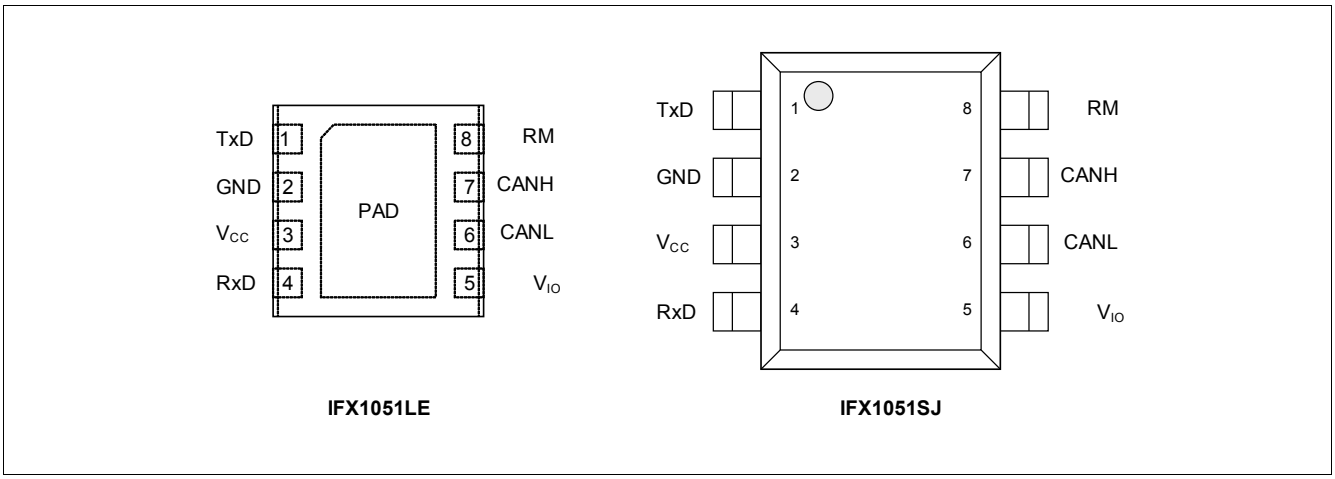


Figure 2 Pin configuration (top-side x-ray view)

3.2 Pin Definitions

Table 1 Pin definitions and functions

Pin No.	Symbol	Function
1	TxD	**Transmit Data Input;** internal pull-up to V_{IO}, “low” for dominant state.
2	GND	**Ground**
3	V_{CC}	**Transmitter Supply Voltage;** 100 nF decoupling capacitor to GND required.
4	RxD	**Receive Data Output;** “low” in dominant state.
5	V_{IO}	**Digital Supply Voltage;** supply voltage input to adapt the logical input and output voltage levels of the transceiver to the microcontroller supply, 100 nF decoupling capacitor to GND required.
6	CANL	**CAN Bus Low Level I/O;** “low” in dominant state.
7	CANH	**CAN Bus High Level I/O;** “high” in dominant state.
8	RM	**Receive-only Mode Input;** internal pull-down to GND, “low” for normal-operating mode.
PAD (IFX1051LE only)	–	Exposed Pad; Connect to PCB heat sink area. Do not connect to other potential than GND.

4 Functional Description

HS CAN is a serial bus system that connects microcontrollers, sensors and actuators for real-time control applications. The use of the Controller Area Network (abbreviated CAN) is described by the international standard ISO 11898. According to the 7-layer OSI reference model the physical layer of a HS CAN bus system specifies the data transmission from one CAN node to all other available CAN nodes within the network. The physical layer specification of a CAN bus system includes all electrical and mechanical specifications of a CAN network. The CAN transceiver is part of the physical layer specification. Several different physical layer standards of CAN networks have been developed in recent years. The IFX1051 is a High Speed CAN transceiver without a wake-up function and defined by the international standard ISO 11898-2.

4.1 High Speed CAN Physical Layer

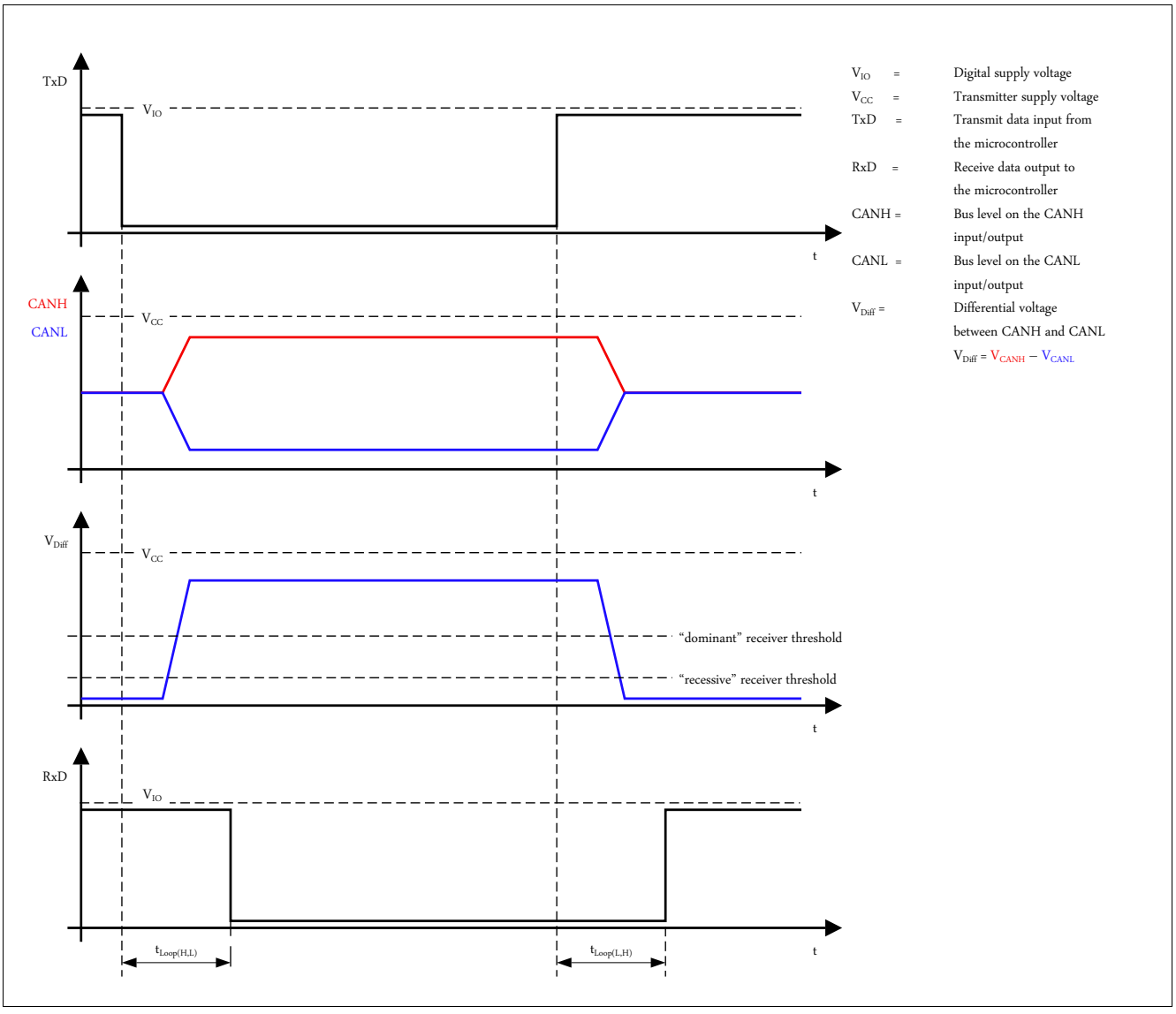


Figure 3 High speed CAN bus signals and logic signals

Functional Description

The IFX1051 is a High-Speed CAN transceiver, operating as an interface between the CAN controller and the physical bus medium. A HS CAN network is a two wire, differential bus network which allows data transmission rates for CAN FD frames up to 2 MBit/s. Main characteristics for HS CAN networks are the two signal states on the HS CAN bus: dominant and recessive (see **Figure 3**).

V_{CC}, V_{IO} and GND are the supply pins for the IFX1051. The pins CANH and CANL are the interface to the HS CAN bus and operate in both directions, as an input and as an output. RxD and TxD pins are the interface to the CAN controller, the TxD pin is an input pin and the RxD pin is an output pin. The RM pin is the input pin for the mode selection (see **Figure 4**).

By setting the TxD input pin to logical “low” the transmitter of the IFX1051 drives a dominant signal to the CANH and CANL pins. Setting TxD input to logical “high” turns off the transmitter and the output voltage on CANH and CANL discharges towards the recessive level. The recessive output voltage is provided by the bus biasing (see **Figure 1**). The output of the transmitter is considered to be dominant, when the voltage difference between CANH and CANL is at least higher than 1.5 V ($V_{Diff} = V_{CANH} - V_{CANL}$).

Parallel to the transmitter the normal-mode receiver monitors the signal on the CANH and CANL pins and indicates it on the RxD output pin. A dominant signal on the CANH and CANL pins sets the RxD output pin to logical “low”, vice versa a recessive signal sets the RxD output to logical “high”. The normal-mode receiver considers a voltage difference (V_{Diff}) between CANH and CANL above 0.9 V as dominant and below 0.5 V as recessive.

To be conform with HS CAN features, like the bit to bit arbitration, the signal on the RxD output has to follow the signal on the TxD input within a defined loop delay $t_{Loop} \leq 255$ ns.

The thresholds of the digital inputs (TxD and RM) and also the RxD output voltage are adapted to the digital power supply V_{IO}.

4.2 Modes of Operation

The IFX1051 supports two different modes of operation, receive-only mode and normal-operating mode while the transceiver is supplied according to the specified functional range. The mode of operation is selected by the RM input pin (see **Figure 4**).

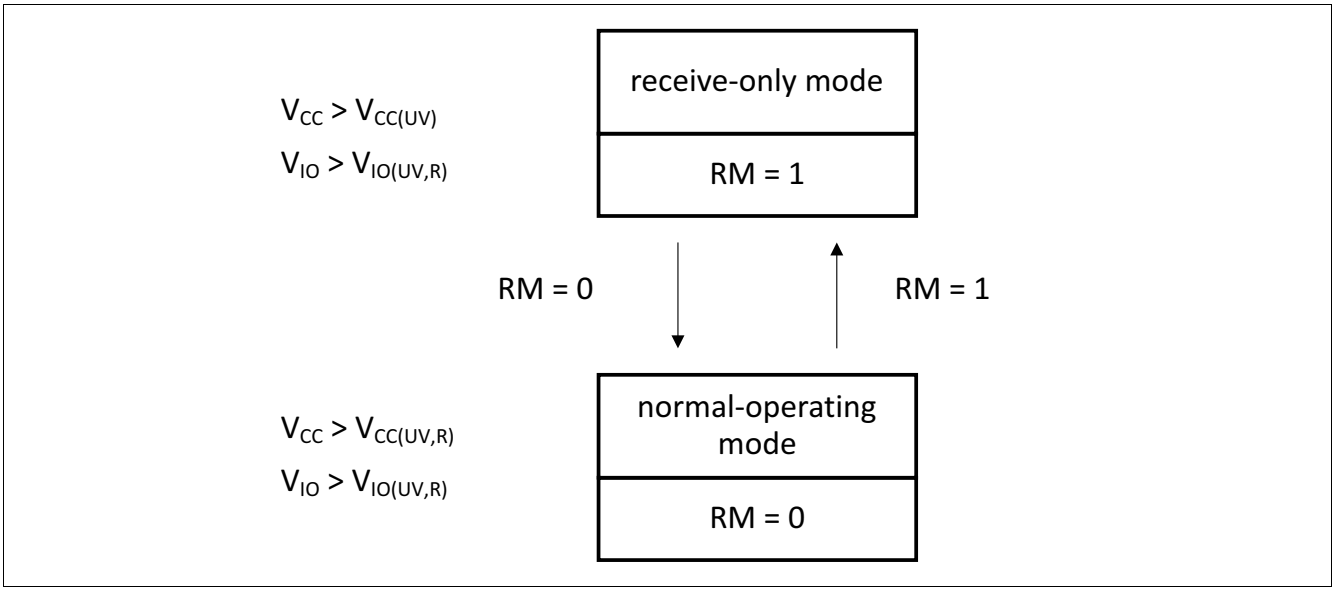


Figure 4 Mode state diagram

4.2.1 Normal-operating Mode

In normal-operating mode the transmitter and the receiver of the HS CAN transceiver IFX1051 are active (see **Figure 1**). The HS CAN transceiver sends the serial data stream on the TxD input pin to the CAN bus. The data on the CAN bus is displayed at the RxD pin simultaneously. A logical “low” signal on the RM pin selects the normal-operating mode, while the transceiver is supplied by V_{CC} and V_{IO} (see **Table 2** for details).

4.2.2 Receive-only Mode

In receive-only mode the normal-mode receiver is active and the transmitter is turned off. The IFX1051 can receive data from the HS CAN bus, but cannot send any data to the HS CAN bus.

A logical “high” signal on the RM pin selects the receive-only mode, while the transceiver is supplied by V_{CC} and V_{IO} (see **Table 2** for details).

4.3 Power-up and Undervoltage Condition

By detecting an undervoltage event, either on the transmitter supply V_{CC} or the digital supply V_{IO}, the transceiver IFX1051 changes the mode of operation. When the digital power supply V_{IO} is switched off, the transceiver powers down and remains in the power-down state. When switching off the transmitter supply V_{CC}, the transceiver changes to the forced power-save mode, (details see **Figure 5**).

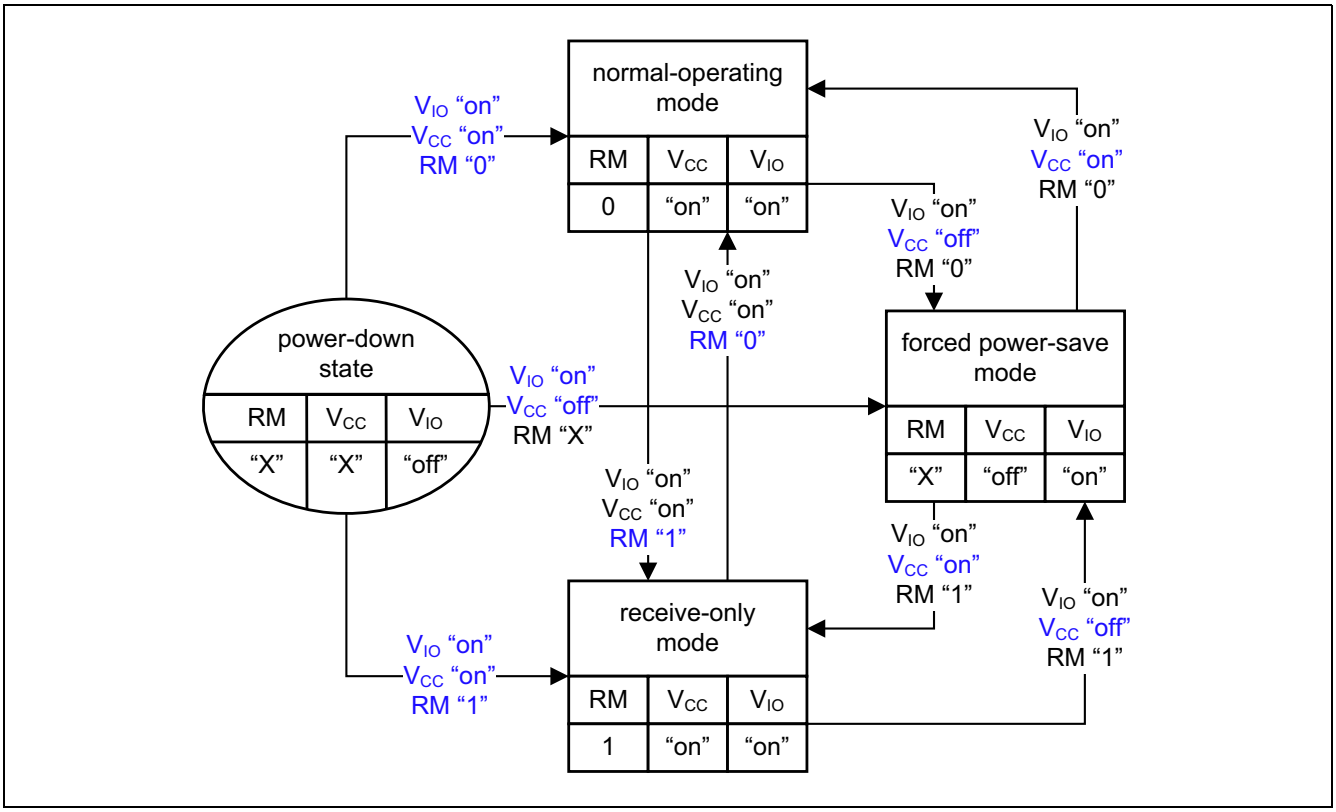


Figure 5 Power-up and undervoltage

Table 2 Modes of operation

Mode	RM	V_{IO}	V_{CC}	Bus Bias	Transmitter	Normal-mode Receiver	Low-power Receiver
Normal-operating	"low"	"on"	"on"	$V_{CC}/2$	"on"	"on"	not available
Receive-only	"high"	"on"	"on"	$V_{CC}/2$	"off"	"on"	not available
Forced power-save	"X"	"on"	"off"	floating	"off"	"off"	not available
Power-down state	"X"	"off"	"X"	floating	"off"	"off"	not available

4.3.1 Power-down State

Independent of the transmitter supply V_{CC} and of the RM input pin, the IFX1051 is in power-down state when the digital supply voltage V_{IO} is turned off (see **Figure 5**).

In the power-down state the input resistors of the receiver are disconnected from the bus biasing $V_{CC}/2$. The CANH and CANL bus interface of the IFX1051 is floating and acts as a high-impedance input with a very small leakage current. The high-ohmic input does not influence the recessive level of the CAN network and allows an optimized EME performance of the entire HS CAN network (see also **Table 2**).

4.3.2 Forced Power-save Mode

The forced power-save mode is a fail-safe mode to avoid any disturbance on the HS CAN bus, while the IFX1051 faces a loss of the transmitter supply V_{CC}.

In forced power-save mode, the transmitter and the normal-mode receiver are turned off and therefore the transceiver IFX1051 can not disturb the bus media.

The RxD output pin is permanently set to logical “high”. The bus biasing is floating (details see **Table 2**).

The forced power-save mode can only be entered when the transmitter supply V_{CC} is not available, either by powering up the digital supply V_{IO} only or by turning off the transmitter supply in normal-operating mode or in receive-only mode (see **Figure 5**). While the transceiver IFX1051 is in forced power-save mode the RM pin is disabled.

4.3.3 Power-up

The HS CAN transceiver IFX1051 powers up if at least the digital supply V_{IO} is connected to the device. By default the device powers up in normal-operating mode, due to the internal pull-down resistor on the RM pin to GND.

In case the device needs to power-up in receive-only mode, the RM pin needs to be pulled active to logical “high” and the supplies V_{IO} and V_{CC} have to be connected.

By supplying only the digital power supply V_{IO} the IFX1051 powers up in forced power-save mode (see **Figure 5**).

4.3.4 Undervoltage on the Digital Supply V_{IO}

If the voltage on V_{IO} supply input falls below the threshold $V_{IO} < V_{IO(U,F)}$, the transceiver IFX1051 powers down and changes to the power-down state.

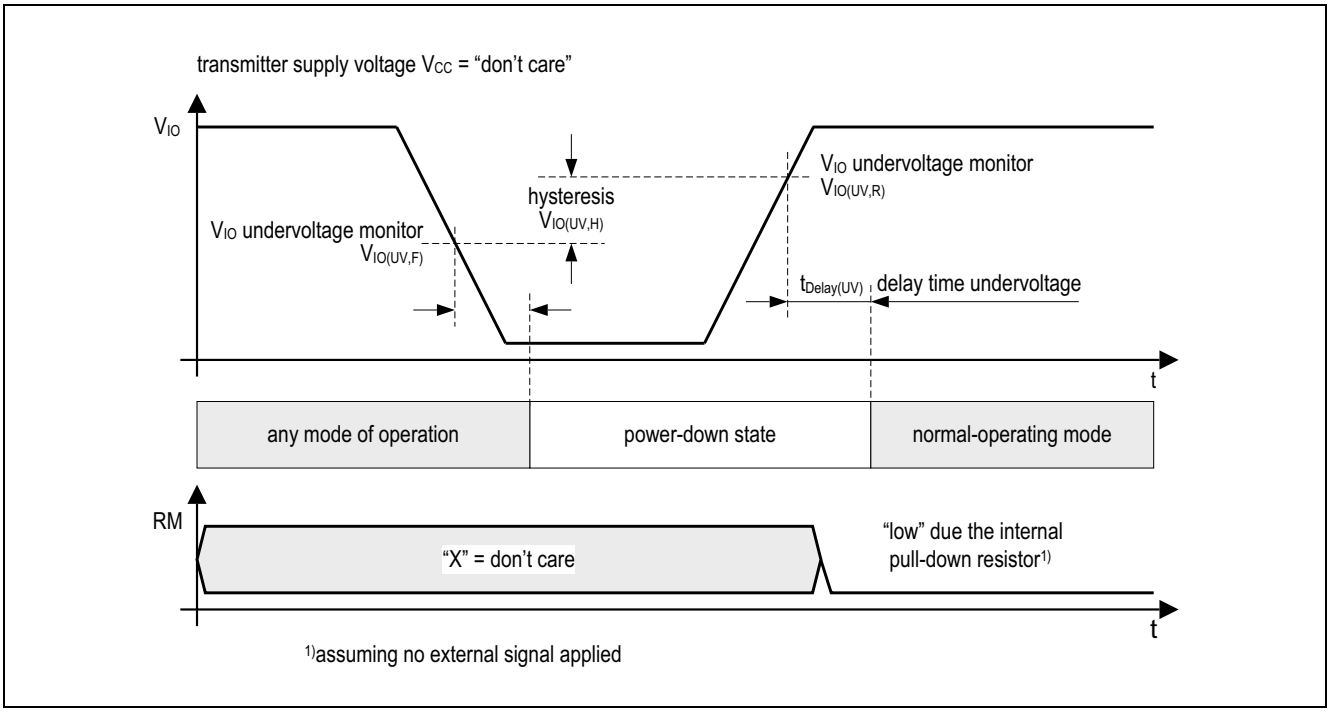


Figure 6 Undervoltage on the digital supply V_{IO}

4.3.5 Undervoltage on the Transmitter Supply V_{CC}

In case the transmitter supply V_{CC} falls below the threshold $V_{CC} < V_{CC(UV,F)}$, the transceiver IFX1051 changes the mode of operation to forced power-save mode. The transmitter and also the normal-mode receiver of the IFX1051 are powered by the V_{CC} supply. In case of an insufficient V_{CC} supply, the IFX1051 can neither transmit the CANH and CANL signals correctly to the bus, nor can it receive them properly. Therefore the IFX1051 blocks the transmitter and the receiver in forced power-save mode (see **Figure 7**).

The undervoltage detection on the transmitter supply V_{CC} is active in normal-operating mode and in receive-only mode (see **Figure 5**).

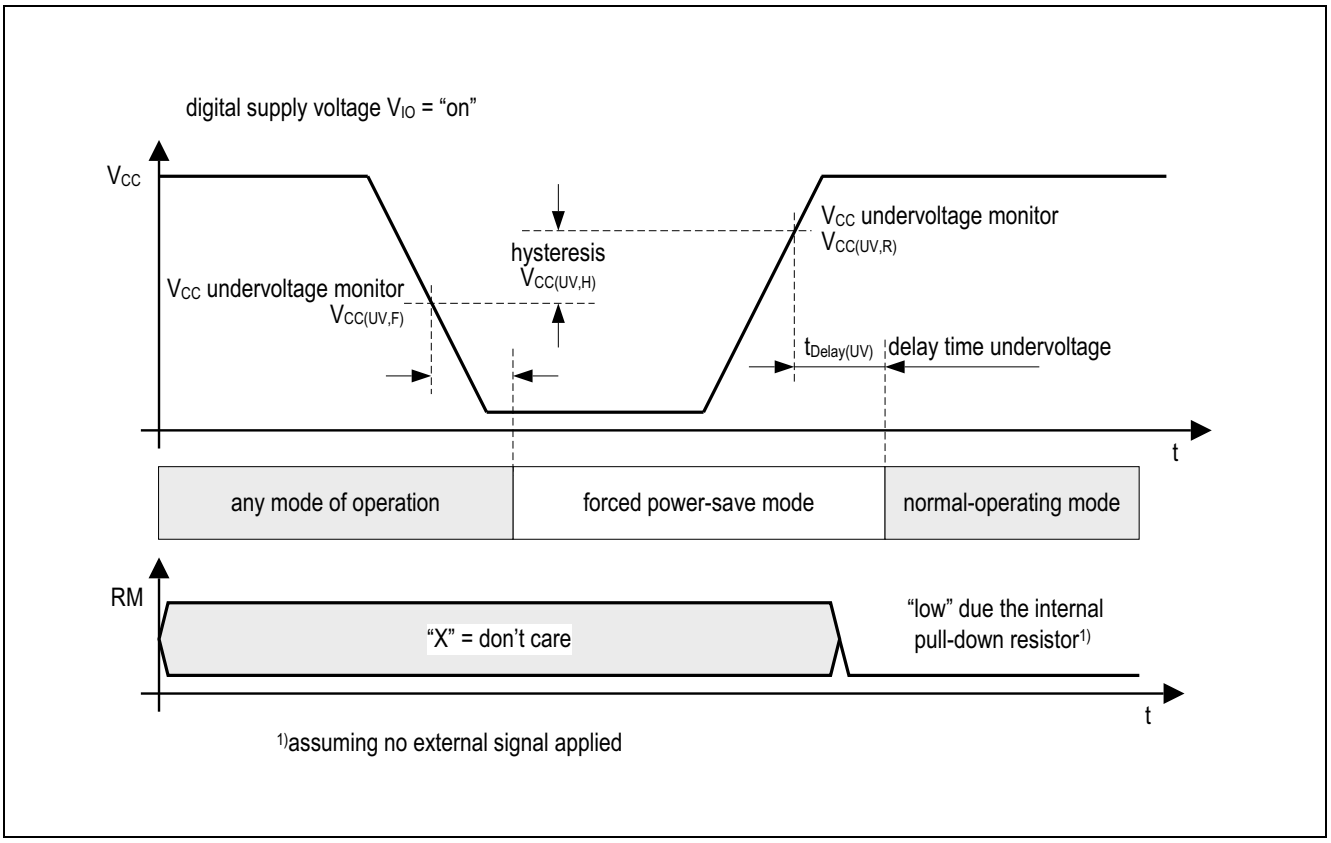


Figure 7 Undervoltage on the transmitter supply V_{CC}

4.3.6 Voltage Adaption to the Microcontroller Supply

The HS CAN transceiver IFX1051 has two different power supplies, V_{CC} and V_{IO}. The power supply V_{CC} supplies the transmitter and the normal-mode receiver. The power supply V_{IO} supplies the digital input and output buffers and it is also the main power domain of the internal logic.

To adjust the digital input and output levels of the IFX1051 to the I/O levels of the external microcontroller, connect the power supply V_{IO} to the microcontroller I/O supply voltage (see **Figure 13**).

Note: In case the digital supply voltage V_{IO} is not required in the application, connect the digital supply voltage V_{IO} to the transmitter supply V_{CC}.

5 Fail Safe Functions

5.1 Short Circuit Protection

The CANH and CANL bus outputs are short circuit proof, either against GND or a positive supply voltage. A current limiting circuit protects the transceiver against damages. If the device is heating up due to a continuous short on the CANH or CANL, the internal overtemperature protection switches off the bus transmitter.

5.2 Unconnected Logic Pins

All logic input pins have an internal pull-up resistor to V_{IO} or a pull-down resistor to GND. In case the V_{IO} supply is activated and the logical pins are open, the IFX1051 enters into the normal-operating mode by default. The TxD input is pulled to logical “high” due to the internal pull-up resistor to V_{IO}. The HS CAN transceiver IFX1051 will not influence the data on the CAN bus as long the TxD input pin remains logical “high”.

5.3 TxD Time-out Function

The TxD time-out feature protects the CAN bus against being permanently blocked in case the logical signal at the TxD pin of a singular node on the bus is continuously “low”. A continuous “low” signal at the TxD pin might have its root cause in a locked-up microcontroller or in a short circuit on the printed circuit board, for example. In normal-operating mode, a logical “low” signal applied to the TxD pin for the time $t > t_{TxD}$ triggers the TxD time-out feature and the IFX1051 disables the transmitter (see **Figure 8**). The receiver is still active and the data on the bus can be still monitored by the RxD output pin.

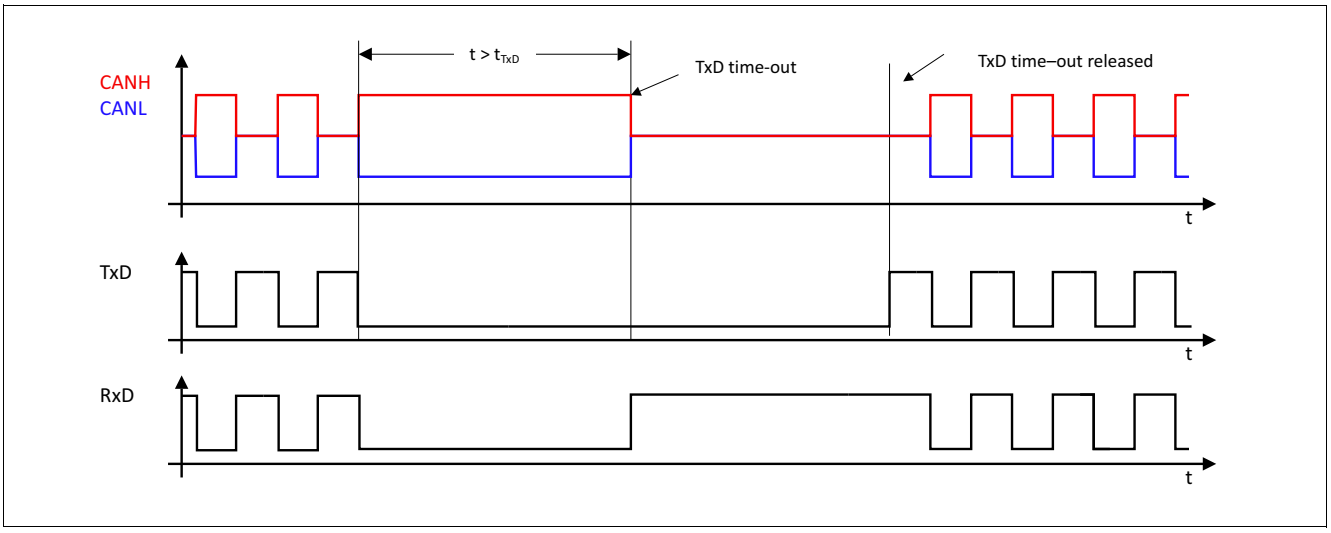


Figure 8 TxD time-out function

Figure 8 illustrates how the transmitter is deactivated and activated again. A permanent “low” signal on the TxD input pin activates the TxD time-out function and deactivates the transmitter. To release the transmitter after a TxD time-out event the IFX1051 requires a signal change on the TxD input pin from logical “low” to logical “high”.

The TxD Time-out Function is a very effective feature to keep the system communication alive in case of a malfunction of an individual node inside the network. But as a side effect any TxD time-out delay t_{TxD} inevitably will also limit the minimum possible bit rate of the network. An insufficient minimum bit rate

capability may become an issue when realizing very long bus networks because the theoretical maximum physical bus length is always connected with the applied signalling rate due to the bit-wise arbitration concept of CAN. Therefore the TxD time-out delay t_{TXD} of the IFX1051 has been implemented sufficiently long [1] so that for practical cases no negative effects of the TxD Time-out feature with respect to a possible minimum bit rate limitation needs to be expected - even for the usage even inside very long bus networks [2]. By this the IFX1051 allows the user to benefit from the TxD-Time-out as a protection feature assuring reliable CAN communication without being limited by the TxD-Time-out within longer bus networks.

5.4 Overtemperature Protection

The IFX1051 has an integrated overtemperature detection to protect the IFX1051 against thermal overstress of the transmitter. The overtemperature protection is active in normal-operating mode and disabled in receive-only mode. In case of an overtemperature condition, the temperature sensor will disable the transmitter (see **Figure 1**) while the transceiver remains in normal-operating mode.

After the device has cooled down the transmitter is activated again (see **Figure 9**). A hysteresis is implemented within the temperature sensor circuit.

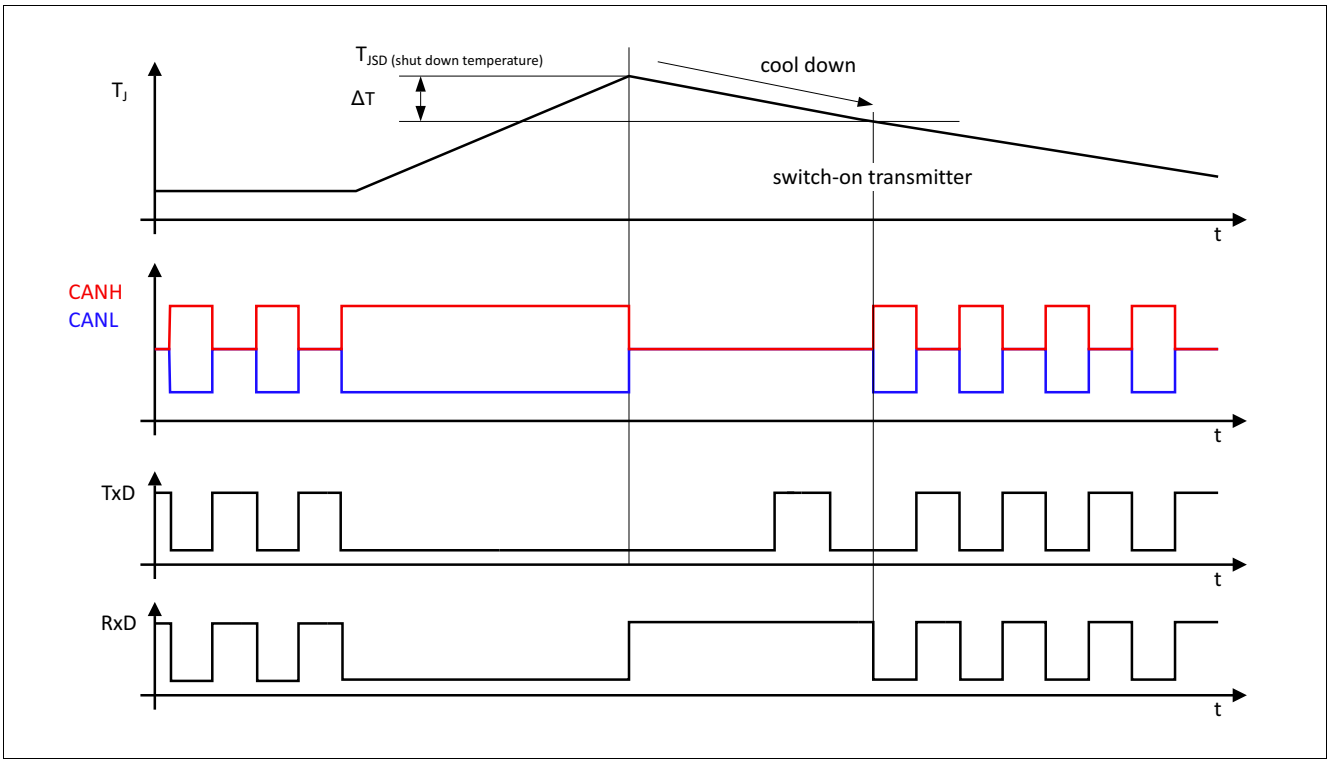


Figure 9 Overtemperature protection

5.5 Delay Time for Mode Change

The HS CAN transceiver IFX1051 changes the mode of operation within the time window t_{Mode}. During the mode change the normal-mode receiver and the RxD output are active and reflect the on the HS CAN input pins (see as an example **Figure 14** and **Figure 15**).

1) $t_{TXD} \geq 4.5$ ms; resulting in minimum achievable bit rates down to ~ 4 kbit/s

2) please note that when realizing very long bus networks also other influences or limitations next to the theoretical minimum bit rate limitation caused by the TxD-time-out function may apply and even may be dominating (for example bus impedance).

6 General Product Characteristics

6.1 Absolute Maximum Ratings

Table 3 Absolute maximum ratings voltages, currents and temperatures[1)]

All voltages with respect to ground; positive current flowing into pin;
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Transmitter supply voltage	V_{CC}	-0.3	–	6.0	V	–	P_6.1.1
Digital supply voltage	V_{IO}	-0.3	–	6.0	V	–	P_6.1.2
CANH DC voltage versus GND	V_{CANH}	-40	–	40	V	–	P_6.1.3
CANL DC voltage versus GND	V_{CANL}	-40	–	40	V	–	P_6.1.4
Differential voltage between CANH and CANL	V_{CAN_Diff}	-40	–	40	V	–	P_6.1.5
Voltages at the input pins: RM, TxD	V_{MAX_IN}	-0.3	–	6.0	V	–	P_6.1.6
Voltages at the output pin: RxD	V_{MAX_OUT}	-0.3	–	V_{IO}	V	–	P_6.1.7
Currents							
RxD output current	I_{RxD}	-20	–	20	mA	–	P_6.1.8
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_6.1.9
Storage temperature	T_S	-55	–	150	°C	–	P_6.1.10
ESD Resistivity							
ESD immunity at CANH, CANL versus GND	$V_{ESD_HBM_CAN}$	-10	–	10	kV	HBM (100 pF via 1.5 kΩ)[2)]	P_6.1.11
ESD immunity at all other pins	$V_{ESD_HBM_ALL}$	-2	–	2	kV	HBM (100 pF via 1.5 kΩ)[2)]	P_6.1.12
ESD immunity to GND	V_{ESD_CDM}	-750	–	750	V	CDM[3)]	P_6.1.13

1) Not subject to production test, specified by design
2) ESD susceptibility, Human Body Model “HBM” according to ANSI/ESDA/JEDEC JS-001
3) ESD susceptibility, Charge Device Model “CDM” according to EIA/JESD22-C101 or ESDA STM5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal-operating range. Protection functions are not designed for continuos repetitive operation.

6.2 Functional Range

Table 4 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
Transmitter supply voltage	V_{CC}	4.5	–	5.5	V	–	P_6.2.1
Digital supply voltage	V_{IO}	3.0	–	5.5	V	–	P_6.2.2
Thermal Parameters							
Junction temperature	T_j	-40	–	125	°C	1)	P_6.2.3

1) Not subject to production test, specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

6.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, please visit **www.jedec.org**.*

Table 5 Thermal resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal Resistances							
Junction to Ambient PG-TSON-8	R_{thJA}	–	55	–	K/W	2) IFX1051LE	P_6.3.1
Junction to Ambient PG-DSO-8	R_{thJA}	–	130	–	K/W	2) IFX1051SJ	P_6.3.4
Thermal Shutdown (junction temperature)							
Thermal shutdown temperature	T_{JSD}	150	175	200	°C	–	P_6.3.2
Thermal shutdown hysteresis	ΔT	–	10	–	K	–	P_6.3.3

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board. The product (IFX1051) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu).

7 Electrical Characteristics

7.1 Functional Device Characteristics

Table 6 Electrical characteristics

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption							
Current consumption at V_{CC} normal-operating mode	I_{CC}	–	2.6	4	mA	recessive state, V_{TxD} = V_{IO}, V_{RM} = 0 V;	P_7.1.1
Current consumption at V_{CC} normal-operating mode	I_{CC}	–	38	60	mA	dominant state, V_{TxD} = V_{RM} = 0 V;	P_7.1.2
Current consumption at V_{IO} normal-operating mode	I_{IO}	–	–	1	mA	V_{RM} = 0 V;	P_7.1.3
Current consumption at V_{CC} receive-only mode	$I_{CC(ROM)}$	–	–	2	mA	V_{RM} = V_{TxD} = V_{IO};	P_7.1.4
Current consumption at V_{IO} receive-only mode	$I_{IO(ROM)}$	–	–	1	mA	V_{RM} = V_{IO};	P_7.1.5
Supply Resets							
V_{CC} undervoltage monitor rising edge	$V_{CC(UV,R)}$	3.8	4.0	4.3	V	–	P_7.1.6
V_{CC} undervoltage monitor falling edge	$V_{CC(UV,F)}$	3.65	3.85	4.3	V	–	P_7.1.7
V_{CC} undervoltage monitor hysteresis	$V_{CC(UV,H)}$	–	150	–	mV	1)	P_7.1.8
V_{IO} undervoltage monitor rising edge	$V_{IO(UV,R)}$	2.0	2.5	3.0	V	–	P_7.1.9
V_{IO} undervoltage monitor falling edge	$V_{IO(UV,F)}$	1.8	2.3	3.0	V	–	P_7.1.10
V_{IO} undervoltage monitor hysteresis	$V_{IO(UV,H)}$	–	200	–	mV	1)	P_7.1.11
V_{CC} and V_{IO} undervoltage delay time	$t_{Delay(UV)}$	–	–	100	µs	1) (see **Figure 6** and **Figure 7**);	P_7.1.12
Receiver Output RxD							
“High” level output current	$I_{RD,H}$	–	-4	-2	mA	V_{RxD} = V_{IO} - 0.4 V, V_{Diff} < 0.5 V;	P_7.1.13
“Low” level output current	$I_{RD,L}$	2	4	–	mA	V_{RxD} = 0.4 V, V_{Diff} > 0.9 V;	P_7.1.14

Table 6 Electrical characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Transmission Input TxD							
"High" level input voltage threshold	$V_{TxD,H}$	–	0.5 × V_{IO}	0.7 × V_{IO}	V	recessive state;	P_7.1.15
"Low" level input voltage threshold	$V_{TxD,L}$	0.3 × V_{IO}	0.4 × V_{IO}	–	V	dominant state;	P_7.1.16
Pull-up resistance	R_{TxD}	10	25	50	kΩ	–	P_7.1.17
Input hysteresis	$V_{HYS(TxD)}$	–	450	–	mV	1)	P_7.1.18
Input capacitance	C_{TxD}	–	–	10	pF	1)	P_7.1.19
TxD permanent dominant time-out	t_{TxD}	4.5	–	16	ms	normal-operating mode;	P_7.1.20
Receive-only Input RM							
"High" level input voltage threshold	$V_{RM,H}$	–	0.5 × V_{IO}	0.7 × V_{IO}	V	receive-only mode;	P_7.1.21
"Low" level input voltage threshold	$V_{RM,L}$	0.3 × V_{IO}	0.4 × V_{IO}	–	V	normal-operating mode;	P_7.1.22
Pull-down resistance	R_{RM}	10	25	50	kΩ	–	P_7.1.23
Input capacitance	C_{RM}	–	–	10	pF	1)	P_7.1.24
Input hysteresis	$V_{HYS(RM)}$	–	200	–	mV	1)	P_7.1.25
Bus Receiver							
Differential receiver threshold dominant normal-operating mode and receive-only mode	V_{Diff_D}	–	0.75	0.9	V	2)	P_7.1.26
Differential receiver threshold recessive normal-operating mode and receive-only mode	V_{Diff_R}	0.5	0.66	–	V	2)	P_7.1.27
Differential range dominant Normal-operating mode	$V_{Diff_D_Range}$	0.9	–	8.0	V	1) 2)	P_7.1.28
Differential range recessive Normal-operating mode	$V_{Diff_R_Range}$	-3.0	–	0.5	V	1) 2)	P_7.1.29
Common mode range	CMR	-12	–	12	V	V_{CC} = 5 V;	P_7.1.30
Differential receiver hysteresis normal-operating mode	$V_{Diff,hys}$	–	90	–	mV	1)	P_7.1.31
CANH, CANL input resistance	R_i	10	20	30	kΩ	recessive state;	P_7.1.32
Differential input resistance	R_{Diff}	20	40	60	kΩ	recessive state;	P_7.1.33

Table 6 Electrical characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input resistance deviation between CANH and CANL	ΔR_i	- 1	–	1	%	recessive state;	P_7.1.34
Input capacitance CANH, CANL versus GND	C_{In}	–	20	40	pF	[1] $V_{TxD} = V_{IO}$;	P_7.1.35
Differential input capacitance	C_{In_Diff}	–	10	20	pF	[1] $V_{TxD} = V_{IO}$;	P_7.1.36

Table 6 Electrical characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Bus Transmitter							
CANL/CANH recessive output voltage normal-operating mode	$V_{CANL/H}$	2.0	2.5	3.0	V	$V_{TxD} = V_{IO}$, no load;	P_7.1.37
CANH, CANL recessive output voltage difference normal-operating mode	V_{Diff_NM}	-500	–	50	mV	$V_{TxD} = V_{IO}$, no load;	P_7.1.38
CANL dominant output voltage normal-operating mode	V_{CANL}	0.5	–	2.25	V	V_{TxD} = 0 V;	P_7.1.39
CANH dominant output voltage normal-operating mode	V_{CANH}	2.75	–	4.5	V	V_{TxD} = 0 V;	P_7.1.40
CANH, CANL dominant output voltage difference normal-operating mode *according to ISO 11898-2* $V_{Diff} = V_{CANH} - V_{CANL}$	V_{Diff}	1.5	–	3.0	V	V_{TxD} = 0 V, 50 Ω < R_L < 65 Ω, 4.75 < V_{CC} < 5.25 V;	P_7.1.41
CANH, CANL dominant output voltage difference normal-operating mode $V_{Diff} = V_{CANH} - V_{CANL}$	V_{Diff_EXT}	1.4	–	3.3	V	V_{TxD} = 0 V, 45 Ω < R_L < 70 Ω, 4.75 < V_{CC} < 5.25 V;	P_7.1.42
Differential voltage dominant high extended bus load Normal-operating mode	$V_{Diff_HEX_BL}$	1.5	–	5.0	V	V_{TxD} = 0 V, R_L = 2240Ω, 4.75 V < V_{CC} < 5.25 V, static behavior;[1)]	P_7.1.43
Driver dominant symmetry normal-operating mode $V_{SYM} = V_{CANH} + V_{CANL}$	V_{SYM}	4.5	5	5.5	V	V_{CC} = 5.0 V, V_{TxD} = 0 V;	P_7.1.44
CANL short circuit current	I_{CANLsc}	40	75	100	mA	$V_{CANLshort}$ = 18 V, V_{CC} = 5.0 V, t < t_{TxD}, V_{TxD} = 0 V;	P_7.1.45
CANH short circuit current	I_{CANHsc}	-100	-75	-40	mA	$V_{CANHshort}$ = -3 V, V_{CC} = 5.0 V, t < t_{TxD}, V_{TxD} = 0 V;	P_7.1.46
Leakage current, CANH	$I_{CANH,lk}$	-5	–	5	µA	$V_{CC} = V_{IO}$ = 0 V, 0 V < V_{CANH} < 5 V, $V_{CANH} = V_{CANL}$;	P_7.1.47
Leakage current, CANL	$I_{CANL,lk}$	-5	–	5	µA	$V_{CC} = V_{IO}$ = 0 V, 0 V < V_{CANL} < 5 V, $V_{CANH} = V_{CANL}$;	P_7.1.48

Table 6 Electrical characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Dynamic CAN-Transceiver Characteristics							
Propagation delay TxD-to-RxD "low" ("recessive to dominant)	$t_{Loop(H,L)}$	–	170	230	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF;	P_7.1.49
Propagation delay TxD-to-RxD "high" (dominant to recessive)	$t_{Loop(L,H)}$	–	170	230	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF;	P_7.1.50
Propagation delay TxD "low" to bus dominant	$t_{d(L),T}$	–	90	140	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF;	P_7.1.51
Propagation delay TxD "high" to bus recessive	$t_{d(H),T}$	–	90	140	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF;	P_7.1.52
Propagation delay bus dominant to RxD "low"	$t_{d(L),R}$	–	90	140	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF;	P_7.1.53
Propagation delay bus recessive to RxD "high"	$t_{d(H),R}$	–	90	140	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF;	P_7.1.54
Delay Times							
Delay time for mode change	t_{Mode}	–	–	20	µs	[1] (see **Figure 14** and **Figure 15**);	P_7.1.55
CAN FD Characteristics							
Received recessive bit width at 2 MBit/s	$t_{Bit(RxD)_2MB}$	430	500	530	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF, t_{Bit} = 500 ns, (see **Figure 12**);	P_7.1.56
Transmitted recessive bit width at 2 MBit/s	$t_{Bit(Bus)_2MB}$	450	500	530	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF, t_{Bit} = 500 ns, (see **Figure 12**);	P_7.1.57
Receiver timing symmetry at 2 MBit/s $\Delta t_{Rec} = t_{Bit(RxD)} - t_{Bit(Bus)}$	Δt_{Rec_2MB}	-45	–	20	ns	C_L = 100 pF, 4.75 V < V_{CC} < 5.25 V, C_{RxD} = 15 pF, t_{Bit} = 500 ns, (see **Figure 12**);	P_7.1.58

1) Not subject to production test, specified by design.
2) In respect to common mode range.

7.2 Diagrams

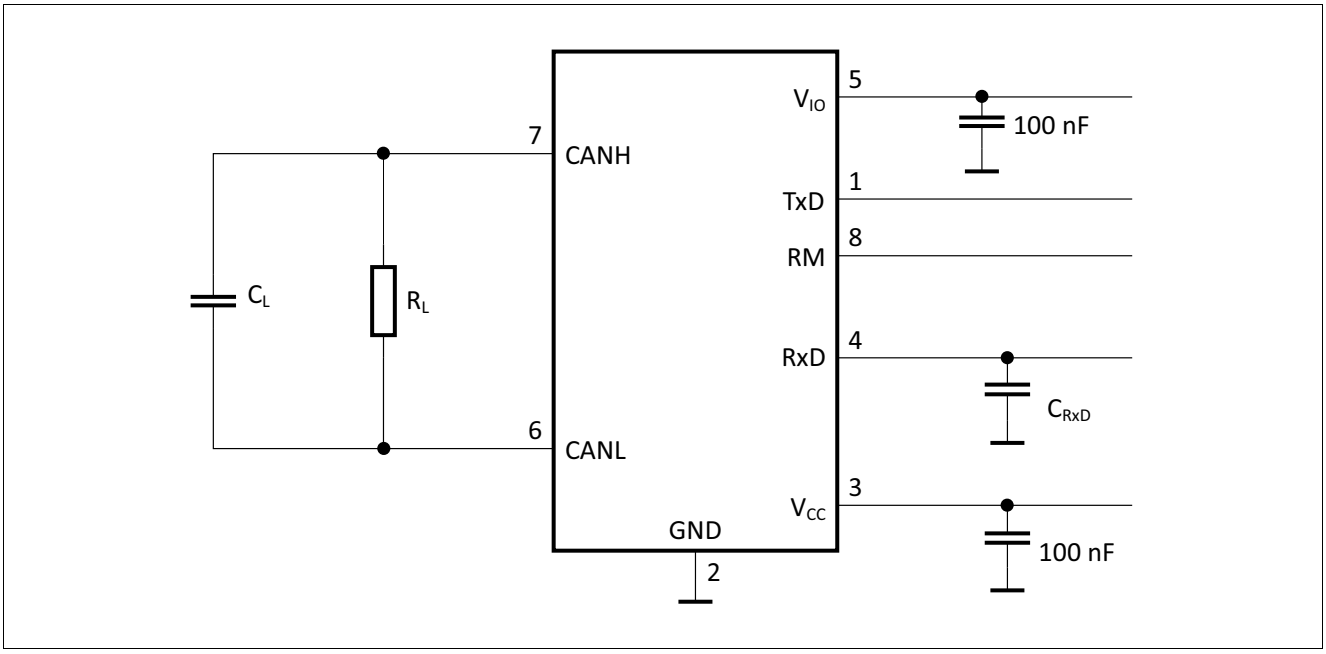


Figure 10 Test circuits for dynamic characteristics

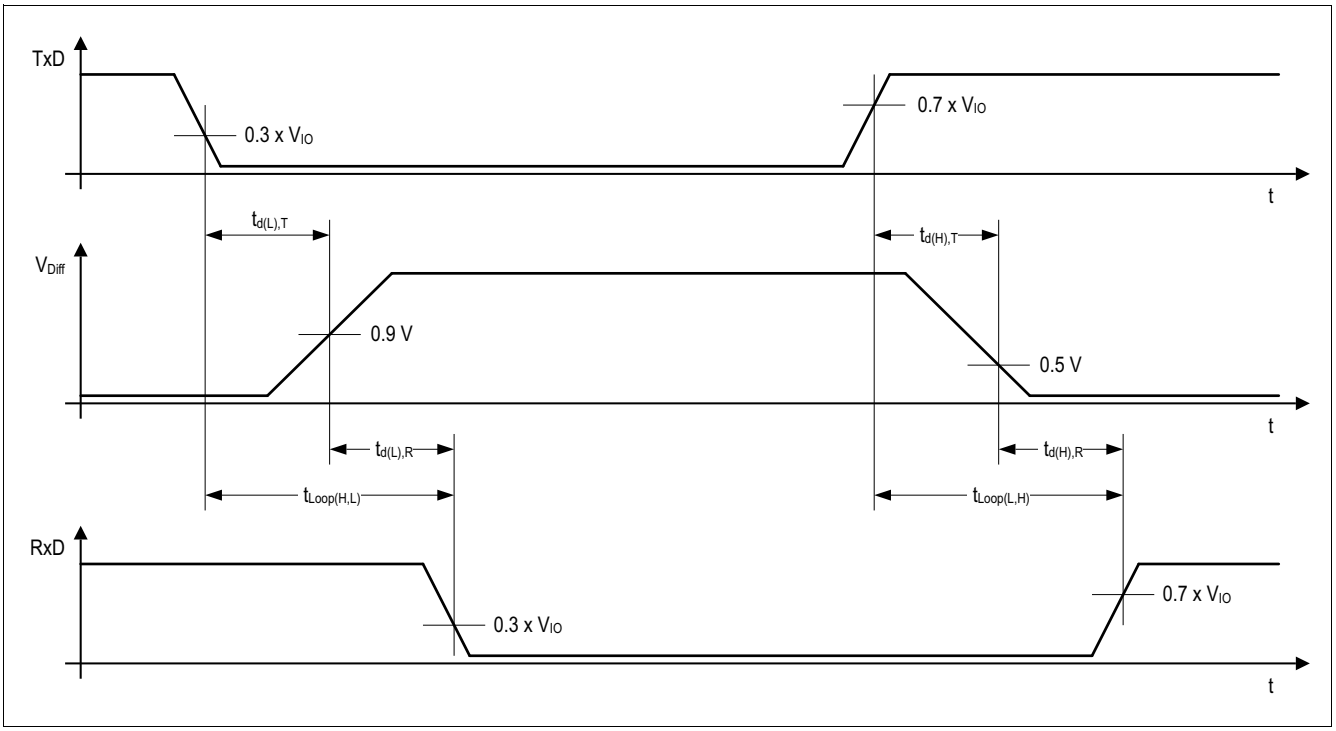


Figure 11 Timing diagrams for dynamic characteristics

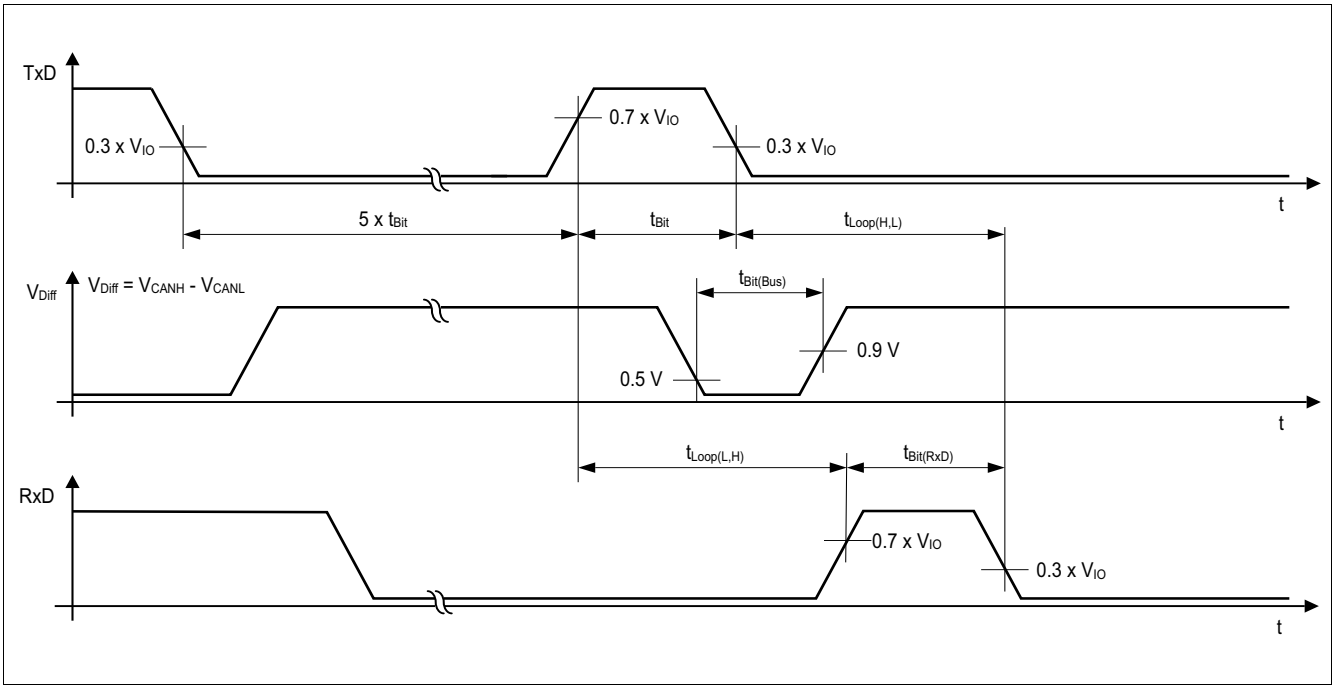


Figure 12 Recessive bit time - five dominant bits followed by one recessive bit

8 Application Information

8.1 ESD Robustness according to IEC61000-4-2

Test for ESD robustness according to IEC61000-4-2 “Gun test” (150 pF, 330 Ω) have been performed. The results and test conditions are available in a separate test report.

Table 7 ESD robustness according to IEC61000-4-2

Performed Test	Result	Unit	Remarks
Electrostatic discharge voltage at pin CANH and CANL versus GND	≥ +8	kV	[1)]Positive pulse
Electrostatic discharge voltage at pin CANH and CANL versus GND	≤ -8	kV	[1)]Negative pulse

1) ESD susceptibility “ESD GUN” according to GIFT / ICT paper: “EMC Evaluation of CAN Transceivers, version 03/02/IEC TS62228”, section 4.3. (DIN EN61000-4-2)
Tested by external test facility (IBEE Zwickau).

8.2 Application Example

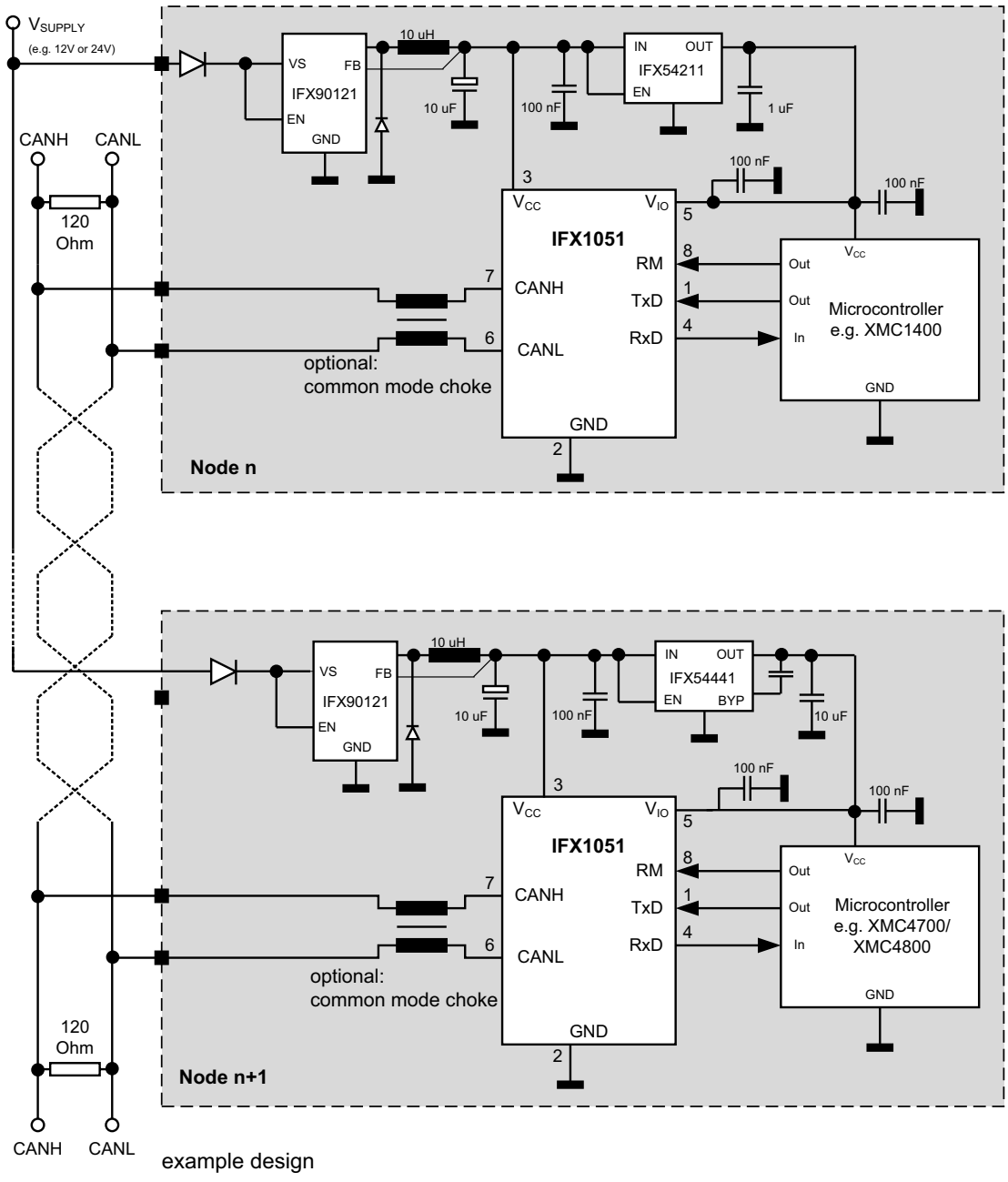


Figure 13 Application circuit

8.3 Examples for Mode Changes

- The mode change is executed independently of the signal on the HS CAN bus. The CANH, CANL inputs may be either dominant or recessive. They can be also permanently shorted to GND or V_{CC}.
- A mode change is performed independently of the signal on the TxD input. The TxD input may be either logical “high” or “low”.

Analog to that, changing the RM input pin to logical “high” changes the mode of operation to the receive-only mode independent on the signals at the CANH, CANL and TxD pins.

Note: In case the TxD signal is “low” setting the RM input pin to logical “low” changes the operating mode of the device to normal-operating mode and drives a dominant signal to the HS CAN bus.

Note: The TxD time-out is only effective in normal-operating mode. The TxD time-out timer starts when the IFX1051 enters normal-operating mode and the TxD input is set to logical “low”.

8.3.1 Mode Change while the TxD Signal is “low”

The example in **Figure 14** shows a mode change to normal-operating mode while the TxD input is logical “low”. The HS CAN signal is recessive, assuming all other HS CAN bus subscribers are also sending a recessive bus signal.
While the transceiver IFX1051 is in receive-only mode the transmitter is turned off. The IFX1051 drives no signal to the HS CAN bus. The normal-mode receiver is active in receive-only mode and the RxD indicates the recessive signal on the HS CAN bus with a logical “high” output signal.
Changing the RM to logical “low” turns the mode of operation to normal-operating mode, while the TxD input remains logical “low”. The transmitter remains disabled until the mode change is completed. The normal-mode receiver remains active also during the mode change. In normal-operating mode the transmitter becomes active and the logical “low” signal on the TxD input drives a dominant signal to the HS CAN bus. The dominant bus signal is indicated on the RxD output by a logical “low” signal.
Changing the RM pin back to logical “high”, disables the transmitter. The normal-mode receiver and the RxD output remain active and the recessive bus signal is indicated on the RxD output by a logical “high” signal.

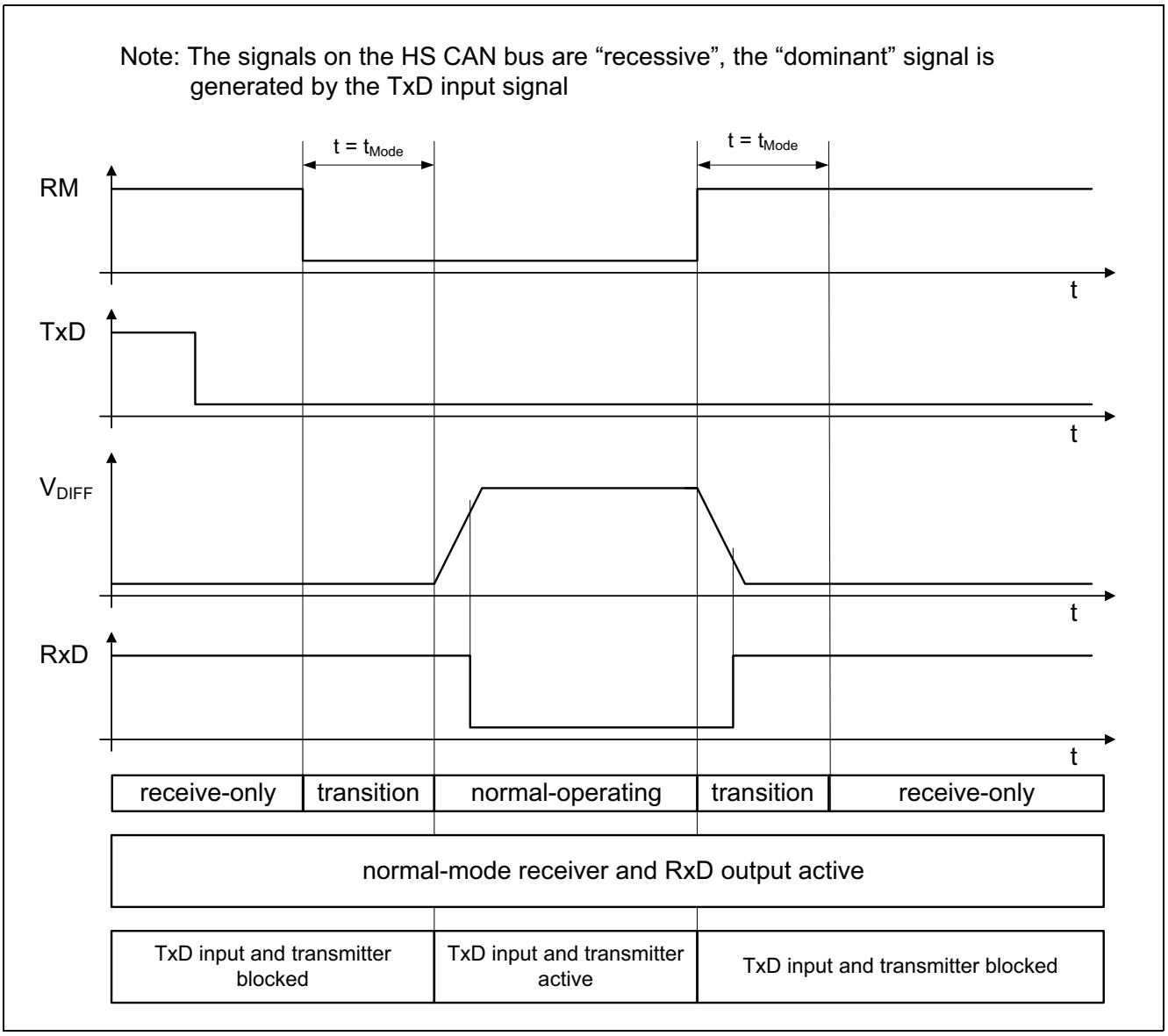


Figure 14 Example for a mode change while the TxD is “low”

8.3.2 Mode Change while the Bus Signal is dominant

The example in **Figure 15** shows a mode change while the bus is dominant and the TxD input signal is set to logical “high”.
While the transceiver IFX1051 is in receive-only mode the transmitter is turned off. The IFX1051 drives no signal to the HS CAN bus. The normal-mode receiver is active in receive-only mode and the RxD indicates the dominant signal on the HS CAN bus with a logical “low” output signal.
Changing the RM to logical “low” turns the mode of operation to normal-operating mode, while the TxD input remains logical “high”. The transmitter remains disabled until the mode change is completed. The normal-mode receiver remains active also during the mode change. In normal-operating mode the transmitter becomes active, the bus remains dominant since the bus signal is driven from another HS CAN bus subscriber. The dominant bus signal is indicated on the RxD output by a logical “low” signal.
Regardless which mode of operation is selected by the RM input pin, the RxD output indicates the signal on the HS CAN bus. Also during the mode transition from receive-only mode to normal-operating mode or vice versa.

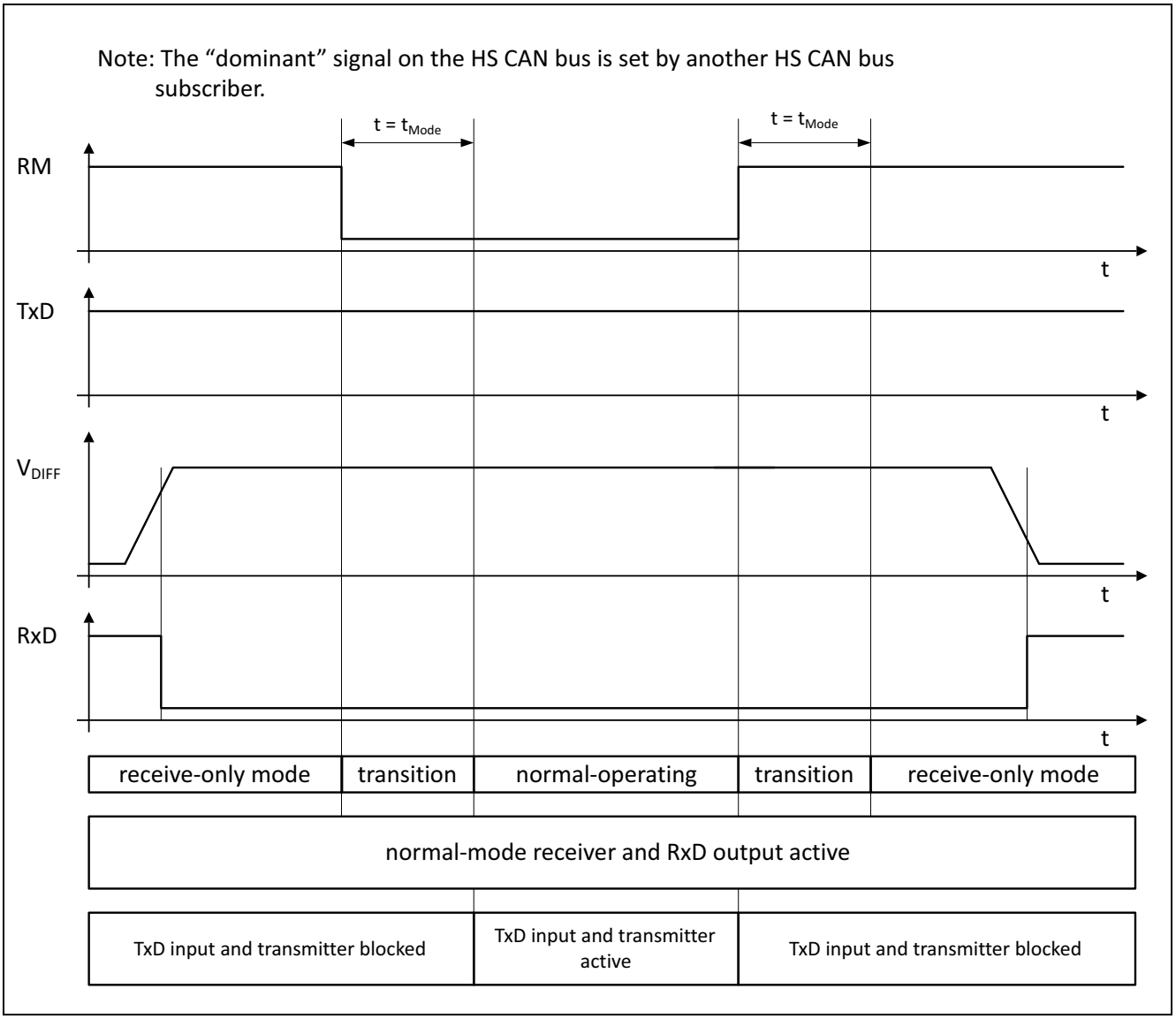


Figure 15 Example for a mode change while the HS CAN is dominant

9 Package Outline

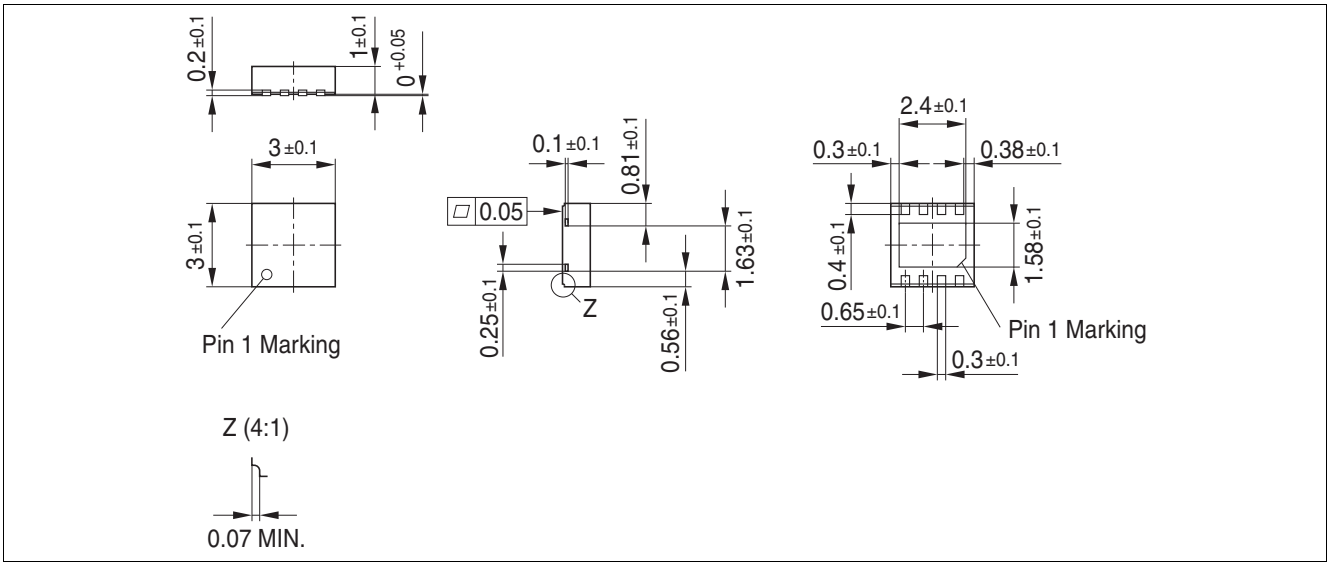


Figure 16 PG-TSON-8 (Plastic Thin Small Outline Nonleaded PG-TSON-8)

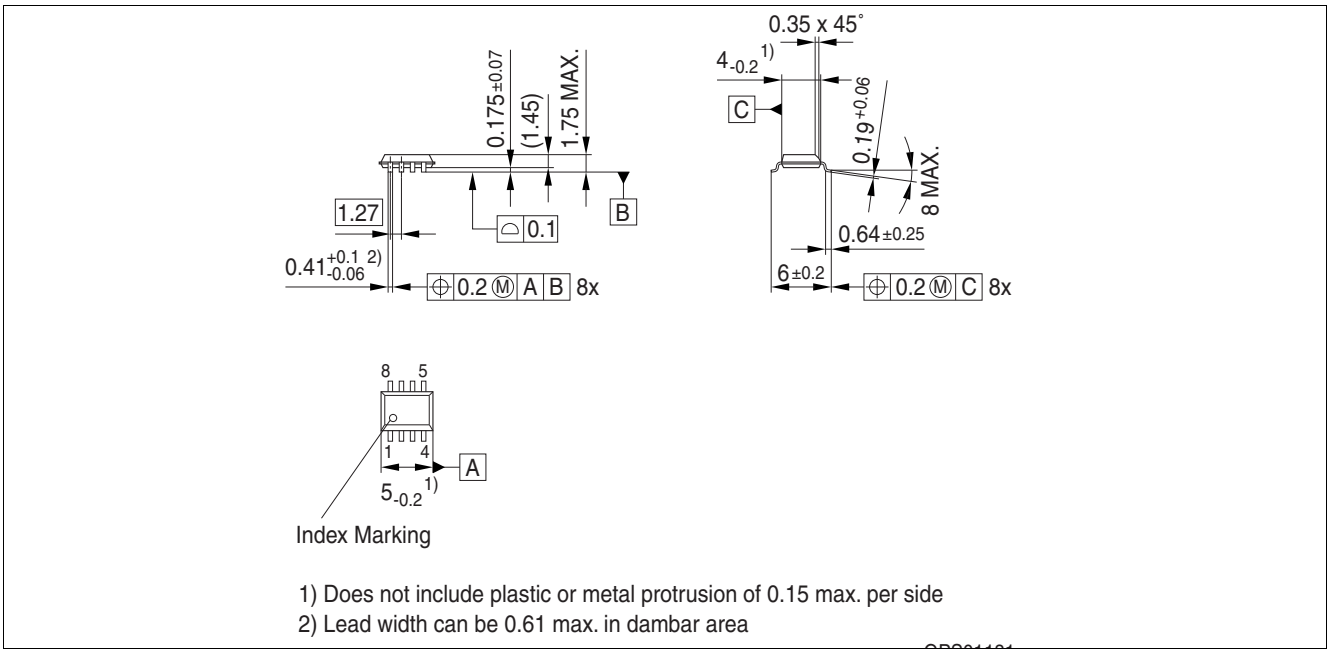


Figure 17 PG-DSO-8 (Plastic Dual Small Outline PG-DSO-8)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

10 Revision History

Revision	Date	Changes
1.0	2017-03-15	Data Sheet – Initial Release

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