



# STK15C68

## 8K x 8 *AutoStore*<sup>TM</sup> nvSRAM

### *QuantumTrap*<sup>TM</sup> CMOS Nonvolatile Static RAM

**Obsolete - Not Recommend for new Deisgns**

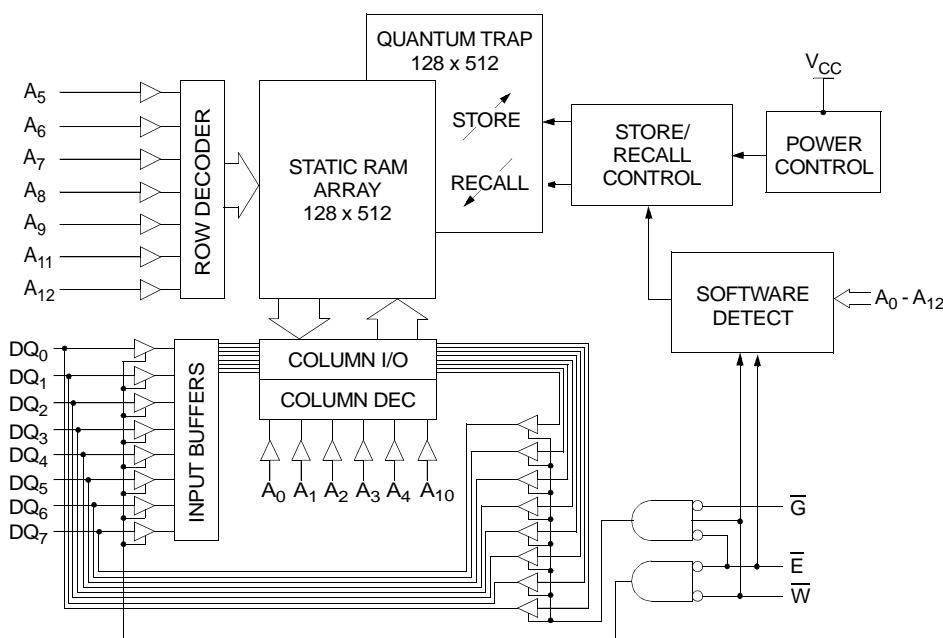
#### FEATURES

- Nonvolatile Storage without Battery Problems
- Directly Replaces 8K x 8 Static RAM, Battery-Backed RAM or EEPROM
- 25ns, 35ns and 45ns Access Times
- *STORE* to Nonvolatile Elements Initiated by Software or *AutoStore*<sup>TM</sup> on Power Down
- *RECALL* to SRAM Initiated by Software or Power Restore
- 10mA Typical I<sub>CC</sub> at 200ns Cycle Time
- Unlimited READ, WRITE and *RECALL* Cycles
- 1,000,000 *STORE* Cycles to Nonvolatile Elements
- 100-Year Data Retention over Full Industrial Temperature Range
- No Data Loss from Undershoot
- Commercial and Industrial Temperatures
- 28-Pin 600 or 300 mil PDIP and 350 mil SOIC Packages

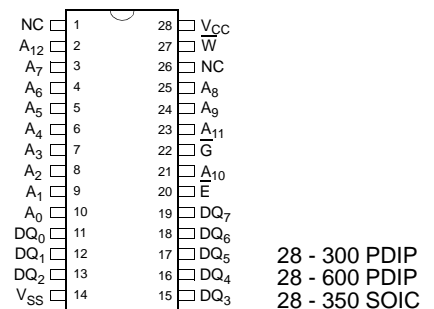
#### DESCRIPTION

The STK15C68 is a fast SRAM with a nonvolatile element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in Nonvolatile Elements. Data transfers from the SRAM to the Nonvolatile Elements (the *STORE* operation) can take place automatically on power down using charge stored in system capacitance. Transfers from the Nonvolatile Elements to the SRAM (the *RECALL* operation) take place automatically on restoration of power. Initiation of *STORE* and *RECALL* cycles can also be controlled by entering control sequences on the SRAM inputs. The STK15C68 is pin-compatible with 8k x 8 SRAMs and battery-backed SRAMs, allowing direct substitution while enhancing performance. A similar device (STK16C68) with an internally integrated capacitor is available for systems with very fast slew rates. The STK12C68, which uses an external capacitor, is an alternative for these applications.

#### BLOCK DIAGRAM



#### PIN CONFIGURATIONS



#### PIN NAMES

A <sub>0</sub> - A <sub>12</sub>	Address Inputs
$\bar{W}$	Write Enable
DQ <sub>0</sub> - DQ <sub>7</sub>	Data In/Out
$\bar{E}$	Chip Enable
$\bar{G}$	Output Enable
V <sub>CC</sub>	Power (+ 5V)
V <sub>SS</sub>	Ground

### ABSOLUTE MAXIMUM RATINGS<sup>a</sup>

Voltage on Input Relative to Ground . . . . . -0.5V to 7.0V  
 Voltage on Input Relative to V<sub>SS</sub> . . . . . -0.6V to (V<sub>CC</sub> + 0.5V)  
 Voltage on DQ<sub>0-7</sub> . . . . . -0.5V to (V<sub>CC</sub> + 0.5V)  
 Temperature under Bias . . . . . -55°C to 125°C  
 Storage Temperature . . . . . -65°C to 150°C  
 Power Dissipation . . . . . 1W  
 DC Output Current (1 output at a time, 1s duration) . . . . . 15mA

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### DC CHARACTERISTICS

(V<sub>CC</sub> = 5.0V ± 10%)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I <sub>CC1</sub> <sup>b</sup>	Average V <sub>CC</sub> Current		85		90	mA	t <sub>AVAV</sub> = 25ns
			75		75	mA	t <sub>AVAV</sub> = 35ns
			65		65	mA	t <sub>AVAV</sub> = 45ns
I <sub>CC2</sub> <sup>c</sup>	Average V <sub>CC</sub> Current during STORE		3		3	mA	All Inputs Don't Care, V <sub>CC</sub> = max
I <sub>CC3</sub> <sup>b</sup>	Average V <sub>CC</sub> Current at t <sub>AVAV</sub> = 200ns 5V, 25°C, Typical		10		10	mA	$\bar{W} \geq (V_{CC} - 0.2V)$ All Others Cycling, CMOS Levels
I <sub>CC4</sub> <sup>c</sup>	Average V <sub>CC</sub> Current during AutoStore™ Cycle		2		2	mA	All Inputs Don't Care
I <sub>SB1</sub> <sup>d</sup>	Average V <sub>CC</sub> Current (Standby, Cycling TTL Input Levels)		27		28	mA	t <sub>AVAV</sub> = 25ns, $\bar{E} \geq V_{IH}$
			23		24	mA	t <sub>AVAV</sub> = 35ns, $\bar{E} \geq V_{IH}$
			20		21	mA	t <sub>AVAV</sub> = 45ns, $\bar{E} \geq V_{IH}$
I <sub>SB2</sub> <sup>d</sup>	V <sub>CC</sub> Standby Current (Standby, Stable CMOS Input Levels)		1.5		1.5	mA	$\bar{E} \geq (V_{CC} - 0.2V)$ All Others V <sub>IN</sub> ≤ 0.2V or ≥ (V <sub>CC</sub> - 0.2V)
I <sub>ILK</sub>	Input Leakage Current		±1		±1	µA	V <sub>CC</sub> = max V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>
I <sub>OLK</sub>	Off-State Output Leakage Current		±5		±5	µA	V <sub>CC</sub> = max V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub> , $\bar{E}$ or $\bar{G} \geq V_{IH}$
V <sub>IH</sub>	Input Logic "1" Voltage	2.2	V <sub>CC</sub> + .5	2.2	V <sub>CC</sub> + .5	V	All Inputs
V <sub>IL</sub>	Input Logic "0" Voltage	V <sub>SS</sub> - .5	0.8	V <sub>SS</sub> - .5	0.8	V	All Inputs
V <sub>OH</sub>	Output Logic "1" Voltage	2.4		2.4		V	I <sub>OUT</sub> = -4mA
V <sub>OL</sub>	Output Logic "0" Voltage		0.4		0.4	V	I <sub>OUT</sub> = 8mA
T <sub>A</sub>	Operating Temperature	0	70	-40	85	°C	

Note b: I<sub>CC1</sub> and I<sub>CC3</sub> are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

Note c: I<sub>CC2</sub> and I<sub>CC4</sub> are the average currents required for the duration of the respective STORE cycles (t<sub>STORE</sub>).

Note d:  $\bar{E} \geq V_{IH}$  will not produce standby current levels until any nonvolatile cycle in progress has timed out.

### AC TEST CONDITIONS

Input Pulse Levels . . . . .	0V to 3V
Input Rise and Fall Times . . . . .	≤ 5ns
Input and Output Timing Reference Levels . . . . .	1.5V
Output Load . . . . .	See Figure 1

### CAPACITANCE<sup>e</sup> (T<sub>A</sub> = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C <sub>IN</sub>	Input capacitance	8	pF	ΔV = 0 to 3V
C <sub>OUT</sub>	Output Capacitance	7	pF	ΔV = 0 to 3V

Note e: These parameters are guaranteed but not tested.

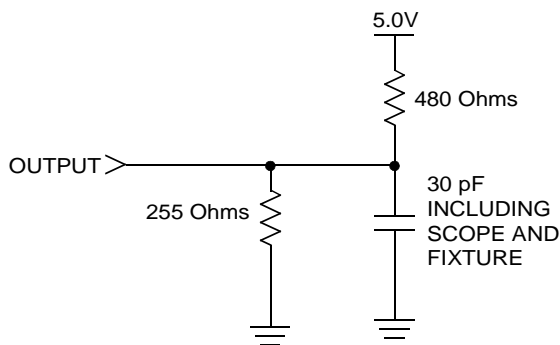


Figure 1: AC Output Loading

SRAM READ CYCLES #1 & #2

( $V_{CC} = 5.0V \pm 10\%$ )

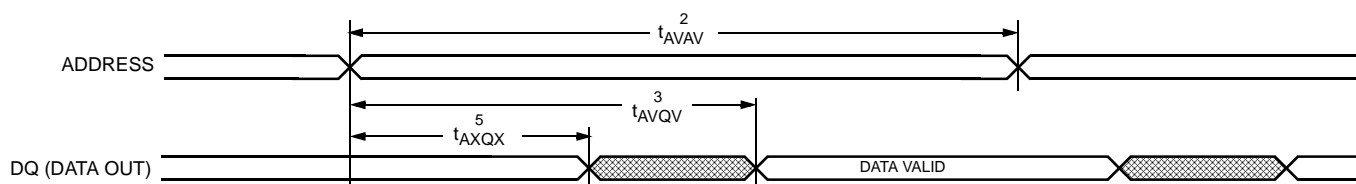
NO.	SYMBOLS		PARAMETER	STK15C68-25		STK15C68-35		STK15C68-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{ELQV}$	$t_{ACS}$	Chip Enable Access Time		25		35		45	ns
2	$t_{AVAV}^f$	$t_{RC}$	Read Cycle Time	25		35		45		ns
3	$t_{AVQV}^g$	$t_{AA}$	Address Access Time		25		35		45	ns
4	$t_{GLQV}$	$t_{OE}$	Output Enable to Data Valid		10		15		20	ns
5	$t_{AXQX}^g$	$t_{OH}$	Output Hold after Address Change	5		5		5		ns
6	$t_{ELQX}$	$t_{LZ}$	Chip Enable to Output Active	5		5		5		ns
7	$t_{EHQZ}^h$	$t_{HZ}$	Chip Disable to Output Inactive		10		13		15	ns
8	$t_{GLQX}$	$t_{OLZ}$	Output Enable to Output Active	0		0		0		ns
9	$t_{GHQZ}^h$	$t_{OHZ}$	Output Disable to Output Inactive		10		13		15	ns
10	$t_{ELICCH}^e$	$t_{PA}$	Chip Enable to Power Active	0		0		0		ns
11	$t_{EHICCL}^{d,e}$	$t_{PS}$	Chip Disable to Power Standby		25		35		45	ns

Note f:  $\bar{W}$  must be high during SRAM READ cycles and low during SRAM WRITE cycles.

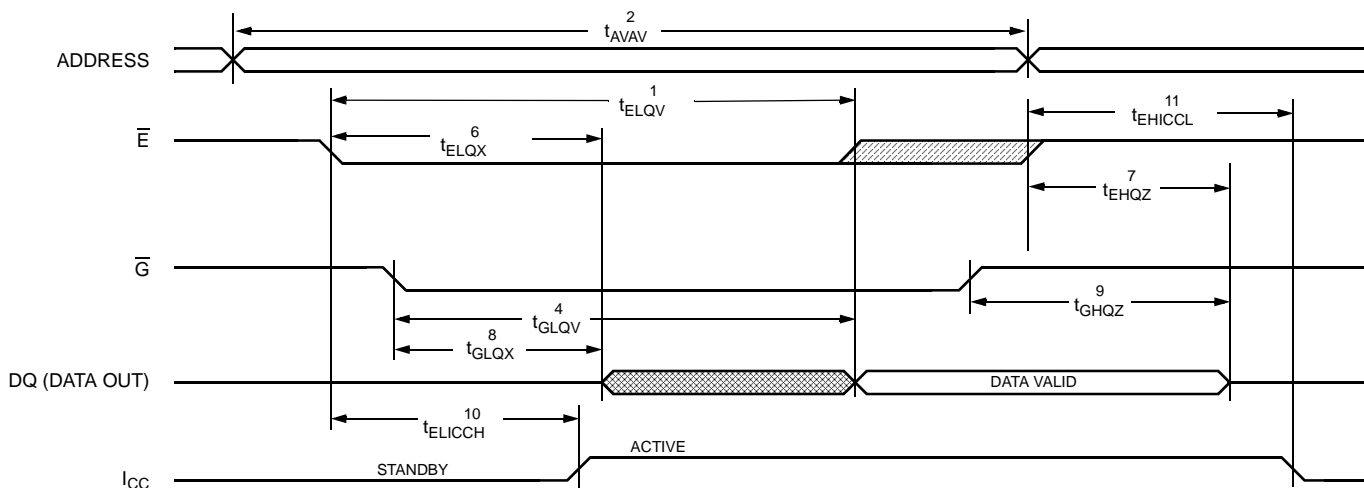
Note g: I/O state assumes  $\bar{E}, \bar{G} \leq V_{IL}$  and  $\bar{W} \geq V_{IH}$ ; device is continuously selected.

Note h: Measured  $\pm 200mV$  from steady state output voltage.

SRAM READ CYCLE #1: Address Controlled<sup>f, 9</sup>



SRAM READ CYCLE #2:  $\bar{E}$  Controlled<sup>f</sup>



SRAM WRITE CYCLES #1 & #2

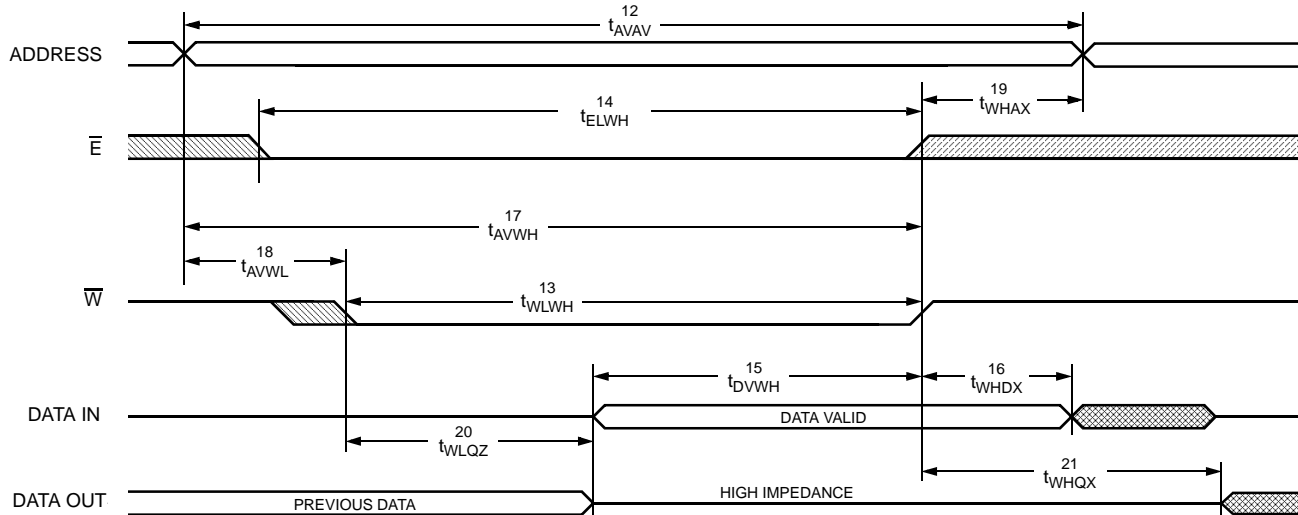
( $V_{CC} = 5.0V \pm 10\%$ )

NO.	SYMBOLS			PARAMETER	STK15C68-25		STK15C68-35		STK15C68-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	$t_{AVAV}$	$t_{AVAV}$	$t_{WC}$	Write Cycle Time	25		35		45		ns
13	$t_{WLWH}$	$t_{WLEH}$	$t_{WP}$	Write Pulse Width	20		25		30		ns
14	$t_{ELWH}$	$t_{ELEH}$	$t_{CW}$	Chip Enable to End of Write	20		25		30		ns
15	$t_{DVWH}$	$t_{DVEH}$	$t_{DW}$	Data Set-up to End of Write	10		12		15		ns
16	$t_{WHDX}$	$t_{EHDX}$	$t_{DH}$	Data Hold after End of Write	0		0		0		ns
17	$t_{AVWH}$	$t_{AVEH}$	$t_{AW}$	Address Set-up to End of Write	20		25		30		ns
18	$t_{AVWL}$	$t_{AVEL}$	$t_{AS}$	Address Set-up to Start of Write	0		0		0		ns
19	$t_{WHAX}$	$t_{EHAX}$	$t_{WR}$	Address Hold after End of Write	0		0		0		ns
20	$t_{WLQZ}^{h,i}$		$t_{WZ}$	Write Enable to Output Disable		10		13		15	ns
21	$t_{WHQX}$		$t_{OW}$	Output Active after End of Write	5		5		5		ns

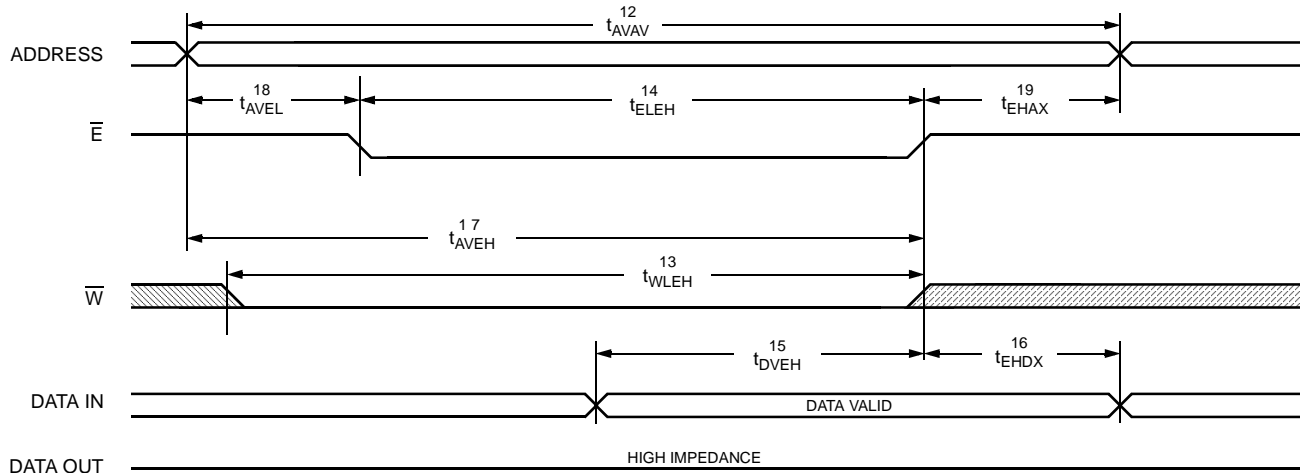
Note i: If  $\bar{W}$  is low when  $\bar{E}$  goes low, the outputs remain in the high-impedance state.

Note j:  $\bar{E}$  or  $\bar{W}$  must be  $\geq V_{IH}$  during address transitions.

SRAM WRITE CYCLE #1:  $\bar{W}$  Controlled<sup>j</sup>



SRAM WRITE CYCLE #2:  $\bar{E}$  Controlled<sup>j</sup>



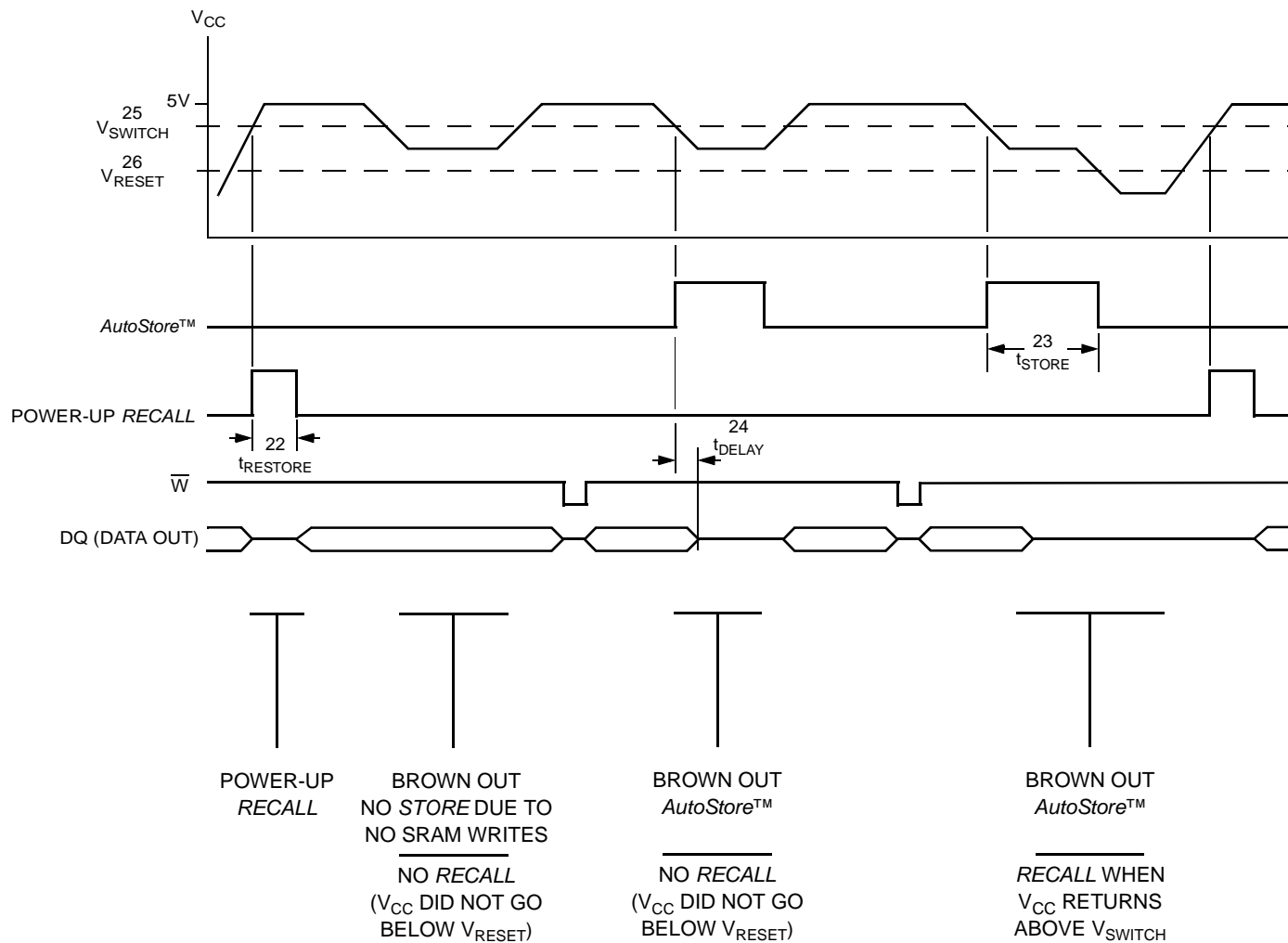
**AutoStore™/POWER-UP RECALL**

( $V_{CC} = 5.0V \pm 10\%$ )

NO.	SYMBOLS	PARAMETER	STK15C68		UNITS	NOTES
	Standard		MIN	MAX		
22	$t_{RESTORE}$	Power-up <i>RECALL</i> Duration		550	$\mu s$	k
23	$t_{STORE}$	<i>STORE</i> Cycle Duration		10	ms	g
24	$t_{DELAY}$	Time Allowed to Complete SRAM Cycle	1		$\mu s$	g
25	$V_{SWITCH}$	Low Voltage Trigger Level	4.0	4.5	V	
26	$V_{RESET}$	Low Voltage Reset Level		3.6	V	e

Note k:  $t_{RESTORE}$  starts from the time  $V_{CC}$  rises above  $V_{SWITCH}$ .

**AutoStore™/POWER-UP RECALL**



### SOFTWARE STORE/RECALL MODE SELECTION

$\bar{E}$	$\bar{W}$	$\bar{G}$	A <sub>12</sub> - A <sub>0</sub> (hex)	MODE	I/O with $\bar{G}$ Low	I/O with $\bar{G}$ High	NOTES
L	H	X	0000	Read SRAM	Output Data	Output High Z	I
			1555	Read SRAM	Output Data	Output High Z	
			0AAA	Read SRAM	Output Data	Output High Z	
			1FFF	Read SRAM	Output Data	Output High Z	
			10F0	Read SRAM	Output Data	Output High Z	
			0F0F	Nonvolatile STORE	Output High Z	Output High Z	
L	H	X	0000	Read SRAM	Output Data	Output High Z	I
			1555	Read SRAM	Output Data	Output High Z	
			0AAA	Read SRAM	Output Data	Output High Z	
			1FFF	Read SRAM	Output Data	Output High Z	
			10F0	Read SRAM	Output Data	Output High Z	
			0F0E	Nonvolatile RECALL	Output High Z	Output High Z	

Note I: The six consecutive addresses must be in the order listed.  $\bar{W}$  must be high during all six consecutive cycles to enable a nonvolatile cycle.

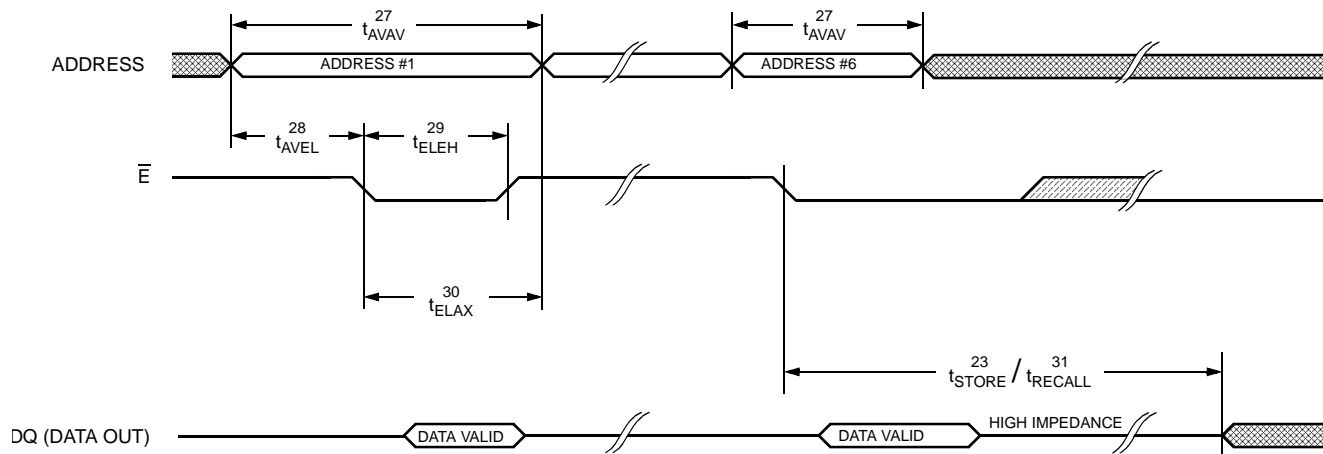
### SOFTWARE STORE/RECALL CYCLE<sup>m, n</sup> (V<sub>CC</sub> = 5.0V ± 10%)

NO.	SYMBOLS	PARAMETER	STK15C68-25		STK15C68-35		STK15C68-45		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
27	t <sub>AVAV</sub>	STORE/RECALL Initiation Cycle Time	25		35		45		ns
28	t <sub>AVEL</sub> <sup>m</sup>	Address Set-Up Time	0		0		0		ns
29	t <sub>ELEH</sub> <sup>m</sup>	Clock Pulse Width	20		25		30		ns
30	t <sub>ELAX</sub> <sup>g, m</sup>	Address Hold Time	20		20		20		ns
31	t <sub>RECALL</sub>	RECALL Cycle Duration		20		20		20	μs

Note m: The software sequence is clocked with  $\bar{E}$  controlled READs.

Note n: The six consecutive addresses must be in the order listed in the Software STORE/RECALL Mode Selection Table: (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a STORE cycle or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E) for a RECALL cycle.  $\bar{W}$  must be high during all six consecutive cycles.

### SOFTWARE STORE/RECALL CYCLE: $\bar{E}$ Controlled<sup>n</sup>



## DEVICE OPERATION

The STK15C68 is a versatile memory chip that provides several modes of operation. The STK15C68 can operate as a standard 8K x 8 SRAM. It has an 8K x 8 Nonvolatile Elements shadow to which the SRAM information can be copied, or from which the SRAM can be updated in nonvolatile mode.

### NOISE CONSIDERATIONS

Note that the STK15C68 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1 $\mu$ F connected between  $V_{CC}$  and  $V_{SS}$ , using leads and traces that are as short as possible. As with all high-speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

### SRAM READ

The STK15C68 performs a READ cycle whenever  $\overline{E}$  and  $\overline{G}$  are low and  $\overline{W}$  is high. The address specified on pins  $A_{0-12}$  determines which of the 8,192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of  $t_{AVQV}$  (READ cycle #1). If the READ is initiated by  $\overline{E}$  or  $\overline{G}$ , the outputs will be valid at  $t_{ELQV}$  or at  $t_{GLQV}$ , whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the  $t_{AVQV}$  access time without the need for transitions on any control input pins, and will remain valid until another address change or until  $\overline{E}$  or  $\overline{G}$  is brought high or  $\overline{W}$  is brought low.

### SRAM WRITE

A WRITE cycle is performed whenever  $\overline{E}$  and  $\overline{W}$  are low. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either  $\overline{E}$  or  $\overline{W}$  goes high at the end of the cycle. The data on the common I/O pins  $DQ_{0-7}$  will be written into the memory if it is valid  $t_{DVWH}$  before the end of a  $\overline{W}$  controlled WRITE or  $t_{DVEH}$  before the end of an  $\overline{E}$  controlled WRITE.

It is recommended that  $\overline{G}$  be kept high during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If  $\overline{G}$  is left low, internal circuitry will turn off the output buffers  $t_{WLQZ}$  after  $\overline{W}$  goes low.

### SOFTWARE NONVOLATILE STORE

The STK15C68 software *STORE* cycle is initiated by executing sequential READ cycles from six specific address locations. During the *STORE* cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for *STORE* initiation, it is important that no other READ or WRITE accesses intervene in the sequence or the sequence will be aborted and no *STORE* or *RECALL* will take place.

To initiate the software *STORE* cycle, the following READ sequence must be performed:

1. Read address	0000 (hex)	Valid READ
2. Read address	1555 (hex)	Valid READ
3. Read address	0AAA (hex)	Valid READ
4. Read address	1FFF (hex)	Valid READ
5. Read address	10F0 (hex)	Valid READ
6. Read address	0F0F (hex)	Initiate <i>STORE</i> cycle

The software sequence must be clocked with  $\overline{E}$  controlled READs.

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that  $\overline{G}$  be low for the sequence to be valid. After the  $t_{STORE}$  cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

### SOFTWARE NONVOLATILE RECALL

A software *RECALL* cycle is initiated with a sequence of READ operations in a manner similar to the software *STORE* initiation. To initiate the *RECALL* cycle, the following sequence of READ operations must be performed:

1. Read address	0000 (hex)	Valid READ
2. Read address	1555 (hex)	Valid READ
3. Read address	0AAA (hex)	Valid READ
4. Read address	1FFF (hex)	Valid READ
5. Read address	10F0 (hex)	Valid READ
6. Read address	0F0E (hex)	Initiate <i>RECALL</i> cycle

Internally, *RECALL* is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the  $t_{RECALL}$  cycle time the SRAM will once again be ready for READ and WRITE operations. The *RECALL* operation in no way alters the data in the Nonvolatile Elements. The nonvolatile data can be recalled an unlimited number of times.

**AutoStore™ OPERATION**

The STK15C68 uses the intrinsic system capacitance to perform an automatic store on power down. As long as the system power supply takes at least  $t_{STORE}$  to decay from  $V_{SWITCH}$  down to 3.6V, the STK15C68 will safely and automatically store the SRAM data in Nonvolatile Elements on power down.

In order to prevent unneeded *STORE* operations, automatic *STORE* will be ignored unless at least one WRITE operation has taken place since the most recent *STORE* or *RECALL* cycle. Software-initiated *STORE* cycles are performed regardless of whether a WRITE operation has taken place.

**POWER-UP RECALL**

During power up, or after any low-power condition ( $V_{CC} < V_{RESET}$ ), an internal *RECALL* request will be latched. When  $V_{CC}$  once again exceeds the sense voltage of  $V_{SWITCH}$ , a *RECALL* cycle will automatically be initiated and will take  $t_{RESTORE}$  to complete.

If the STK15C68 is in a WRITE state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected either between  $\bar{W}$  and system  $V_{CC}$  or between  $\bar{E}$  and system  $V_{CC}$ .

**HARDWARE PROTECT**

The STK15C68 offers hardware protection against inadvertent *STORE* operation and SRAM WRITES during low-voltage conditions. When  $V_{CC} < V_{SWITCH}$ , software *STORE* operations and SRAM WRITES are inhibited.

**LOW AVERAGE ACTIVE POWER**

The STK15C68 draws significantly less current when it is cycled at times longer than 50ns. Figure 2 shows the relationship between  $I_{CC}$  and READ cycle time. Worst-case current consumption is shown for both CMOS and TTL input levels (commercial temperature range,  $V_{CC}= 5.5V$ , 100% duty cycle on chip enable). Figure 3 shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK15C68 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READS to WRITES; 5) the operating temperature; 6) the  $V_{CC}$  level; and 7) I/O loading.

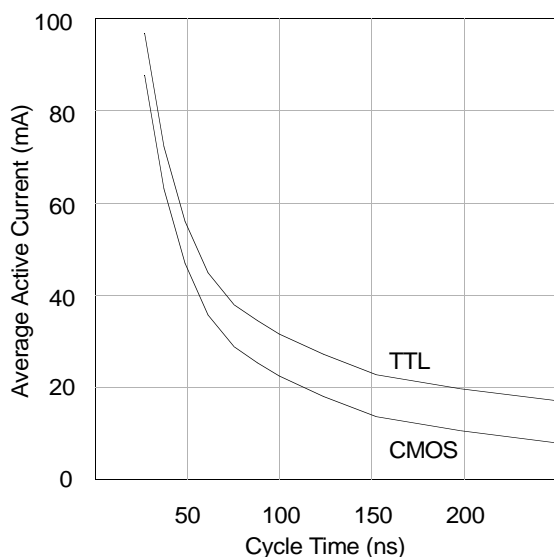


Figure 2:  $I_{CC}$  (max) Reads

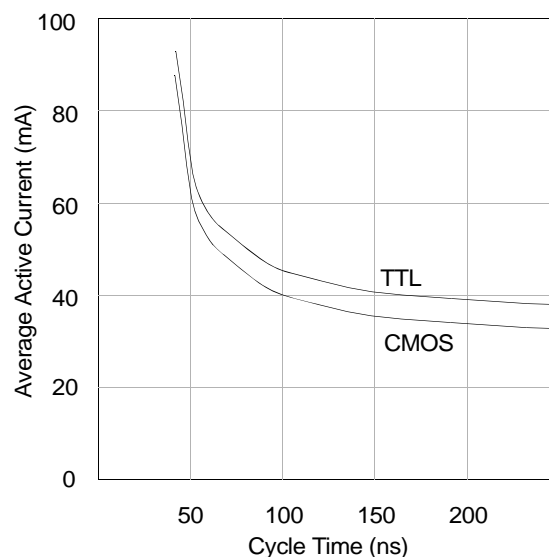
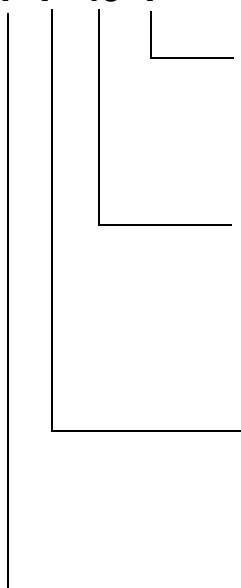


Figure 3:  $I_{CC}$  (max) Writes



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**ORDERING INFORMATION****STK15C68 - P F 45 I****Temperature Range**

Blank = Commercial (0 to 70°C)

I = Industrial (-40 to 85°C)

**Access Time**

25 = 25ns

35 = 35ns

45 = 45ns

**Lead Finish**

Blank = 85%Sn/15%Pb

F = 100% Sn (Matte Tin)

**Package**

W = Plastic 28-pin 600 mil DIP

P = Plastic 28-pin 300 mil DIP

S = Plastic 28-pin 350 mil SOIC

**Document Revision History**

Revision	Date	Summary
0.0	December 2002	
0.1	September 2003	Added lead-free lead finish
0.2	March 2006	Marked as Obsolete, Not recommended for new design.