THS6301 G.Fast DSL Line Driver

1 Features

- Designed for G.Fast 106-MHz, 212-MHz DSL Profiles
- Supports Legacy VDSL and ADSL2+ Applications
- Excellent MTPR for G.Fast and Legacy Applications (Line Power = 8 dBm):
  - ADSL2+ = 75 dB
  - VDSL-17a = 74 dB
  - VDSL-30a = 70 dB
  - G.Fast 106 MHz = 60 dB
  - G.Fast 212 MHz = 48 dB
- Multiple Power Modes for Different Profiles
- Adjustable Bias Current with External Resistor
- Low-Power Line Termination Mode: 10.2 mA
- Power-Down Mode
- 12-V Technology to Support High-Power Output

2 Applications

- G.Fast and Legacy DSL Line Drivers
- Generic Wideband Line Drivers

3 Description

The THS6301 is a current-feedback architecture, differential line driver designed for G.Fast and a variety of digital subscriber line (DSL) systems. The device is targeted for use in G.Fast digital subscriber line systems that enable native discrete multitone modulation (DMT) signals and supports an 8-dBm line power up to 212 MHz with good linearity.

The unique architecture of this device allows minimal quiescent current while still achieving very high linearity. Internally-fixed bias settings of the amplifier offer enhanced power savings for line-driving modes where the full performance of the amplifier is not required. To allow for even more flexibility and power savings, the overall quiescent current is adjustable by a single external bias resistor connected to one of the device pins. The device also features two line-termination modes to maintain impedance matching at very low power consumption.

The device is available in a 4-mm × 4-mm, 16-pin, VQFN package.

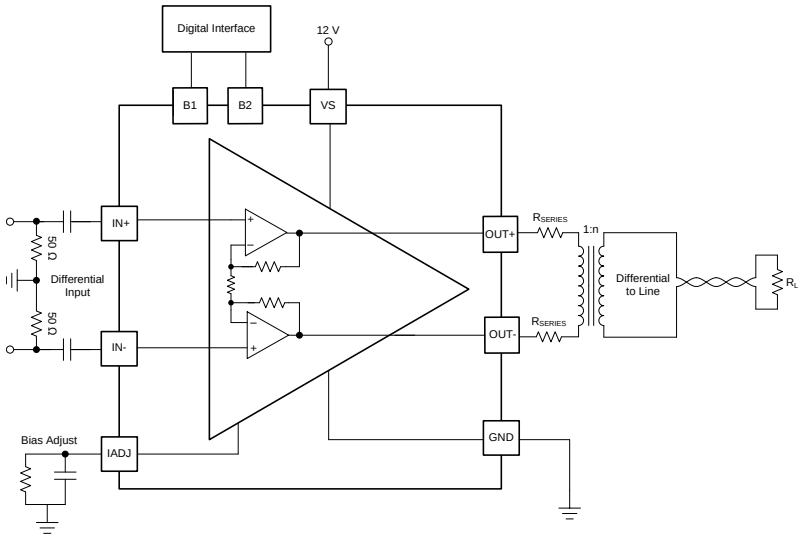
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
THS6301	VQFN (16)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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Multitone Power Ratio (MTPR) Profile (G.Fast, 212 MHz, 8 dBm)



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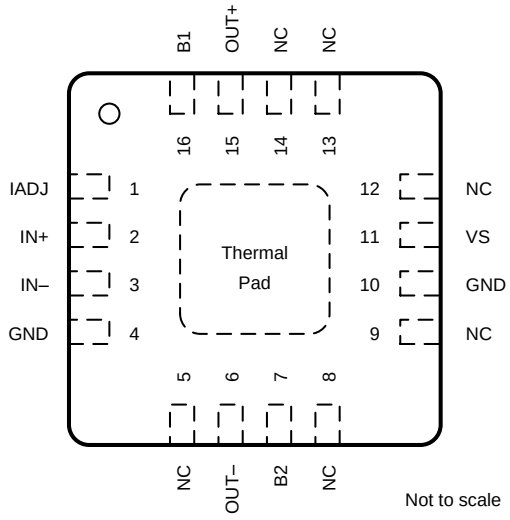
4 Revision History

DATE	REVISION	NOTES
April 2018	*	Initial release.

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5 Pin Configuration and Functions

RSA Package
16-Pin VQFN
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
B1	16	I	Most significant bit (MSB)
B2	7	I	Least significant bit (LSB)
GND	4, 10	—	Ground
IADJ	1	—	Bias current reference pin
IN–	3	I	Negative input
IN+	2	I	Positive input
NC	5, 8, 9, 12, 13, 14	—	Not connected
OUT–	6	O	Negative output
OUT+	15	O	Positive output
VS	11	—	Positive supply voltage connection
Thermal pad		—	Device thermal pad is dielectrically isolated from the die. Thus, the pad can be connected to either GND or to a different voltage within the supply voltage range.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	VS pin to GND (all modes)		13.2	V
Digital inputs to GND	B1, B2	–0.3	5.5	V
Analog inputs to GND	VIN+, VIN-	–0.3	12	V
Continuous power dissipation		See Thermal Information		
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		TBD	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins(1)	±2000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VS	Supply voltage	11.4	12	12.6	V
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		THS6301 RSA (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

at T_A = 25°C, VS = 12 V, GND = 0 V, voltage gain (A_V) = 8.5 V/V, R_{LOAD} = 100 Ω, R_{SERIES} = 47.5 Ω, R_{IREF} = 75 kΩ, C_{IREF} = 100 pF, G.Fast 106-MHz bias mode, and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE							
SSBW	Small-signal bandwidth	ADSL2+ bias mode		TBD		MHz	C
		VDSL mid-power bias mode		TBD			C
		G.Fast mid-power bias mode		TBD			C
		G.Fast high-power bias mode		1100			C
LSBW	Large-signal bandwidth	V_{OUT} = 15 V_{PP}, ADSL2+ bias mode		140		MHz	C
		V_{OUT} = 15 V_{PP}, VDSL mid-power bias mode		180			C
		V_{OUT} = 15 V_{PP}, G.Fast mid-power bias mode		220			C
		V_{OUT} = 15 V_{PP}, G.Fast high-power bias mode		320			C
	Gain flatness referenced to 1 MHz	ADSL2+ bias mode, 4 kHz to 2.208 MHz		±0.01		dB	C
		VDSL2 mid-power bias mode, 4 kHz to 17.6 MHz		±0.05			C
		VDSL2 mid-power bias mode, 4 kHz to 30 MHz		±0.1			C
		G.Fast mid-power bias mode, 4 kHz to 106 MHz		±0.25			C
		G.Fast high-power bias mode, 4 kHz to 212 MHz		±0.5			C
SR	Slew rate	ADSL2+ bias mode, 10%-90% 15-V_{PP} pulse	4300	5100		V/µs	B
		VDSL2 mid-power, 10%-90% 15-V_{PP} pulse	4900	6600			B
		VDSL2 high-power, 10%-90% 15-V_{PP} pulse	4900	6600			B
		G.Fast mid-power bias mode, 10%-90% 15-V_{PP} pulse	5400	7400			B
		G.Fast high-power bias mode, 10%-90% 15-V_{PP} pulse	8500	10600			B
e_n	Input-referred voltage noise	f > 100 kHz, ADSL2+ bias mode		4.3		nV/√Hz	C
		f > 100 kHz, VDSL2 mid-power bias mode		3.9			C
		f > 100 kHz, VDSL2 high-power bias mode		3.9			C
		f > 100 kHz, G.Fast mid-power bias mode		3.7			C
		f > 100 kHz, G.Fast high-power bias mode		3.5			C
	Noise floor, line termination mode	Line-termination modes, referred to R_{SERIES}		–158	–155	dBm/Hz	B
		Power-down mode, referred to R_{SERIES}		–170			C
	ADSL2+ MTPR	Line power = 8 dBm, f ≤ 552 kHz, PAR = TBD	73			dB	B
		Line power = 8 dBm, f ≤ 1.104 MHz, PAR = TBD	72				B
		Line power = 8 dBm, f ≤ 2.208 MHz, PAR = TBD	69				B
	VDSL2-17a MTPR	Line power = 8 dBm, f ≤ 14 MHz, PAR = TBD	70			dB	B
		Line power = 8 dBm, f ≤ 17.6 MHz, PAR = TBD	68				B
	VDSL2-30a MTPR	Line power = 8 dBm, f ≤ 30 MHz, PAR = TBD	70			dB	B
	VDSL2-35b MTPR	Line power = 4 dBm, f ≤ 106 MHz, PAR = TBD	TBD			dB	B
	G.Fast 106-MHz MTPR	Line power = 4 dBm, f ≤ 106 MHz, PAR = TBD	65			dB	B
		Line power = 8 dBm, f ≤ 106 MHz, PAR = 15 dB	60	63.5			B
		Line-termination mode, line power = 8 dBm, PAR = TBD		60			D
	G.Fast 212-MHz MTPR	Line power = 4 dBm, f ≤ 212 MHz, PAR = 15 dB	60	63		dB	B
		Line power = 8 dBm, f ≤ 212 MHz, PAR = 15 dB	50	55			B
		Line-termination mode, line power = 4 dBm, PAR = TBD		48			D

(1) Test levels (all values set by characterization and simulation): (A) 100% tested at T_A ≈ 25°C. (B) Not tested in production; limits set by characterization and simulation. (C) Typical value only for information. (D) Simulated value only for information.

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Electrical Characteristics (continued)

at T_A = 25°C, VS = 12 V, GND = 0 V, voltage gain (A_V) = 8.5 V/V, R_{LOAD} = 100 Ω, R_{SERIES} = 47.5 Ω, R_{IREF} = 75 kΩ, C_{IREF} = 100 pF, G.Fast 106-MHz bias mode, and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL (1)
	Differential output impedance	G.Fast high-power bias mode, f = 100 kHz		TBD		Ω	C
		G.Fast high-power bias mode, f = 50 MHz		1.6			C
		G.Fast high-power bias mode, f = 106 MHz		3.6			C
		G.Fast high-power bias mode, f = 212 MHz		10			C
		Power-down bias mode		2800			C
		Line-termination modes		TBD			C
DC PERFORMANCE							
A_V	Differential gain	At dc, no load, all modes	TBD	8.5	TBD	V/V	A
	Differential output offset	G.Fast mid-power bias mode	TBD		TBD	mV	A
	Maximum output swing	Differential, at dc, 200-Ω load at amplifier output		18.5		V_{PP}	A
	Linear output current	ADSL2+ bias mode, sourcing, output offset < 20-mV deviation		50		mA	A
		ADSL2+ bias mode, sinking, output offset < 20-mV deviation		50			A
		G.Fast high-power bias mode, sourcing, output offset < 20-mV deviation		90			A
		G.Fast high-power bias mode, sinking, output offset < 20-mV deviation		90			A
		High-power receive mode, sourcing, output offset < 20-mV deviation		60			A
		High-power receive mode, sinking, output offset < 20-mV deviation		60			A
		Low-power receive mode, sourcing, output offset < 20-mV deviation		50			A
		Low-power receive mode, sinking, output offset < 20-mV deviation		50			A
COMMON MODE							
	Input CM bias voltage			6		V	A
	Output CM bias voltage			6		V	A
POWER SUPPLY							
	Supply voltage range	All modes	11.4	12	12.6	V	A
PSRR	Power-supply rejection ratio	f = dc	TBD			dB	A
I_Q	Quiescent current	ADSL2+ bias mode		15.1		mA	A
		VDSL2 low-power bias mode		19.4			A
		VDSL2 mid-power bias mode		26.5			A
		VDSL2 high-power, G.Fast low-power bias mode		29.2			A
		G.Fast mid-power bias mode		38.2			A
		G.Fast high-power bias mode		44.8			A
		Line-termination high-power mode		15.1			A
		Line-termination low-power mode		9.2			A
		Power-down bias mode		1.9			A

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Electrical Characteristics (continued)

at T_A = 25°C, VS = 12 V, GND = 0 V, voltage gain (A_V) = 8.5 V/V, R_{LOAD} = 100 Ω, R_{SERIES} = 47.5 Ω, R_{IREF} = 75 kΩ, C_{IREF} = 100 pF, G.Fast 106-MHz bias mode, and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL (1)
Dynamic power consumption	ADSL2+ bias mode, line power = 8 dBm		220		mW	C
	VDSL2 low-power bias mode, line power = 8 dBm		280			C
	VDSL2 mid-power bias mode, line power = 8 dBm		340			C
	VDSL2 high-power, G.Fast low-power bias mode, line power = 8 dBm		375			C
	G.Fast mid-power bias mode, line power = 4 dBm		470			C
	G.Fast high-power bias mode, line power = 8 dBm		600			C
	Line-termination high-power mode, line power = 4 dBm		190			C
	Line-termination low-power mode, line power = 4 dBm		120			C
	Power-down bias mode		23			C

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Minimum logic high level	All digital pins, high	2.3			V
V_{IL}	Maximum logic low level	All digital pins, low			0.6	V
V_{MID}	Logic mid range	All digital pins, driven externally	1.2		1.6	V
V_{Float}	Logic self-bias voltage	All digital pins, floating	1.3	1.4	1.5	V
I_{IH}	Logic high-level leakage current	All digital pins, logic level = 3.6 V		110	135	µA
I_{IL}	Logic low-level leakage current	All digital pins, logic level = ground	–85	–75		µA
Turn-on switching time		Line-termination mode (bias 00) to G.Fast 212-MHz mode (bias 10)		64		ns
		Line-termination mode (bias Z0) to G.Fast 212-MHz mode (bias 10)		50		
		Power-down mode (bias ZZ) to G.Fast 212-MHz mode (bias 10)		60		
Turn-off switching time		G.Fast 212-MHz mode (bias 10) to line-termination mode (bias 00)		76		ns
		G.Fast 212-MHz mode (bias 10) to line-termination mode (bias Z0)		400		
		G.Fast 212-MHz mode (bias 10) to power-down mode (bias ZZ)		380		

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7 Detailed Description

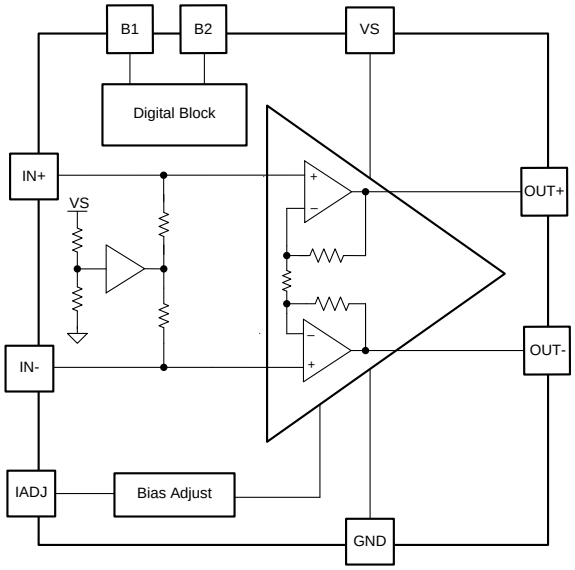
7.1 Overview

The THS6301 is a current-feedback architecture, differential line driver designed for G.Fast and xDSL systems. The device is targeted for use in G.Fast digital subscriber line (DSL) systems that enable native discrete multitone modulation (DMT) signals and supports an 8-dBm line power up to 212 MHz with good linearity.

The device consists of a unique architecture consisting of an amplifier in a noninverting configuration with an internally-fixed gain of 8.5 V/V. The THS6301 is designed to drive the high-performance G.Fast 212-MHz DSL profile, but is also backwards-compatible to drive lower frequency profiles. The device features selectable bias modes for the G.Fast 106-MHz profile, VDSL profiles, and ADSL profiles. These modes reduce the quiescent current of the device based on the frequency requirements of the various DSL profiles to maximize power efficiency. Along with adjustable bias modes, the device features two line-termination modes that maintain an output impedance match with low power consumption. The line-termination modes allow for the device to be in a low-power state without causing distortion on a shared signal line.

For further flexibility, the THS6301 features an IADJ pin that is used to further adjust the quiescent current of the device. A resistor connected to this pin can be changed to increase or decrease the device current to meet performance requirements and uses the lowest amount of power possible.

7.2 Functional Block Diagram



7.3 Feature Description

The THS6301 is a line driver that has a high current drive and a differential input and output. Figure 1 shows an example circuit of the THS6301 configured to drive the G.Fast 212-MHz DSL profile. The bias control pins B1 and B2 are set to 3.3 V and ground, respectively, to put the device in the G.Fast 212-MHz bias mode. This bias mode optimizes the internal power consumption of the device to meet performance specifications of the G.Fast 212-MHz profile and can be changed to meet several different DSL profiles and other modes listed in Table 1. The IADJ pin is biased with a 75-kΩ (R_{IADJ}) resistor that adjusts the device quiescent current to a nominal state. R_{IADJ} can be increased to lower the quiescent current or decreased to raise the quiescent current of the device for fine-tuning. C_{IADJ} provides decoupling for the IADJ pin and is typically 100 pF.

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Feature Description (continued)

The THS6301 has a 10-kΩ, internally-set differential input impedance and low output impedance. In Figure 1 the input impedance is matched to 100 Ω by using a 100-Ω resistor connected differentially across the inputs. This value can easily be changed by using a different resistor to create the desired impedance at the input. Remember that the impedance in the device is actually the parallel combination of 10 kΩ and the external input resistor. For low impedances, this effect is minimal, but must be considered if the matched input impedance is increased. The output impedance of the THS6301 in Figure 1 is set by the two R_{SERIES} resistors to match 100 Ω. The internal output resistance is very low (< 2 Ω per output), so the output impedance is primarily set by the R_{SERIES} resistors. These resistors can be adjusted to match various output impedance values.

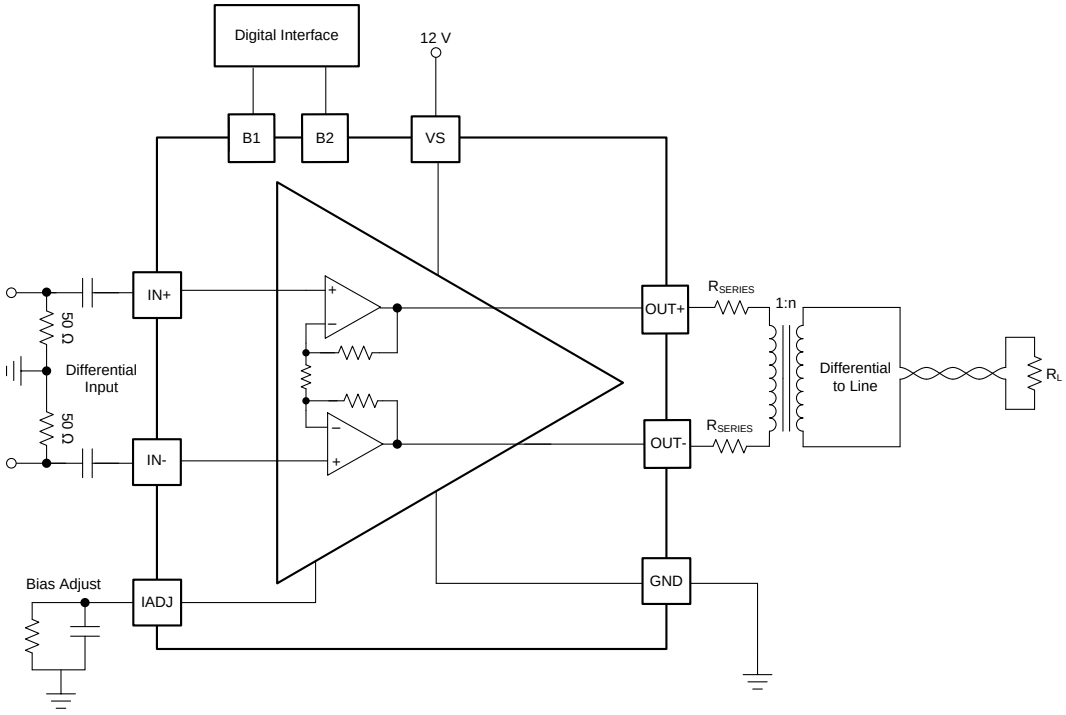


Figure 1. G.Fast, 212-MHz Driving Mode Example Circuit

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7.4 Device Functional Modes

The THS6301 features nine different device operational modes, as listed in Table 1, to accommodate the G.Fast, xDSL, line termination, and power-down scenarios. The device is controlled by a 2-pin parallel interface that uses three-level logic to control the device state. The G.Fast and xDSL modes change the quiescent current of the device to meet signal performance requirements and maintain the lowest power possible, which allows for legacy DSL compatibility with maximum power efficiency. The two line-termination modes maintain a low impedance at the output and place the device in a low-power state. The line-termination modes allow for the muxing of multiple devices to one output line by putting the non-driving devices in a state that does not add distortion to the line. A power-down mode is also included to digitally shut down the device for the highest level of power savings. Table 1 lists the device power modes and the typical quiescent currents for each mode.

Table 1. Bias Modes Truth Table

BIAS CONTROL PINS		BIAS MODE DESCRIPTION	TYPICAL QUIESCENT CURRENT (mA)
B1	B2		
0	0	Line termination, high power	16
Z	0	Line termination, low power	10.2
1	0	G.Fast 212 MHz	45.3
0	Z	ADSL2+	15.9
Z	Z	Power down	1.91
1	Z	Alternate VDSL (high power)	29.8
0	1	Alternate G.Fast 106 MHz (low power)	38.9
Z	1	VDSL	20.1
1	1	G.Fast 106 MHz	27.2

7.5 Programming

The THS6301 programming is controlled by two parallel pins, B1 and B2. These pins use three-level logic to create nine different combinations for each pair of pins. The pins have a high state (*1*) when the pin voltage is greater than 2.3 V, a low state (*0*) when the pin voltage is less than 0.6 V, and an open state (*Z*) where the pin floats at approximately 1.4 V or can be driven between 1.2 V and 1.6 V. Table 1 lists the logic combinations for the two pins and the corresponding power modes.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device is a single-port, very-high-bit-rate linear xDSL, G.Fast differential line driver where the device drives a twisted pair cable. The signal is generated by a high-speed, digital-to-analog converter (DAC) at low signal swings that is amplified by the G.Fast line driver.

The G.Fast system is ac-coupled when transmitting information above the audio band. On the input of the line driver, this ac-coupling translates into the series capacitors to isolate the dc voltage coming from the DAC output common-mode voltage. On the output, a transformer is used to help isolate the 48 V present between the tip and ring of the telephone line.

The transformer can be set to any useful ratio. In practice, the transformer-turn ratio is set between 1:1 and 1:1.4 for the device. The output transformer usually has the active impedance synthesis factor set to 5. This synthesis factor means that the termination resistor (R_T) is 1/5th of the load impedance reflected to the transformer secondary. Thus, the correct termination can be selected based on the transformer-turn ratio.

Note that the resulting load detected by the amplifier may affect the amplifier linearity or output voltage swing capabilities.

8.2 Typical Application

Figure 2 shows a typical application circuit for this device.

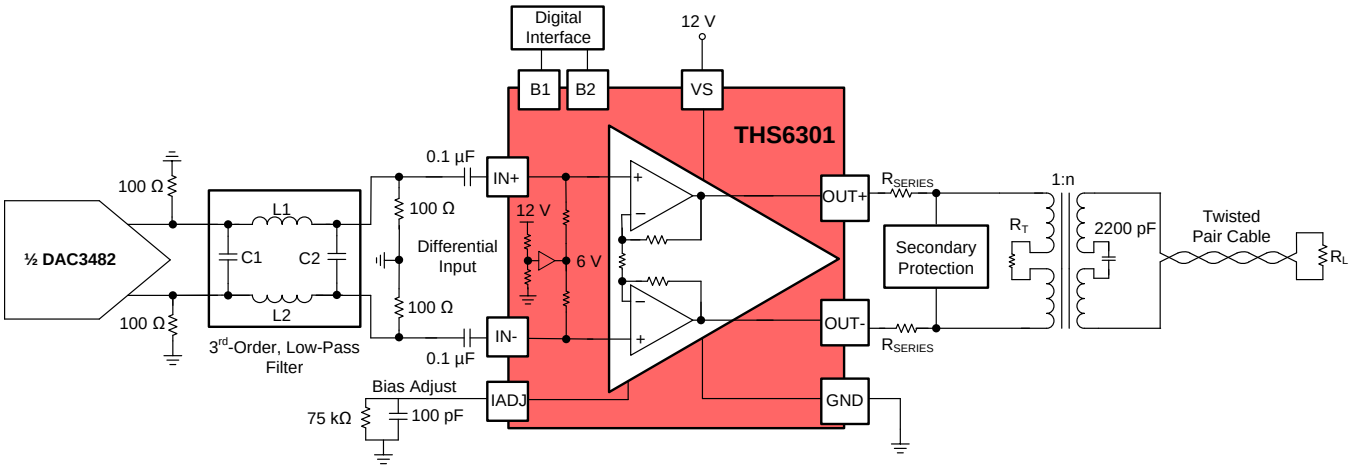


Figure 2. Typical G.FAST Line Driver Configuration

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Typical Application (continued)

8.2.1 Design Requirements

Table 2 provides the design requirements for a G.Fast line driver, which is met by the THS6301 device.

Table 2. Design Requirements

DESIGN REQUIREMENT	CONDITION
G.Fast, 106-MHz, 212-MHz transmit profile	Yes, using the bias control pins for line power = 8 dBm and PAR = 15 dBm
Legacy DSL profile support	Yes
Supply voltage	12 V
Output current drive	±80 mA, each output
Power-down functionality	High isolation from input to output
Input interface	AC coupled
Output transformer ratio	1:1.5
Surge protection	External needed

8.2.2 Detailed Design Procedure

The G.Fast signal input to the THS6301 comes from a high-speed DAC whose interleaving spurs are filtered out using either a 3rd- or 5th-order filter. Digital pre-emphasis can be employed in the DAC output such that the differential line driver compensates for the transmission line cable losses at long distance and high frequency. The THS6301 is operated on a 12-V single supply. Resulting from the single-supply operation, the device input is AC-coupled using a capacitor that blocks any DC current flowing out of the inputs to the adjacent circuitry. The AC-coupling capacitor forms a high-pass filter with the device input impedance. This pole must be set at a frequency low enough to not interfere with the desired xDSL or G.Fast signal.

The THS6301 differential outputs usually drive a 1:n output transformer with a transformer turns ratio that can be changed depending upon the application. The output transformer selected must have low insertion loss in the desired frequency band in order to maintain good multi-tone power rejection (MTPR) for a given line power. The load is expected to be a transmission line with 100-Ω characteristic impedance on the primary side of the transformer. Referred to the transformer secondary, the load detected by the amplifier is $1 / n^2$ with 1:n being the transformer turn ratio. Practical limitations force the transformer-turn ratio to be between 1:1 and 1:1.6. At the lighter load detected by the amplifier (1:1), the voltage swing is limited by the class AB output stage and the maximum achievable swing of the amplifier. At the heaviest load (1:1.6), the voltage swing is limited by the current drive capability of the amplifier. To satisfy the synthesis impedance factor and the loading, the termination resistance (R_T) can be set to $R_T = R_L / 5 = 100\ \Omega / (5 \times n^2)$.

For surge protection, consider adding a gas discharge tube (GDT) on the primary side of the output transformer. The gas discharge tube is required to shunt the large current that could flow through the cables during lightning surge, and protect the device outputs. The secondary protection is also normally added after the series resistance on the secondary transformer side. The secondary protection could be in the form of back to back switching diodes, which also help limit the residual surge current flowing into the device outputs.

For the power-supply bypass, consider using X7R or X5R because of the better stability of these materials over temperature.

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9 Power Supply Recommendations

The THS6301 is recommended to operate using a total supply voltage of 12 V. If a lower or higher supply voltage is required, select one that is between 11.4 V and 12.6 V for optimal performance. Use supply-decoupling capacitors on the power-supply pins to minimize distortion caused by parasitic signals on the power supply. This usage is especially important in applications where many devices share a single power-supply bus.

The device can be operated on split supplies (such as ±6 V). However, the bias adjust resistor must be tied to the negative supply for proper device operation. When operating the device on split supply, pins 4 and 10 act as the negative supply voltage pin. The thermal pad must be tied to either GND or the negative supply voltage in split-supply operation. The device bias mode pins are now referenced to the negative supply voltage for the different logic levels.

10 Layout

10.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the THS6301 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

a. Minimize parasitic capacitance to any ac ground for all signal I/O pins. Excessive parasitic capacitance on the input pin can cause instability. In the line driver application, the parasitic capacitance forms a pole with the load detected by the amplifier and can reduce the effective bandwidth of the application circuit, thus leading to degraded performance. To reduce unwanted capacitance, open a window around the signal I/O pins in all ground and power planes around those pins. Otherwise, make sure that ground and power planes are unbroken elsewhere on the board.

b. Minimize the distance (< 0.25") from the power-supply pins to high-frequency, 0.1-µF decoupling capacitors. At the device pins, make sure that the ground and power-plane layout are not in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and decoupling capacitors. Always decouple the power-supply connections with these capacitors.

c. Make sure the bias adjust resistor connected to the IADJ pin is not routed close to the device inputs in-order to avoid any high-frequency noise coupling into the IADJ pin and result in unexpected device behavior.

d. Careful selection and placement of external components preserves the high-frequency performance of the device. Use very-low reactance-type resistors. Surface-mount resistors function best and allow a tighter overall layout. Metal-film or carbon composition, axially-leaded resistors also provide good high-frequency performance. Again, keep the leads and printed circuit board (PCB) traces as short as possible. Never use wire-wound type resistors in a high-frequency application.

e. Connections to other wideband devices on the board can be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Use relatively wide traces (50 mils to 100 mils), preferably with ground and power planes opened up around them.

f. Do not socket a high-speed part such as the THS6301. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that makes achieving a smooth, stable frequency response almost impossible. Best results are obtained by soldering the device onto the board.

g. TI recommends soldering the thermal pad to the PCB in order to conduct heat out of the device package. Vias underneath the part help regulate the flow of free air and also help conduct heat out of the package.

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Layout Guidelines (continued)

10.1.1 Power Dissipation and Thermal Considerations

For maximum performance and reliability, the designer must ensure that the design does not exceed a junction temperature of 125°C. Between 125°C and 150°C, damage does not occur, but the performance of the amplifier begins to degrade and long-term reliability suffers. The thermal characteristics of the device are dictated by the package and the PCB. Equation 1 calculates maximum power dissipation for a given package:

$$P_{D(MAX)} = (T_{J(MAX)} – T_A) / R_{\theta JA} \quad (1)$$

where

- $P_{D(MAX)}$ is the maximum power dissipation in the amplifier (W)
- $T_{J(MAX)}$ is the absolute maximum junction temperature (°C)
- T_A is the ambient temperature (°C)
- $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$
- $R_{\theta JC}$ is the thermal coefficient from silicon transistors to the case (°C/W)
- $R_{\theta CA}$ is the thermal coefficient from case to ambient temperature (°C/W)

For systems where heat dissipation is more critical, the THS6301 is offered in an 16-pin VQFN package with thermal pad. Because of the thermal pad, the thermal coefficient for the VQFN package is substantially improved over the traditional SOIC. The data for the VQFN packages with thermal pad assume a board layout that follows the thermal pad layout guidelines referenced in this section and detailed in the *Quad Flatpack No-Lead Logic Packages* application note. If the thermal pad is not soldered to the PCB, the thermal impedance increases substantially, which may cause serious heat and performance issues. Be sure to always solder the thermal pad to the PCB for optimum performance.

When determining whether or not the device satisfies the maximum power dissipation requirement, consider not only quiescent power dissipation, but also dynamic power dissipation. Often times, this dissipation is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

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10.2 Layout Example

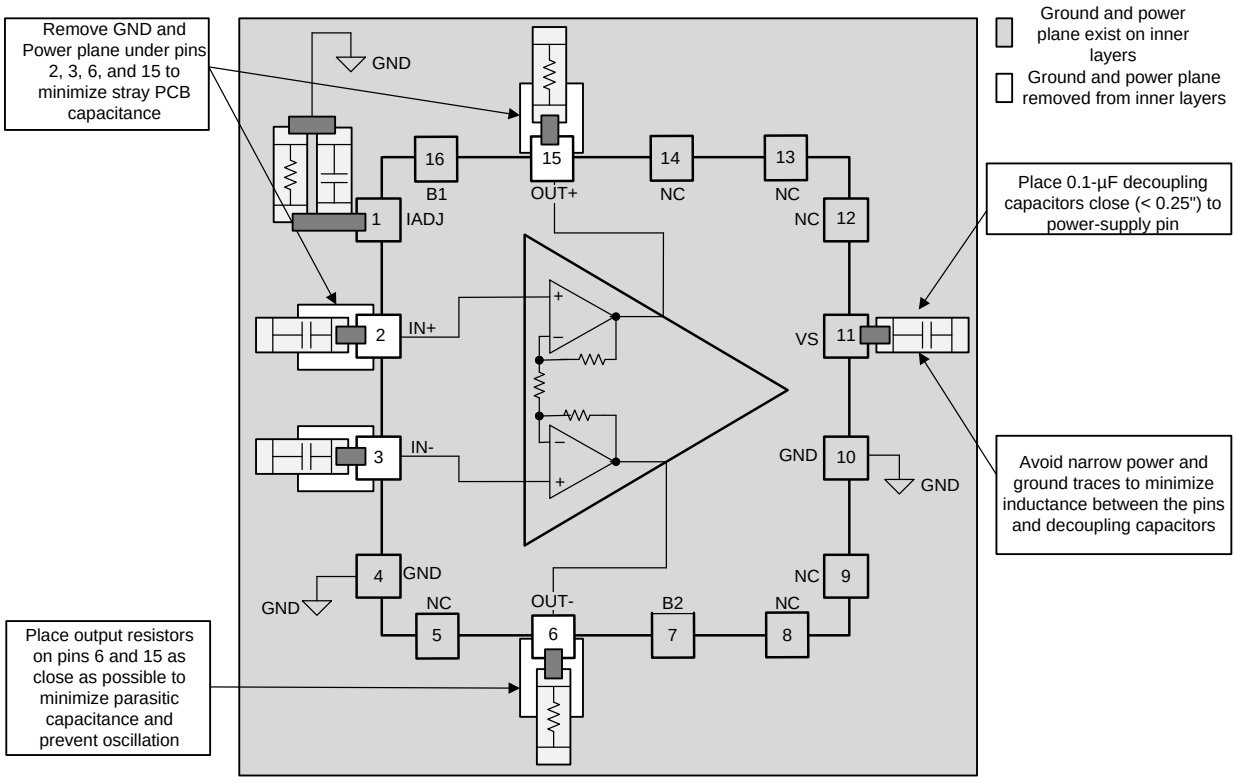


Figure 3. Example Layout

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Quad Flatpack No-Lead Logic Packages* Application Note
- *Active output impedance for ADSL line drivers* Application Note

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS6301IRSAR	PREVIEW	QFN	RSA	16	3000	TBD	Call TI	Call TI	-40 to 85		
THS6301IRSAT	PREVIEW	QFN	RSA	16	250	TBD	Call TI	Call TI	-40 to 85		
XTHS6301IRSAT	ACTIVE	QFN	RSA	16	250	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

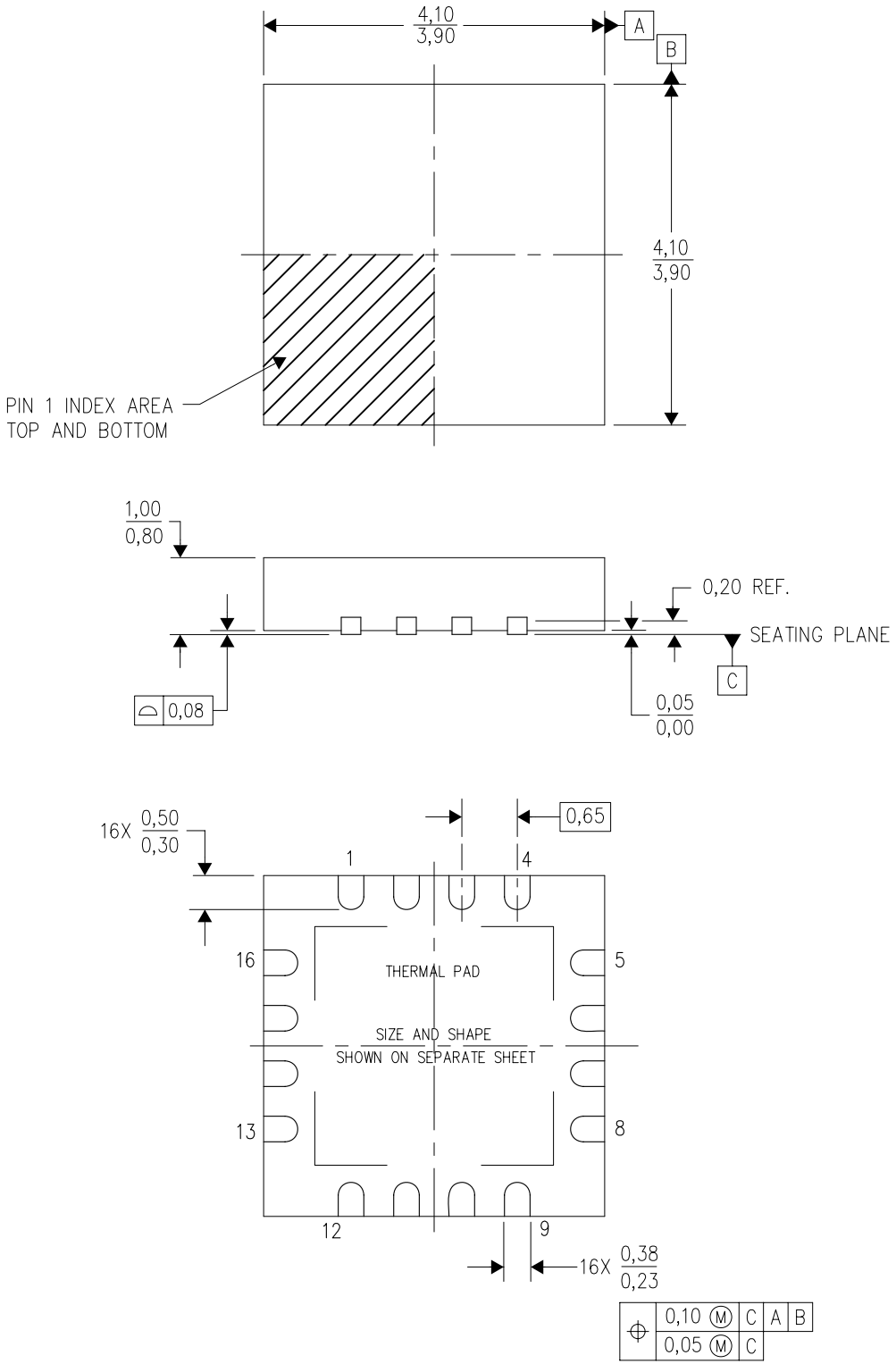
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

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