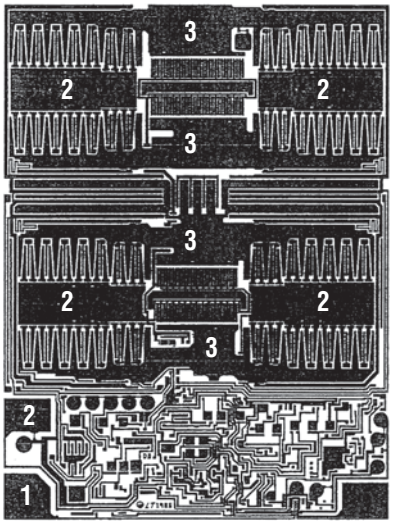
LINEAR TECHNOLOGY

DICE/DWF SPECIFICATION

RH1083CK
7.5A Low Dropout Positive Adjustable Regulator



160mils × 121mils
Backside metal: Alloyed gold layer
Backside potential: substrate to Pad 2

PAD FUNCTION

1. ADJUST
2. V_{OUT}
3. V_{IN}

DIE CROSS REFERENCE

LTC Finished Part Number	Order DICE CANDIDATE Part Number Below
RH1083CK RH1083CK	RH1083CK DICE RH1083CK DWF*

Please refer to LTC standard product data sheet for other applicable product information.
***DWF = DICE in wafer form.**

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DICE/DWF ELECTRICAL TEST LIMITS

PARAMETER	CONDITIONS	NOTES	MIN	MAX	UNITS
Reference Voltage	I_{OUT} = 10mA, (V_{IN} – V_{OUT}) = 3V		1.238	1.262	V
	10mA ≤ I_{OUT} ≤ 50mA 1.5V ≤ (V_{IN} – V_{OUT}) ≤ 25V		1.225	1.270	V
Line Regulation	I_{OUT} = 10mA, 1.5V ≤ (V_{IN} – V_{OUT}) ≤ 15V 15V ≤ (V_{IN} – V_{OUT}) ≤ 30V	1, 2		0.2 0.5	% %
Load Regulation	(V_{IN} – V_{OUT}) = 3V 10mA ≤ I_{OUT} ≤ 50mA	1, 2		0.35	%
Dropout Voltage	ΔV_{REF} = 1%, I_{OUT} = 50mA	3		1.5	V
Current Limit	(V_{IN} – V_{OUT}) = 5V		8		A
Minimum Load Current	(V_{IN} – V_{OUT}) = 25V			10	mA
ADJUST Pin Current	T_J = 25°C			120	µA
ADJUST Pin Current Change	10mA ≤ I_{OUT} ≤ 50mA 1.5V ≤ (V_{IN} – V_{OUT}) ≤ 25V			5	µA

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

DICE/DWF ELECTRICAL TEST LIMITS

Note 1: See the LT®1083 data sheet thermal regulation specifications for changes in output voltage due to heating effects. Line and load regulation are measured at a constant junction temperature by low duty cycle pulse testing.

Note 2: Power dissipation is determined by the input/output differential voltage and the output current.

Note 3: Dropout voltage is tested at 50mA but guaranteed over the full output current range of the device. Test points and limits are shown on the Dropout Voltage curve in the LT1083 data sheet.

Rad Hard die require special handling as compared to standard IC chips.

Rad Hard die are susceptible to surface damage because there is no silicon nitride passivation as on standard die. Silicon nitride protects the die surface from scratches by its hard and dense properties. The passivation on Rad Hard die is silicon dioxide that is much “softer” than silicon nitride.

LTC recommends that die handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die around from the chip tray, use a Teflon-tipped vacuum wand. This wand can be made by pushing a small diameter Teflon tubing onto the tip of a steel-tipped wand. The inside diameter of the Teflon tip should match the die size for efficient pickup. The tip of the Teflon should be cut square and flat to ensure good vacuum to die surface. Ensure the Teflon tip remains clean from debris by inspecting under stereoscope.

During die attach, care must be exercised to ensure no tweezers touch the top of the die.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

I.D.No. 66-13-1083ck

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

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