MP2735/MP2736

Low-Voltage 0.45Ω Dual SPDT Analog Switches

The Future of Analog IC Technology

GENERAL DESCRIPTION

The MP2735/MP2736 are low voltage, low on-resistance, dual single-pole , double-throw (SPDT) monolithic CMOS analog switches designed for high performance switching of analog signals. Combining low-power, high speed, low on-resistance, and small package size, the MP2735/MP2736 are ideal for portable and battery power applications.

The MP2735/MP2736 have an operation range from 1.65V to 5.5V single supply. The MP2735 has two separate control pins and two separate SPDT switches. The MP2736 includes an $\overline{EN}$ pin. All switches are at high impedance mode when the $\overline{EN}$ is high.

The MP2735/MP2736 are guaranteed 1.65V logic compatible for V+<3.3V, allowing the easy interface with low voltage DSP or MCU control logic and ideal for one cell Li-ion battery direct power.

The switch conducts signals within power rails equally well in both directions when on, and blocks up to the power supply level when off. Break-before-make is guaranteed.

The MP2735/MP2736 are offered in a QFN10 package.

FEATURES

- Low Voltage Operation (1.65V to 5.5V)
- Low On-Resistance - R_{ON}: 0.45Ω at 2.7V
- Fast Switching: T_{ON} = 29ns at 2.7V
- T_{OFF} = 23ns at 2.7V
- Latch-Up Current >300mA (JESD78)
- 1.4mm x 1.8mm QFN10 Package
- ESD Human-Body Model ±4000V

APPLICATIONS

- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Powered Systems
- Portable Media Player
- Handheld Test Instruments

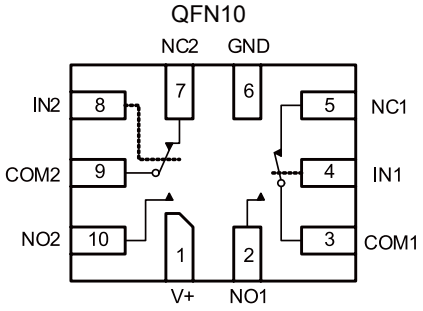
TRUTH TABLE

	IN1/2	$\overline{EN}$	NC1/2	NO1/2
MP2735	0	-	ON	OFF
	1	-	OFF	ON
MP2736	0	1	OFF	OFF
	1	1	OFF	OFF
	0	0	ON	OFF
	1	0	OFF	ON

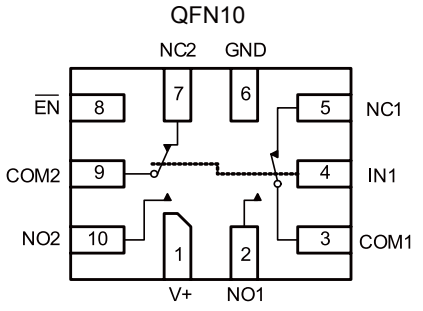
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FUNCTIONAL BLOCK DIAGRAM PIN CONFIGURATION

MP2735DQG



MP2736DQG



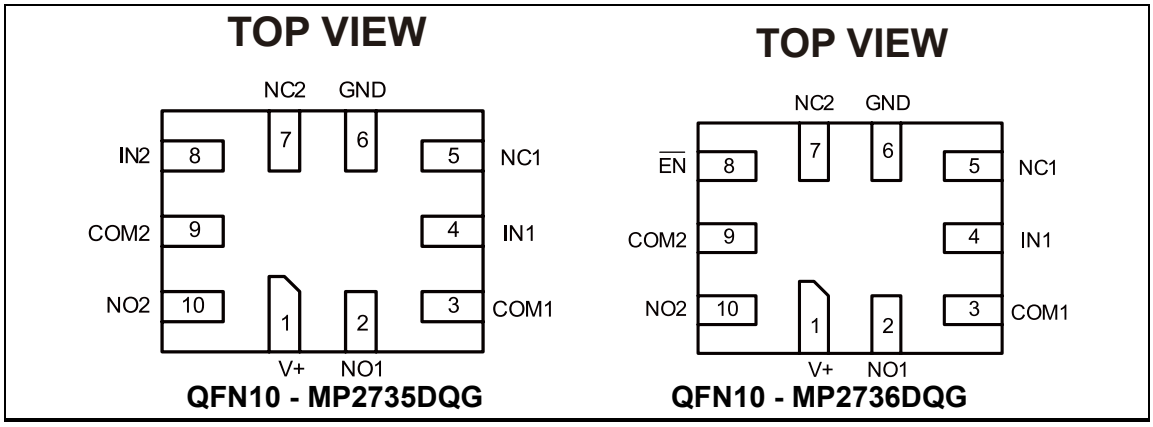
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ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP2735DQG	QFN10 (1.4mm x1.8mm)	$\overline{2T}$	-40°C to +85°C
MP2736DQG		$\overline{AM}$	

* For Tape & Reel, add suffix –Z (e.g. MP2735DQG–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MP2735DQG–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS

V+ Supply Voltage .....-0.3V to +6V
IN/COM/NC/NO Voltage (1) ... -0.3V to V+ + 0.3V
Current
(Any terminal except NO, NC or COM) .....
..... 30mA
Continuous Current (NO, NC or COM) .....
..... ±250mA
Peak Current
(Pulsed at 1ms, 10% duty cycle) ..... ±500mA
Storage Temperature..... -65°C to +150°C
Power Dissipation (QFN10 (2)) (3) 208mW

Notes:

1) Signals on NC, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2) Derate 4.0mW/℃ above 70℃.
3) All leads welded or soldered to PC Board.

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ELECTRICAL CHARACTERISTICS

V+=3V, ±10%, V_{IN}=0.4 or 1.65V, unless otherwise noted.

Parameter	Symbol	Condition		Min	Typ	Max	Units
Analog Switch							
Analog Signal Range	V_{analog}	$r_{DS(on)}$, T_A= -40°C to +85°C		0		V+	V
On-Resistance	$r_{DS(on)}$	V+=2.7V, $I_{NO/NC}$=100mA, V_{COM}=0.5V	T_A= +25°C		0.28	0.45	Ω
		V+=2.7V, $I_{NO/NC}$=100mA, V_{COM}=1.5V					
		V+=2.7V, $I_{NO/NC}$=100mA, V_{COM}=0.5V	T_A= -40°C to +85°C		0.30		
		V+=2.7V, $I_{NO/NC}$=100mA, V_{COM}=1.5V					
		V+=5.5V, $I_{NO/NC}$=100mA, V_{COM}=0.9V	T_A= +25°C		0.20	0.30	
		V+=5.5V, $I_{NO/NC}$=100mA, V_{COM}=2.5V			0.18		
		V+=5.5V, $I_{NO/NC}$=100mA, V_{COM}=0.9V	T_A= -40°C to +85°C		0.25		
		V+=5.5V, $I_{NO/NC}$=100mA, V_{COM}=2.5V					
r_{ON} Match	Δr_{on}	V+=2.7V, $I_{NO/NC}$=100mA, V_{COM}=0.5V/1.5V	T_A= +25°C		0.01	0.02	
		V+=5.5V, $I_{NO/NC}$=100mA, V_{COM}=0.9V/2.5V					
r_{ON} Flatness	r_{ON} Flatness	V+=2.7V, $I_{NO/NC}$=100mA, V_{COM}=0.5V/1.5V				0.15	
Switch Off Leakage Current	$I_{NO/NC(off)}$	V+=5.5V, $V_{NO/NC}$=0.3V/4.0V, V_{COM}=4.0V/0.3V	T_A= +25°C	-40		40	nA
			T_A= -40°C to +85°C	-100		100	
	$I_{COM(off)}$		T_A= +25°C	-40		40	
			T_A= -40°C to +85°C	-100		100	
Channel-On Leakage Current	$I_{COM(on)}$	V+=5.5V, $V_{NO/NC}$=V_{COM}=4.0V/0.3V	T_A= +25°C	-40		40	
			T_A= -40°C to +85°C	-150		150	
Digital Control							
Input High Voltage	V_{INH}		T_A= -40°C to +85°C	1.65			V
Input Low Voltage	V_{INL}					0.4	
Input Capacitance	C_{IN}				6		pF
Input Current	I_{INL} or I_{INH}	V_{IN}=0 or V+		-1		1	µA

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ELECTRICAL CHARACTERISTICS *(continued)*

V+=3V, ±10%, V_{IN}=0.4 or 1.65V, unless otherwise noted.

Parameter	Symbol	Condition		Min	Typ	Max	Units
Dynamic Characteristics							
Break-Before-Make Time	t_{BBM}	V+=3.6V, V_{NO}/V_{NC}=1.5V, R_L=50Ω, C_L=35pF	T_A= +25°C		10		ns
Turn-On Time	t_{ON}		T_A= +25°C		24	36	
			T_A= -40°C to +85°C			40	
Turn-Off Time	t_{OFF}		T_A= +25°C		20	30	
			T_A= -40°C to +85°C			35	
Enable Turn-On Time MP2736 ($\overline{EN}$)	$t_{ON(EN)}$		T_A= +25°C		24	36	
			T_A= -40°C to +85°C			40	
Enable Turn-Off Time MP2736 ($\overline{EN}$)	$t_{OFF(EN)}$		T_A= +25°C		20	30	
			T_A= -40°C to +85°C			35	
Off-Isolation(4)	OIRR	R_L=50Ω, C_L=5pF, f=100kHz	T_A= +25°C		-70		dB
Crosstalk(4)	XTALK				-70		dB
3dB Bandwidth		R_L=50Ω, C_L=5pF			50		MHz
NO, NC Off Capacitance(4)	$C_{NO(off)}$	V_{IN}=0V, or V+, f=1MHz			55		pF
	$C_{NC(off)}$				55		
Channel On Capacitance(4)	$C_{NO(on)}$				130		
	$C_{NC(on)}$				130		
Power Supply							
Power Supply Range	V+			1.65		5.5	V
Power Supply Current	I+	V_{IN}=0 or V+	T_A= -40°C to +85°C	-1		1	µA

Note:

4) Guarantee by design, not subjected to production test.

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PIN FUNCTIONS

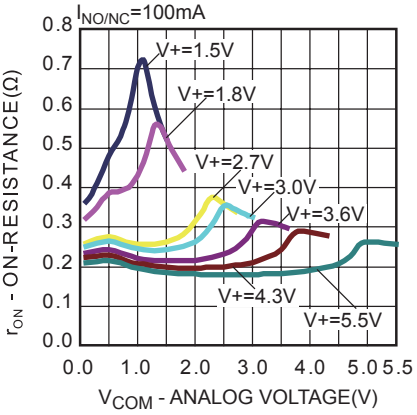
(MP2735DQG) Pin #	(MP2736DQG) Pin #	Name	Description
1	1	V+	Supply Voltage
2	2	NO1	Normally open I/O port of switch1
3	3	COM1	Commom I/O port for NC and NO channels of switch1
4	4	IN1	Channel select signal for switch1. IN1 high, NO1 channel is selected. Otherwise, NC1 channel is selected in default. For MP2736, IN1 controls both switch1 and switch2
5	5	NC1	Normally closed I/O port of switch1
6	6	GND	Ground
7	7	NC2	Normally closed I/O port of switch2
8		IN2	Channel select signal for switch2. IN2 high, NO2 channel is selected. Otherwise, NC2 channel is selected in default
	8	$\overline{EN}$	Enable for two channels, active low
9	9	COM2	Commom I/O port for NC and NO channels of switch2
10	10	NO2	Normally open I/O port of switch2

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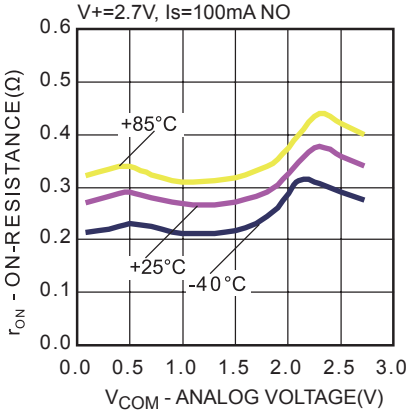
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25°C, unless otherwise noted.

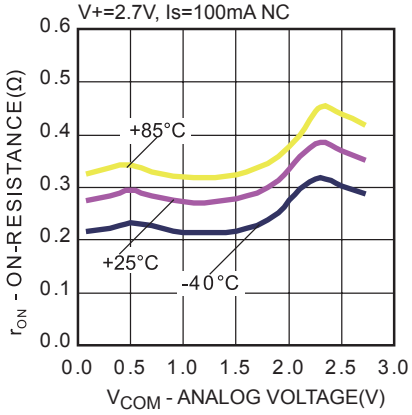
r_{ON} vs. V_{COM} and Supply Voltage



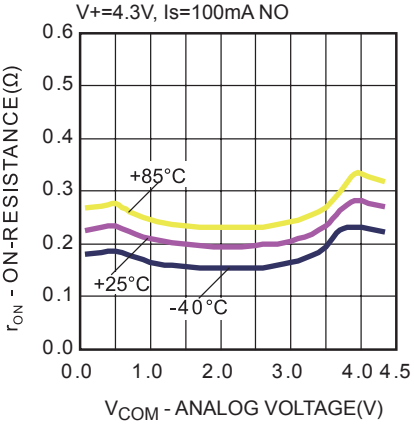
r_{ON} vs. V_{COM} and Temperature



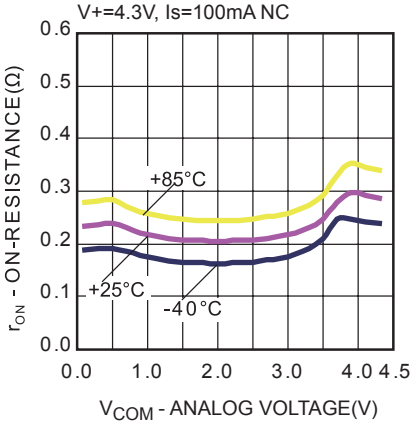
r_{ON} vs. V_{COM} and Temperature



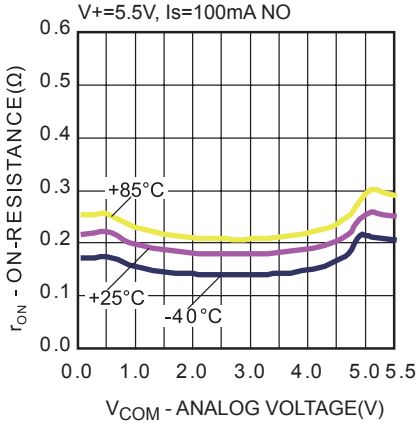
r_{ON} vs. V_{COM} and Temperature



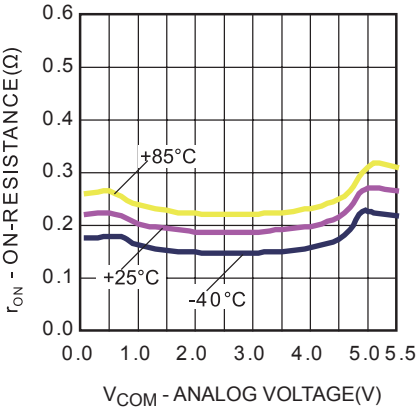
r_{ON} vs. V_{COM} and Temperature



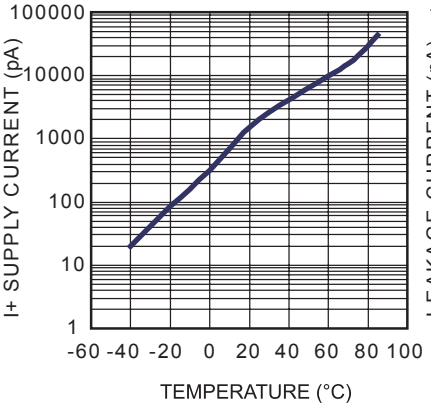
r_{ON} vs. V_{COM} and Temperature



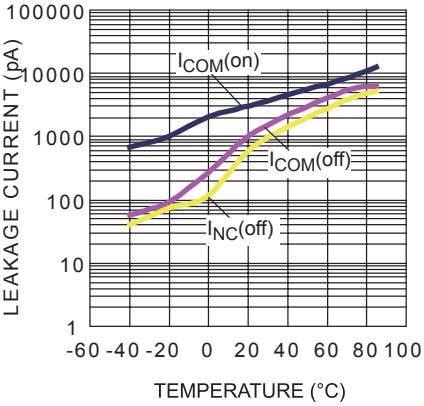
r_{ON} vs. V_{COM} and Temperature



Supply Current vs. Temperature



Leakage Current vs. Temperature



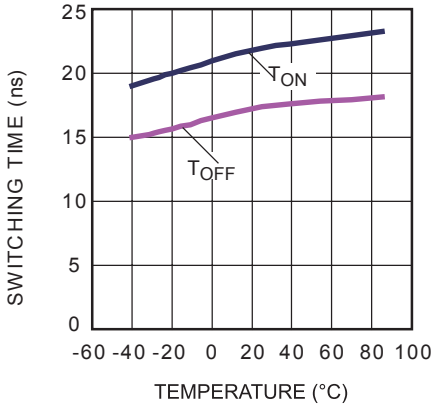
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

T_A = +25°C, unless otherwise noted.

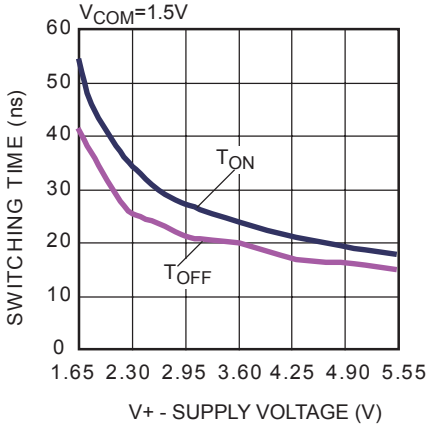
Switching Time vs. Temperature

V+=4.3V

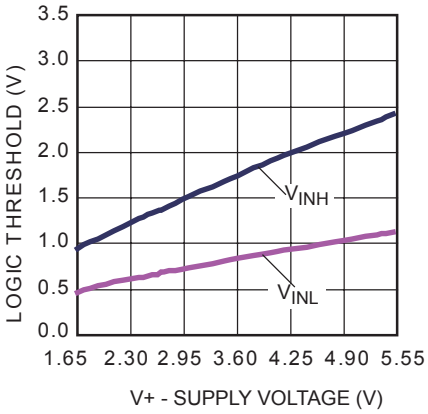


Switching Time vs. Supply Voltage

V_{COM}=1.5V

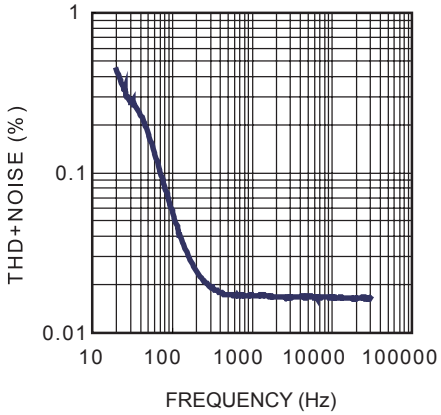


Logic Threshold vs. Supply Voltage



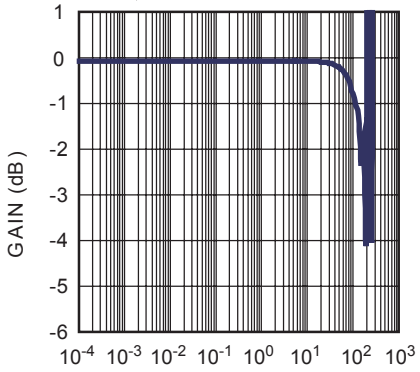
Total Harmonic Distortion vs. Frequency

V+=3V



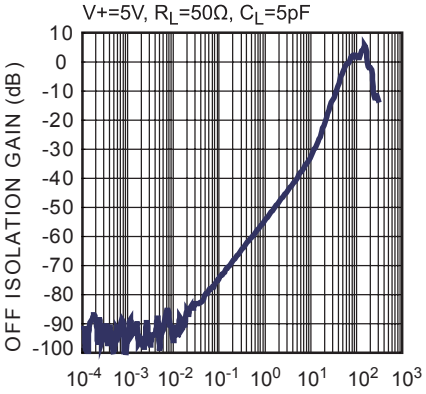
Bandwidth vs. Frequency

V+=5V, R_L=50Ω, C_L=5pF,
IN1=0, NC1 to COM1 On



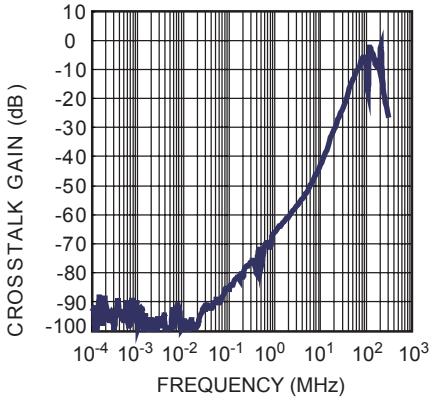
Off Isolation vs. Frequency

V+=5V, R_L=50Ω, C_L=5pF



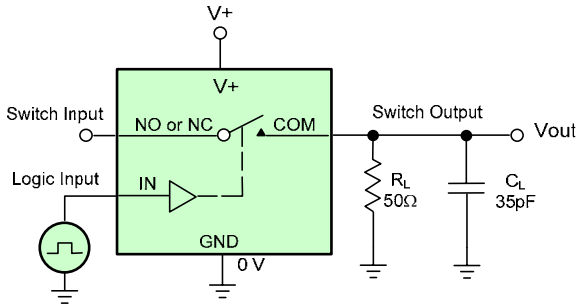
Crosstalk vs. Frequency

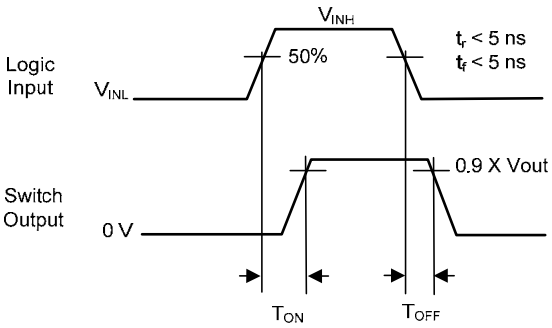
V+=5V, R_L=50Ω, C_L=5pF



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TEST CIRCUITS



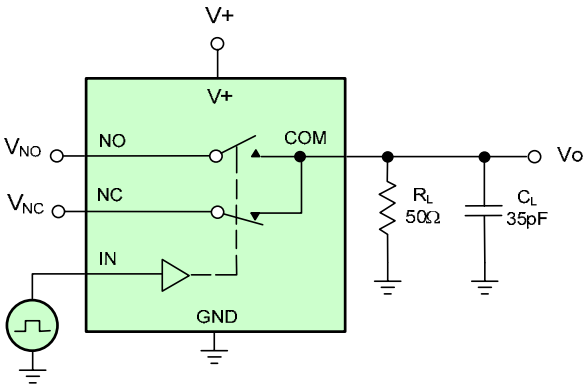


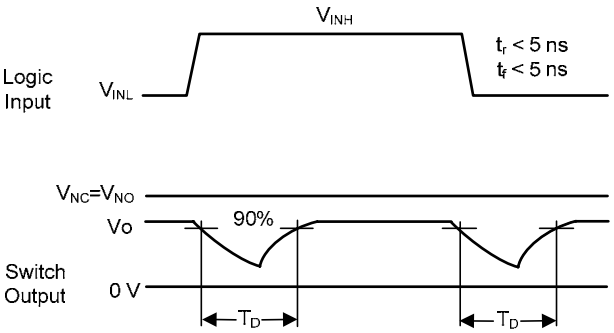
C_L (includes fixture and stray capacitance)

$$V_{out} = V_{COM}(\frac{R_L}{R_L + R_{ON}})$$

Logic "1" = Switch on
Logic input waveforms inverted for switches that have the opposite logic sense.

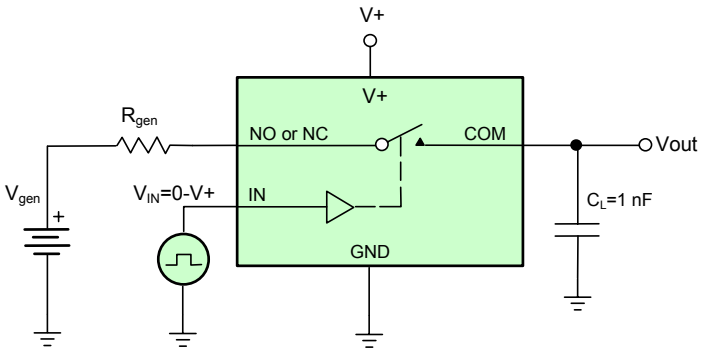
Figure 1 — Switching Time

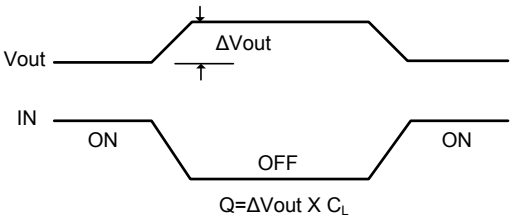




C_L (includes fixture and stray capacitance)

Figure 2 — Break-Before-Make Interval

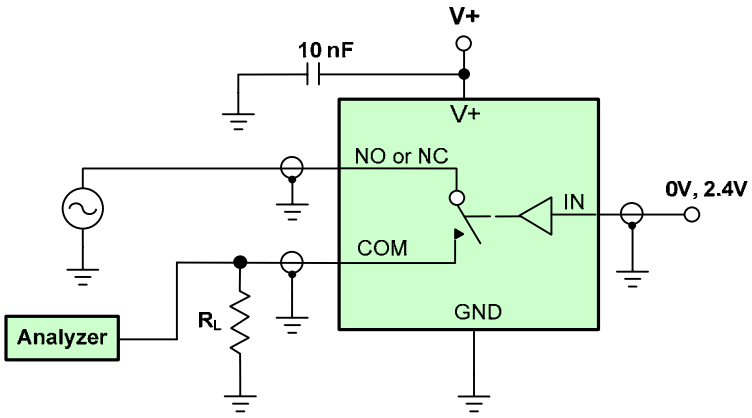




IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3 — Charge Injection

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$$\text{Off Isolation} = 20\log\frac{V_{COM}}{V_{NO/NC}}$$

Figure 4 — Off-Isolation

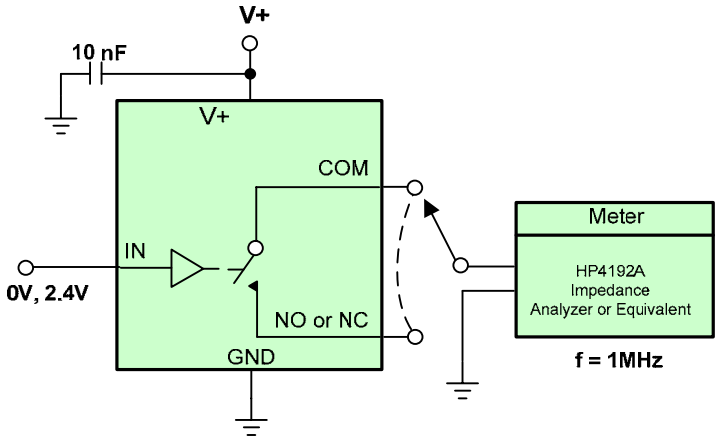
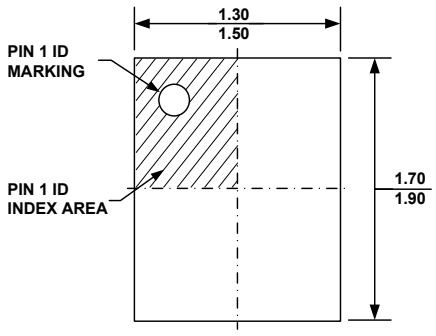


Figure 5 — Channel Off/On Capacitance

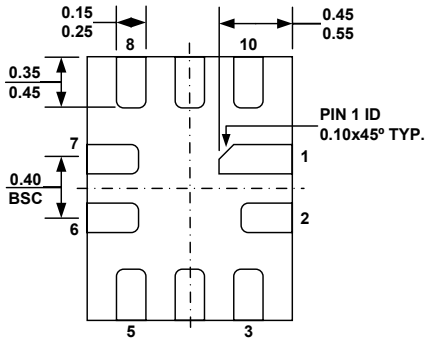
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PACKAGE INFORMATION

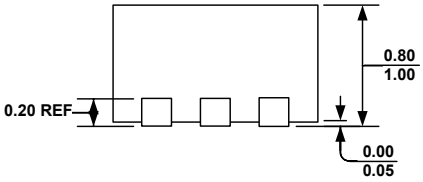
PACKAGE OUTLINE DRAWING FOR 10L FCQFN (1.4x1.8mm)
MF-PO-D-0084 revision 0.0



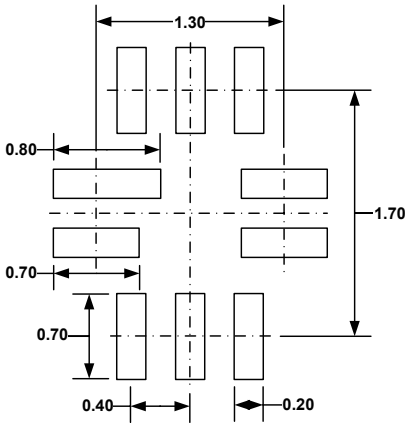
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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