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ON Semiconductor®

FQD2N90 / FQU2N90

N-Channel QFET® MOSFET

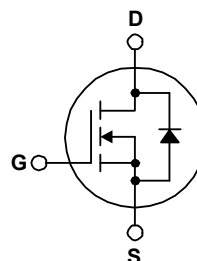
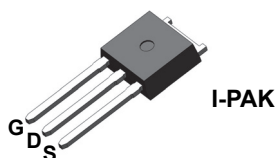
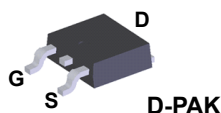
900 V, 1.7 A, 7.2 Ω

Description

This N-Channel enhancement mode power MOSFET is produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 1.7 A, 900 V, $R_{DS(on)} = 7.2 \Omega$ (Max.) @ $V_{GS} = 10 \text{ V}$, $I_D = 0.85 \text{ A}$
- Low Gate Charge (Typ. 12 nC)
- Low C_{rss} (Typ. 5.5 pF)
- 100% Avalanche Tested
- RoHS Compliant



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQD2N90TM FQU2N90TU-WS FQU2N90TU-AM002	Unit
V_{DSS}	Drain-Source Voltage	900	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	1.7	A
	- Continuous ($T_C = 100^\circ\text{C}$)	1.08	A
I_{DM}	Drain Current - Pulsed (Note 1)	6.8	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	170	mJ
I_{AR}	Avalanche Current (Note 1)	1.7	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.0	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) *	2.5	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	50	W
	- Derate above 25°C	0.4	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FQD2N90TM FQU2N90TU-WS FQU2N90TU-AM002	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (minimum pad of 2 oz copper), Max.	110	
	Thermal Resistance, Junction to Ambient (*1 in ² pad of 2 oz copper), Max.	50	

FQD2N90 / FQU2N90 — N-Channel QFET® MOSFET

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQD2N90TM	FQD2N90	D-PAK	Tape and Reel	330 mm	16 mm	2500 units
FQU2N90TU-WS	FQU2N90S	I-PAK	Tube	N/A	N/A	75 units
FQU2N90TU-AM002	FQU2N90	I-PAK	Tube	N/A	N/A	75 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	900	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	1.0	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 900\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	μA
		$V_{DS} = 720\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 0.85\text{ A}$	--	5.6	7.2	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 0.85\text{ A}$	--	1.7	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	390	500	pF
C_{oss}	Output Capacitance		--	45	60	pF
C_{rss}	Reverse Transfer Capacitance		--	5.5	7.0	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 450\text{ V}, I_D = 2.2\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4)	--	15	40	ns
t_r	Turn-On Rise Time		--	35	80	ns
$t_{d(off)}$	Turn-Off Delay Time		--	20	50	ns
t_f	Turn-Off Fall Time		--	30	70	ns
Q_g	Total Gate Charge	$V_{DS} = 720\text{ V}, I_D = 2.2\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4)	--	12	15	nC
Q_{gs}	Gate-Source Charge		--	2.8	--	nC
Q_{gd}	Gate-Drain Charge		--	6.1	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	1.7	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	6.8	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.7 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 2.2 A,	--	400	--	ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs	--	1.6	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 111\text{ mH}, I_{AS} = 1.7\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 2.2\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Essentially independent of operating temperature

Typical Characteristics

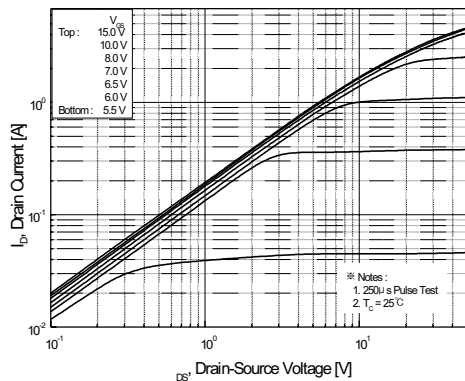


Figure 1. On-Region Characteristics

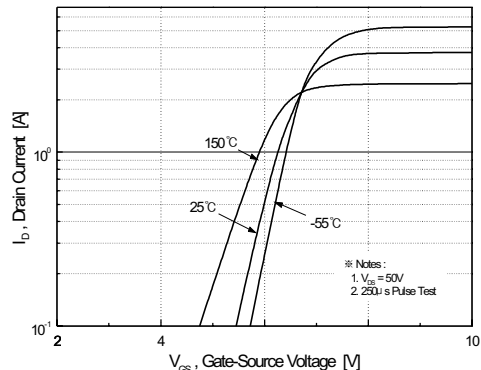


Figure 2. Transfer Characteristics

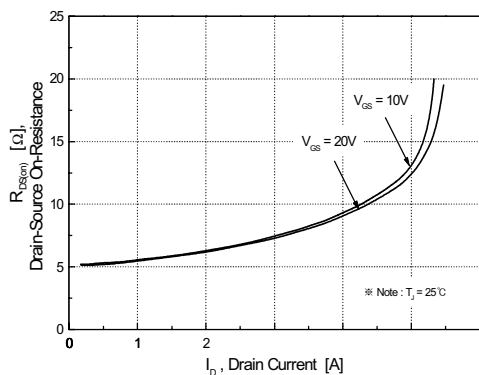


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

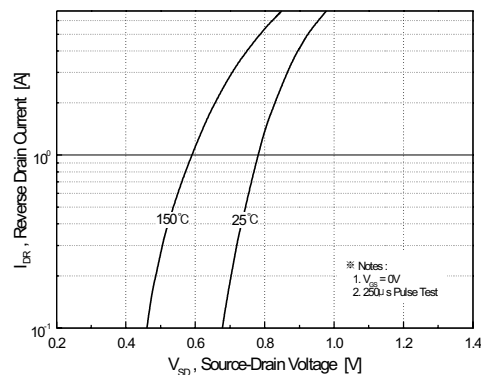


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

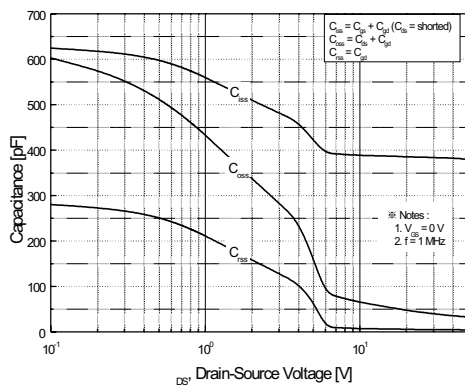


Figure 5. Capacitance Characteristics

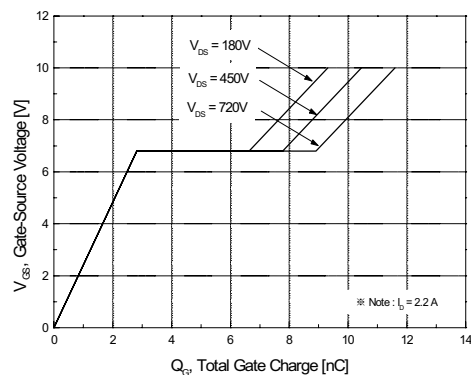


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

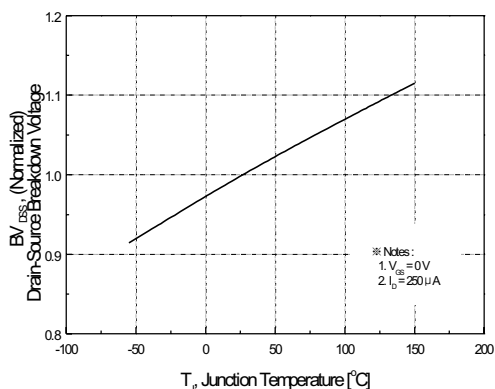


Figure 7. Breakdown Voltage Variation vs. Temperature

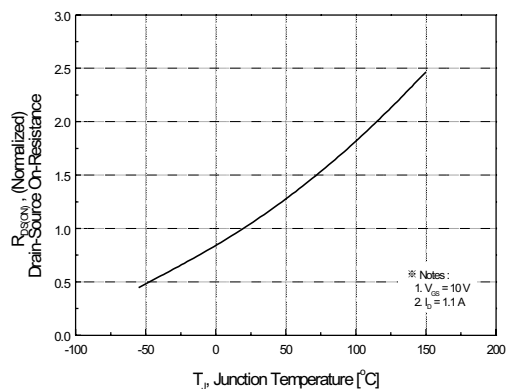


Figure 8. On-Resistance Variation vs. Temperature

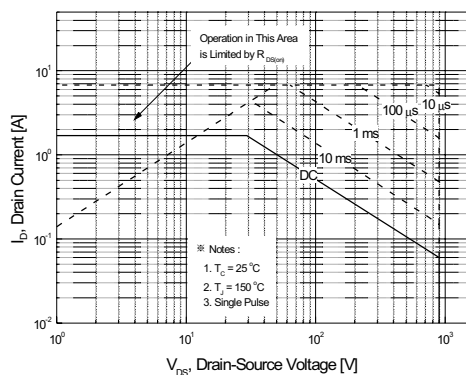


Figure 9. Maximum Safe Operating Area

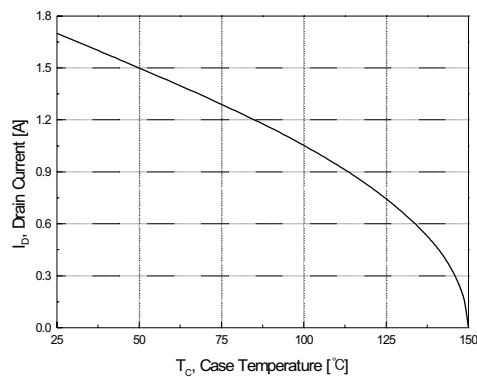


Figure 10. Maximum Drain Current vs. Case Temperature

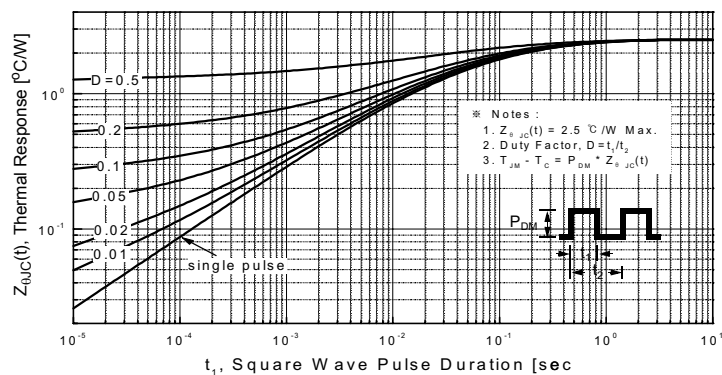


Figure 11. Transient Thermal Response Curve

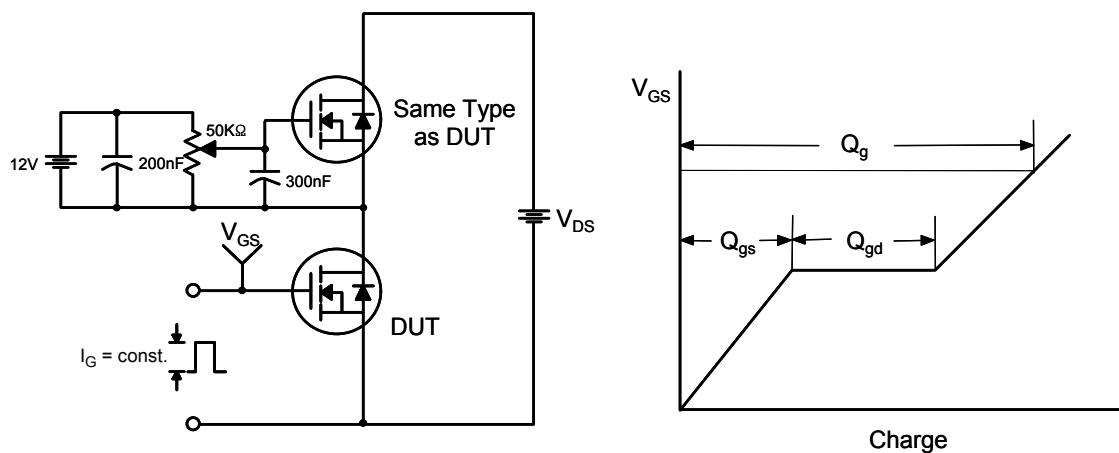


Figure 12. Gate Charge Test Circuit & Waveform

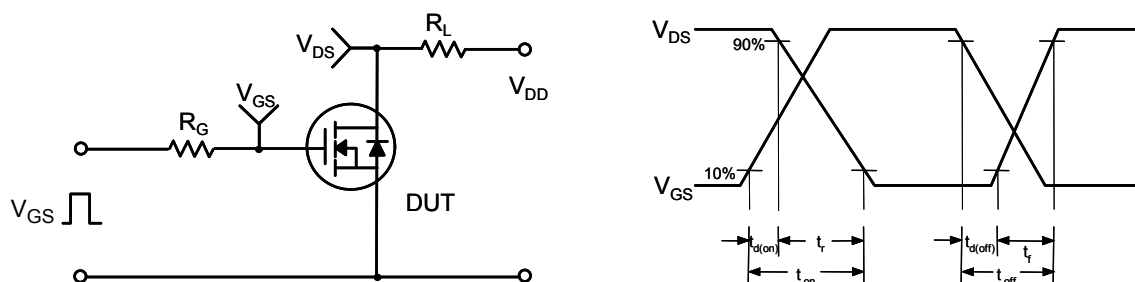


Figure 13. Resistive Switching Test Circuit & Waveforms

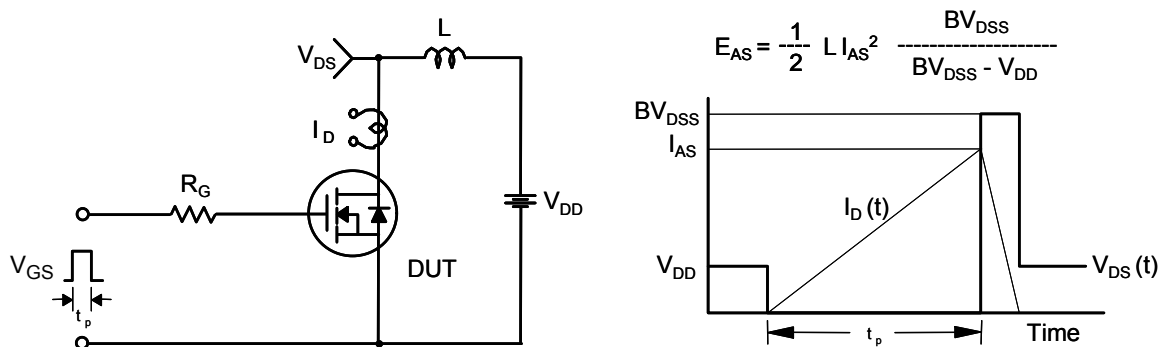


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

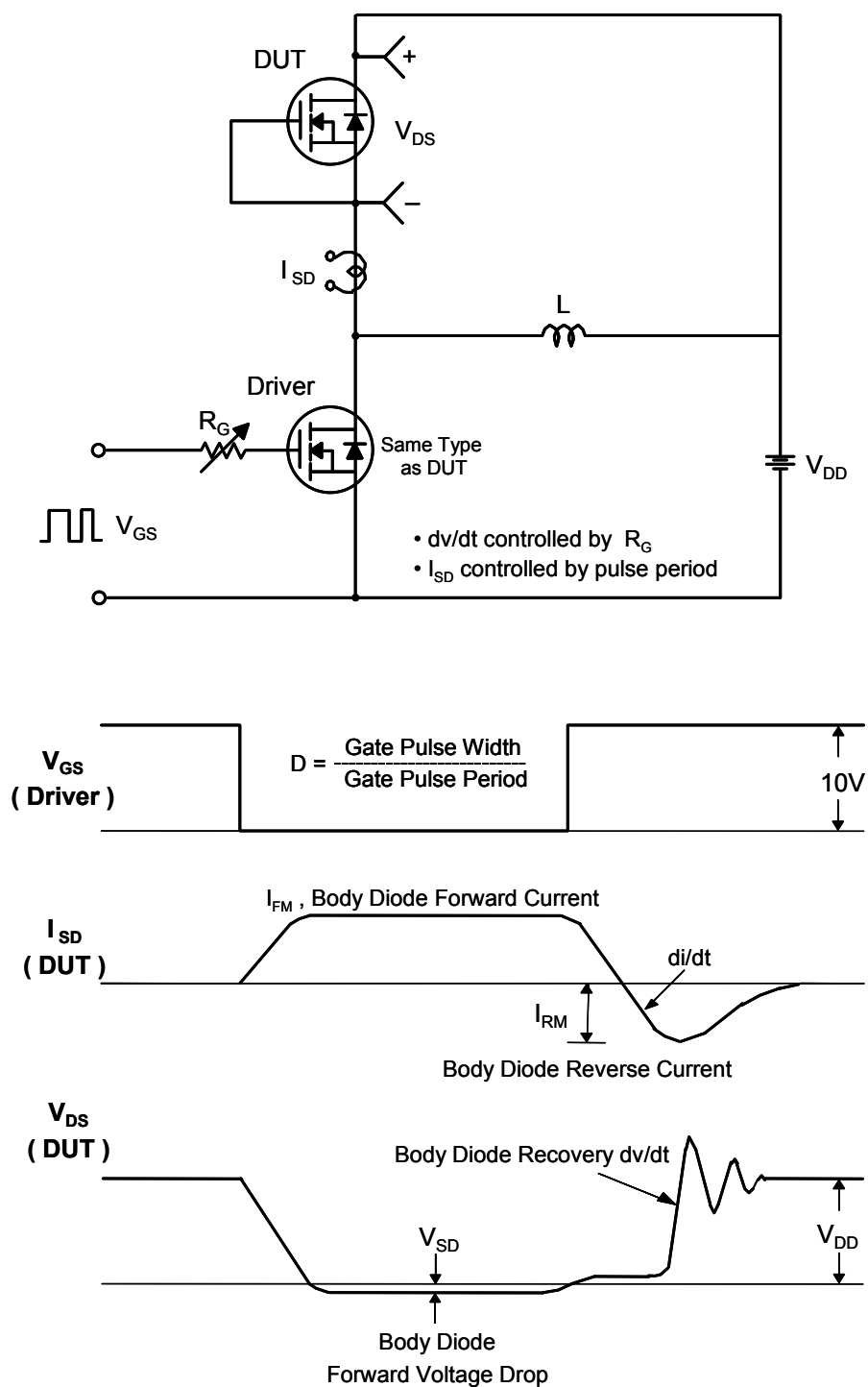
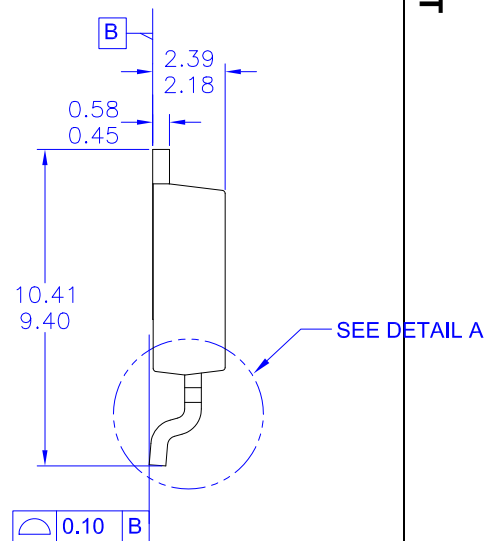
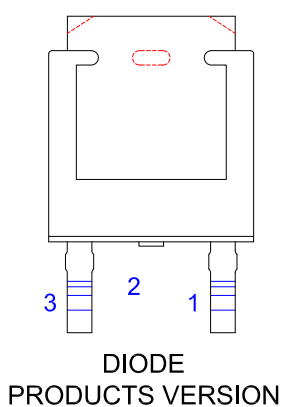
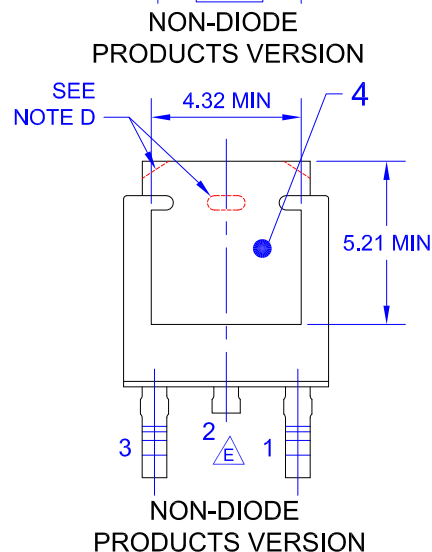
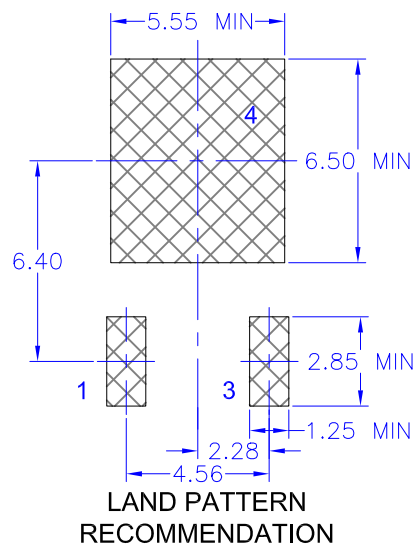
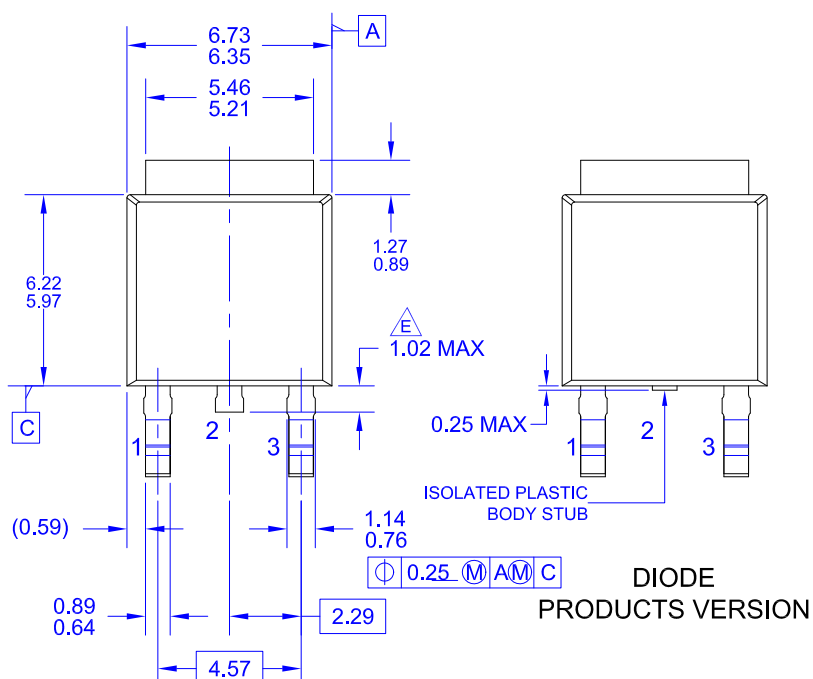


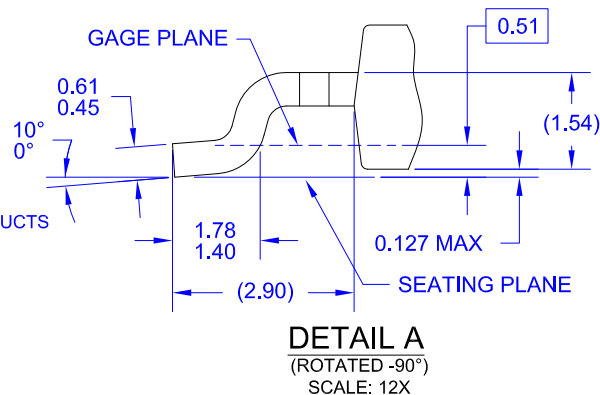
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

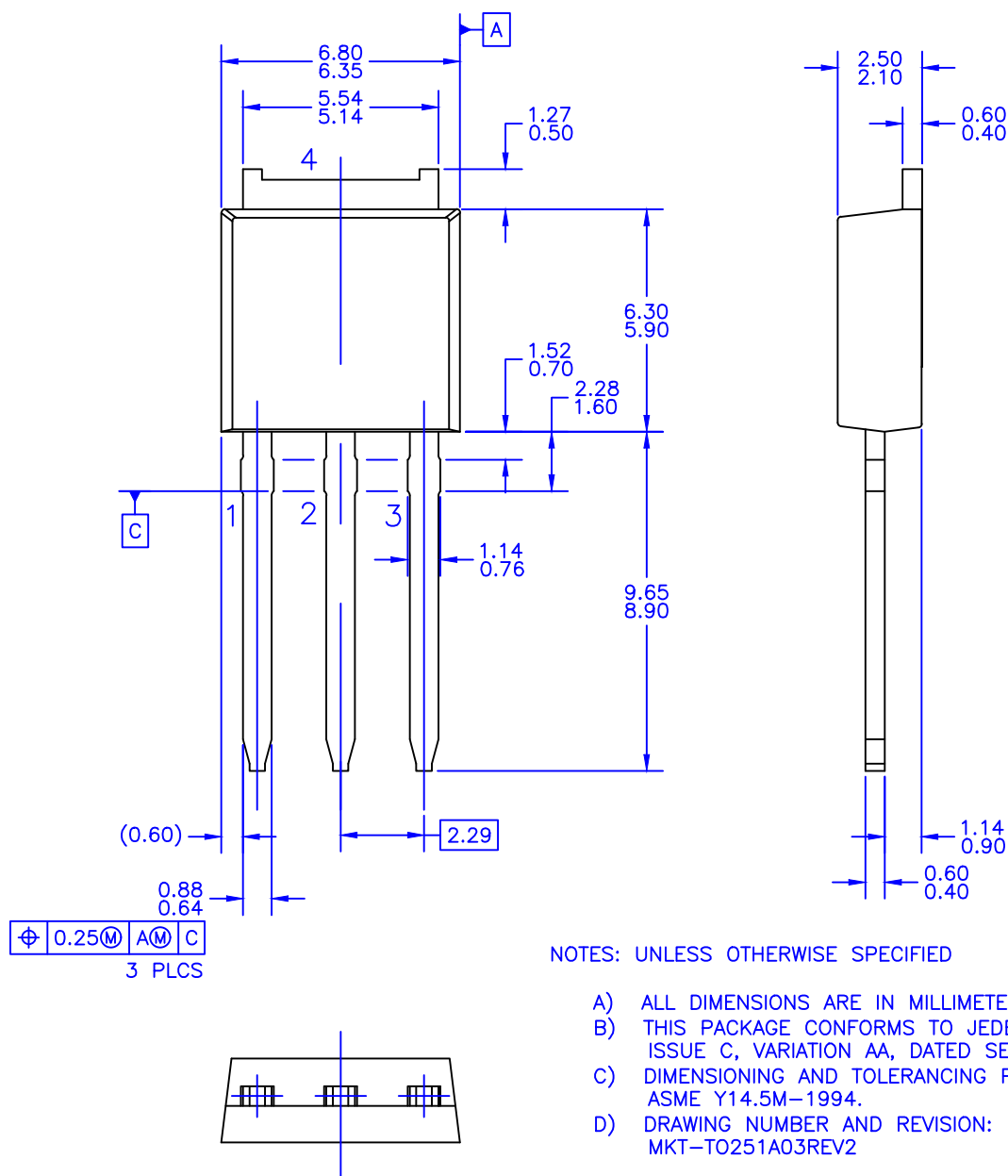


NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



Mechanical Dimensions



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