USB 2.0 Hi-Speed 3-Port Hub Controller

Highlights

- Hub Controller IC with 3 downstream ports
- USB-IF Battery Charger revision 1.2 support on up & downstream ports (DCP, CDP, SDP)
- Battery charging support for Apple® devices
- **FlexConnect**: Downstream port 1 able to swap with upstream port, allowing master capable devices to control other devices on the hub
- USB to I^2C bridge endpoint support
- USB Link Power Management (LPM) support
- SUSPEND pin for remote wakeup indication to host
- Vendor Specific Messaging (VSM) support
- Enhanced OEM configuration options available through a single serial I^2C EEPROM, OTP, or SMBus Slave Port
- 36-pin (6x6mm) SQFN, RoHS compliant package
- Footprint compatible with USB2513B

Target Applications

- LCD monitors and TVs
- Multi-function USB peripherals
- PC mother boards
- Set-top boxes, DVD players, DVR/PVR
- Printers and scanners
- PC media drive bay
- Portable hub boxes
- Mobile PC docking
- Embedded systems

Additional Features

- **MultiTRAK™**
  - Dedicated Transaction Translator per port
- PortMap
  - Configurable port mapping and disable sequencing
- PortSwap
  - Configurable differential intra-pair signal swapping
- **PHYBoost™**
  - Programmable USB transceiver drive strength for recovering signal integrity
- **VariSense™**
  - Programmable USB receiver sensitivity
- Low power operation
- Full Power Management with individual or ganged power control of each downstream port
- Built-in Self-Powered or Bus-Powered internal default settings provide flexibility in the quantity of USB expansion ports utilized without redesign
- Supports “Quad Page” configuration OTP flash
  - Four consecutive 200 byte configuration pages
- Fully integrated USB termination and Pull-up/Pull-down resistors
- On-chip Power On Reset (POR)
- Internal 3.3V and 1.2V voltage regulators
- On Board 24MHz Crystal Driver, Resonator, or External 24MHz clock input
- Environmental
  - Commercial temperature range support (0ºC to 70ºC)
  - Industrial temperature range support (-40ºC to 85ºC)

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1.0 INTRODUCTION

The USB2533 is a low-power, OEM configurable, MTT (Multi-Transaction Translator) USB 2.0 hub controller with 3 downstream ports and advanced features for embedded USB applications. The USB2533 is fully compliant with the USB 2.0 Specification, USB 2.0 Link Power Management Addendum and will attach to an upstream port as a Full-Speed hub or as a Full-/Hi-Speed hub. The 3-port hub supports Low-Speed, Full-Speed, and Hi-Speed (if operating as a Hi-Speed hub) downstream devices on all of the enabled downstream ports.

The USB2533 has been specifically optimized for embedded systems where high performance, and minimal BOM costs are critical design requirements. Standby mode power has been minimized and reference clock inputs can be aligned to the customer's specific application. Additionally, all required resistors on the USB ports are integrated into the hub, including all series termination and pull-up/pull-down resistors on the D+ and D– pins.

The USB2533 supports both upstream battery charger detection and downstream battery charging. The USB2533 integrated battery charger detection circuitry supports the USB-IF Battery Charging (BC1.2) detection method and most Apple devices. These circuits are used to detect the attachment and type of a USB charger and provide an interrupt output to indicate charger information is available to be read from the device's status registers via the serial interface. The USB2533 provides the battery charging handshake and supports the following USB-IF BC1.2 charging profiles:

- DCP: Dedicated Charging Port (Power brick with no data)
- CDP: Charging Downstream Port (1.5A with data)
- SDP: Standard Downstream Port (0.5A with data)
- Custom profiles loaded via SMBus or OTP

The USB2533 provides an additional USB endpoint dedicated for use as a USB to I^2C interface, allowing external circuits or devices to be monitored, controlled, or configured via the USB interface. Additionally, the USB2533 includes many powerful and unique features such as:

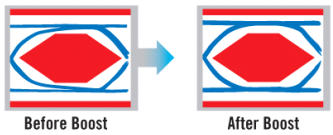
FlexConnect, which provides flexible connectivity options. The USB2533's downstream port 1 can be swapped with the upstream port, allowing master capable devices to control other devices on the hub.

MultiTRAK™ Technology, which utilizes a dedicated Transaction Translator (TT) per port to maintain consistent full-speed data throughput regardless of the number of active downstream connections. MultiTRAK™ outperforms conventional USB 2.0 hubs with a single TT in USB full-speed data transfers.

PortMap, which provides flexible port mapping and disable sequences. The downstream ports of a USB2533 hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB2533 hub controllers automatically reorder the remaining ports to match the USB host controller's port numbering scheme.

PortSwap, which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.

PHYBoost, which provides programmable levels of Hi-Speed USB signal drive strength in the downstream port transceivers. PHYBoost attempts to restore USB signal integrity in a compromised system environment. The graphic on the right shows an example of Hi-Speed USB eye diagrams before and after PHYBoost signal integrity restoration.



VariSense, which controls the USB receiver sensitivity enabling programmable levels of USB signal receive sensitivity. This capability allows operation in a sub-optimal system environment, such as when a captive USB cable is used.

The USB2533 is available in commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature range versions.

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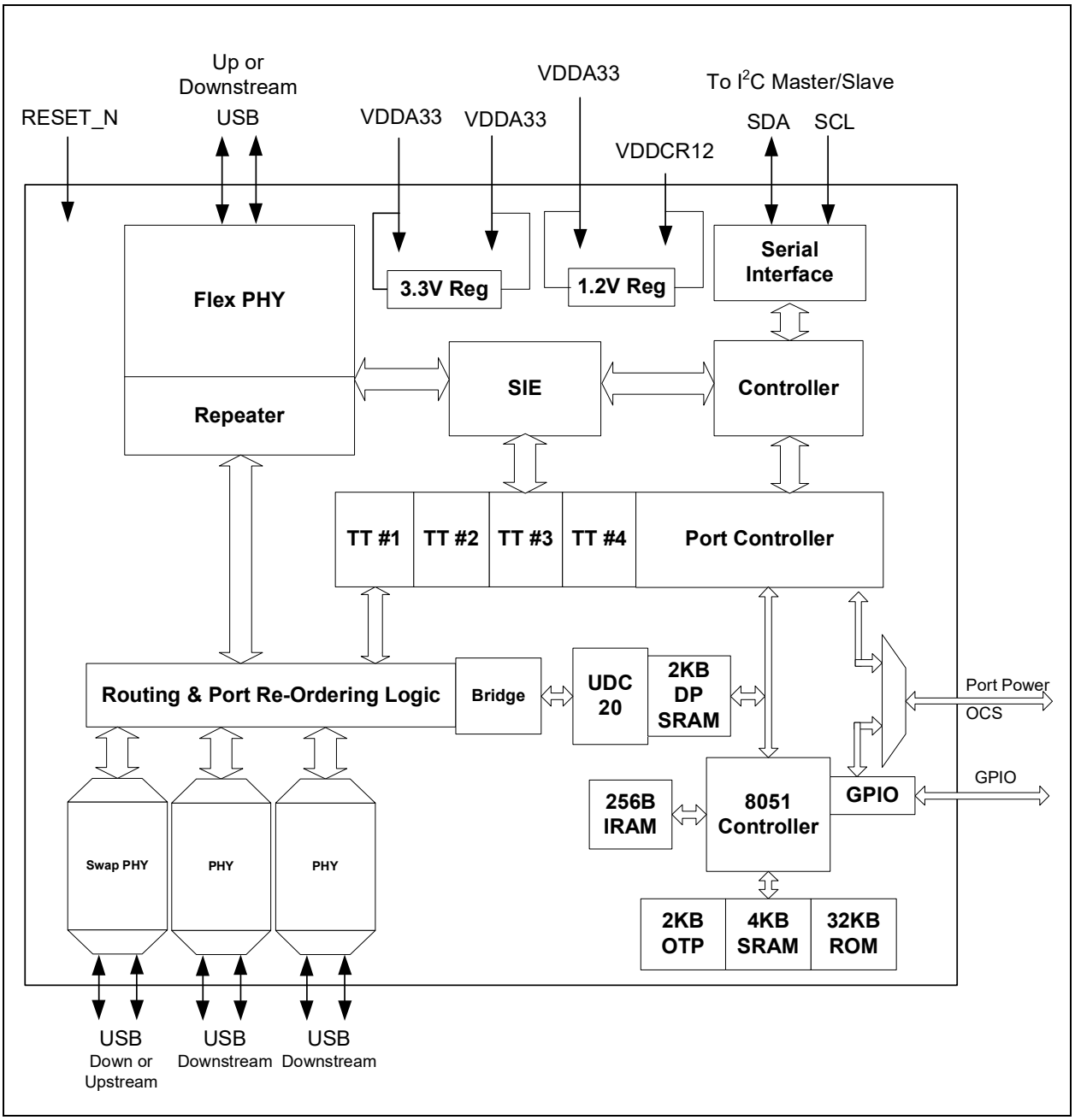
1.1 Block Diagram

Figure 1-1 details the internal block diagram of the USB2533.

FIGURE 1-1: SYSTEM BLOCK DIAGRAM



2.0 ACRONYMS AND DEFINITIONS

2.1 Acronyms

EOP: End of Packet

EP: Endpoint

FS: Full-Speed

GPIO: General Purpose I/O (that is input/output to/from the device)

HS: Hi-Speed

HSOS: High Speed Over Sampling

I^2C: Inter-Integrated Circuit

LS: Low-Speed

OTP: One Time Programmable

PCB: Printed Circuit Board

PCS: Physical Coding Sublayer

PHY: Physical Layer

SMBus: System Management Bus

UUID: Universally Unique IDentification

2.2 Reference Documents

1. *UNICODE UTF-16LE For String Descriptors* USB Engineering Change Notice, December 29th, 2004, http://www.usb.org
2. *Universal Serial Bus Specification*, Revision 2.0, April 27th, 2000, http://www.usb.org
3. *Battery Charging Specification*, Revision 1.2, Dec. 07, 2010, http://www.usb.org
4. *I^2C-Bus Specification*, Version 1.1, http://www.nxp.com
5. *System Management Bus Specification*, Version 1.0, http://smbus.org/specs

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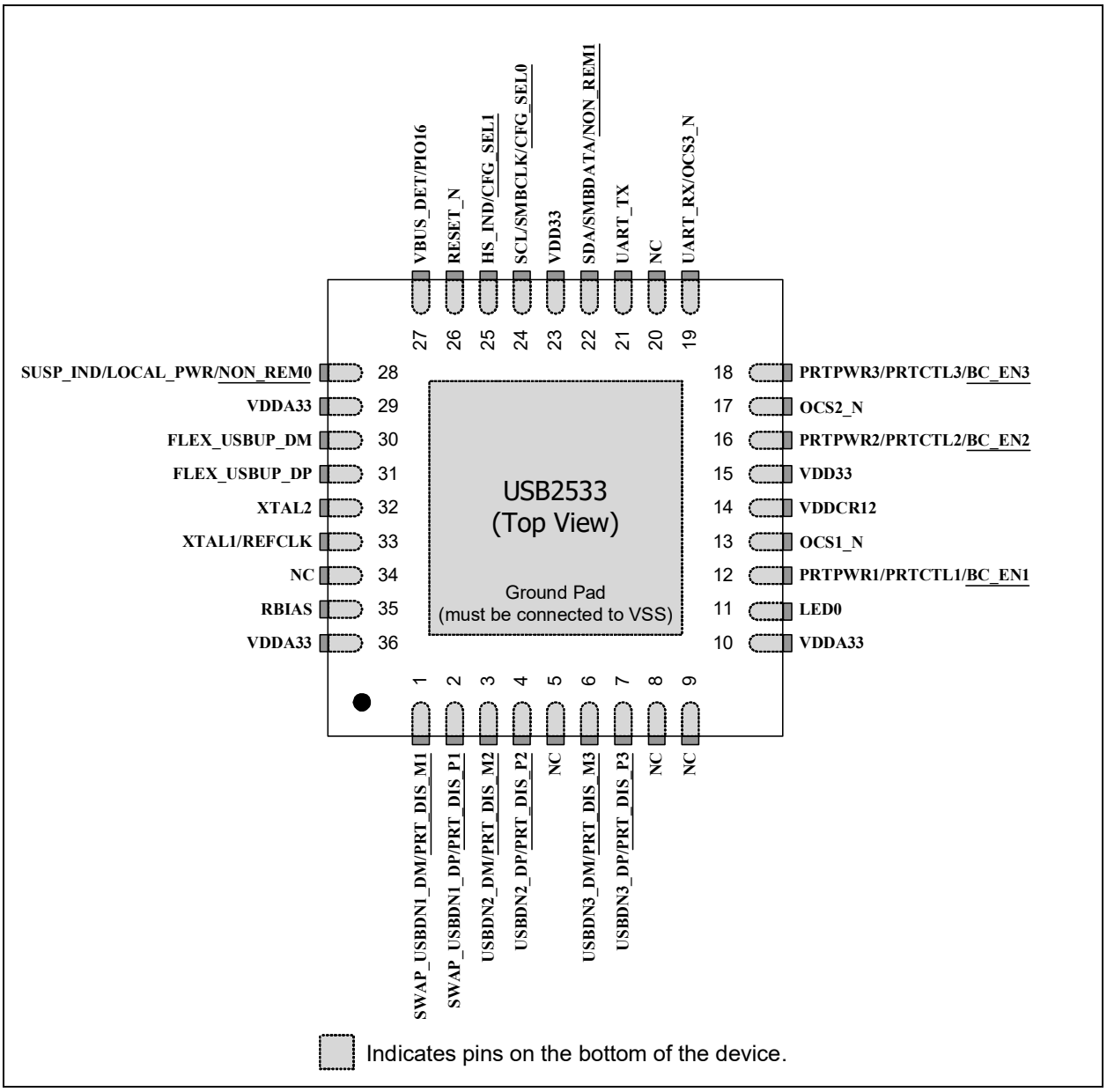
3.0 PIN DESCRIPTIONS

FIGURE 3-1: 36-SQFN PIN ASSIGNMENTS



3.1 Pin Descriptions

This section provides a detailed description of each pin. The signals are arranged in functional groups according to their associated interface.

The "_N" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, RESET_N indicates that the reset signal is active low. When "_N" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of "active low" and "active high" signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

Note: The buffer type for each signal is indicated in the BUFFER TYPE column of Table 3-1. A description of the buffer types is provided in Section 3.3.

Note: Compatibility with the UCS100x family of USB port power controllers requires the UCS100x be connected on Port 1 of the USB2533. Additionally, both PRTPWR1 and OCS1_N must be pulled high at Power-On Reset (POR).

TABLE 3-1: PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
USB/HSIC INTERFACES				
1	Upstream USB D+ (Flex Port 0)	FLEX_USBUP_DP	AIO	Upstream USB Port 0 D+ data signal. **Note:** The upstream Port 0 signals can be optionally swapped with the downstream Port 1 signals.
1	Upstream USB D- (Flex Port 0)	FLEX_USBUP_DM	AIO	Upstream USB Port 0 D- data signal. **Note:** The upstream Port 0 signals can be optionally swapped with the downstream Port 1 signals.
1	Downstream USB D+ (Swap Port 1)	SWAP_USBDN1_DP	AIO	Downstream USB Port 1 D+ data signal. **Note:** The downstream Port 1 signals can be optionally swapped with the upstream Port 0 signals.
	Port 1 D+ Disable Configuration Strap	PRT_DIS_P1	IS	This strap is used in conjunction with PRT_DIS_M1 to disable USB Port 1. 0 = Port 1 D+ Enabled 1 = Port 1 D+ Disabled **Note:** Both PRT_DIS_P1 and PRT_DIS_M1 must be tied to VDD33 at reset to disable the associated port. See Note 3-3 for more information on configuration straps.

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TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Downstream USB D- (Swap Port 1)	SWAP_USBDN1_DM	AIO	Downstream USB Port 1 D- data signal. **Note:** The downstream Port 1 signals can be optionally swapped with the upstream Port 0 signals.
	Port 1 D- Disable Configuration Strap	PRT_DIS_M1	IS	This strap is used in conjunction with PRT_DIS_P1 to disable USB Port 1. 0 = Port 1 D- Enabled 1 = Port 1 D- Disabled **Note:** Both PRT_DIS_P1 and PRT_DIS_M1 must be tied to VDD33 at reset to disable the associated port. See Note 3-3 for more information on configuration straps.
1	Downstream USB D+ (Port 2)	USBDN2_DP	AIO	Downstream USB Port 2 D+ data signal.
	Port 2 D+ Disable Configuration Strap	PRT_DIS_P2	IS	This strap is used in conjunction with PRT_DIS_M2 to disable USB Port 2. 0 = Port 2 D+ Enabled 1 = Port 2 D+ Disabled **Note:** Both PRT_DIS_P2 and PRT_DIS_M2 must be tied to VDD33 at reset to disable the associated port. See Note 3-3 for more information on configuration straps.
1	Downstream USB D- (Port 2)	USBDN2_DM	AIO	Downstream USB Port 2 D- data signal.
	Port 2 D- Disable Configuration Strap	PRT_DIS_M2	IS	This strap is used in conjunction with PRT_DIS_P2 to disable USB Port 2. 0 = Port 2 D- Enabled 1 = Port 2 D- Disabled **Note:** Both PRT_DIS_P2 and PRT_DIS_M2 must be tied to VDD33 at reset to disable the associated port. See Note 3-3 for more information on configuration straps.
1	Downstream USB D+ (Port 3)	USBDN3_DP	AIO	Downstream USB Port 3 D+ data signal.
	Port 3 D+ Disable Configuration Strap	PRT_DIS_P3	IS	This strap is used in conjunction with PRT_DIS_M3 to disable USB Port 3. 0 = Port 3 D+ Enabled 1 = Port 3 D+ Disabled **Note:** Both PRT_DIS_P3 and PRT_DIS_M3 must be tied to VDD33 at reset to disable the associated port. See Note 3-3 for more information on configuration straps.

TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Downstream USB D- (Port 3)	USBDN3_DM	AIO	Downstream USB Port 3 D- data signal.
	Port 3 D- Disable Configuration Strap	PRT_DIS_M3	IS	This strap is used in conjunction with PRT_DIS_P3 to disable USB Port 3. 0 = Port 3 D- Enabled 1 = Port 3 D- Disabled **Note:** Both PRT_DIS_P3 and PRT_DIS_M3 must be tied to VDD33 at reset to disable the associated port. See Note 3-3 for more information on configuration straps.
I²C/SMBUS INTERFACE				
1	I²C Serial Clock Input	SCL	I_SMB	I²C serial clock input
	SMBus Clock	SMBCLK	I_SMB	SMBus serial clock input
	Configuration Select 0 Configuration Strap	CFG_SEL0	I_SMB	This strap is used in conjunction with CFG_SEL1 to set the hub configuration method. Refer to Section 6.3.2, "Configuration Select (CFG_SEL[1:0])," on page 24 for additional information. See Note 3-3 for more information on configuration straps.
1	I²C Serial Data	SDA	IS/OD8	I²C bidirectional serial data
	SMBus Serial Data	SMBDATA	IS/OD8	SMBus bidirectional serial data
	Non-Removable Device 1 Configuration Strap	NON_REM1 (Note 3-2)	IS	This strap is used in conjunction with NON_REM0 to configure the downstream ports as non-removable devices. Refer to Section 6.3.1, "Non-Removable Device (NON_REM[1:0])," on page 23 for additional information. See Note 3-3 for more information on configuration straps.
MISC.				
1	Port 1 Over-Current Sense Input	OCS1_N	IS (PU)	This active-low signal is input from an external current monitor to indicate an over-current condition on USB Port 1.
1	Port 2 Over-Current Sense Input	OCS2_N	IS (PU)	This active-low signal is input from an external current monitor to indicate an over-current condition on USB Port 2.
1	UART Receive Input	UART_RX	IS	Internal UART receive input **Note:** This is a 3.3V signal. For RS232 operation, an external 12V translator is required.
	Port 3 Over-Current Sense Input	OCS3_N	IS (PU)	This active-low signal is input from an external current monitor to indicate an over-current condition on USB Port 3.
1	UART Transmit Output	UART_TX	O8	Internal UART transmit output **Note:** This is a 3.3V signal. For RS232 operation, an external 12V driver is required.

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TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	System Reset Input	RESET_N	I_RST	This active-low signal allows external hardware to reset the device. **Note:** The active-low pulse must be at least 5us wide. Refer to Section 8.3.2, "External Chip Reset (RESET_N)," on page 29 for additional information.
1	Crystal Input	XTAL1	ICLK	External 24 MHz crystal input
	Reference Clock Input	REFCLK	ICLK	Reference clock input. The device may be alternatively driven by a single-ended clock oscillator. When this method is used, XTAL2 should be left unconnected.
1	Crystal Output	XTAL2	OCLK	External 24 MHz crystal output
1	External USB Transceiver Bias Resistor	RBIAS	AI	A 12.0kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.
1	LED 0 Output	LED0	O8	General purpose LED 0 output that is configurable to blink or "breathe" at various rates. **Note:** LED0 must be enabled via the Protouch configuration tool.
1	Detect Upstream VBUS Power	VBUS_DET	IS	Detects state of upstream bus power. When designing a detachable hub, this pin must be connected to the VBUS power pin of the upstream USB port through a resistor divider (50kΩ by 100kΩ) to provide 3.3V. For self-powered applications with a permanently attached host, this pin must be connected to either 3.3V or 5.0V through a resistor divider to provide 3.3V. In embedded applications, VBUS_DET may be controlled (toggled) when the host desires to renegotiate a connection without requiring a full reset of the device.

TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Remote Wakeup Indicator	SUSP_IND	OD8	Configurable sideband signal used to indicate Suspend status (default) or Remote Wakeup events to the Host. Suspend Indicator (default configuration): 0 = Unconfigured, or configured and in USB suspend mode 1 = Device is configured and is active (i.e., not in suspend) For Remote Wakeup Indicator mode: Refer to Section 8.5, "Remote Wakeup Indicator (SUSP_IND)," on page 30. Refer to Section 6.3.1, "Non-Removable Device (NON_REM[1:0])," on page 23 for information on LED polarity when using this signal.
	Local Power Detect	LOCAL_PWR	IS	Detects the availability of a local self-power source. 0 = Self/local power source is NOT available. (i.e., device must obtain all power from upstream USB VBUS) 1 = Self/local power source is available See Note 3-1 for more information on this pin.
	Non-Removable Device 0 Configuration Strap	NON_REM0 (Note 3-2)	IS	This strap is used in conjunction with NON_REM1 to configure the downstream ports as non-removable devices. Refer to Section 6.3.1, "Non-Removable Device (NON_REM[1:0])," on page 23 for additional information. See Note 3-3 for more information on configuration straps.
1	High Speed Indicator	HS_IND	O8	Indicates a high speed connection on the upstream port. The active state of the LED will be determined as follows: If CFG_SEL1 = 0, HS_IND is active high. If CFG_SEL1 = 1, HS_IND is active low. Asserted = hub is connected at high speed Negated = Hub is connected at full speed
	Configuration Select 1 Configuration Strap	CFG_SEL1	IS	This strap is used in conjunction with CFG_SEL0 to set the hub configuration method. Refer to Section 6.3.2, "Configuration Select (CFG_SEL[1:0])," on page 24 for additional information. See Note 3-3 for more information on configuration straps.

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TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Port 1 Power Output	PRTPWR1	O8	Enables power to a downstream USB device attached to Port 1. 0 = Power disabled on downstream Port 1 1 = Power enabled on downstream Port 1
	Port 1 Control	PRTCTL1	OD8/IS (PU)	When configured as PRTCTL1, this pin functions as both the Port 1 power enable output (PRTPWR1) and the Port 1 over-current sense input (OCS1_N). Refer to the PRTPWR1 and OCS1_N descriptions for additional information.
	Port 1 Battery Charging Configuration Strap	BC_EN1	IS	This strap is used to indicate support of the battery charging protocol on Port 1. Enabling battery charging support allows a device on the port to draw currents per the USB battery charging specification. 0 = Battery charging is not supported on Port 1 1 = Battery charging is supported on Port 1 See Note 3-3 for more information on configuration straps.
1	Port 2 Power Output	PRTPWR2	O8	Enables power to a downstream USB device attached to Port 2. 0 = Power disabled on downstream Port 2 1 = Power enabled on downstream Port 2
	Port 2 Control	PRTCTL2	OD8/IS (PU)	When configured as PRTCTL2, this pin functions as both the Port 2 power enable output (PRTPWR2) and the Port 2 over-current sense input (OCS2_N). Refer to the PRTPWR2 and OCS2_N descriptions for additional information.
	Port 2 Battery Charging Configuration Strap	BC_EN2	IS	This strap is used to indicate support of the battery charging protocol on Port 2. Enabling battery charging support allows a device on the port to draw currents per the USB battery charging specification. 0 = Battery charging is not supported on Port 2 1 = Battery charging is supported on Port 2 See Note 3-3 for more information on configuration straps.
1	Port 3 Power Output	PRTPWR3	O8	Enables power to a downstream USB device attached to Port 3. 0 = Power disabled on downstream Port 3 1 = Power enabled on downstream Port 3
	Port 3 Control	PRTCTL3	OD8/IS (PU)	When configured as PRTCTL3, this pin functions as both the Port 3 power enable output (PRTPWR3) and the Port 3 over-current sense input (OCS3_N). Refer to the PRTPWR3 and OCS3_N descriptions for additional information.
	Port 3 Battery Charging Configuration Strap	BC_EN3	IS	This strap is used to indicate support of the battery charging protocol on Port 3. Enabling battery charging support allows a device on the port to draw currents per the USB battery charging specification. 0 = Battery charging is not supported on Port 3 1 = Battery charging is supported on Port 3 See Note 3-3 for more information on configuration straps.

TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
5	No Connect	NC	-	These pins must be left floating for normal device operation.
POWER				
3	+3.3V Analog Power Supply	VDDA33	P	+3.3V analog power supply. Refer to Section 4.0, "Power Connections," on page 16 for power connection information.
2	+3.3V Power Supply	VDD33	P	+3.3V power supply. These pins must be connected to VDDA33. Refer to Section 4.0, "Power Connections," on page 16 for power connection information.
1	+1.2V Core Power Supply	VDDCR12	P	+1.2V core power supply. A 1.0 µF (<1 Ω ESR) capacitor to ground is required for regulator stability. The capacitor should be placed as close as possible to the device. Refer to Section 4.0, "Power Connections," on page 16 for power connection information.
Exposed Pad on package bottom (Figure 3-1)	Ground	VSS	P	Common ground. This exposed pad must be connected to the ground plane with a via array.

Note 3-1 The LOCAL_PWR pin is sampled during the configuration state, immediately after negation of reset, to determine whether the device is bus-powered or self-powered. When configuration is complete, the latched value will not change until the next reset assertion. To enable dynamic local power switching, the DYNAMIC_POWER register at location 0x4134 must be programmed with 0x41. If dynamic power switching is not required, the DYNAMIC_POWER register should be left at the default value of 0xC1. Programming may be performed through the SMBus interface, or permanently via OTP. Refer to the Protouch MPT User Manual for additional information.

Note 3-2 If using the local power detect function (LOCAL_PWR pin), the NON_REM[1:0] configuration straps cannot be used to configure the non-removable state of the USB ports. In this case, the non-removable state of the ports must be configured in internal device registers via the Protouch tool or SMBus.

Note 3-3 Configuration strap values are latched on Power-On Reset (POR) and the rising edge of RESET_N (external chip reset). Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 6.3, "Device Configuration Straps," on page 23 for additional information.

3.2 Pin Assignments

TABLE 3-2: 36-SQFN PACKAGE PIN ASSIGNMENTS

Pin Num	Pin Name	Pin Num	Pin Name
1	SWAP_USBDN1_DM/PRT_DIS_M1	19	UART_RX/OCS3_N
2	SWAP_USBDN1_DP/PRT_DIS_P1	20	NC
3	USBDN2_DM/PRT_DIS_M2	21	UART_TX/
4	USBDN2_DP/PRT_DIS_P2	22	SDA/SMBDATA/NON_REM1
5	NC	23	VDD33
6	USBDN3_DM/PRT_DIS_M3	24	SCL/SMBCLK/CFG_SEL0
7	USBDN3_DP/PRT_DIS_P3	25	HS_IND/CFG_SEL1
8	NC	26	RESET_N
9	NC	27	VBUS_DET

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TABLE 3-2: 36-SQFN PACKAGE PIN ASSIGNMENTS (CONTINUED)

Pin Num	Pin Name	Pin Num	Pin Name
10	VDDA33	28	SUSP_IND/LOCAL_PWR/NON_REM0
11	LED0	29	VDDA33
12	PRTPWR1/PRTCTL1/BC_EN1	30	FLEX_USBUP_DM
13	OCS1_N	31	FLEX_USBUP_DP
14	VDDCR12	32	XTAL2
15	VDD33	33	XTAL1/REFCLK
16	PRTPWR2/PRTCTL2/BC_EN2	34	NC
17	OCS2_N	35	RBIAS
18	PRTPWR3/PRTCTL3/BC_EN3	36	VDDA33

3.3 Buffer Type Descriptions

TABLE 3-3: BUFFER TYPES

Buffer Type	Description
IS	Schmitt-triggered input
I_RST	Reset Input
I_SMB	I^2C/SMBus Clock Input
O8	Output with 8 mA sink and 8 mA source
OD8	Open-drain output with 8 mA sink
OD12	Open-drain output with 12 mA sink
PU	50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
AIO	Analog bi-directional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin

4.0 POWER CONNECTIONS

4.1 Integrated Power Regulators

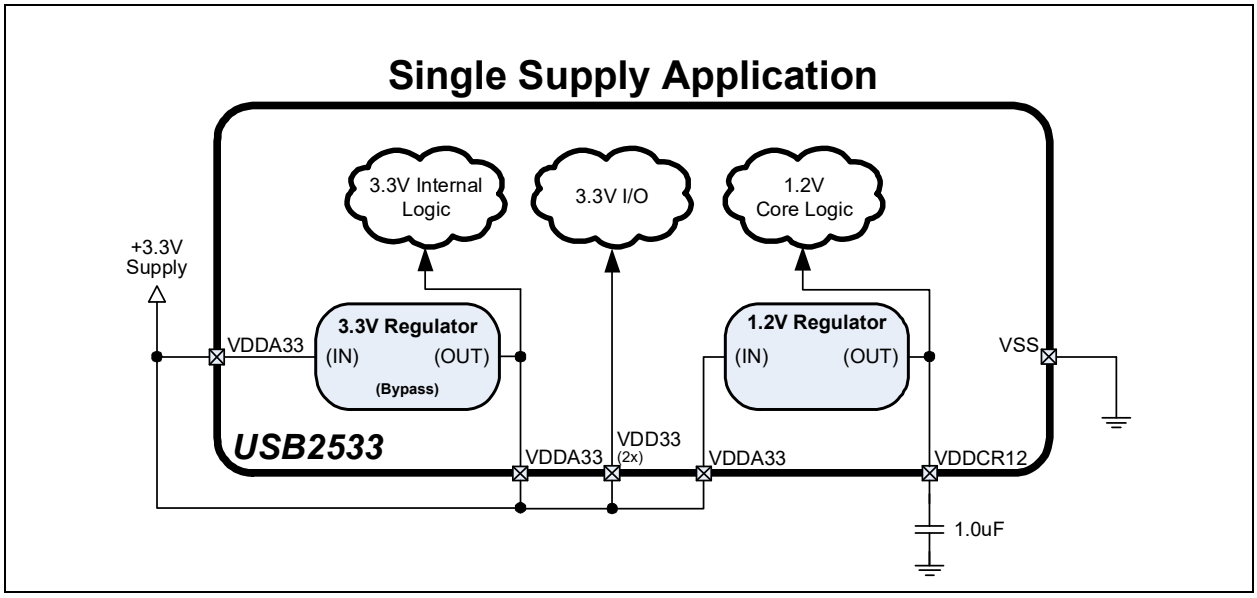
The integrated 3.3V and 1.2V power regulators allow the device to be supplied via a single 3.3V external power supply.

The regulators are controlled by RESET_N. When RESET_N is brought high, the 3.3V regulator will turn on. When RESET_N is brought low the 3.3V regulator will turn off.

4.2 Power Connection Diagrams

Figure 4-1 illustrates the power connections for the USB2533.

FIGURE 4-1: POWER CONNECTIONS



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5.0 MODES OF OPERATION

The device provides two main modes of operation: Standby Mode and Hub Mode. The operating mode of the device is selected by setting values on primary inputs according to the table below.

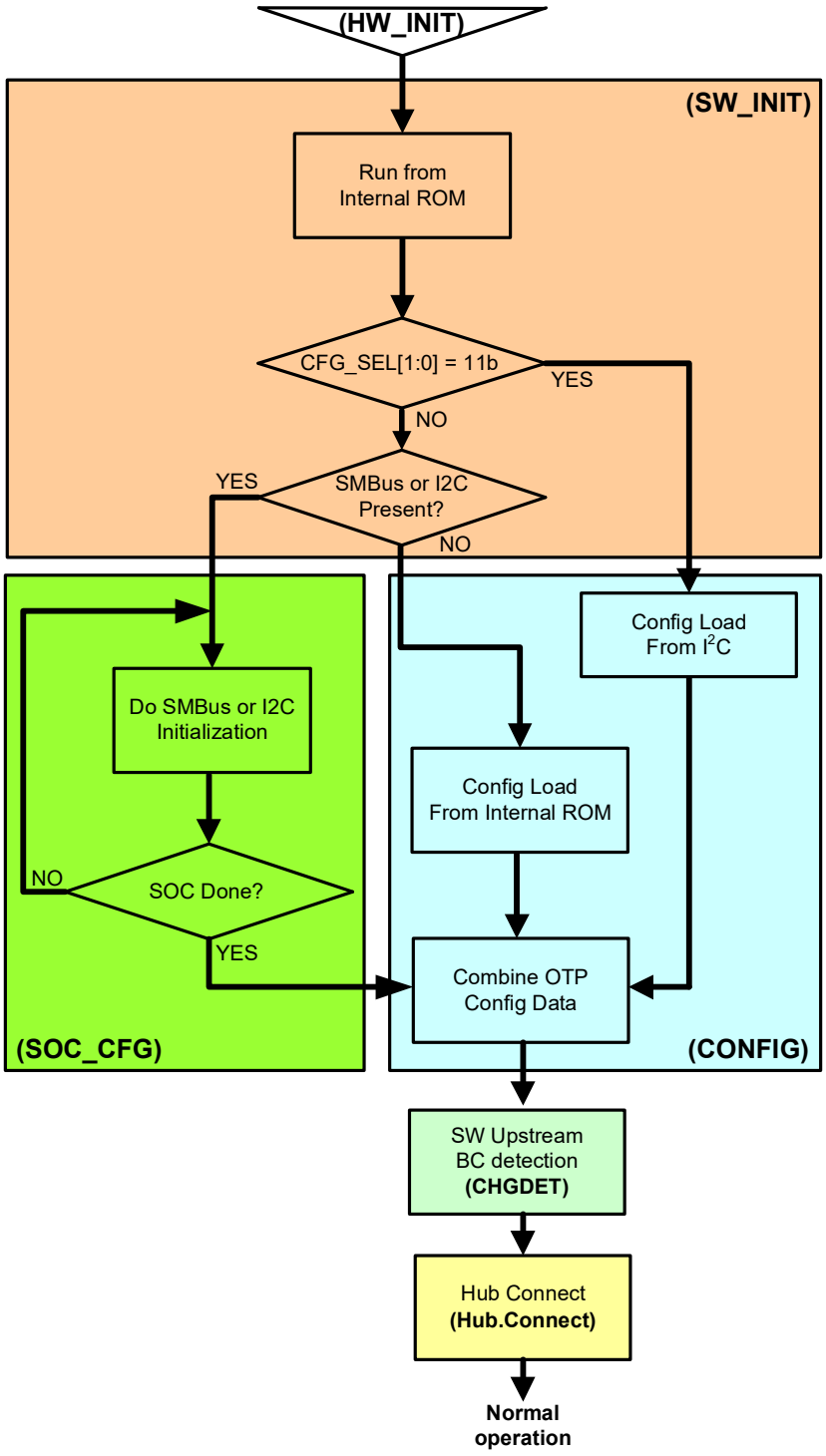
TABLE 5-1: CONTROLLING MODES OF OPERATION

RESET_N Input	Resulting Mode	Summary
0	Standby	**Lowest Power Mode**: No functions are active other than monitoring the RESET_N input. All port interfaces are high impedance. All regulators are powered off.
1	Hub	**Full Feature Mode**: Device operates as a configurable USB hub with battery charger detection. Power consumption is based on the number of active ports, their speed, and amount of data transferred.

Note: Refer to Section 8.3.2, "External Chip Reset (RESET_N)," on page 29 for additional information on RESET_N.

The flowchart in Figure 5-1 shows the modes of operation. It also shows how the device traverses through the Hub mode stages (shown in bold.) The flow of control is dictated by control register bits shown in italics as well as other events such as availability of a reference clock. The remaining sections in this chapter provide more detail on each stage and mode of operation.

FIGURE 5-1: HUB OPERATIONAL MODE FLOWCHART



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5.1 Boot Sequence

5.1.1 STANDBY MODE

If the external hardware reset is asserted, the hub will be in Standby Mode. This mode provides a very low power state for maximum power efficiency when no signaling is required. This is the lowest power state. In Standby Mode all internal regulators are powered off, the PLL is not running, and core logic is powered down in order to minimize power consumption. Because core logic is powered off, no configuration settings are retained in this mode and must be re-initialized after RESET_N is negated high.

5.1.2 HARDWARE INITIALIZATION STAGE (HW_INIT)

The first stage is the initialization stage and occurs on the negation of RESET_N. In this stage the 1.2V regulator is enabled and stabilizes, internal logic is reset, and the PLL locks if a valid REFCLK is supplied. Configuration registers are initialized to their default state and strap input values are latched. The device will complete initialization and automatically enter the next stage. Because the digital logic within the device is not yet stable, no communication with the device using the SMBus is possible. Configuration registers are initialized to their default state.

If there is a REFCLK present, the next state is SW_INIT.

5.1.3 SOFTWARE INITIALIZATION STAGE (SW_INIT)

Once the hardware is initialized, the firmware can begin to execute from the internal ROM. The firmware checks the CFG_SEL[1:0] configuration strap values to determine if it is configured for I^2C Master loading. If so, the configuration is loaded from an external I^2C ROM in the device's CONFIG state.

For all other configurations, the firmware checks for the presence of an external I^2C/SMBus. It does this by asserting two pull down resistors on the data and clock lines of the bus. The pull downs are typically 50Kohm. If there are 10Kohm pull-ups present, the device becomes aware of the presence of an external SMBus/I^2C bus. If a bus is detected, the firmware transitions to the SOC_CFG state.

5.1.4 SOC CONFIGURATION STAGE (SOC_CFG)

In this stage, the SOC may modify any of the default configuration settings specified in the integrated ROM such as USB device descriptors, or port electrical settings, and control features such as upstream battery charging detection.

There is no time limit. In this stage the firmware will wait indefinitely for the SMBus/I^2C configuration. When the SOC has completed configuring the device, it must write to register 0xFF to end the configuration.

5.1.5 CONFIGURATION STAGE (CONFIG)

Once the SOC has indicated that it is done with configuration, then all the configuration data is combined. The default data, the SOC configuration data, the OTP data are all combined in the firmware and device is programmed.

After the device is fully configured, it will go idle and then into suspend if there is no VBUS or Hub.Connect present. Once VBUS is present, and upstream battery charging is enabled, the device will transition to the Battery Charger Detection Stage (CHGDET). If VBUS is present, and upstream battery charging is not enabled, the device will transitions to the Connect (Hub.Connect) stage.

5.1.6 BATTERY CHARGER DETECTION STAGE (CHGDET)

After configuration, if enabled, the device enters the Battery Charger Detection Stage. If the battery charger detection feature was disabled during the CONFIG stage, the device will immediately transition to the Hub Connect (Hub.Connect) stage. If the battery charger detection feature remains enabled, the battery charger detection sequence is started automatically.

If the charger detection remains enabled, the device will transition to the Hub.Connect stage if using the hardware detection mechanism.

5.1.7 HUB CONNECT STAGE (HUB.CONNECT)

Once the CHGDET stage is completed, the device enters the Hub.Connect stage.

5.1.8 NORMAL MODE

Lastly the SOC enters the Normal Mode of operation. In this stage, full USB operation is supported under control of the USB Host on the upstream port. The device will remain in the normal mode until the operating mode is changed by the system.

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If RESET_N is asserted low, then Standby Mode is entered. The device may then be placed into any of the designated Hub stages. Asserting the soft disconnect on the upstream port will cause the Hub to return to the Hub.Connect stage until the soft disconnect is negated.

To save power, communication over the SMBus is not supported while in USB Suspend. The system can prevent the device from going to sleep by asserting the ClkSusp control bit of the Configure Portable Hub Register anytime before entering USB Suspend. While the device is kept awake during USB Suspend, it will provide the SMBus functionality at the expense of not meeting USB requirements for average suspend current consumption.

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6.0 DEVICE CONFIGURATION

The device supports a large number of features (some mutually exclusive), and must be configured in order to correctly function when attached to a USB host controller. The hub can be configured either internally or externally depending on the implemented interface.

Microchip provides a comprehensive software programming tool, Pro-Touch, for configuring the USB2533 functions, registers and OTP memory. All configuration is to be performed via the Pro-Touch programming tool. For additional information on the Pro-Touch programming tool, contact your local Microchip sales representative.

6.1 Configuration Method Selection

The CFG_SEL[1:0] configuration straps and the SDA pin are used to determine the hub configuration method, as shown in Table 6-1. The software reads the SDA pin and the CFG_SEL[1:0] bits and configures the system appropriately.

TABLE 6-1: HUB CONFIGURATION SELECTION

SDA	CFG_SEL1	CFG_SEL0	Description
X	0	0	Configuration is based on the configuration strap options and internal OTP settings. This configuration sets the device Self powered operation.
0	0	1	Invalid
X	1	0	Configuration based on the configuration strap options and internal OTP settings. This configuration sets the device for Bus powered operation.
1	1	1	Firmware performs a configuration load from 2-wire (I^2C) EEPROM. The device does not perform an SMBus Master detection. Configuration is controlled by EEPROM values and OTP settings. Strap options are disabled.
1	0	1	Firmware must wait for configuration from an SMBus Master. Configuration is controlled by SMBus Master and OTP settings. Strap options are disabled.

Note: Refer to Section 7.0, "Device Interfaces," on page 25 for detailed information on each device configuration interface.

6.2 Customer Accessible Functions

The following USB or SMBus accessible functions are available to the customer via the Pro-Touch Programming Tool.

Note: For additional programming details, refer to the Pro-Touch Programming Tool User Manual.

6.2.1 USB ACCESSIBLE FUNCTIONS

6.2.1.1 VSM commands over USB

By default, Vendor Specific Messaging (VSM) commands to the hub are enabled. The supported commands are:

- Enable Embedded Controller
- Disable Embedded Controller
- Enable Special Resume
- Disable Special Resume
- Reset Hub

6.2.1.2 I^2C Master Access over USB

Access to I^2C devices is performed as a pass-through operation from the USB Host. The device firmware has no knowledge of the operation of the attached I^2C device. The supported commands are:

- Enable I^2C pass through mode
- Disable I^2C pass through mode

- I^2C write
- I^2C read
- Send I^2C start
- Send I^2C stop

6.2.1.3 OTP Access over USB

The OTP ROM in the device is accessible via the USB bus. All OTP parameters can modified via the USB Host. The OTP operates in Single Ended mode. The supported commands are:

- Enable OTP reset
- Set OTP operating mode
- Set OTP read mode
- Program OTP
- Get OTP status
- Program OTP control parameters

6.2.1.4 Battery Charging Access over USB

The Battery charging behavior of the device can be dynamically changed by the USB Host when something other than the preprogrammed or OTP programmed behavior is desired. The supported commands are:

- Enable/Disable battery charging
- Upstream battery charging mode control
- Downstream battery charging mode control
- Battery charging timing parameters
- Download custom battery charging algorithm

6.2.1.5 Other Embedded Controller functions over USB

The following miscellaneous functions may be configured via USB:

- Enable/Disable Embedded controller enumeration
- Program Configuration parameters.
- Program descriptor fields:
  - Language ID
  - Manufacturer string
  - Product string
  - idVendor
  - idProduct
  - bcdDevice

6.2.2 SMBUS ACCESSIBLE FUNCTIONS

6.2.2.1 OTP Access over SMBus

The device’s OTP ROM is accessible over SMBus. All OTP parameters can modified via the SMbus Host. The OTP can be programmed to operate in Single-Ended, Differential, Redundant, or Differential Redundant mode, depending on the level of reliability required. The supported commands are:

- Enable OTP reset
- Set OTP operating mode
- Set OTP read mode
- Program OTP
- Get OTP Status
- Program OTP control parameters

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6.2.2.2 Configuration Access over SMBus

The following functions are available over SMBus prior to the hub attaching to the USB host:

- Program Configuration parameters.
- Program descriptor fields:
  - Language ID
  - Manufacturer string
  - Product string
  - idVendor
  - idProduct
  - bcdDevice
- Program Control Register

6.3 Device Configuration Straps

Configuration straps are multi-function pins that are driven as outputs during normal operation. During a Power-On Reset (POR) or an External Chip Reset (RESET_N), these outputs are tri-stated. The high or low state of the signal is latched following de-assertion of the reset and is used to determine the default configuration of a particular feature. Configuration straps are latched as a result of a Power-On Reset (POR) or a External Chip Reset (RESET_N). Configuration strap signals are noted in Section 3.0, "Pin Descriptions," on page 7 and are identified by an underlined symbol name. The following sub-sections detail the various configuration straps.

Configuration straps include internal resistors in order to prevent the signal from floating when unconnected. If a particular configuration strap is connected to a load, an external pull-up or pull-down should be used to augment the internal resistor to ensure that it reaches the required voltage level prior to latching. The internal resistor can also be overridden by the addition of an external resistor.

Note:

- The system designer must ensure that configuration straps meet the timing requirements specified in Section 9.6.2, "Reset and Configuration Strap Timing," on page 36 and Section 9.6.1, "Power-On Configuration Strap Valid Timing," on page 36. If configuration straps are not at the correct voltage level prior to being latched, the device may capture incorrect strap values.
- Configuration straps must never be driven as inputs. If required, configuration straps can be augmented, or overridden with external resistors.

6.3.1 NON-REMOVABLE DEVICE (NON_REM[1:0])

The NON_REM[1:0] configuration straps are sampled at RESET_N negation to determine if ports [3:1] contain permanently attached (non-removable) devices as follows. Additionally, because the SUSP_IND indicator functionality is shared with the NON_REM0 configuration strap, the active state of the LED connected to SUSP_IND will be determined as follows:

TABLE 6-2: NON_REM[1:0] CONFIGURATION DEFINITIONS

NON_REM[1:0]	Definition
‘00’	All USB ports removable, SUSP_IND LED active high
‘01’	Port 1 is non-removable, SUSP_IND LED active low
‘10’	Ports 1 & 2 are non-removable, SUSP_IND LED active high
‘11’	Ports 1, 2 & 3 are non-removable, SUSP_IND LED active low

Note: If using the local power detect function (LOCAL_PWR pin), the NON_REM[1:0] configuration straps cannot be used to configure the non-removable state of the USB ports. In this case, the non-removable state of the ports must be configured in internal device registers via the Protouch tool or SMBus.

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6.3.2 CONFIGURATION SELECT (CFG_SEL[1:0])

Refer to Section 6.1, "Configuration Method Selection," on page 21 for details on CFG_SEL[1:0].

6.3.3 DOWNSTREAM BATTERY CHARGING ENABLE (BC_EN[3:1])

The battery charging enable configuration straps are used to enable battery charging on the corresponding downstream port. For example, if BC_EN1 is driven high during the configuration strap latching time, downstream port 1 will indicate support of battery charging. Refer to Section 8.1.2, "Downstream Battery Charging," on page 28 for additional information on battery charging.

6.3.4 PORT DISABLE (PRT_DIS_M*X*/PRT_DIS_P*X*)

These configuration straps disable the associated USB ports D- and D+ signals, respectively, where "*x*" is the USB port number. Both the negative "M" and positive "P" port disable configuration straps for a given USB port must be tied high at reset to disable the associated port.

TABLE 6-3: PRT_DIS_M*X*/PRT_DIS_P*X* CONFIGURATION DEFINITIONS

PRT_DIS_M*x*/PRT_DIS_P*x*	Definition
'0'	Port *x* D-/D+ Signal is Enabled (Default)
'1'	Port *x* D-/D+ Signal is Disabled

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7.0 DEVICE INTERFACES

The USB2533 provides multiple interfaces for configuration and external memory access. This chapter details the various device interfaces and their usage.

Note: For information on device configuration, refer to Section 6.0, "Device Configuration," on page 21.

7.1 I²C Master Interface

The I²C master interface implements a subset of the I²C Master Specification (Please refer to the *Philips Semiconductor Standard I²C-Bus Specification* for details on I²C bus protocols). The device's I²C master interface is designed to attach to a single "dedicated" I²C EEPROM for loading configuration data and conforms to the Standard-Mode I²C Specification (100 kbit/s transfer rate and 7-bit addressing) for protocol and electrical compatibility. The device acts as the master and generates the serial clock SCL, controls the bus access (determines which device acts as the transmitter and which device acts as the receiver), and generates the START and STOP conditions.

Note:

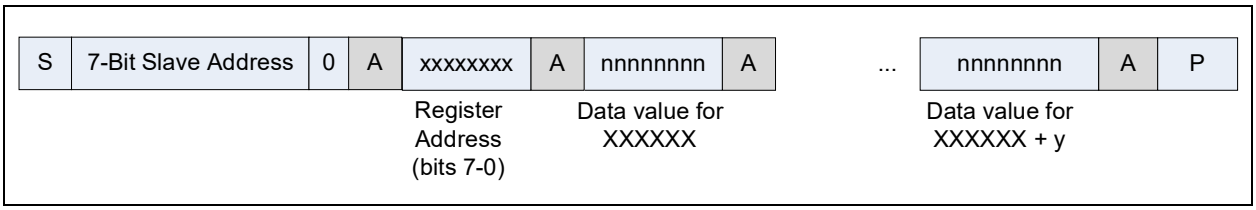
- Extensions to the I²C Specification are not supported.
- All device configuration must be performed via the Pro-Touch Programming Tool. For additional information on the Pro-Touch programming tool, contact your local sales representative.

7.1.1 I²C MESSAGE FORMAT

7.1.1.1 Sequential Access Writes

The I²C interface supports sequential writing of the device's register address space. This mode is useful for configuring contiguous blocks of registers. Figure 7-1 shows the format of the sequential write operation. Where color is visible in the figure, blue indicates signaling from the I²C master, and gray indicates signaling from the slave.

FIGURE 7-1: I²C SEQUENTIAL ACCESS WRITE FORMAT



In this operation, following the 7-bit slave address, the 8-bit register address is written indicating the start address for sequential write operation. Every subsequent access is a data write to a data register, where the register address increments after each access and an ACK from the slave occurs. Sequential write access is terminated by a Stop condition.

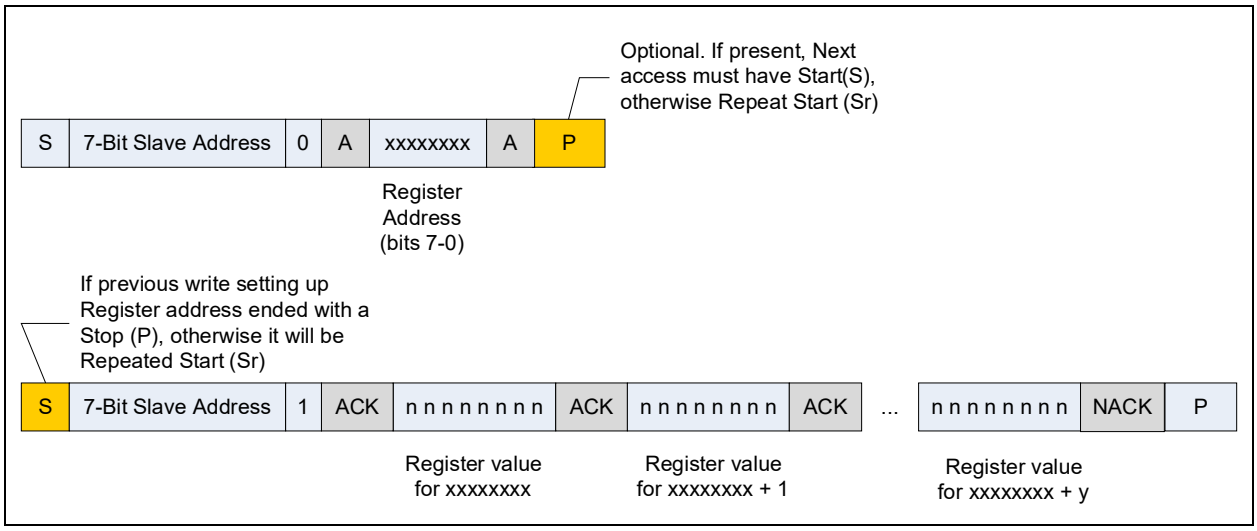
7.1.1.2 Sequential Access Reads

The I²C interface supports direct reading of the device registers. In order to read one or more register addresses, the starting address must be set by using a write sequence followed by a read. The read register interface supports auto-increment mode. The master must send a NACK instead of an ACK when the last byte has been transferred.

In this operation, following the 7-bit slave address, the 8-bit register address is written indicating the start address for the subsequent sequential read operation. In the read sequence, every data access is a data read from a data register where the register address increments after each access. The write sequence can end with optional Stop (P). If so, the read sequence must begin with a Start (S). Otherwise, the read sequence must start with a Repeated Start (Sr).

Figure 7-2 shows the format of the read operation. Where color is visible in the figure, blue and gold indicate signaling from the I²C master, and gray indicates signaling from the slave.

FIGURE 7-2: I²C SEQUENTIAL ACCESS READ FORMAT



7.1.2 PULL-UP RESISTORS FOR I²C

The circuit board designer is required to place external pull-up resistors (10 kΩ recommended) on the SDA & SCL signals (per SMBus 1.0 Specification) to Vcc in order to assure proper operation.

7.2 SMBus Slave Interface

The USB2533 includes an integrated SMBus slave interface, which can be used to access internal device run time registers or program the internal OTP memory. SMBus detection is accomplished by detection of pull-up resistors (10 KΩ recommended) on both the SMBDATA and SMBCLK signals. To disable the SMBus, a pull-down resistor of 10 KΩ must be applied to SMBDATA. The SMBus interface can be used to configure the device as detailed in Section 6.1, "Configuration Method Selection," on page 21.

Note:	All device configuration must be performed via the Pro-Touch Programming Tool. For additional information on the Pro-Touch programming tool, contact your local Microchip sales representative.

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8.0 FUNCTIONAL DESCRIPTIONS

This chapter provides additional functional descriptions of key device features.

8.1 Battery Charger Detection & Charging

The USB2533 supports both upstream battery charger detection and downstream battery charging. The integrated battery charger detection circuitry supports the USB-IF Battery Charging (BC1.2) detection method and most Apple devices. These circuits are used to detect the attachment and type of a USB charger and provide an interrupt output to indicate charger information is available to be read from the device's status registers via the serial interface. The USB2533 provides the battery charging handshake and supports the following USB-IF BC1.2 charging profiles:

- DCP: Dedicated Charging Port (Power brick with no data)
- CDP: Charging Downstream Port (1.5A with data)
- SDP: Standard Downstream Port (0.5A with data)
- Custom profiles loaded via SMBus or OTP

The following sub-sections detail the upstream battery charger detection and downstream battery charging features.

8.1.1 UPSTREAM BATTERY CHARGER DETECTION

Battery charger detection is available on the upstream facing port. The detection sequence is intended to identify chargers which conform to the Chinese battery charger specification, chargers which conform to the USB-IF Battery Charger Specification 1.2, and most Apple devices.

In order to detect the charger, the device applies and monitors voltages on the upstream DP and DM pins. If a voltage within the specified range is detected, the device will be updated to reflect the proper status.

The device includes the circuitry required to implement battery charging detection using the Battery Charging Specification. When enabled, the device will automatically perform charger detection upon entering the Hub.ChgDet stage in Hub Mode. The device includes a state machine to provide the detection of the USB chargers listed in the table below.

TABLE 8-1: CHARGERS COMPATIBLE WITH UPSTREAM DETECTION

USB Attach TypeE	DP/DM Profile	Charger Type
DCP (Dedicated Charging Port)	Shorted < 200ohm	001
CDP (Charging Downstream Port)	VDP reflected to VDM	010 (EnhancedChrgDet = 1)
SDP (Standard Downstream Port) USB Host or downstream hub port	15Kohm pull-down on DP and DM	011
Apple Low Current Charger	Apple	100
Apple High Current Charger	Apple	101
Apple Super High Current Charger	DP=2.7V DM=2.0V	110
Apple Charger Low Current Charger (500mA)	DP=2.0V DM=2.0V	100
Apple Charger High Current Charger (1000mA)	DP=2.0V DM=2.7V	101

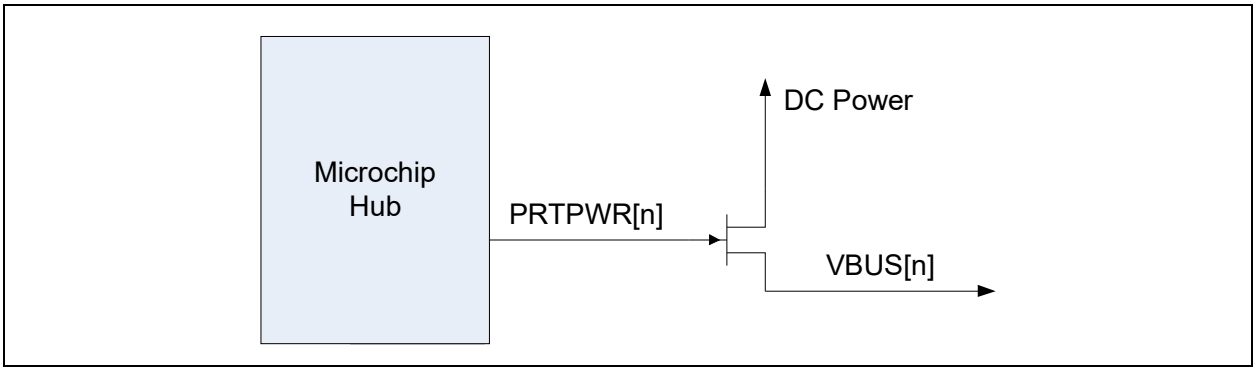
If a custom charger detection algorithm is desired, the SMBus registers can also be used to control the charger detection block to implement a custom charger detection algorithm. In order to avoid negative interactions with automatic battery charger detection or normal hub operation, the user should only attempt Custom battery charger detection during the Hub.Config stage or Hub.Connect stage. No logic is implemented to disable custom detection at other times - it is up to the user software to observe this restriction.

There is a possibility that the system is not running the reference clock when battery charger detection is required (for example if the battery is dead or missing). During the Hub.WaitRefClk stage the battery charger detection sequence can be configured to be followed regardless of the activity of REFCLK by relying on the operation of the internal oscillator.

8.1.2 DOWNSTREAM BATTERY CHARGING

The device can be configured by an OEM to have any of the downstream ports to support battery charging. The Hub's role in battery charging is to provide an acknowledge to a device's query as to if the hub system supports USB battery charging. The hub silicon does not provide any current or power FETs or any additional circuitry to actually charge the device. Those components must be provided as externally by the OEM.

FIGURE 8-1: BATTERY CHARGING EXTERNAL POWER SUPPLY



If the OEM provides an external supply capable of supplying current per the battery charging specification, the hub can be configured to indicate the presence of such a supply to the device. This indication, via the PRTPWR[1:4] output pins, is on a per/port basis. For example, the OEM can configure two ports to support battery charging through high current power FET's and leave the other two ports as standard USB ports.

8.1.2.1 Downstream Battery Charging Modes

In the terminology of the USB Battery Charging Specification, if a port is configured to support battery charging, the downstream port is a considered a CDP (Charging Downstream Port) if connected to a USB host, or a DCP (Dedicated Charging Port) if not connected to a USB host. If the port is not configured to support battery charging, the port is considered an SDP (Standard Downstream Port). All charging ports have electrical characteristics different from standard non-charging ports.

A downstream port will behave as a CDP, DCP, or SDP depending on the port’s configuration and mode of operation. The port will not switch between a CDP/DCP or SDP at any time after initial power-up and configuration. A downstream port can be in one of three modes shown in the table below.

TABLE 8-2: DOWNSTREAM PORT TYPES

USB Attach Type	DP/DM Profile
DCP (Dedicated Charging Port)	Apple charging mode or China Mode (Shorted < 200ohm) or MCHP custom mode
CDP (Charging Downstream Port)	VDP reflected to VDM
SDP (Standard Downstream Port) USB Host or downstream hub port	15Kohm pull-down on DP and DM

8.1.2.2 Downstream Battery Charging Configuration

Configuration of ports to support battery charging is performed via the BC_EN configuration straps, USB configuration, SMBus configuration, or OTP. The Battery Charging Enable Register provides per port battery charging configuration. Starting from bit 1, this register enables battery charging for each down stream port when asserted. Bit 1 represents port 1 and so on. Each port with battery charging enabled asserts the corresponding PRTPWR register bit.

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8.1.2.3 Downstream Over-Current Management

It is the devices responsibility to manage over-current conditions. Over-Current Sense (OCS) is handled according to the USB specification. For battery charging ports, PRTPWR is driven high (asserted) after hardware initialization. If an OCS event occurs, the PRTPWR is negated. PRTPWR will be negated for all ports in a ganged configuration. Only the respective PRTPWR will be negated in the individual configuration.

If there is an over-current event in DCP mode, the port is turned off for one second and is then re-enabled. If the OCS event persists, the cycle is repeated for a total or three times. If after three attempts, the OCS still persists, the cycle is still repeated, but with a retry interval of ten seconds. This retry persists for indefinitely. The indefinite retry prevents a defective device from permanently disabling the port.

In CDP or SDP mode, the port power and over-current events are controlled by the USB host. The OCS event does not have to be registered. When and if the hub is connected to a host, the host will initialize the hub and enable its port power. If the over current still exists, it will be notified at that point.

8.2 Flex Connect

This feature allows the upstream port to be swapped with downstream physical port 1. Only downstream port 1 can be swapped physically. Using port remapping, any logical port (number assignment) can be swapped with the upstream port (non-physical).

Flex Connect is enabled/disabled via two control bits in the Connect Configuration Register. The FLEXCONNECT configuration bit switches the port, and EN_FLEX_MODE enables the mode.

8.2.1 PORT CONTROL

Once EN_FLEX_MODE bit is set, the functions of certain pins change, as outlined below.

If EN_FLEX_MODE is set and FLEXCONNECT is not set:

1. PRTPWR1 enters combined mode, becoming PRTPWR1/OCS1_N
2. OCS1_N becomes a don’t care
3. SUSPEND outputs ‘0’ to keep any upstream power controller off

If EN_FLEX_MODE is set and FLEXCONNECT is set:

1. The normal upstream VBUS pin becomes a don’t care
2. PRTPWR1 is forced to a ‘1’ in combined mode, keeping the port power on to the application processor.
3. OCS1 becomes VBUS from the application processor through a GPIO
4. SUSPEND becomes PRTPWR1/OCS1_N for the port power controller for the connector port

8.3 Resets

The device has the following chip level reset sources:

- Power-On Reset (POR)
- External Chip Reset (RESET_N)
- USB Bus Reset

8.3.1 POWER-ON RESET (POR)

A power-on reset occurs whenever power is initially supplied to the device, or if power is removed and reapplied to the device. A timer within the device will assert the internal reset per the specifications listed in Section 9.6.1, "Power-On Configuration Strap Valid Timing," on page 36.

8.3.2 EXTERNAL CHIP RESET (RESET_N)

A valid hardware reset is defined as assertion of RESET_N, after all power supplies are within operating range, per the specifications in Section 9.6.2, "Reset and Configuration Strap Timing," on page 36. While reset is asserted, the device (and its associated external circuitry) enters Standby Mode and consumes minimal current.

Assertion of RESET_N causes the following:

1. The PHY is disabled and the differential pairs will be in a high-impedance state.
2. All transactions immediately terminate; no states are saved.

3. All internal registers return to the default state.
4. The external crystal oscillator is halted.
5. The PLL is halted.

Note: All power supplies must have reached the operating levels mandated in Section 9.2, "Operating Conditions**," on page 33, prior to (or coincident with) the assertion of RESET_N.

8.3.3 USB BUS RESET

In response to the upstream port signaling a reset to the device, the device performs the following:

Note: The device does not propagate the upstream USB reset to downstream devices.

1. Sets default address to 0.
2. Sets configuration to: Unconfigured.
3. Moves device from suspended to active (if suspended).
4. Complies with Section 11.10 of the USB 2.0 Specification for behavior after completion of the reset sequence.

The host then configures the device in accordance with the USB Specification.

8.4 Link Power Management (LPM)

The device supports the L0 (On), L1 (Sleep), and L2 (Suspend) link power management states per the USB 2.0 Link Power Management Addendum. These supported LPM states offer low transitional latencies in the tens of microseconds versus the much longer latencies of the traditional USB suspend/resume in the tens of milliseconds. The supported LPM states are detailed in Table 8-3. For additional information, refer to the USB 2.0 Link Power Management Addendum.

TABLE 8-3: LPM STATE DEFINITIONS

State	Description	Entry/Exit Time to L0
L2	Suspend	Entry: ~3 ms Exit: ~2 ms
L1	Sleep	Entry: ~65 us Exit: ~100 us
L0	Fully Enabled (On)	-

Note:
- State change timing is approximate and is measured by change in power consumption.
- System clocks are stopped only in suspend mode or when power is removed from the device.

8.5 Remote Wakeup Indicator (SUSP_IND)

The remote wakeup indicator feature uses the SUSP_IND as a side band signal to wake up the host when in suspend. This feature is enabled and disabled via the HUB_RESUME_INHIBIT configuration bit in the hub configuration space register CFG3. The only way to control the bit is by configuration EEPROM, SMBus or internal ROM default setting. The state is only modified during a power on reset, or hardware reset. No dynamic reconfiguring of this capability is possible.

When HUB_RESUME_INHIBIT = ‘0’, Normal Resume Behavior per the USB 2.0 specification

When HUB_RESUME_INHIBIT = ‘1’, Modified Resume Behavior is enabled

Refer to the following subsections for additional details.

8.5.1 NORMAL RESUME BEHAVIOR

VBUS_DET is used to detect presence of the Host. If VBUS_DET = ‘1’, then D+ pull-up is asserted and normal USB functionality is enabled. The SUSP_IND provides an indication of the active or suspended state of the hub.

The Hub will drive a ‘K’ on the upstream port if required to do so by USB protocol.

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If VBUS_DET = ‘0’, then the D+ pull-up is negated. If battery charging is not enabled, the internal hub logic will be reset, thus negating all downstream ports and associated downstream VBUS enable signals. The hub will need to be re-enumerated to function, much like a new connect or after a complete system reset.

8.5.2 MODIFIED RESUME BEHAVIOR

When the modified resume feature is enabled, the hub functions as follows:

VBUS_DET is used to detect presence of the Host. If VBUS_DET = ‘1’, then D+ pull-up is asserted and normal USB functionality is enabled. SUSP_IND provides an indication of the active or suspended state of the hub.

The device will drive a ‘K’ on the upstream port and downstream ports if required to do so by USB protocol. The device will act as a controlling hub if required to do so by the USB protocol.

If VBUS_DET = ‘0’, then the D+ pull-up is negated, but the hub will not be internally reset. It will power-on the downstream ports. The hub is able to continue to detect downstream remote wake events.

SUSP_IND provides an indication of the active or suspended state of the hub.

If a USB 2.0 specification compliant resume or wake event is detected by the device, the device is remote wake enabled, and a port status change event occurs, SUSP_IND will be driven for the time given in the GLOBAL_RESUME_TIME register.

If a remote wake event is detected on a downstream port:

1. Device disconnect
2. Device connect
3. A currently connected device requests remote wake-up.

Note:	Downstream resume events are filtered for approximately 100uS by internal logic.

The device will not drive a ‘K’ on the upstream port. Instead, the SUSP_IND will be driven for approximately 14 ms. The ‘K’ is not driven upstream because this would potentially back drive a powered-down host. The device will drive RESUME to only the downstream ports which transmitted the remote wake signal per the requirements of the USB 2.0 specification for controlling hub behavior.

Note:	SUSP_IND is a one shot event. It will assert with each wake event detection. It will not repeatedly assert in proxy for downstream devices.

For the case where the Host responds and turns on VBUS and can drive a ‘K’ downstream within the 14 ms time frame of a standard resume (measured from the SUSP_IND pin), then the hub detects the ‘K’. It will discontinue “Controlling Hub” activities, drive resume signaling on any other ports, and function as expected per the USB 2.0 Specification with respect to a resume event. It will permit the host to take over resume signaling.

For the case where the host is not able to drive a ‘K’ within the 14 ms time frame, the hub will stop sending a ‘K’ on the upstream and downstream ports. It must follow through as a controlling hub and properly terminate the resume with either an EOP or with HS terminations as is currently implemented in the selective resume case, per the USB specification.

8.6 High Speed Indicator (HS_IND)

The HS_IND pin can be used to drive an LED. The active state of the LED will be determined as follows:

- If CFG_SEL1 = ‘0’, HS_IND is active high.
- If CFG_SEL1 = ‘1’, then HS_IND is active low.

Assertion of HS_IND indicates the device is connected at high speed. Negation of HS_IND indicates the device is connected at full speed.

Note:	This pin shares functionality with the CFG_SEL1 configuration strap. The logic state of this pin is internally latched on the rising edge of RESET_N (RESET_N negation), and is used to determine the hub configuration method. Refer to Section 6.3.2, "Configuration Select (CFG_SEL[1:0])," on page 24 for additional information.

9.0 OPERATIONAL CHARACTERISTICS

9.1 Absolute Maximum Ratings*

+3.3 V Supply Voltage (VDD33, VDDA33) (Note 9-1)..... 0 V to +3.6 V

Positive voltage on input signal pins, with respect to ground (Note 9-2).....3.6 V

Negative voltage on input signal pins, with respect to ground ..... -0.5 V

Positive voltage on XTAL1/REFCLK, with respect to ground..... VDDCR12

Positive voltage on USB DP/DM signals, with respect to ground (Note 9-3) .....5.5 V

Storage Temperature..... .-55°C to +150°C

Lead Temperature Range.....Refer to JEDEC Spec. J-STD-020

HBM ESD Performance .....JEDEC Class 3A

Note 9-1 When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested to use a clamp circuit.

Note 9-2 This rating does not apply to the following signals: All USB DM/DP pins, XTAL1/REFCLK, XTAL2.

Note 9-3 This rating applies only when VDD33 is powered.

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 9.2, "Operating Conditions**", Section 9.5, "DC Specifications", or any other applicable section of this specification is not implied. Note, device signals are NOT 5 volt tolerant unless specified otherwise.

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9.2 Operating Conditions**

+3.3 V Supply Voltage (VDD33, VDDA33)..... +3.0 V to 3.6 V

Power Supply Rise Time..... Note 9-4

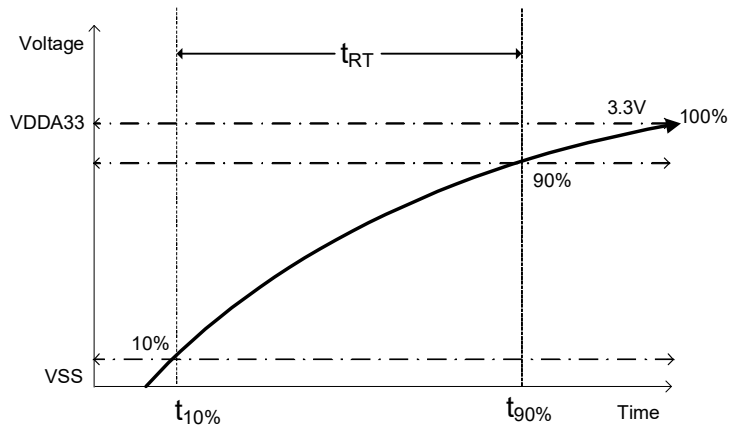
Ambient Operating Temperature in Still Air (T_A)..... Note 9-5

Note 9-4 The power supply rise time requirements vary dependent on the usage of the external reset (RESET_N). If RESET_N is asserted at power-on, the power supply rise time must be 10mS or less ($t_{RT(max)}$ = 10mS). If RESET_N is not used at power-on (tied high), the power supply rise time must be 1mS or less ($t_{RT(max)}$ = 1mS). Figure 9-1 illustrates the supply rise time requirements.

Note 9-5 0°C to +70°C for commercial version, -40°C to +85°C for industrial version.

**Proper operation of the device is ensured only within the ranges specified in this section.

FIGURE 9-1: SUPPLY RISE TIME MODEL



9.3 Power Consumption

This section details the power consumption of the device as measured during various modes of operation. Power dissipation is determined by temperature, supply voltage, and external source/sink requirements.

9.3.1 OPERATIONAL / UNCONFIGURED

TABLE 9-1: OPERATIONAL/UNCONFIGURED POWER CONSUMPTION

	Typical (mA)	Maximum (mA)
	VDD33	VDD33
HS Host / 1 HS Device	65	75
HS Host / 2 HS Devices	95	110
HS Host / 3 HS Devices	125	145
HS Host / 1 FS Device	45	50
HS Host / 2 FS Devices	50	60
HS Host / 3 FS Devices	55	70
Unconfigured	30	-

9.3.2 SUSPEND / STANDBY

TABLE 9-2: SUSPEND/STANDBY POWER CONSUMPTION

Mode	Symbol	Typical @ 25°C	Commercial MAX	Industrial MAX	Unit
Suspend	I_{VDD33}	320	1250	1750	uA
Standby	I_{VDD33}	75	130	140	uA

Note: Typical values measured with VDD33 = 3.3V. Maximum values measured with VDD33 = 3.6V.

9.4 Package Thermal Specifications

Thermal parameters are measured or estimated for devices with the ground soldered to thermal vias in a multilayer 2S2P PCB per JESD51. Thermal resistance is measured from the die to the ambient air. The values provided are based on the package body, die size, maximum power consumption, 85°C ambient temperature, and 125°C junction temperature of the die.

TABLE 9-3: PACKAGE THERMAL RESISTANCE PARAMETERS

Symbol	°C/W	Velocity (Meter/s)
Θ_{JA}	35	0
	30	1
	27	2.5
Θ_{JB}	20	-
Θ_{JC}	3.4	-
Ψ_{JT}	0.3	0
Ψ_{JB}	19	0

Use the following formulas to calculate the junction temperature:

$\mathbf{T_J = P \times \Theta_{JA} + T_A}$

$\mathbf{T_J = P \times \Psi_{JT} + T_T}$

$T_J = P \times \Theta_{JC} + T_C$

TABLE 9-4: PACKAGE THERMALS LEGEND

Symbol	Description
$\mathbf{T_J}$	Junction temperature
P	Power dissipated
$\mathbf{\Theta_{JA}}$	Junction-to-ambient-temperature
$\mathbf{\Theta_{JC}}$	Junction-to-top-of-package
$\mathbf{\Psi_{JT}}$	Junction-to-bottom-of-case
$\mathbf{T_A}$	Ambient temperature
$\mathbf{T_C}$	Temperature of the bottom of the case
$\mathbf{T_T}$	Temperature of the top of the case

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9.5 DC Specifications

TABLE 9-5: DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	MIN	TYP	MAX	Units	Notes
IS Type Input Buffer						
Low Input Level	V_{IL}	-0.3		0.8	V	
High Input Level	V_{IH}	2.0		3.6	V	
I_RST Type Input Buffer						
Low Input Level	V_{IL}	-0.3		0.4	V	
High Input Level	V_{IH}	1.25		3.6	V	
I_SMB Type Input Buffer						
Low Input Level	V_{IL}	-0.3		0.35	V	
High Input Level	V_{IH}	1.25		3.6	V	
O8 Type Buffers						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA
High Output Level	V_{OH}	VDD33 - 0.4			V	I_{OH} = -8 mA
OD8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA
OD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA
ICLK Type Buffer (XTAL1/REFCLK Input)						
Low Input Level	V_{IL}	-0.3		0.35	V	
High Input Level	V_{IH}	0.8		3.6	V	

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9.6 AC Specifications

This section details the various AC timing specifications of the device.

9.6.1 POWER-ON CONFIGURATION STRAP VALID TIMING

Figure 9-2 illustrates the configuration strap timing requirements, in relation to power-on, for applications where RESET_N is not used at power-on. The operational level (V_{opp}) for the external power supply is detailed in Section 9.2, "Operating Conditions**," on page 33.

Note: For RESET_N configuration strap timing requirements, refer to Section 9.6.2, "Reset and Configuration Strap Timing," on page 36.

FIGURE 9-2: POWER-ON CONFIGURATION STRAP VALID TIMING

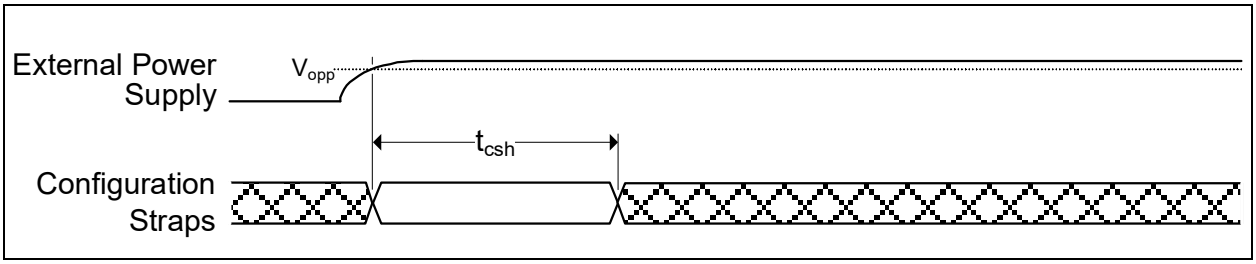

TABLE 9-6: POWER-ON CONFIGURATION STRAP VALID TIMING

Symbol	Description	MIN	TYP	MAX	Units
t_{csh}	Configuration strap hold after external power supply at operational level	1			ms

9.6.2 RESET AND CONFIGURATION STRAP TIMING

Figure 9-3 illustrates the RESET_N timing requirements and its relation to the configuration strap signals. Assertion of RESET_N is not a requirement. However, if used, it must be asserted for the minimum period specified.

Refer to Section 8.3, "Resets," on page 29 for additional information on resets. Refer to Section 6.3, "Device Configuration Straps," on page 23 for additional information on configuration straps.

FIGURE 9-3: RESET_N CONFIGURATION STRAP TIMING

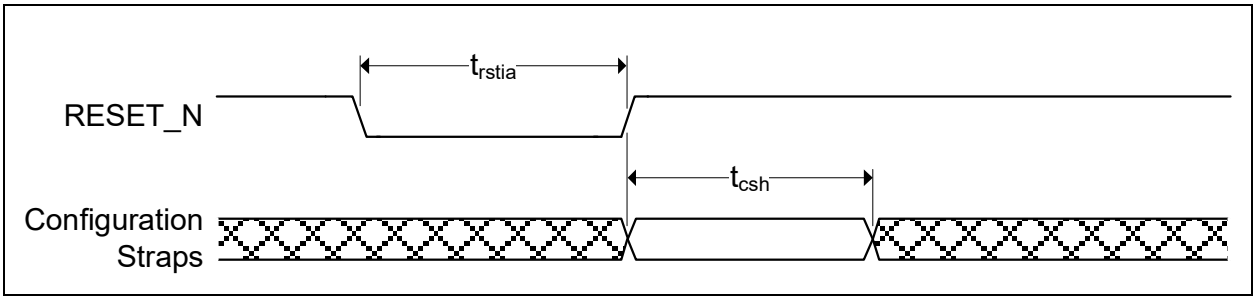

TABLE 9-7: RESET_N CONFIGURATION STRAP TIMING

Symbol	Description	MIN	TYP	MAX	Units
t_{rstia}	RESET_N input assertion time	5			us
t_{csh}	Configuration strap hold after RESET_N deassertion	1			ms

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9.6.3 USB TIMING

All device USB signals conform to the voltage, power, and timing characteristics/specifications as set forth in the *Universal Serial Bus Specification*. Please refer to the *Universal Serial Bus Specification*, Revision 2.0, available at http://www.usb.org.

9.6.4 SMBUS TIMING

All device SMBus signals conform to the voltage, power, and timing characteristics/specifications as set forth in the *System Management Bus Specification*. Please refer to the *System Management Bus Specification*, Version 1.0, available at http://smbus.org/specs.

9.6.5 I^2C TIMING

All device I^2C signals conform to the 100KHz Standard Mode (Sm) voltage, power, and timing characteristics/specifications as set forth in the *I^2C-Bus Specification*. Please refer to the *I^2C-Bus Specification*, available at http://www.nxp.com.

9.7 Clock Specifications

The device can accept either a 24 MHz crystal or a 24 MHz single-ended clock oscillator input. If the single-ended clock oscillator method is implemented, XTAL1 should be left unconnected and REFCLK should be driven with a clock that adheres to the specifications outlined in Section 9.7.2, "External Reference Clock (REFCLK)".

9.7.1 OSCILLATOR/CRYSTAL

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (XTAL1I/XTAL2). See Table 9-8 for the recommended crystal specifications.

TABLE 9-8: CRYSTAL SPECIFICATIONS

Parameter	Symbol	MIN	NOM	MAX	Units	Notes
Crystal Cut	AT, typ					
Crystal Oscillation Mode	Fundamental Mode					
Crystal Calibration Mode	Parallel Resonant Mode					
Frequency	F_{fund}	-	24.000	-	MHz	
Total Allowable PPM Budget		-	-	+/-350	PPM	
Operating Temperature Range		Note 9-1	-	Note 9-2	^oC	

Note 9-1 0^oC for commercial version, -40^oC for industrial version.

Note 9-2 $+70^oC$ for commercial version, $+85^oC$ for industrial version.

9.7.2 EXTERNAL REFERENCE CLOCK (REFCLK)

The following input clock specifications are suggested:

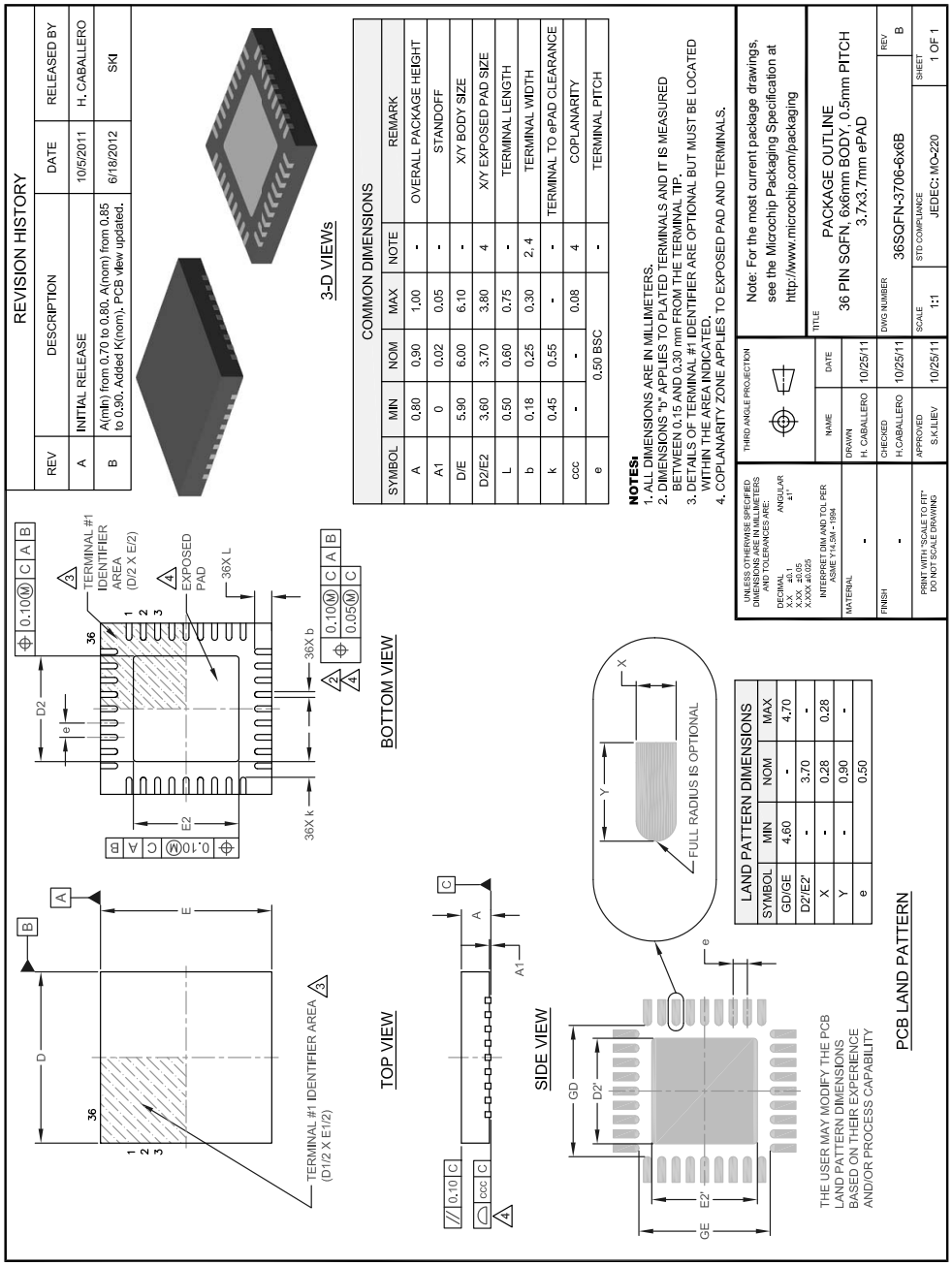
- 24 MHz ± 350 PPM

Note: The external clock is recommended to conform to the signalling levels designated in the JEDEC specification on 1.2V CMOS Logic. XTAL2 should be treated as a no connect when an external clock is supplied.

10.0 PACKAGE OUTLINE

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

FIGURE 10-1: 36-SQFN PACKAGE DRAWING



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APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
DS00001702C (9-08-19)	Section 9.4, "Package Thermal Specifications"	Added table number title to: Table 9-3, "Package Thermal Resistance Parameters"
DS00001702B (7-26-19)	Product Identification System	Added “Direction of Unreeling”, pin 1 drawing.
	Section 9.4, "Package Thermal Specifications"	Updated Table 9-3, "Package Thermal Resistance Parameters"
USB2533 Revision A replaces the previous SMSC version, revision 1.1		
Rev. 1.1 (12-06-13)	SMBus Runtime Registers	Register definitions removed. These definitions are provided in application note *AN 26.18 “SMBus Slave Interface for the USB253x/USB3x13/USB46x4”*.
Rev. 1.1 (09-24-13)	Table 9-5, “DC Electrical Characteristics,” on page 35	Updated ICLK V_{IH} max from “VDDCR12” to “3.6”
	Section 9.7.2, "External Reference Clock (REFCLK)," on page 37	Removed 50% duty cycle requirement.
	Table 6-1, “Hub Configuration Selection,” on page 21	Corrected SDA and CFG_SEL1 values for last two entries in the table.
Rev. 1.0 (06-17-13)	Initial Release	

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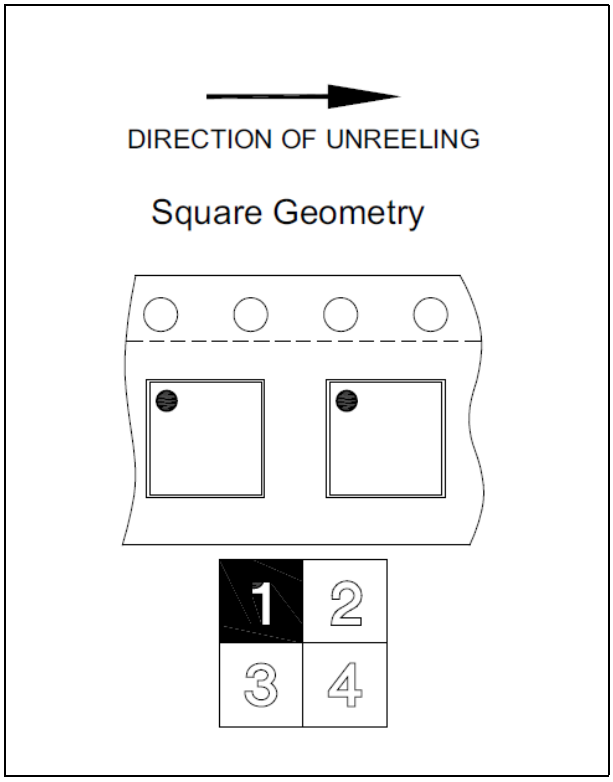
PART NO.	[X]	-	XXX	-	[X](1)
Device	Temperature Range		Package		Tape and Reel Option

Device:	USB2533, USB2533i		
Temperature Range:	Blank	=	0°C to +70°C Commercial
	i	=	-40°C to+85°C Industrial
Package:	1080AEN	=	36-pin SQFN
Tape and Reel Option:	Blank	=	Standard packaging (tray)
	TR	=	Tape and Reel(1)

Examples:

a) USB2533-1080AEN, Commercial Temp 36-pin SQFN Pkg., Tray
b) USB2533-1080AEN-TR, Commercial Temp 36-pin SQFN Pkg., Tape & Reel
c) USB2533i-1080AEN, Industrial Temp 36-pin SQFN Pkg., Tray
d) USB2533i-1080AEN-TR, Industrial Temp 36-pin SQFN Pkg., Tape & Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option. Reel size is 4,000.



PREVIOUS VERSION ORDERING INFORMATION:

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
USB2533-1080AEN	0°C to +70°C	36-pin SQFN
USB2533-1080AEN-TR	0°C to +70°C	36-pin SQFN (Tape & Reel)
USB2533i-1080AEN	-40°C to +85°C	36-pin SQFN
USB2533-1080AEN-TR	-40°C to +85°C	36-pin SQFN (Tape & Reel)

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