# KK74HC161A

# Presettable Counters

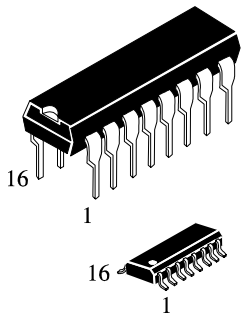
## High-Performance Silicon-Gate CMOS

The KK74HC161A is identical in pinout to the LS/ALS161. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

The KK74HC161A is programmable 4-bit synchronous counter that feature parallel Load, asynchronous Reset, a Carry Output for cascading and count-enable controls.

The KK74HC161A is binary counter with asynchronous Reset.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices




N SUFFIX
PLASTIC

D SUFFIX
SOIC

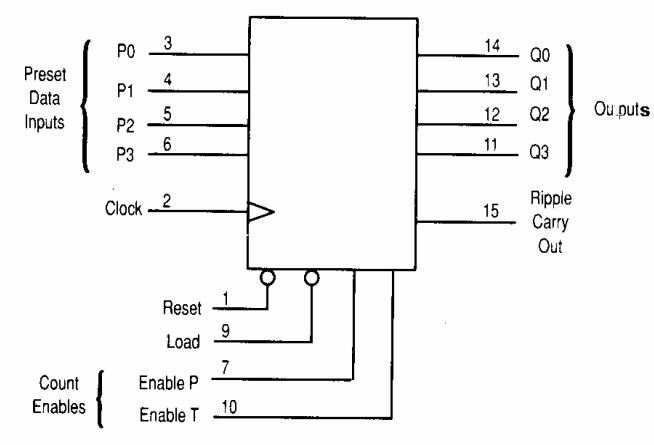
**ORDERING INFORMATION**

**KK**74HC161AN Plastic

KK74HC161AD SOIC

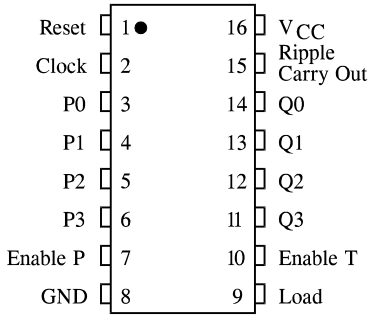
$T_A$ = -55° to 125° C for all packages

## LOGIC DIAGRAM




PIN 16 =$V_{CC}$
PIN 8 = GND

## PIN ASSIGNMENT




## FUNCTION TABLE

| Inputs | | | | | Outputs | | | | Function |
|---|---|---|---|---|---|---|---|---|---|
| Reset | Load | Enable P | Enable T | Clock | Q0 | Q1 | Q2 | Q3 | |
| L | X | X | X | X | L | L | L | L | Reset to “0” |
| H | L | X | X | ⎍ | P0 | P1 | P2 | P3 | Preset Data |
| H | H | X | L | ⎍ | No change | | | | No count |
| H | H | L | X | ⎍ | No change | | | | No count |
| H | H | H | H | ⎍ | Count up | | | | Count |
| H | X | X | X | ⎎ | No change | | | | No count |

X=don’t care

P0,P1,P2,P3 = logic level of Data inputs

Ripple Carry Out = Enable T • Q0 • Q1 • Q2 • Q3

## MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| $V_{IN}$ | DC Input Voltage (Referenced to GND) | -1.5 to $V_{CC}$ +1.5 | V |
| $V_{OUT}$ | DC Output Voltage (Referenced to GND) | -0.5 to $V_{CC}$ +0.5 | V |
| $I_{IN}$ | DC Input Current, per Pin | ±20 | mA |
| $I_{OUT}$ | DC Output Current, per Pin | ±25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ±50 | mA |
| $P_D$ | Power Dissipation in Still Air, Plastic DIP+<br>SOIC Package+ | 750<br>500 | mW |
| Tstg | Storage Temperature | -65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP or SOIC Package) | 260 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | | 2.0 | 6.0 | V |
| $V_{IN}$, $V_{OUT}$ | DC Input Voltage, Output Voltage (Referenced to GND) | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | | -55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time (Figure 1) | $V_{CC}$ =2.0 V<br>$V_{CC}$ =4.5 V<br>$V_{CC}$ =6.0 V | 0<br>0<br>0 | 1000<br>500<br>400 | ns |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, $V_{IN}$ and $V_{OUT}$ should be constrained to the range GND≤($V_{IN}$ or $V_{OUT}$)≤$V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | 25 °C to -55°C | ≤85 °C | ≤125 °C | |
| $V_{IH}$ | Minimum High-Level Input Voltage | $V_{OUT}$=0.1 V or $V_{CC}$-0.1 V<br>$\|I_{OUT}\| \leq 20$ μA | 2.0<br>4.5<br>6.0 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | V |
| $V_{IL}$ | Maximum Low - Level Input Voltage | $V_{OUT}$=0.1 V or $V_{CC}$-0.1 V<br>$\|I_{OUT}\| \leq 20$ μA | 2.0<br>4.5<br>6.0 | 0.5<br>1.35<br>1.8 | 0.5<br>1.35<br>1.8 | 0.5<br>1.35<br>1.8 | V |
| $V_{OH}$ | Minimum High-Level Output Voltage | $V_{IN}$=$V_{IH}$ or $V_{IL}$<br>$\|I_{OUT}\| \leq 20$ μA | 2.0<br>4.5<br>6.0 | 1.9<br>4.4<br>5.9 | 1.9<br>4.4<br>5.9 | 1.9<br>4.4<br>5.9 | V |
| | | $V_{IN}$=$V_{IH}$ or $V_{IL}$<br>$\|I_{OUT}\| \leq 6.0$ mA<br>$\|I_{OUT}\| \leq 7.8$ mA | <br>4.5<br>6.0 | <br>3.98<br>5.48 | <br>3.84<br>5.34 | <br>3.7<br>5.2 | |
| $V_{OL}$ | Maximum Low-Level Output Voltage | $V_{IN}$=$V_{IH}$ or $V_{IL}$<br>$\|I_{OUT}\| \leq 20$ μA | 2.0<br>4.5<br>6.0 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | V |
| | | $V_{IN}$=$V_{IH}$ or $V_{IL}$<br>$\|I_{OUT}\| \leq 6.0$ mA<br>$\|I_{OUT}\| \leq 7.8$ mA | <br>4.5<br>6.0 | <br>0.26<br>0.26 | <br>0.33<br>0.33 | <br>0.4<br>0.4 | |
| $I_{IN}$ | Maximum Input Leakage Current | $V_{IN}$=$V_{CC}$ or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{IN}$=$V_{CC}$ or GND<br>$I_{OUT}$=0μA | 6.0 | 4.0 | 40 | 160 | μA |

## AC ELECTRICAL CHARACTERISTICS ($C_L$=50pF,Input $t_r$=$t_f$=6.0 ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | 25 °C to -55°C | ≤85°C | ≤125°C | |
| $f_{max}$ | Maximum Clock Frequency (Figures 1,6) | 2.0<br>4.5<br>6.0 | 6<br>30<br>35 | 5<br>24<br>28 | 4<br>20<br>24 | MHz |
| $t_{PLH}$ | Maximum Propagation Delay Clock to Q (Figures 1,6) | 2.0<br>4.5<br>6.0 | 120<br>20<br>16 | 160<br>23<br>20 | 200<br>28<br>22 | ns |
| $t_{PHL}$ | | 2.0<br>4.5<br>6.0 | 145<br>22<br>18 | 185<br>25<br>20 | 320<br>30<br>23 | ns |
| $t_{PHL}$ | Maximum Propagation Delay Reset to Q (Figures 2 and 6) | 2.0<br>4.5<br>6.0 | 145<br>20<br>17 | 185<br>22<br>19 | 220<br>25<br>21 | ns |
| $t_{PLH}$ | Maximum Propagation Delay Enable T to Ripple Carry Out (Figures 3,6) | 2.0<br>4.5<br>6.0 | 110<br>16<br>14 | 150<br>18<br>15 | 190<br>20<br>17 | ns |
| $t_{PHL}$ | | 2.0<br>4.5<br>6.0 | 135<br>18<br>15 | 175<br>20<br>16 | 210<br>22<br>20 | ns |
| $t_{PLH}$ | Maximum Propagation Delay Clock to Ripple Carry Out (Figures 1,6) | 2.0<br>4.5<br>6.0 | 120<br>22<br>18 | 160<br>27<br>22 | 200<br>30<br>25 | ns |
| $t_{PHL}$ | | 2.0<br>4.5<br>6.0 | 145<br>22<br>20 | 185<br>28<br>24 | 220<br>35<br>28 | ns |
| $t_{PHL}$ | Maximum Propagation Delay Reset to Ripple Carry Out (Figures 2,6) | 2.0<br>4.5<br>6.0 | 155<br>22<br>18 | 190<br>26<br>22 | 230<br>30<br>25 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, Any Output (Figures 1 and 6) | 2.0<br>4.5<br>6.0 | 75<br>15<br>13 | 95<br>19<br>16 | 110<br>22<br>19 | ns |
| $C_{IN}$ | Maximum Input Capacitance | - | 10 | 10 | 10 | pF |

| | | | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Gate)<br>Used to determine the no-load dynamic power consumption:<br>$P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$ | Typical @25°C,$V_{CC}$=5.0 V<br>30 | pF |

**TIMING REQUIREMENTS** ($C_L$=50pF,Input $t_r$=$t_f$=6.0 ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | 25 °C to -55°C | ≤85°C | ≤125°C | |
| $t_{SU}$ | Minimum Setup Time, Preset Data Inputs to Clock (Figure 4) | 2.0<br>4.5<br>6.0 | 40<br>15<br>12 | 60<br>20<br>18 | 80<br>30<br>20 | ns |
| $t_{SU}$ | Minimum Setup Time, Load to Clock (Figure 4) | 2.0<br>4.5<br>6.0 | 60<br>15<br>12 | 75<br>20<br>18 | 90<br>30<br>20 | ns |
| $t_{SU}$ | Minimum Setup Time, Enable T or Enable P to Clock (Figure 5) | 2.0<br>4.5<br>6.0 | 80<br>20<br>17 | 95<br>25<br>23 | 110<br>35<br>25 | ns |
| $t_h$ | Minimum Hold Time, Clock to Load or Preset Data Inputs (Figure 4) | 2.0<br>4.5<br>6.0 | 3<br>3<br>3 | 3<br>3<br>3 | 3<br>3<br>3 | ns |
| $t_h$ | Minimum Hold Time, Clock to Enable T or Enable P (Figure 5) | 2.0<br>4.5<br>6.0 | 3<br>3<br>3 | 3<br>3<br>3 | 3<br>3<br>3 | ns |
| $t_{rec}$ | Minimum Recovery Time, Reset Inactive to Clock (Figure 2) | 2.0<br>4.5<br>6.0 | 80<br>15<br>12 | 95<br>20<br>17 | 110<br>26<br>23 | ns |
| $t_{rec}$ | Minimum Recovery Time, Load Inactive to Clock (Figure 4) | 2.0<br>4.5<br>6.0 | 80<br>15<br>12 | 95<br>20<br>17 | 110<br>26<br>23 | ns |
| $t_w$ | Minimum Pulse Width, Clock (Figure 1) | 2.0<br>4.5<br>6.0 | 60<br>12<br>10 | 75<br>15<br>13 | 90<br>18<br>15 | ns |
| $t_w$ | Minimum Pulse Width, Reset (Figure 2) | 2.0<br>4.5<br>6.0 | 60<br>12<br>10 | 75<br>15<br>13 | 90<br>18<br>15 | ns |
| $t_r$, $t_f$ | Maximum Input Rise and Fall Times (Figure 1) | 2.0<br>4.5<br>6.0 | 1000<br>500<br>400 | 1000<br>500<br>400 | 1000<br>500<br>400 | ns |

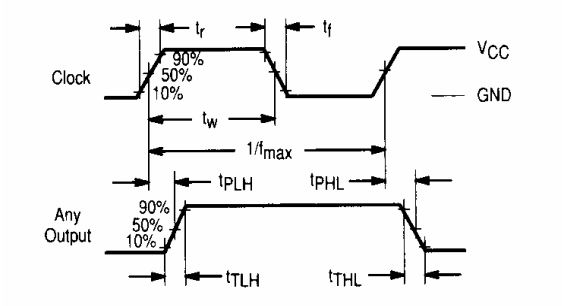



**Figure 1. Switching Waveforms**

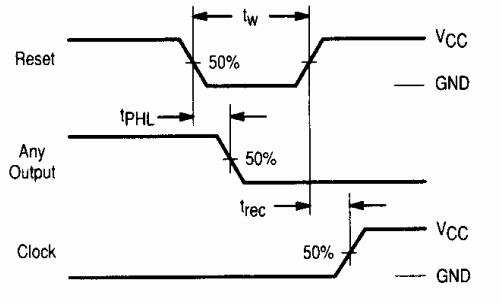



**Figure 2. Switching Waveforms**

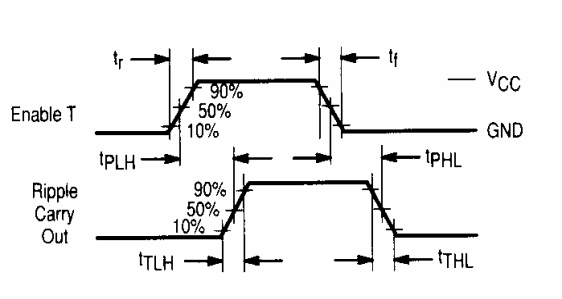



**Figure 3. Switching Waveforms**

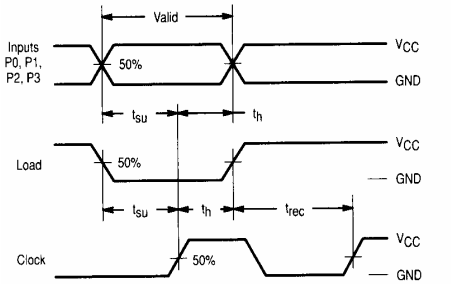



**Figure 4. Switching Waveforms**

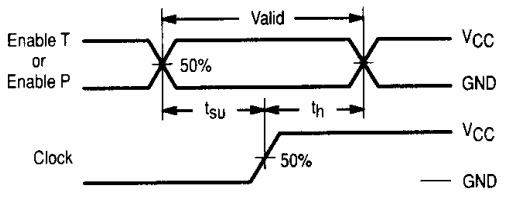



**Figure 5. Switching Waveforms**

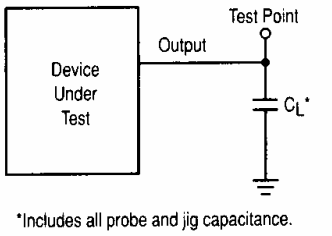
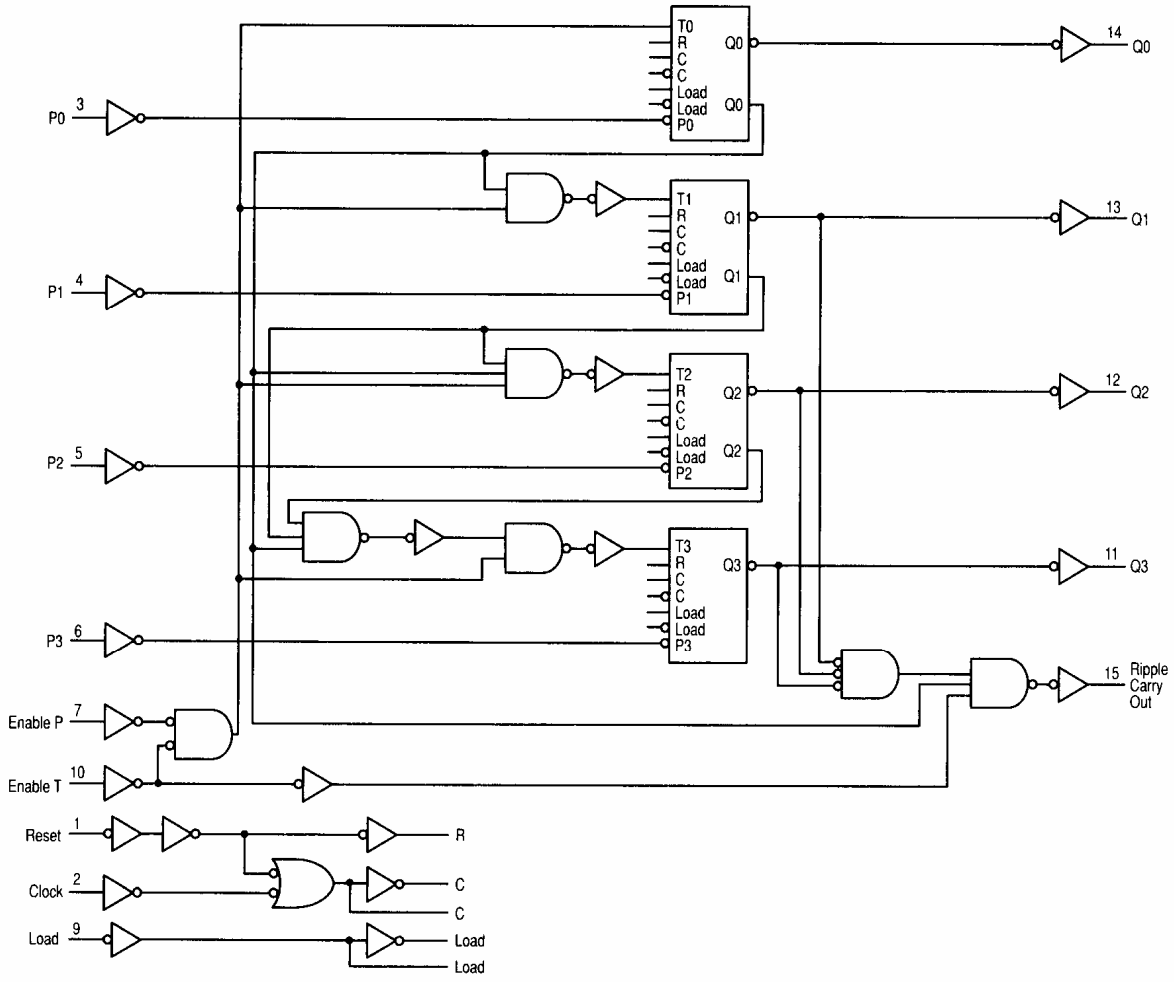



**Figure 6. Test Circuit**

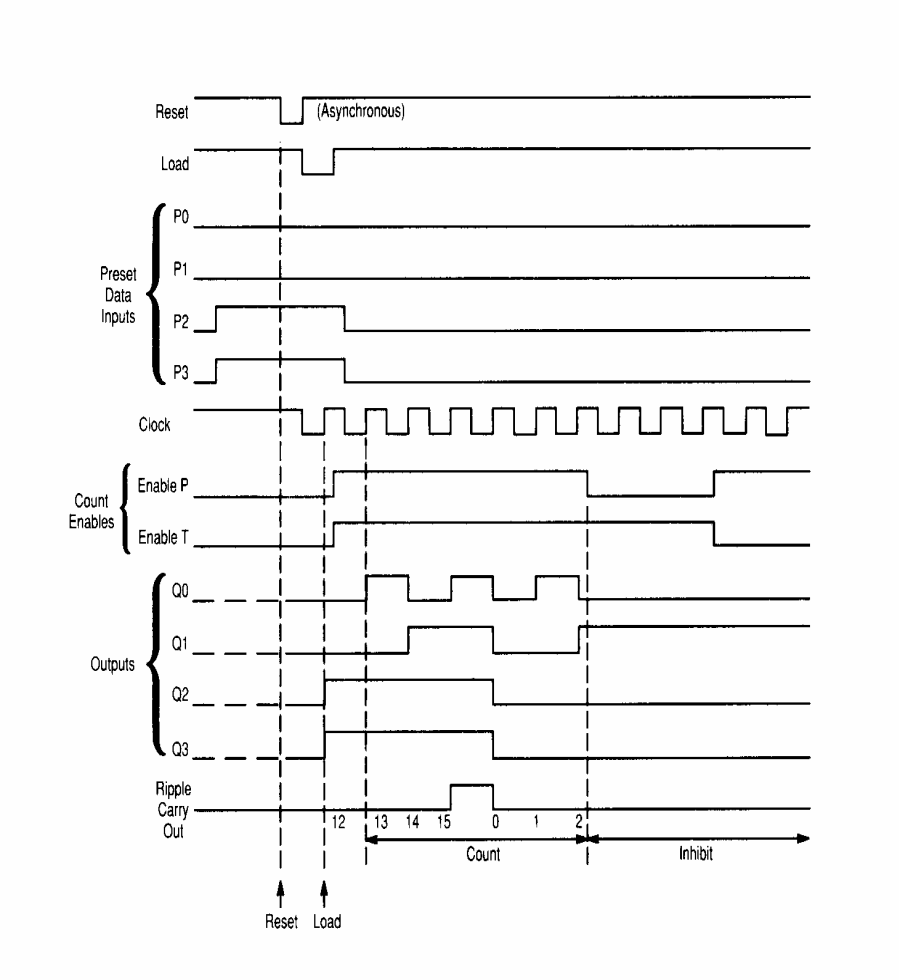



$V_{CC}$=Pin 16
GND=Pin 8

The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

**Figure 7.Expanded logic diagram**

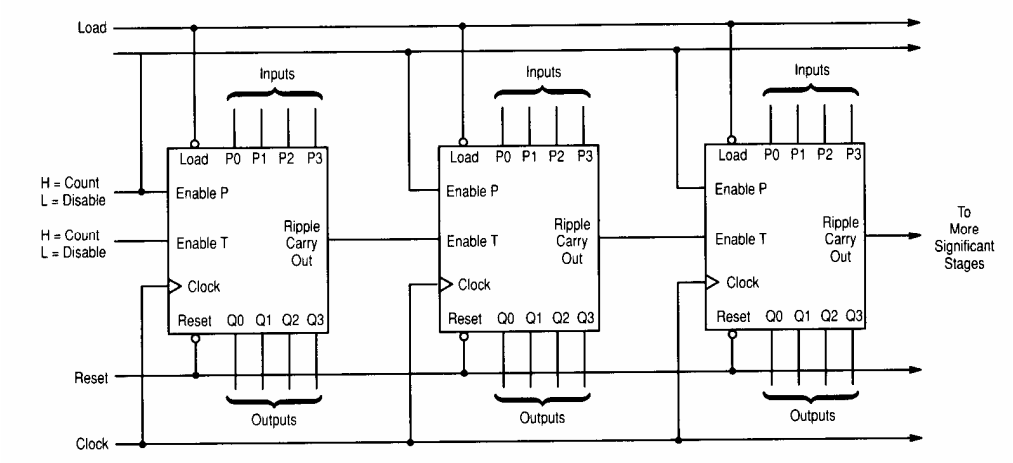



Sequence illustrated in waveforms:

1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.

**Figure 8. Timing Diagram**

## TYPICAL APPLICATIONS CASCADING




Note:When used in these cascaded configurations the clock $f_{max}$ guaranteed limits may not apply. Actual performance will depend on number of stages. This limitation is due to set up times between Enable (Port) and clock.

**Figure 9. N-Bit Synchronous Counters**

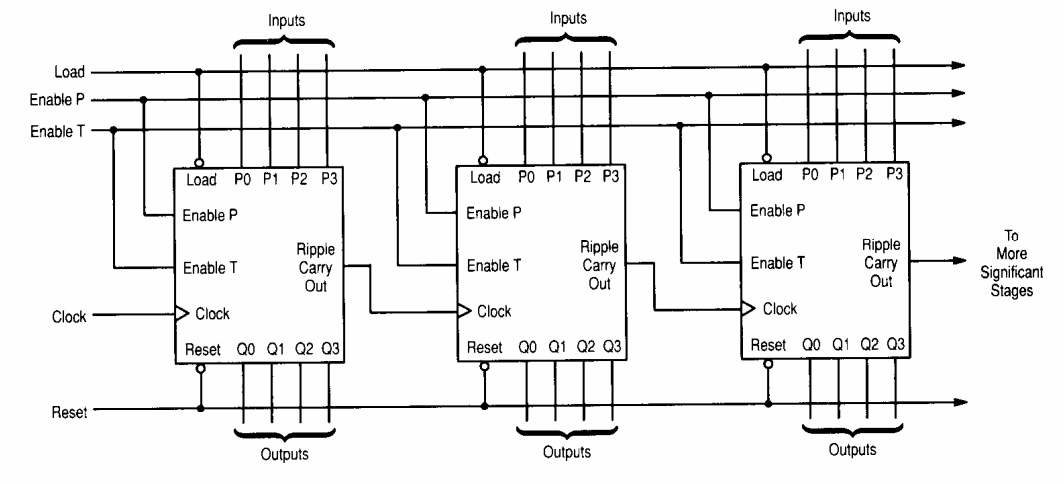
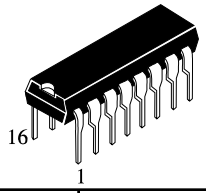
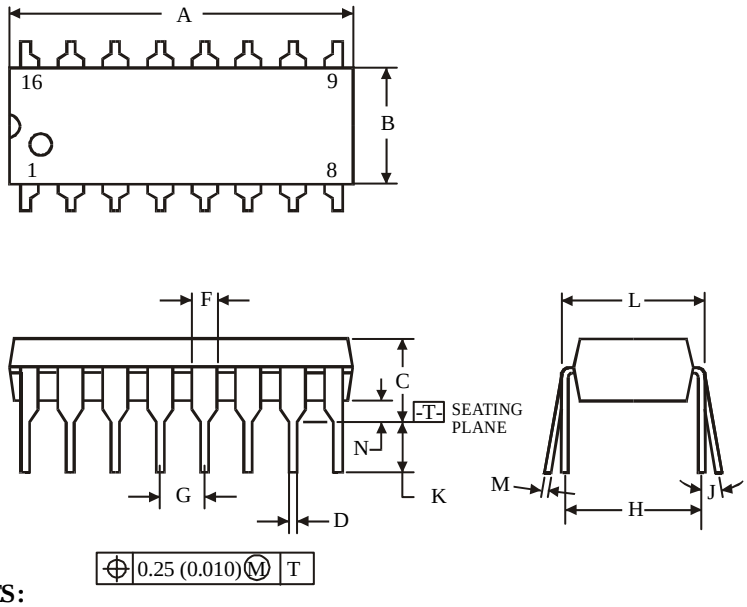



**Figure 10. Nibble Ripple Counter**

## N SUFFIX PLASTIC DIP
## (MS - 001BB)



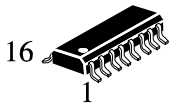



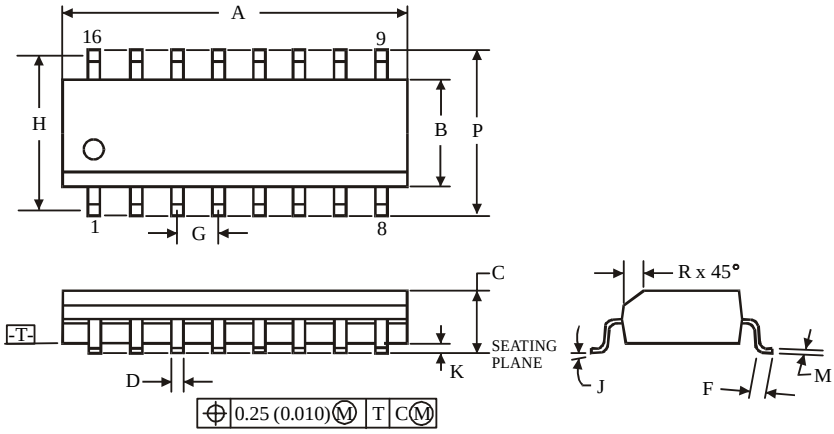

| | Dimension, mm | |
|---|---|---|
| **Symbol** | **MIN** | **MAX** |
| **A** | 18.67 | 19.69 |
| **B** | 6.1 | 7.11 |
| **C** | | 5.33 |
| **D** | 0.36 | 0.56 |
| **F** | 1.14 | 1.78 |
| **G** | 2.54 | |
| **H** | 7.62 | |
| **J** | 0° | 10° |
| **K** | 2.92 | 3.81 |
| **L** | 7.62 | 8.26 |
| **M** | 0.2 | 0.36 |
| **N** | 0.38 | |

**NOTES:**

1. Dimensions “A”, “B” do not include mold flash or protrusions.
   Maximum mold flash or protrusions 0.25 mm (0.010) per side.

## D SUFFIX SOIC
## (MS - 012AC)




| | Dimension, mm | |
|---|---|---|
| **Symbol** | **MIN** | **MAX** |
| **A** | 9.8 | 10 |
| **B** | 3.8 | 4 |
| **C** | 1.35 | 1.75 |
| **D** | 0.33 | 0.51 |
| **F** | 0.4 | 1.27 |
| **G** | 1.27 | |
| **H** | 5.72 | |
| **J** | 0° | 8° |
| **K** | 0.1 | 0.25 |
| **M** | 0.19 | 0.25 |
| **P** | 5.8 | 6.2 |
| **R** | 0.25 | 0.5 |

**NOTES:**

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side
   for A; for B – 0.25 mm (0.010) per side.