

MOS Field Effect Transistor

KPA1792

■ Features

● Low on-state resistance

N-channel $R_{DS(on)1} = 26 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 3.4 \text{ A)}$

$R_{DS(on)2} = 36 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 3.4 \text{ A)}$

$R_{DS(on)3} = 42 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_D = 3.4 \text{ A)}$

● P-channel $R_{DS(on)1} = 36 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -2.9 \text{ A)}$

$R_{DS(on)2} = 54 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.5 \text{ V, } I_D = -2.9 \text{ A)}$

$R_{DS(on)3} = 65 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.0 \text{ V, } I_D = -2.9 \text{ A)}$

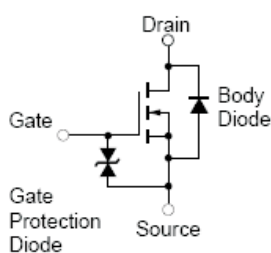
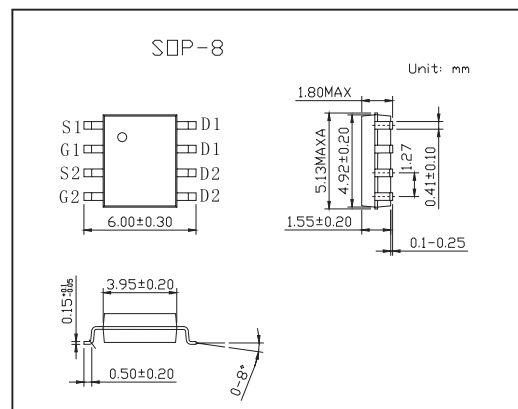
● Low input capacitance

N-channel $C_{iss} = 760 \text{ pF TYP.}$

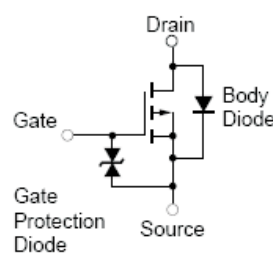
P-channel $C_{iss} = 900 \text{ pF TYP.}$

● Built-in gate protection diode

● Small and surface mount package



N-Channel



P-Channel

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	N-Channel	P- Channel	Unit
Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DS}	30	-30	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GS}	± 20	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 6.8	± 5.8	A
Drain Current (pulse) *1	$I_{D(pulse)}$	± 27.2	± 23.2	A
Total Power Dissipation (1 unit) *2	P_T	1.7		W
Total Power Dissipation (2 units) *2	P_T	2		W
Channel Temperature	T_{ch}	150		$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150		$^\circ\text{C}$

*1 $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

*2 Mounted on ceramic substrate of $2000 \text{ mm}^2 \times 1.6 \text{ mm}$

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■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditions		Min	Typ	Max	Unit
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	N-Ch			10	μ A
		V _{DS} = -30V, V _{GS} = 0 V	P- Ch			-1	
Gate Leakage Current	I _{GSS}	V _{GS} = ±16 V, V _{DS} = 0 V	N-Ch			±10	μ A
		V _{GS} = ±16 V, V _{DS} = 0 V	P- Ch			±10	
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	N-Ch	1.5	2.1	2.5	V
		V _{DS} = -10 V, I _D = -1 mA	P- Ch	-1.5	-2.0	-2.5	
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 3.4 A	N-Ch	3.0	7.5		S
		V _{DS} = -10 V, I _D = -2.9A	P- Ch	3.5	8.0		
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 3.4 A	N-Ch		20.5	26	m Ω
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 3.4 A			27	36	m Ω
	R _{DS(on)3}	V _{GS} = 4.0 V, I _D = 3.4A			31	42	m Ω
	R _{DS(on)1}	V _{GS} = -10 V, I _D = -2.9 A	P- Ch		30	36	m Ω
	R _{DS(on)2}	V _{GS} = -4.5 V, I _D = -2.9 A			43	54	m Ω
	R _{DS(on)3}	V _{GS} = -4.0 V, I _D = -2.9 A			49	65	m Ω
Input Capacitance	C _{iss}	N-Channel V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	N-Ch		760		pF
			P- Ch		900		
Output Capacitance	C _{oss}	P- Channel V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	N-Ch		250		pF
			P- Ch		300		
Reverse Transfer Capacitance	C _{rss}		N-Ch		95		pF
			P- Ch		120		
Turn-on Delay Time	t _{d(on)}	N-Channel V _{DD} = 15 V, I _D = 3.4 A, V _{GS} = 10 V	N-Ch		20		ns
			P- Ch		23		
Rise Time	t _r	R _G = 10 Ω	N-Ch		140		ns
			P- Ch		220		
Turn-off Delay Time	t _{d(off)}	P- Channel V _{DD} = -15 V, I _D = -2.9 A, V _{GS} = -10 V	N-Ch		50		ns
			P- Ch		90		
Fall Time	t _f	R _G = 10 Ω	N-Ch		30		ns
			P- Ch		70		
Total Gate Charge	Q _G	N-Channel I _D = 6.8 A, V _{DD} = 24 V, V _{GS} = 10 V	N-Ch		14		nC
			P- Ch		17		
Gate to Source Charge	Q _{GS}	P- Channel	N-Ch		2		nC
			P- Ch		2.5		
Gate to Drain Charge	Q _{GD}	I _D = -5.8 A, V _{DD} = -24 V, V _{GS} = -10 V	N-Ch		5		nC
			P- Ch		4.0		
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 6.8 A, V _{GS} = 0 V	N-Ch		0.86		V
		I _F = 5.8 A, V _{GS} = 0 V	P- Ch		0.85		
Reverse Recovery Time	t _{rr}	N-Channel I _F = 6.8A, V _{GS} = 0 V, di/dt = 100 A/ μ s	N-Ch		30		ns
			P- Ch		40		
Reverse Recovery Charge	Q _{rr}	P-Channel I _F = 5.8A, V _{GS} = 0 V, di/dt = 100 A/ μ s	N-Ch		20		nC
			P- Ch		30		