NCV4299C

150 mA Low-Dropout Voltage Regulator

The NCV4299C is a family of precision micropower voltage regulators with an output current capability of 150 mA. It is available in 5.0 V or 3.3 V output voltage.

The output voltage is accurate within ±2% with a maximum dropout voltage of 0.5 V at 100 mA. Low Quiescent current is a feature drawing only 80 μA with a 100 μA load. This part is ideal for any and all battery operated microprocessor equipment.

The device features microprocessor interfaces including an adjustable reset output and adjustable system monitor to provide shutdown early warning. An inhibit function is available. With inhibit active, the regulator turns off and the device consumes less than 1.0 μA of quiescent current.

The part can withstand load dump transients making it suitable for use in automotive environments.

Features

- 5.0 V, 3.3 V ±2%, 150 mA
- Extremely Low Current Consumption
  - 80 μA (Typ) in the ON Mode
  - < 1.0 μA in the Off Mode
- Early Warning
- Reset Output Low Down to V_Q = 1.0 V
- Adjustable Reset Threshold
- Wide Temperature Range
- Fault Protection
  - 60 V Peak Transient Voltage
  - −40 V Reverse Voltage
  - Short Circuit
  - Thermal Overload
- Internally Fused Leads on SO−14 Package
- Inhibit Function with 1 μA Current Consumption in the Off Mode
- AEC−Q100 Grade 1 Qualified and PPAP Capable
- These are Pb−Free Devices

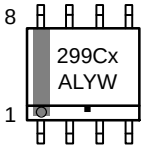
ON Semiconductor®

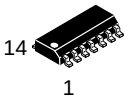
www.onsemi.com

MARKING DIAGRAMS

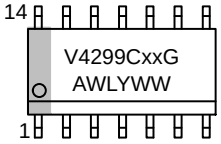


SO−8
D1 SUFFIX
CASE 751





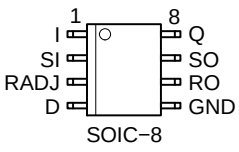
SO−14
D2 SUFFIX
CASE 751A



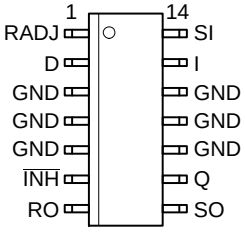
x, xx	= 3 or 33 (3.3 V Version)
	= 5 or 50 (5.0 V Version)
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



SOIC−8



SOIC−14

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

© Semiconductor Components Industries, LLC, 2014

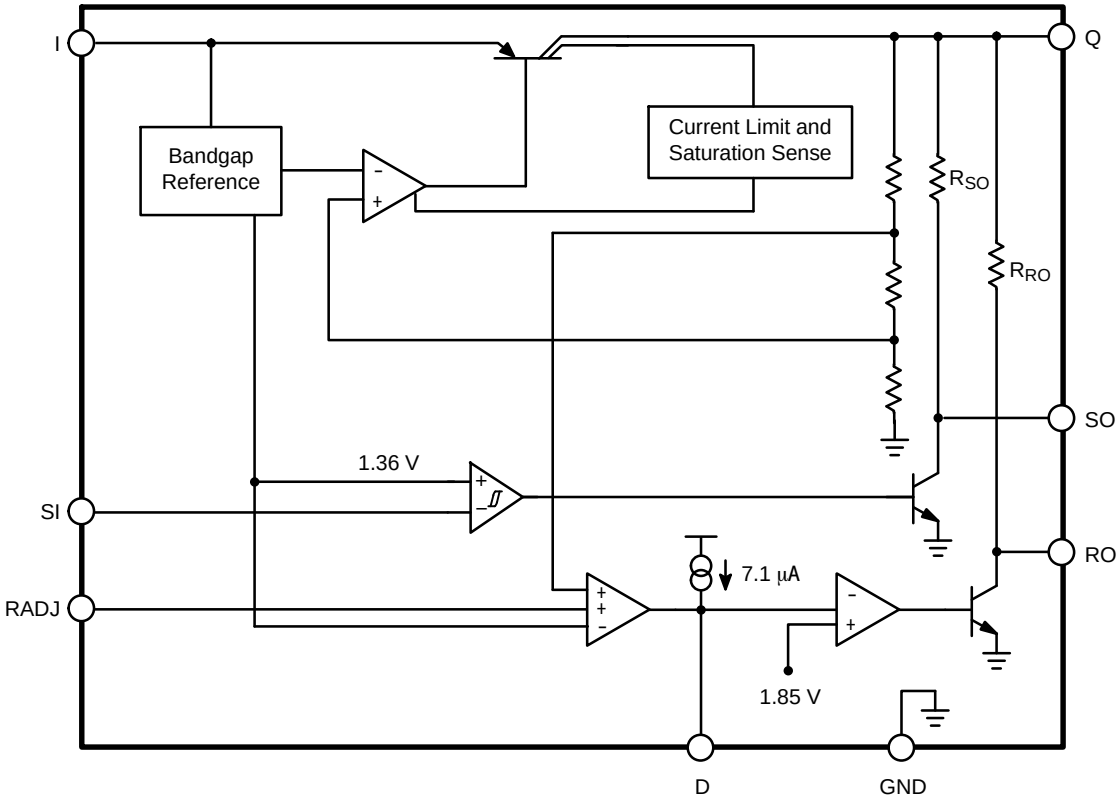


Figure 1. SO−8 Simplified Block Diagram

PIN FUNCTION DESCRIPTION − SO−8 PACKAGE

Pin	Symbol	Description
1	I	Input. Battery Supply Input Voltage. Bypass directly to GND with ceramic capacitor.
2	SI	Sense Input. Can provide an early warning signal of an impending reset condition when used with SO. Connect to Q if not used.
3	RADJ	Reset Adjust. Use resistor divider to Q to adjust reset threshold lower. Connect to GND if not used.
4	D	Reset Delay. Connect external capacitor to ground to set delay time.
5	GND	Ground.
6	RO	Reset Output. NPN collector output with internal 20 kΩ pullup to Q. Notifies user of out of regulation condition. Leave open if not used.
7	SO	Sense Output. NPN collector output with internal 20 kΩ pullup to Q. Can be used to provide early warning of an impending reset condition. Leave open if not used.
8	Q	5.0 V, 3.3 V, ±2%, 150 mA output. Use 22 μF, ESR $<$ 4 Ω to ground.

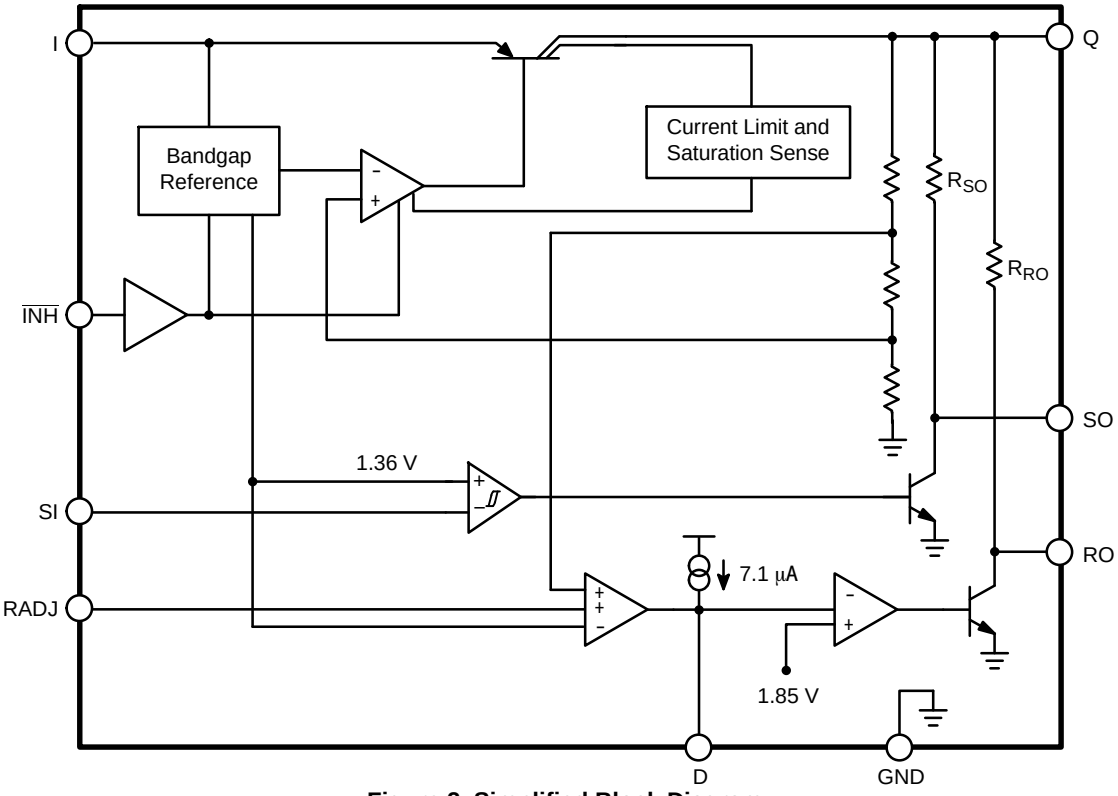


Figure 2. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. SOIC−14	Symbol	Description
1	RADJ	Reset Adjust. Use resistor divider to Q to adjust reset threshold lower. Connect to GND if not used.
2	D	Reset Delay. Connect external capacitor to ground to set delay time.
3	GND	Ground
4	GND	Ground
5	GND	Ground
6	$\overline{\text{INH}}$	Inhibit. Connect to I if not needed. A high turns the regulator on. Use a low pass filter if transients with slew rate in excess of 10 V/μs may be present on this pin during operation. See Figure 34 for details.
7	RO	Reset Output. NPN collector output with internal 20 kΩ pullup to Q. Notifies user of out of regulation condition.
8	SO	Sense Output. NPN collector output with internal 20 kΩ pullup to Q. Can be used to provide early warning of an impending reset condition.
9	Q	5.0 V, 3.3 V, ±2%, 150 mA output. Use 22 μF, ESR < 4 Ω to ground.
10	GND	Ground
11	GND	Ground
12	GND	Ground
13	I	Input. Battery Supply Input Voltage.
14	SI	Sense Input. Can provide an early warning signal of an impending reset condition when used with SO.

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input Voltage to Regulator (DC)	V_I	−40	45	V
Input Peak Transient Voltage to Regulator wrt GND (Note 1)	–	–	60	V
Inhibit ($\overline{INH}$)	$V_{\overline{INH}}$	−40	45	V
Sense Input (SI)	V_{SI}	−40	45	V
Sense Input (SI)	I_{SI}	−1.0	1.0	mA
Reset Threshold (RADJ)	V_{RADJ}	−0.3	7.0	V
Reset Threshold (RADJ)	I_{RADJ}	−10	10	mA
Reset Delay (D)	V_D	−0.3	7.0	V
Reset Output (RO)	V_{RO}	−0.3	7.0	V
Reset Output (RO)	I_{RO}	−20	20	mA
Sense Output (SO)	V_{SO}	−0.3	7.0	V
Output (Q)	V_Q	−0.3	16	V
Output (Q)	I_Q	−5.0	–	mA
ESD Capability, Human Body Model (Note 3)	ESD_{HB}	2.0	–	kV
ESD Capability, Machine Model (Note 3)	ESD_{MM}	200	–	V
ESD Capability, Charged Device Model (Note 3)	ESD_{CDM}	1.0	–	kV
Junction Temperature	T_J	–	150	°C
Storage Temperature	T_{stg}	−50	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING RANGE

Input Voltage	5.0 V Version 3.3 V Version	V_I	5.5 4.4	45 45	V
Junction Temperature		T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

LEAD TEMPERATURE SOLDERING REFLOW (Note 2)

Reflow (SMD styles only), lead free 60 s−150 sec above 217, 40 sec max at peak		T_{SLD}	–	265 Pk	°C
Moisture Sensitivity Level	SO−8 SO−14	MSL	Level 1 Level 1		

1. Load Dump Test B (with centralized load dump suppression) according to ISO16750−2 standard. Guaranteed by design. Not tested in production. Passed Class C according to ISO16750−1
2. Per IPC / JEDEC J−STD−020C.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD HBM tested per AEC−Q100−002 (JS−001−2010)
   ESD MM tested per AEC−Q100−003 (EIA/JESD22−A115)
   ESD CDM tested per AEC−Q100−011 (EIA/JESD22−C101).

THERMAL CHARACTERISTICS

Characteristic		Test Conditions (Typical Value) Note 4	Note 5	Note 6	Unit
Thermal Characteristics, SO−8	Junction−to−Lead (ψ_{JLx}, θ_{JLx}) Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	72 198	58 150.7	58.3 124.5	°C/W
Thermal Characteristics, SO−14	Junction−to−Lead (ψ_{JLx}, θ_{JLx}) Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	15.1 142.7	19.9 101.2	19.3 86.1	°C/W
Thermal Characteristics, TSSOP−14 EP	Junction−to−Tab (ψ_{JLx}, θ_{JLx}) Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	9.7 111.6	11.4 78.7	11.7 53.7	°C/W

4. 2 oz Copper, 50 mm sq Copper area, 1.5 mm thick FR4.
5. 2 oz Copper, 150 mm sq Copper area, 1.5 mm thick FR4.
6. 2 oz Copper, 500 mm sq Copper area, 1.5 mm thick FR4.

ELECTRICAL CHARACTERISTICS (−40°C < T_J < 150°C; V_I = 13.5 V unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
OUTPUT Q						
Output Voltage (5.0 V Version)	V_Q	1.0 mA < I_Q < 150 mA, 6.0 V < V_I < 16 V	4.9	5.0	5.1	V
Output Voltage (3.3 V Version)	V_Q	1.0 mA < I_Q < 150 mA, 5.5 V < V_I < 16 V	3.23	3.3	3.37	V
Current Limit	I_Q	V_Q = 90% of V_{Qnom}	250	430	500	mA
Quiescent Current ($I_q = I_I - I_Q$)	I_q	$\overline{INH}$ ON, I_Q < 100 μA, T_J = 25°C	−	80	90	μA
Quiescent Current ($I_q = I_I - I_Q$)	I_q	$\overline{INH}$ ON, I_Q < 100 μA, $T_J \le$ 125°C	−	80	95	μA
Quiescent Current ($I_q = I_I - I_Q$)	I_q	$\overline{INH}$ ON, I_Q = 10 mA	−	200	500	μA
Quiescent Current ($I_q = I_I - I_Q$)	I_q	$\overline{INH}$ ON, I_Q = 50 mA	−	0.8	2.0	mA
Quiescent Current ($I_q = I_I - I_Q$)	I_q	$\overline{INH}$ = 0 V, T_J = 25°C	−	−	1.0	μA
Dropout Voltage (Note 7)	V_{dr}	I_Q = 100 mA	−	0.26	0.50	V
Load Regulation	ΔV_Q	I_Q = 1.0 mA to 100 mA	−	1.0	30	mV
Line Regulation	ΔV_Q	V_I = 6.0 V to 28 V, I_Q = 1.0 mA	−	2.0	25	mV
Power Supply Ripple Rejection	PSRR	fr = 100 Hz, Vr = 1.0 Vpp, I_Q = 100 mA	−	66	−	dB
INHIBIT ($\overline{INH}$)						
Inhibit Off Voltage	$V_{\overline{INH}OFF}$	V_Q < 0.1 V	−	−	0.8	V
Inhibit On Voltage 5.0 V Version 3.3 V Version	$V_{\overline{INH}ON}$	 V_Q > 4.9 V V_Q > 3.23 V	 3.5 3.5	 − −	 − −	V
Input Current	$I_{\overline{INH}ON}$ $I_{\overline{INH}OFF}$	$\overline{INH}$ = 5 V $\overline{INH}$ = 0 V	− −	3.8 0.01	10 2.0	μA
RESET (RO)						
Switching Threshold 5.0 V Version 3.3 V Version	V_{RT}	−	 4.50 2.96	 4.67 3.07	 4.80 3.16	V
Output Resistance	R_{RO}	−	10	20	40	kΩ
Reset Output Low Voltage 5.0 V Version 3.3 V Version	V_{RO}	 V_Q = 4.5 V, Internal R_{RO}, I_{RO} = −1.0 mA V_Q = 2.96 V, Internal R_{RO}, I_{RO} = −1.0 mA	 − −	 0.05 0.05	 0.40 0.40	V
Allowable External Reset Pullup Resistor	V_{ROext}	External Resistor to Q	5.6	−	−	kΩ
Delay Upper Threshold	V_{UD}	−	1.5	1.85	2.2	V
Delay Lower Threshold	V_{LD}	−	0.4	0.5	0.6	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Only for 5 V version. Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5 V.

ELECTRICAL CHARACTERISTICS (continued) ($-40°C < T_J < 150°C$; V_I = 13.5 V unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
RESET (RO)						
Delay Output Low Voltage 5.0 V Version 3.3 V Version	$V_{D,sat}$	 V_Q = 4.5 V, Internal R_{RO} V_Q = 2.96 V, Internal R_{RO}	 – –	 – 0.017	 0.1 0.1	V
Delay Charge Current	I_D	V_D = 1.0 V	4.0	7.1	12	μA
Power On Reset Delay Time	t_d	C_D = 100 nF	17	28	35	ms
Reset Reaction Time	t_{RR}	C_D = 100 nF	0.5	1.6	4.0	μs
Reset Adjust Switching Threshold 5.0 V Version 3.3 V Version	$V_{RADJ,TH}$	 V_Q = 3.5 V V_Q = 2.3 V	 1.26 1.26	 1.36 1.36	 1.44 1.44	V
INPUT VOLTAGE SENSE (SI and SO)						
Sense Input Threshold High	$V_{SI,High}$	–	1.34	1.45	1.54	V
Sense Input Threshold Low	$V_{SI,Low}$	–	1.26	1.36	1.44	V
Sense Input Hysteresis	–	(Sense Threshold High) – (Sense Threshold Low)	50	90	130	mV
Sense Input Current	I_{SI}	V_{SI} = 1.2 V	−1.0	0.1	1.0	μA
Sense Output Resistance	R_{SO}	–	10	20	40	kΩ
Sense Output Low Voltage	V_{SO}	V_{SI} = 1.2 V, V_I = 5.5 V, I_{SO} = 0 μA	–	0.1	0.4	V
Allowable External Sense Out Pullup Resistor	R_{SOext}	–	5.6	–	–	kΩ
SI High to SO High Reaction Time	t_{PSOLH}	R_{SOext} = 5.6 kΩ	–	1.3	8.0	μs
SI Low to SO Low Reaction Time	t_{PSOHL}	R_{SOext} = 5.6 kΩ	–	2.2	5.0	μs
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 8)	T_{SD}	I_{out} = 1 mA	150	–	200	°C

8. Values based on design and/or characterization.

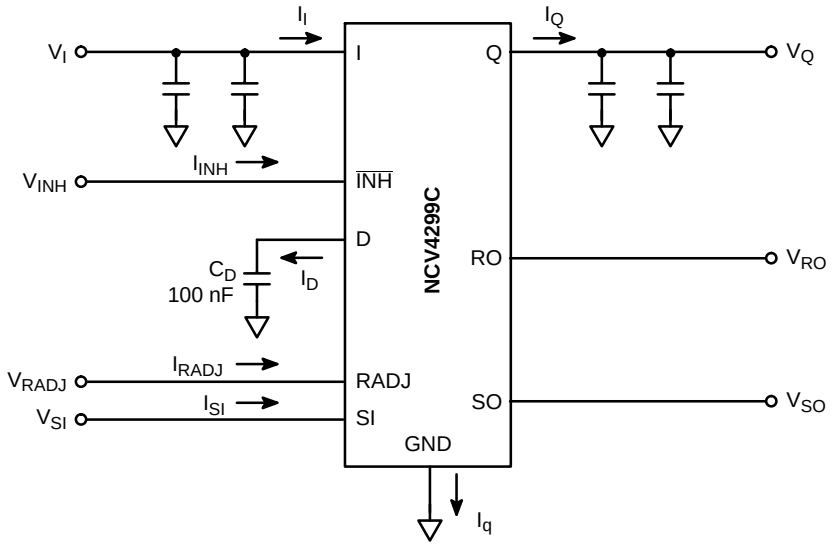


Figure 3. Measurement Circuit

TYPICAL PERFORMANCE CHARACTERISTICS − 5.0 V OPTION

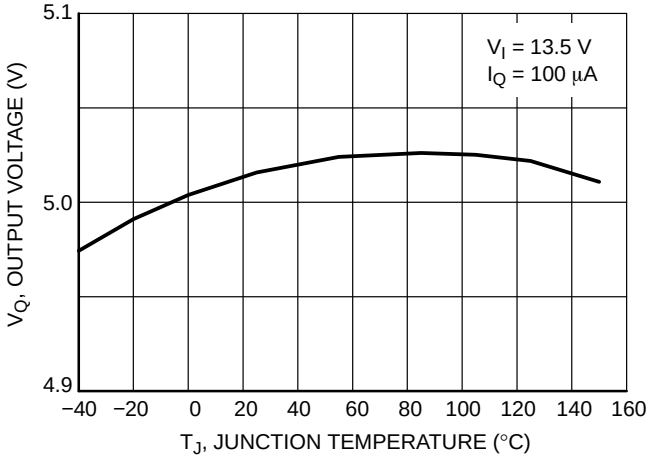


Figure 4. Output Voltage vs. Junction Temperature

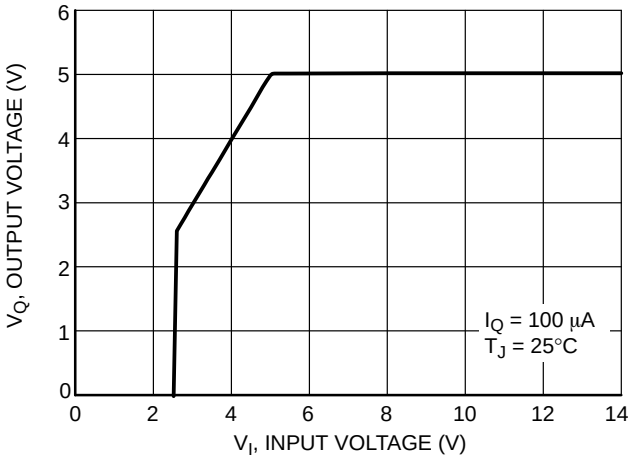


Figure 5. Output Voltage vs. Input Voltage

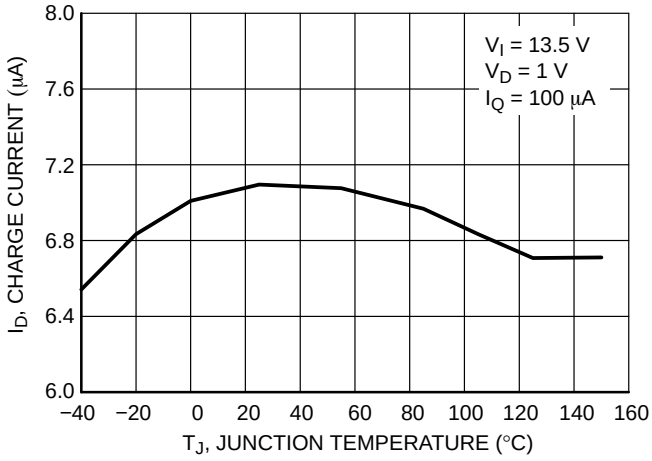


Figure 6. Charge Current vs. Junction Temperature

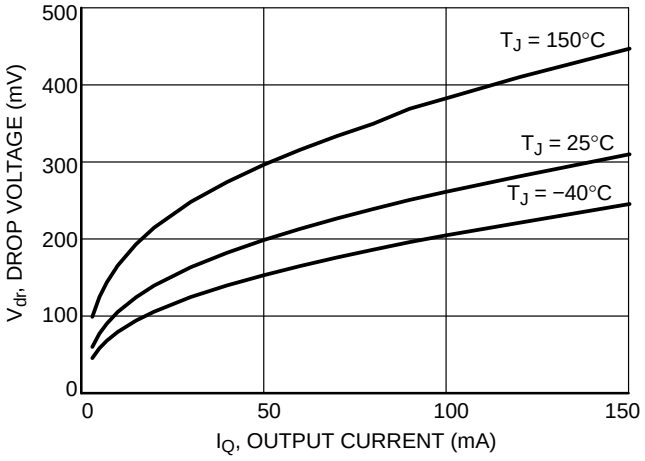


Figure 7. Drop Voltage vs. Output Current

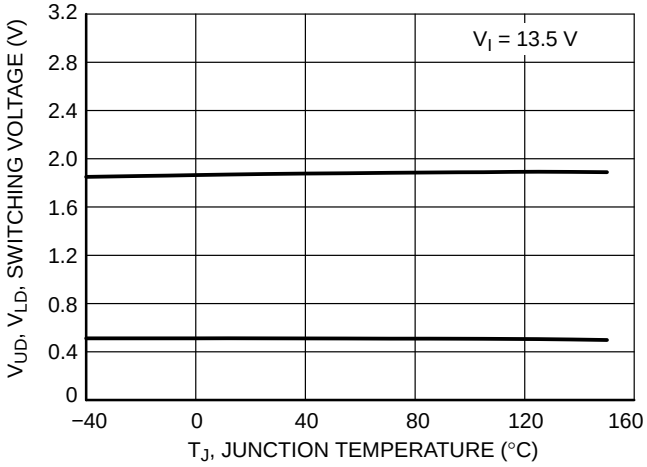


Figure 8. Switching Voltage vs. Junction Temperature

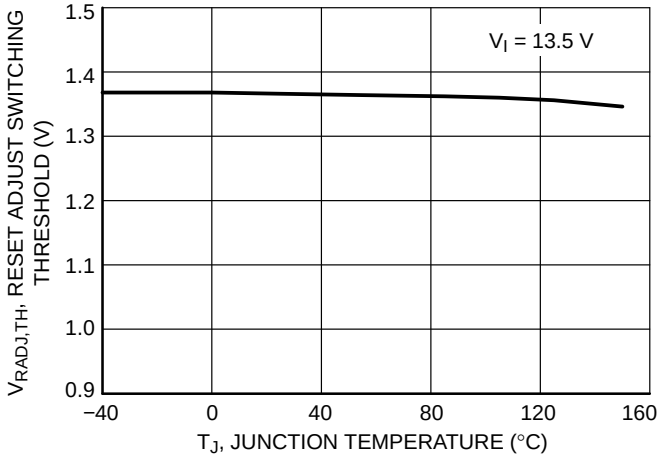


Figure 9. Reset Adjust Switching Threshold vs. Junction Temperature

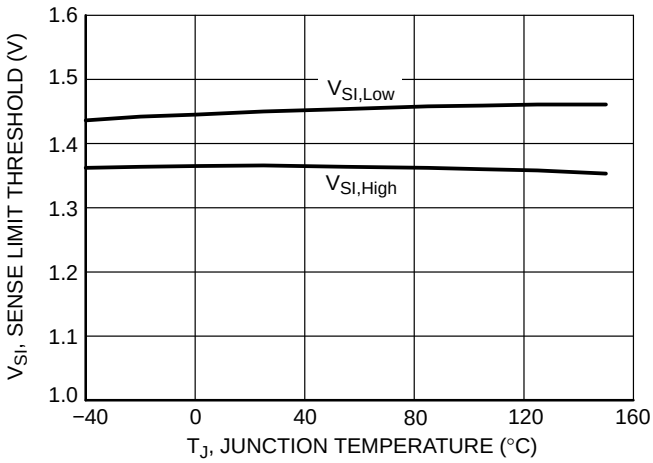


Figure 10. Sense Threshold vs. Junction Temperature

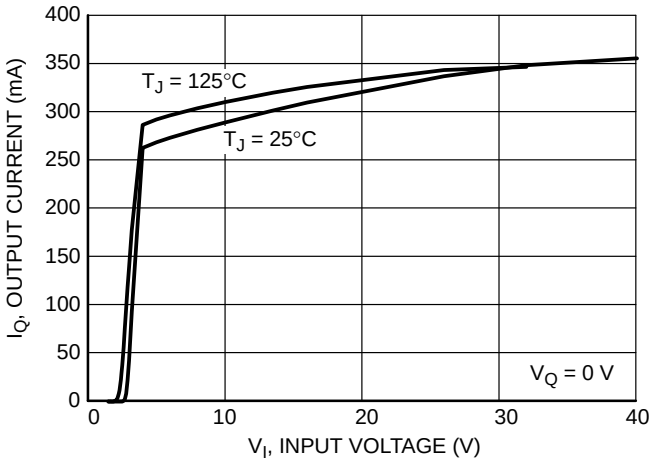


Figure 11. Output Current vs. Input Voltage

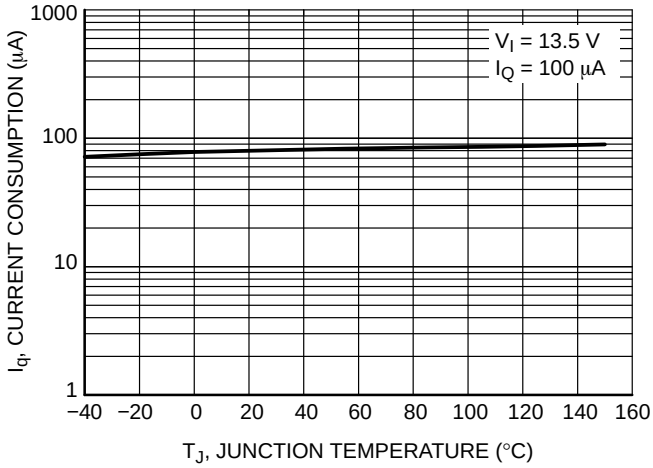


Figure 12. Current Consumption vs. Junction Temperature

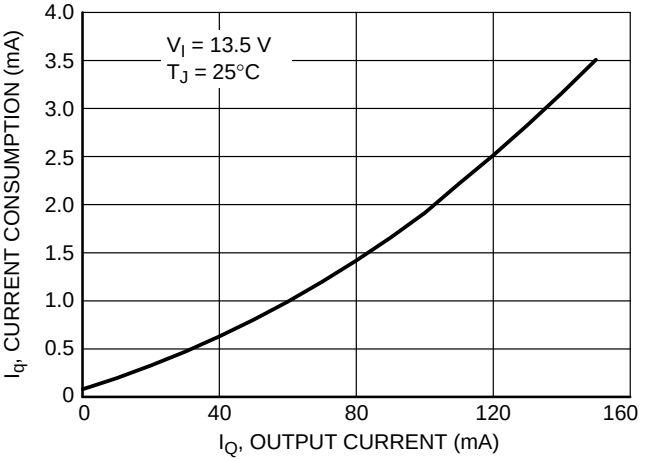


Figure 13. Current Consumption vs. Output Current

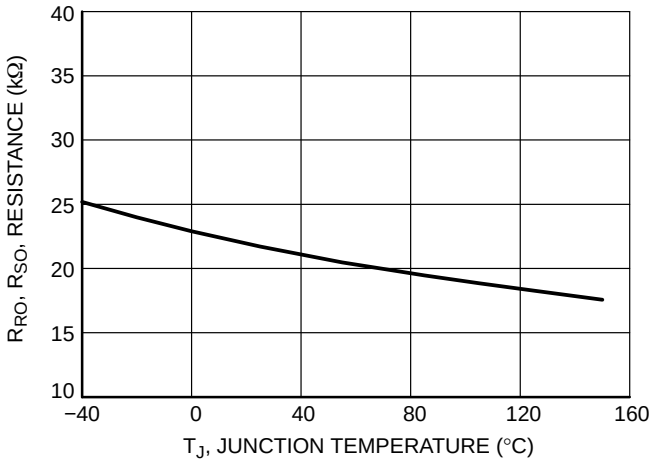


Figure 14. R_{RO}, R_{SO} Resistance vs. Junction Temperature

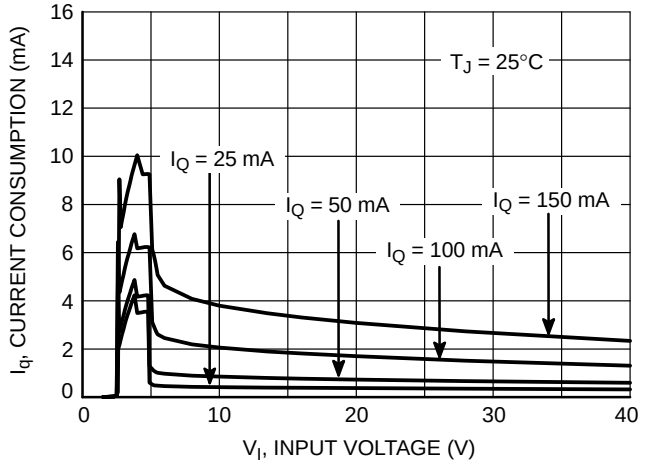


Figure 15. Current Consumption vs. Input Voltage

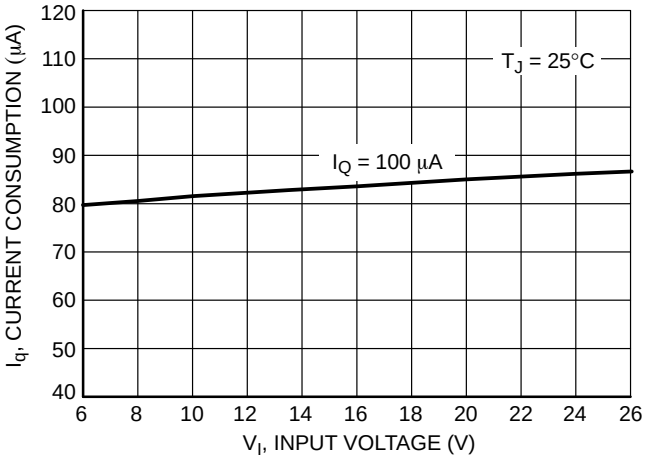


Figure 16. Current Consumption vs. Input Voltage

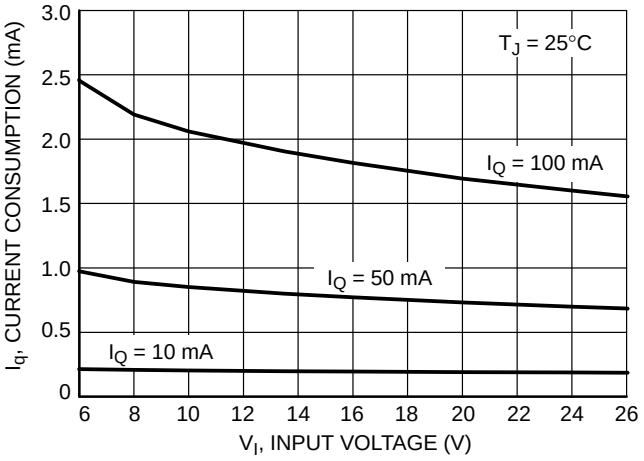


Figure 17. Current Consumption vs. Input Voltage

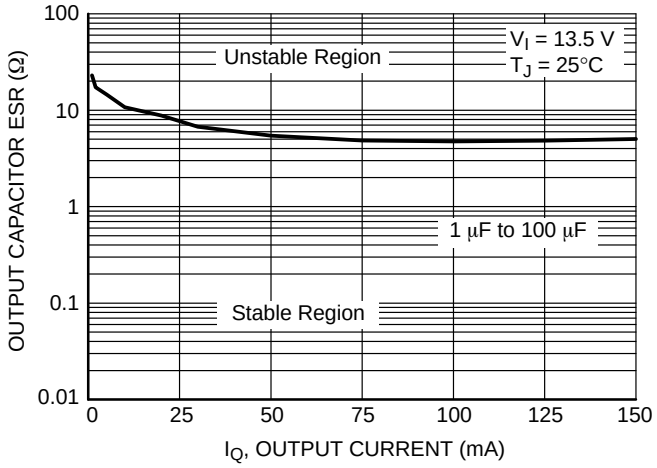


Figure 18. Output Stability vs. Output Capacitor ESR

TYPICAL PERFORMANCE CHARACTERISTICS − 3.3 V OPTION

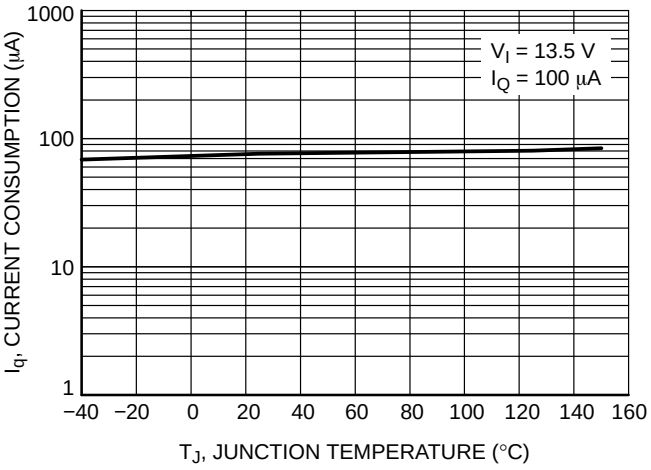


Figure 19. Current Consumption vs. Junction Temperature

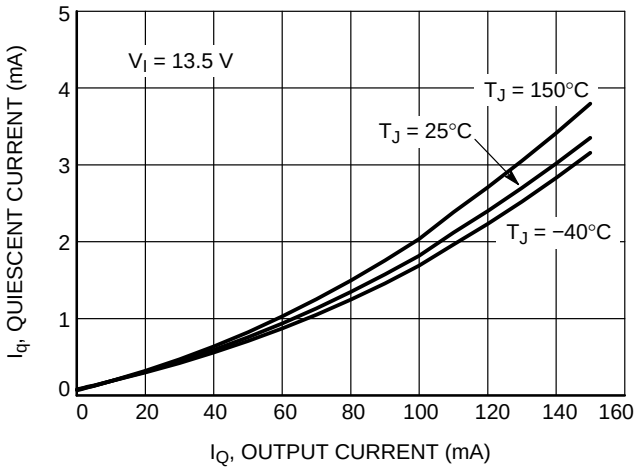


Figure 20. Current Consumption vs. Output Current

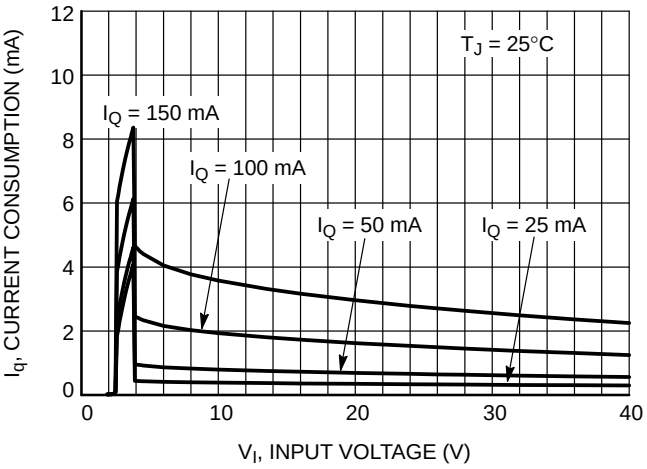


Figure 21. Current Consumption vs. Input Voltage

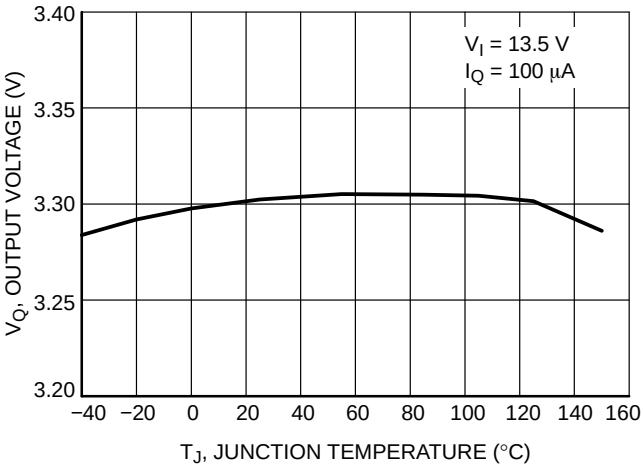


Figure 22. Output Voltage vs. Junction Temperature

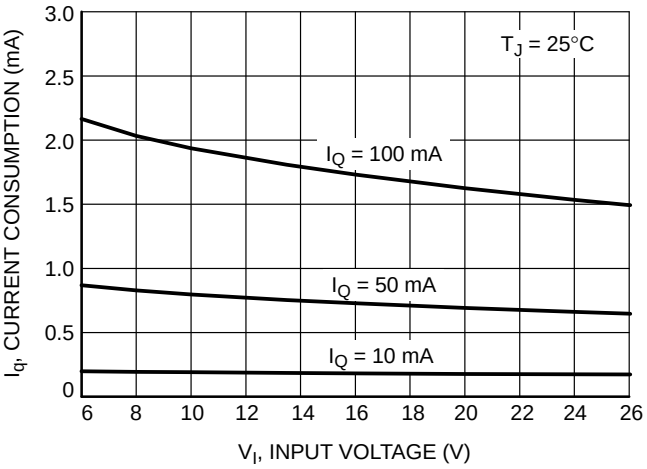


Figure 23. Current Consumption vs. Input Voltage

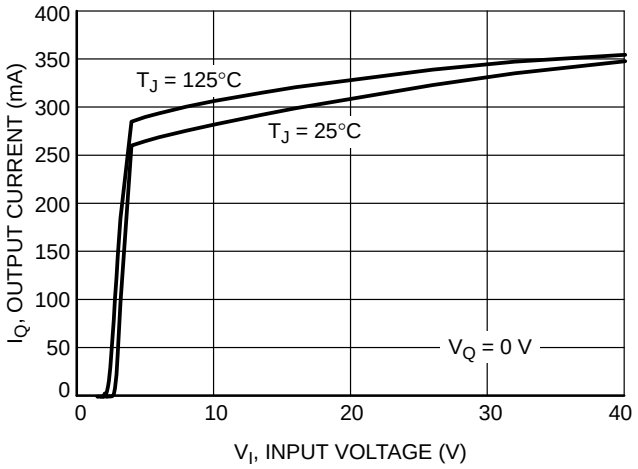


Figure 24. Output Current vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS − 3.3 V OPTION

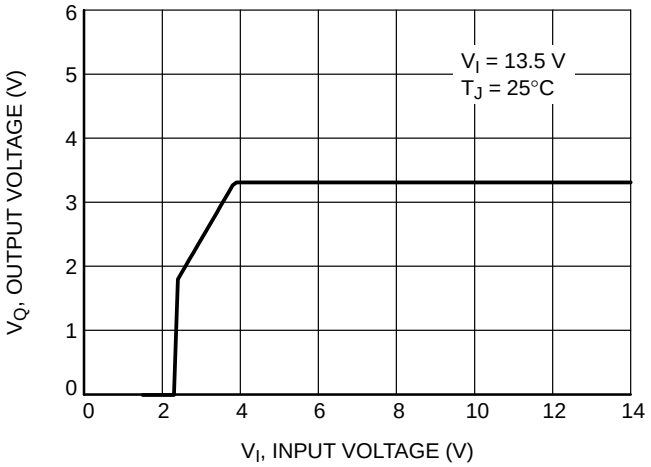


Figure 25. Output Voltage vs. Input Voltage

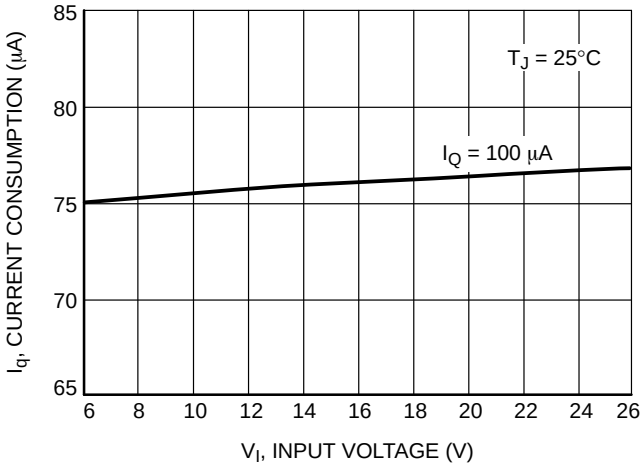


Figure 26. Current Consumption vs. Input Voltage

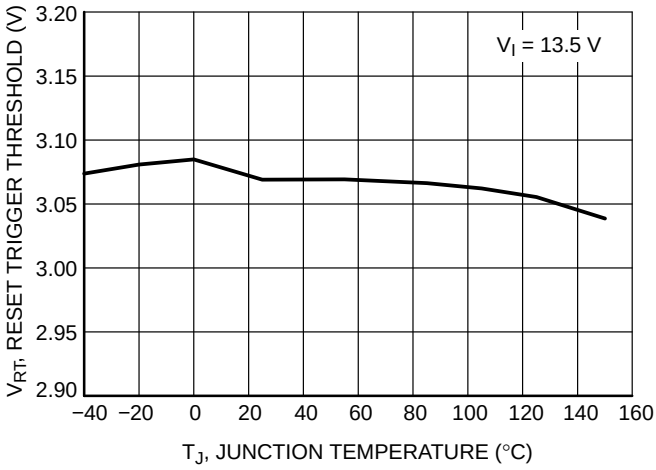


Figure 27. Reset Trigger Threshold vs. Junction Temperature

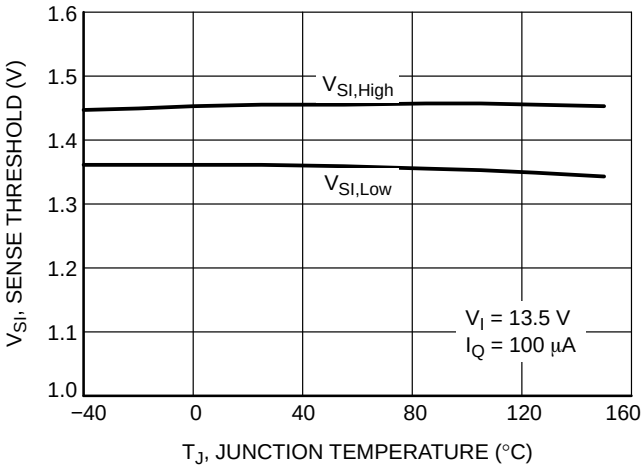


Figure 28. Sense Threshold vs. Junction Temperature

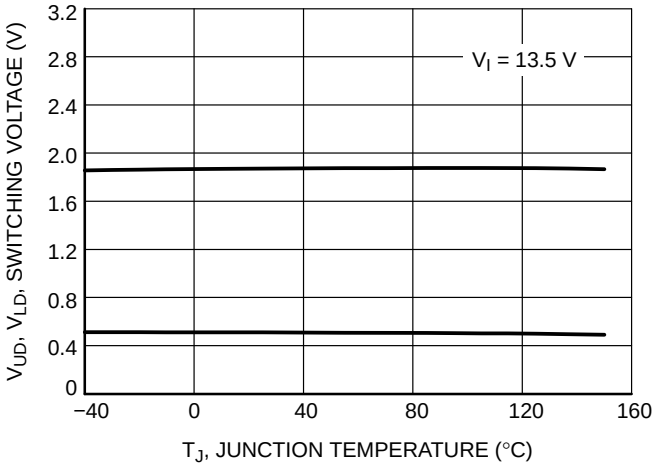


Figure 29. Switching Voltage vs. Junction Temperature

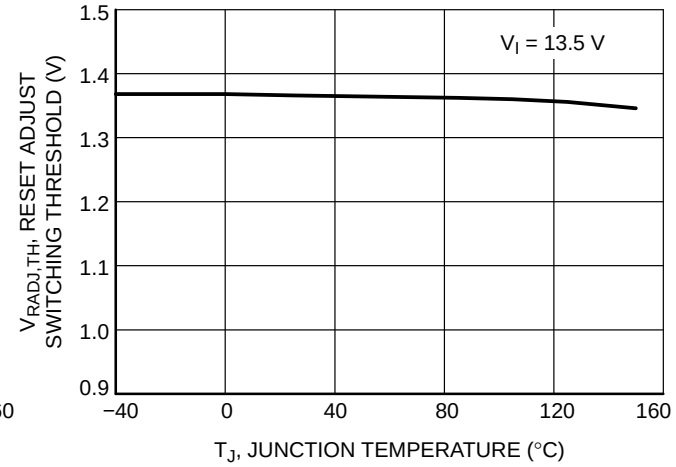


Figure 30. Reset Adjust Switching Threshold vs. Junction Temperature

TYPICAL PERFORMANCE CHARACTERISTICS − 3.3 V OPTION

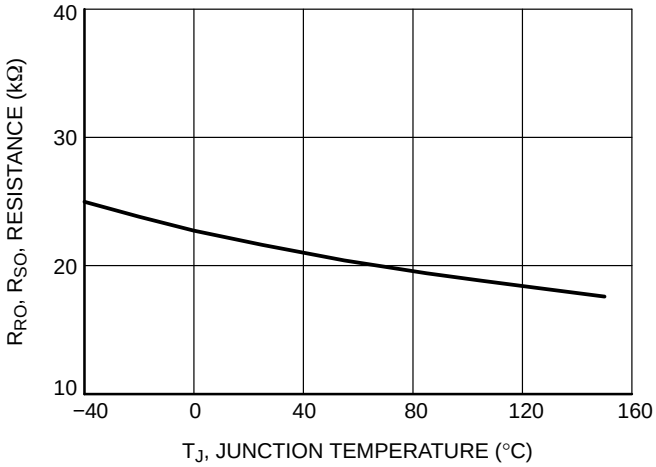


Figure 31. Resistance vs. Junction Temperature

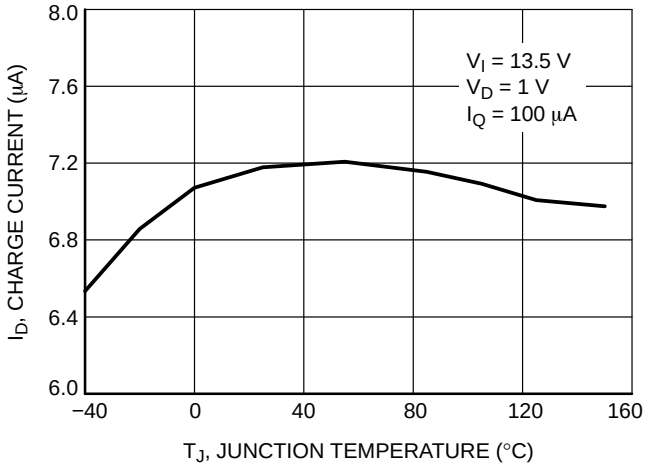


Figure 32. Charge Current vs. Junction Temperature

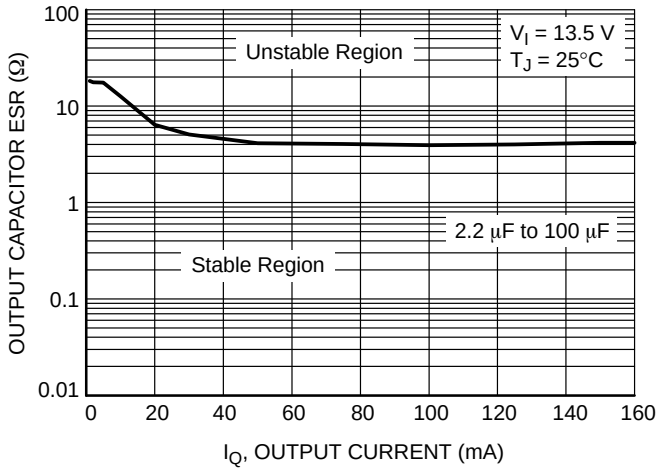


Figure 33. Output Capacitor ESR vs. Output Current

APPLICATION DESCRIPTION

NCV4299C

The NCV4299C is a family of precision micropower voltage regulators with an output current capability of 150 mA at 5.0 V and 3.3 V.

The output voltage is accurate within ±2% with a maximum dropout voltage of 0.5 V at 100 mA. Low quiescent current is a feature drawing only 80 μA with a 100 μA load. This part is ideal for any and all battery operated microprocessor equipment.

Microprocessor control logic includes an active reset output RO (with delay), and a SI/SO monitor which can be used to provide an early warning signal to the microprocessor of a potential impending reset signal. The use of the SI/SO monitor allows the microprocessor to finish any signal processing before the reset shuts the microprocessor down. Internal output resistors on the RO and SO pins pulling up to the output pin Q reduce external component count. An inhibit function is available on the 14−lead part. With inhibit active, the regulator turns off and the device consumes less that 1.0 μA of quiescent current.

The active reset circuit operates correctly at an output voltage as low as 1.0 V. The reset function is activated during the powerup sequence or during normal operation if the output voltage drops outside the regulation limits.

The reset threshold voltage can be decreased by the connection of an external resistor divider to the RADJ lead. The regulator is protected against reverse battery, short circuit, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments.

NCV4299C Circuit Description

The low dropout regulator in the NCV4299C uses a PNP pass transistor to give the lowest possible dropout voltage capability. The current is internally monitored to prevent oversaturation of the device and to limit current during over current conditions. Additional circuitry is provided to protect the device during overtemperature operation.

The regulator provides an output regulated to 2%.

Other features of the regulator include an undervoltage reset function and a sense circuit. The reset function has an adjustable time delay and an adjustable threshold level. The sense circuit trip level is adjustable and can be used as an early warning signal to the controller. An inhibit function that turns off the regulator and reduces the current consumption to less than 1.0 μA is a feature available in the 14 pin package.

Output Regulator

The output is controlled by a precision trimmed reference. The PNP output has saturation control for regulation while the input voltage is low, preventing oversaturation. Current limit and voltage monitors complement the regulator design to give safe operating signals to the processor and control circuits.

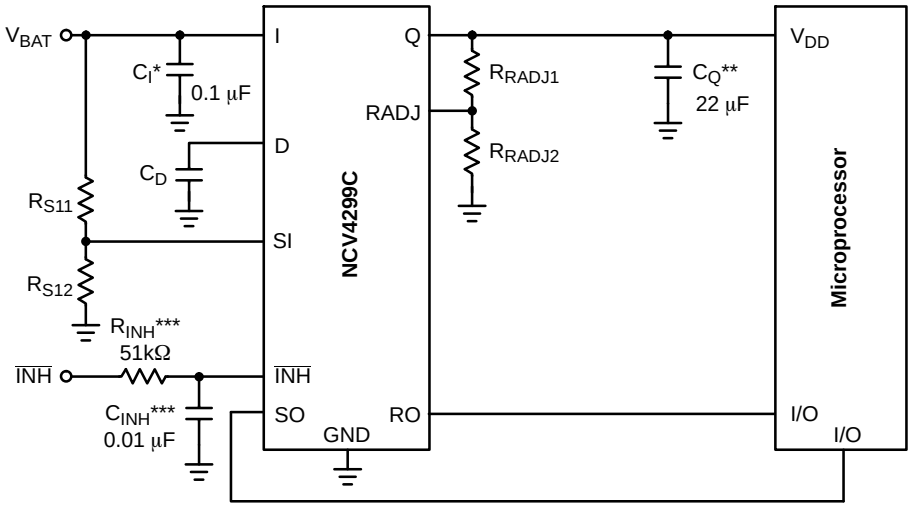
Stability Considerations

The input capacitor C_I is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1.0 Ω in series with C_I.

The output or compensation capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability.

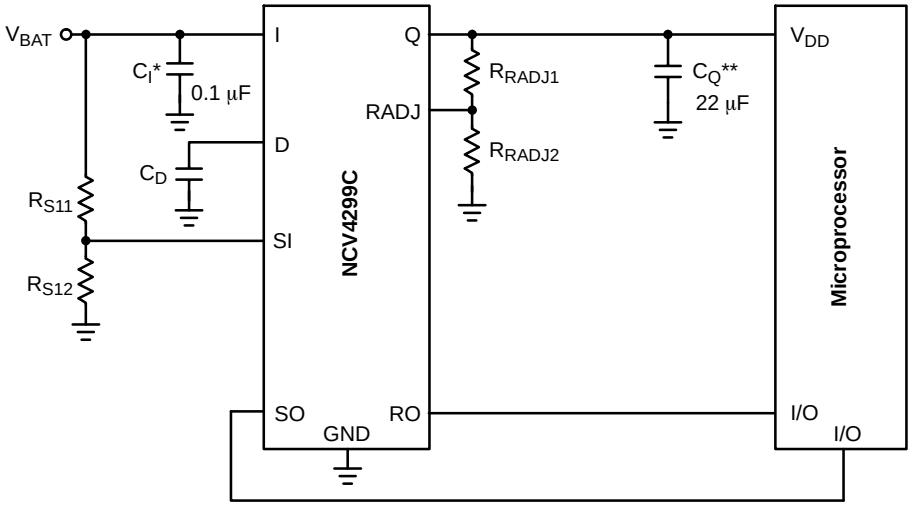
The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information.

The value for the output capacitor C_Q shown in Figure 34 should work for most applications, however, it is not necessarily the optimized solution. Stability is guaranteed at values $C_Q \geq 22$ μF and an ESR ≤ 4 Ω within the operating temperature range. Actual limits are shown in a graph in the typical performance characteristics section.



*C_I required if regulator is located far from the power supply filter.
**C_Q required for stability. Cap must operate at minimum temperature expected.
***This RC filter is only required when transients with slew rate in excess of 10 V/μs may be present on the $\overline{INH}$ voltage source during operation. The filter is not required when $\overline{INH}$ is connected to a noise−free DC voltage.

Figure 34. Test and Application Circuit Showing all Compensation and Sense Elements



*C_I required if regulator is located far from the power supply filter.
**C_Q required for stability. Cap must operate at minimum temperature expected.

Figure 35. Test and Application Circuit Showing all Compensation and Sense Elements for 8 Pin Package Part

Reset Output (RO)

A reset signal, Reset Output (RO, low voltage) is generated as the IC powers up. After the output voltage V_Q increases above the reset threshold voltage V_{RT}, the delay timer D is started. When the voltage on the delay timer V_D passes V_{UD}, the reset signal RO goes high. D pin voltage in steady state is typically 2.5 V. A discharge of the delay timer (V_D) is started when V_Q drops and stays below the reset threshold voltage V_{RT}. When the voltage of the delay timer (V_D) drops below the lower threshold voltage V_{LD}, the reset output voltage V_{RO} is brought low to reset the processor.

The reset output RO is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC, thereby guaranteeing that RO is valid for V_Q as low as 1.0 V.

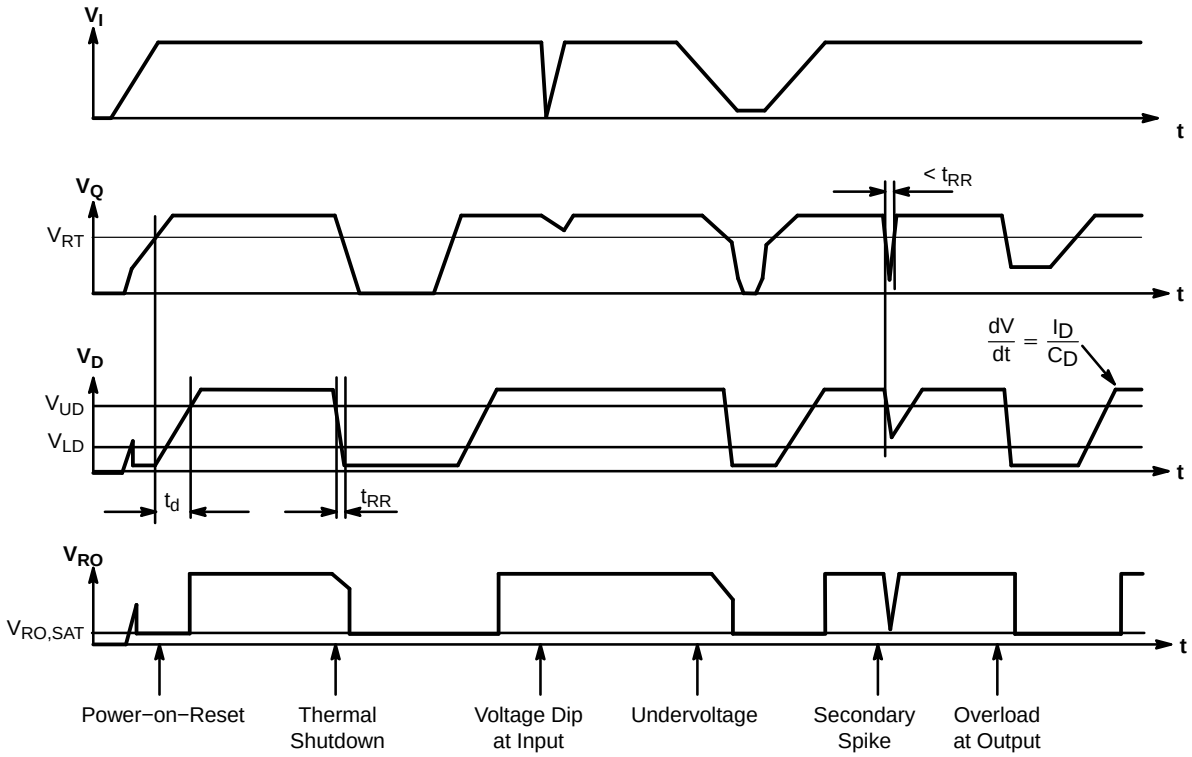


Figure 36. Reset Timing Diagram

Reset Adjust (RADJ)

The reset threshold V_{RT} can be decreased from a typical value of 4.67 V to as low as 3.5 V by using an external voltage divider connected from the Q lead to the pin RADJ, as shown in Figure 34. The resistor divider keeps the voltage above the $V_{RADJ,TH}$, (typ. 1.36 V), for the desired input voltages and overrides the internal threshold detector. Adjust the voltage divider according to the following relationship:

$$V_{THRES} = V_{RADJ,TH} \cdot (R_{ADJ1} + R_{ADJ2})/R_{ADJ2} \quad \text{(eq. 1)}$$

If the reset adjust option is not needed, the RADJ−pin should be connected to GND causing the reset threshold to go to its default value (typ. 4.67 V).

Reset Delay (D)

The reset delay circuit provides a delay (programmable by capacitor C_D) on the reset output RO lead. The delay lead D provides charge current I_D (typically 7.1 μA) to the external delay capacitor C_D during the following times:

1. During Powerup (once the regulation threshold has been exceeded).
2. After a reset event has occurred and the device is back in regulation. The delay capacitor is set to discharge when the regulation (V_{RT}, reset threshold voltage) has been violated. When the delay capacitor discharges to down to V_{LD}, the reset signal RO pulls low.

Setting the Delay Time

The delay time is set by the delay capacitor C_D and the charge current I_D. The time is measured by the delay capacitor voltage charging from the low level of $V_{D,sat}$ to the higher level V_{UD}. The time delay follows the equation:

$$t_d = [C_D (V_{UD} - V_{D,sat})]/I_D \quad \text{(eq. 2)}$$

Example:

Using C_D = 100 nF.
Use the typical value for $V_{D,sat}$ = 0.1 V.
Use the typical value for V_{UD} = 1.85 V.
Use the typical value for Delay Charge Current I_D = 7.1 μA.

$$t_d = [100\ nF(1.85 - 0.1\ V)]/7.1\ \mu A = 24.6\ ms \quad \text{(eq. 3)}$$

When the output voltage V_Q drops below the reset threshold voltage V_{RT}, the voltage on the delay capacitor V_D starts to drop. The time it takes to drop below the lower threshold voltage of V_{LD} is the reset reaction time, t_{RR}. This time is typically 1.6 μs for a delay capacitor of 0.1 μF. The reset reaction time can be estimated from the following relationship:

$$t_{RR} = 16\ ns/nF \times C_D \quad \text{(eq. 4)}$$

Sense Input (SI)/Sense Output (SO) Voltage Monitor

An on−chip comparator is available to provide early warning to the microprocessor of a possible reset signal. The reset signal typically turns the microprocessor off instantaneously. This can cause unpredictable results with the microprocessor. The signal received from the SO pin will allow the microprocessor time to complete its present task before shutting down. This function is performed by a comparator referenced to the band gap voltage. The actual trip point can be programmed externally using a resistor divider to the input monitor (SI) (Figure 34). The typical threshold is 1.36 V on the SI Pin.

Signal Output

Figure 37 shows the SO Monitor waveforms as a result of the circuits depicted in Figure 34. As the output voltage V_Q falls, the monitor threshold $V_{SI,Low}$ is crossed. This causes the voltage on the SO output to go low sending a warning signal to the microprocessor that a reset signal may occur in a short period of time. $T_{WARNING}$ is the time the microprocessor has to complete the function it is currently working on and get ready for the reset shutdown signal. When the voltage on the SO goes low and the RO stays high the current consumption is typically 400 μA.

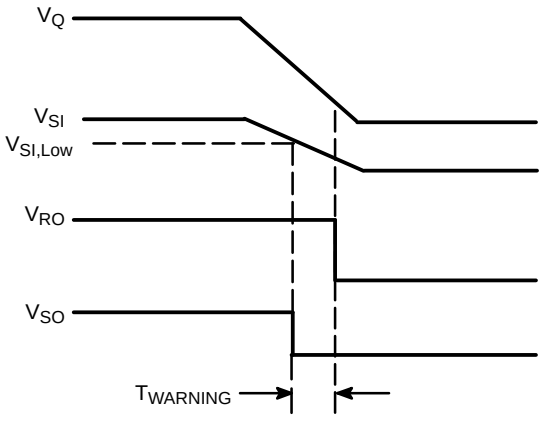


Figure 37. SO Warning Timing Waveform

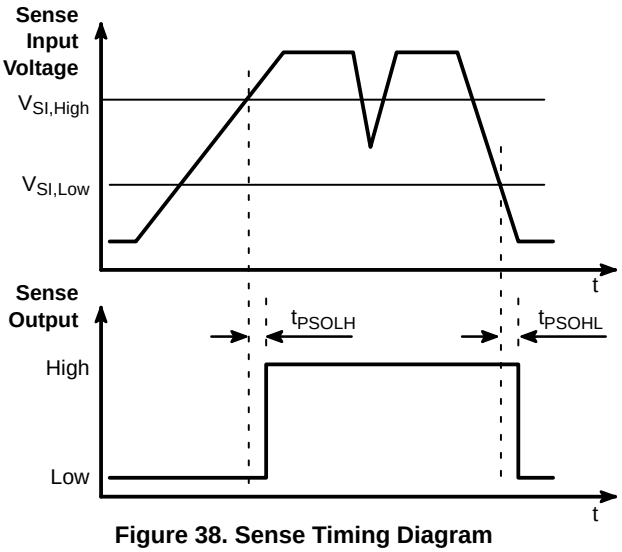


Figure 38. Sense Timing Diagram

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator is:

$$P_{D(max)} = [V_{I(max)} - V_{Q(min)}]\ I_{Q(max)} + V_{I(max)} I_q \quad \text{(eq. 5)}$$

where:

$V_{I(max)}$ is the maximum input voltage,
$V_{Q(min)}$ is the minimum output voltage,
$I_{Q(max)}$ is the maximum output current for the application, and
I_q is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = (150^\circ C - T_A)/P_D \quad \text{(eq. 6)}$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in Equation 6 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required. Thermal Resistance $R_{\theta JA}$ vs. Copper Area is shown in Figure 39.

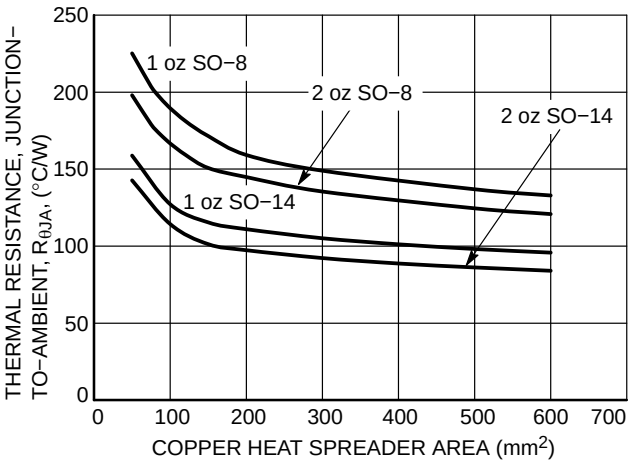


Figure 39. Thermal Resistance $R_{\theta JA}$ vs. Copper Area

Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad \text{(eq. 7)}$$

where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,
$R_{\theta CS}$ = the case−to−heatsink thermal resistance, and
$R_{\theta SA}$ = the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heatsink data sheets of heatsink manufacturers. Thermal, mounting, and heatsinking are discussed in the ON Semiconductor application note AN1040/D, available on the ON Semiconductor website.

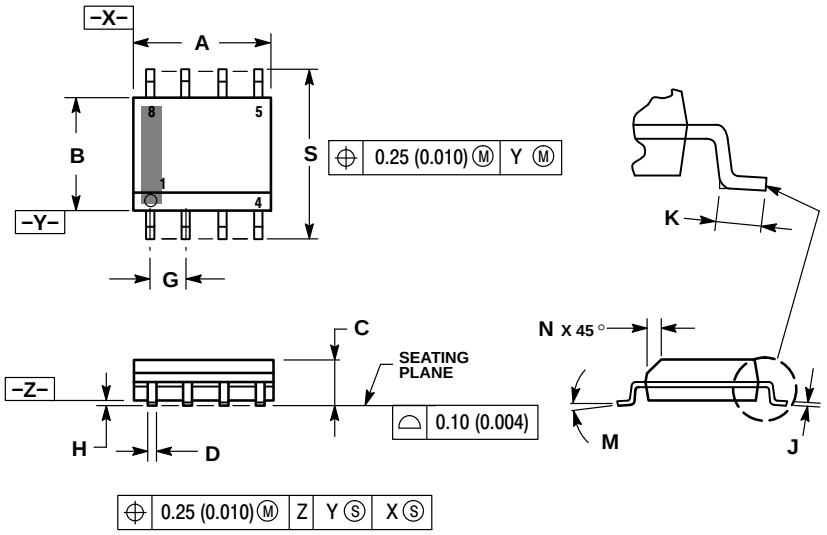
ORDERING INFORMATION

Device	Package	Shipping†
NCV4299CD133R2G	SO−8 (Pb−Free)	2500 / Tape & Reel
NCV4299CD150R2G	SO−8 (Pb−Free)	2500 / Tape & Reel
NCV4299CD233R2G	SO−14 (Pb−Free)	2500 / Tape & Reel
NCV4299CD250R2G	SO−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

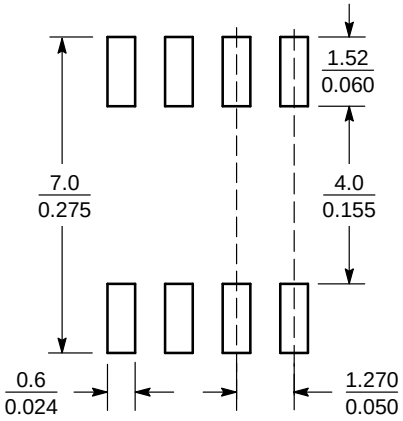
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

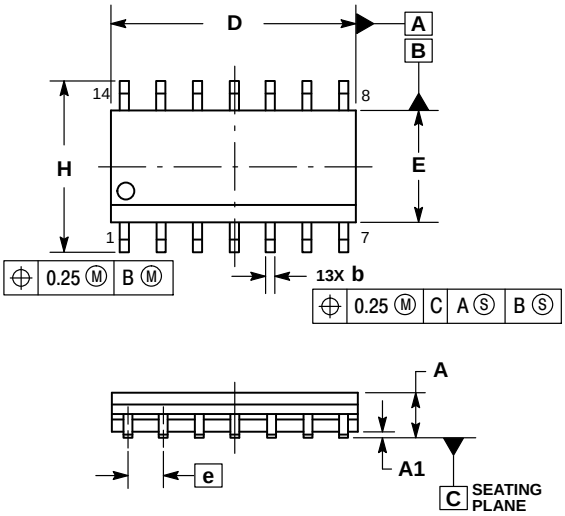


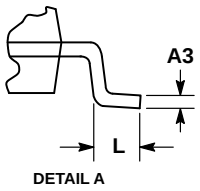
SCALE 6:1 (mm / inches)

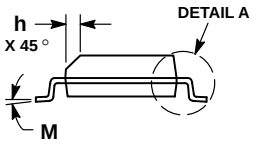
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SOIC−14 NB
CASE 751A−03
ISSUE K



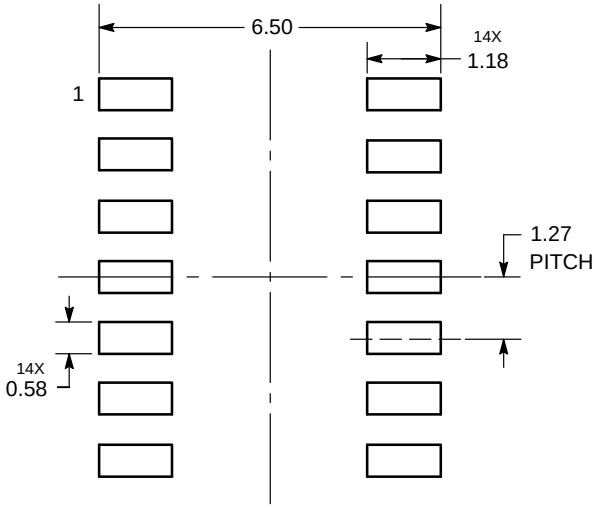




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and the ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative