HARRIS Semiconductor

RFL1N08, RFL1N10

1A, 80V and 100V, 1.200 Ohm, N-Channel, Power MOSFETs

September 1998

Features

- **1A, 80V and 100V**
- **$r_{DS(ON)}$ = 1.200Ω**

Ordering Information

PART NUMBER	PACKAGE	BRAND
RFL1N08	TO-205AF	RFL1N08
RFL1N10	TO-205AF	RFL1N10

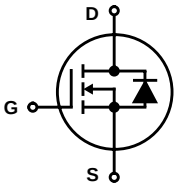
NOTE: When ordering, use the entire part number.

Description

These are N-channel enhancement mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

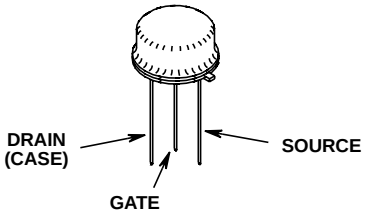
Formerly developmental type TA09282.

Symbol



Packaging

JEDEC TO-204AA



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

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File Number **1385.2**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFL1N08	RFL1N10	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	80	100	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	80	100	V
Continuous Drain Current	I_D	1	1	A
Pulsed Drain Current (Note 3	I_{DM}	5	5	A
Gate to Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation	P_D	8.33	8.33	W
Linear Derating Factor		0.0667	0.0667	W/^{o}C
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	-55 to 150	^{o}C
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10s	T_L	260	260	^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage RFL1N08	BV_{DSS}	I_D = 250μA, V_{GS} = 0V	80	-	-	V
RFL1N10			100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA, (Figure 8)	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_J = 125^oC$	-	-	25	μA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, V_{GS} = 10V	1	-	-	A
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 5.6A, V_{GS} = 10V, (Figures 6, 7)			1.200	Ω
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, V_{GS} = 10V, $I_D \approx$ 1A, R_G = 50Ω, R_L = 50Ω (Figures 10, 11, 12) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	17	25	ns
Rise Time	t_r		-	30	45	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	30	45	ns
Fall Time	t_f		-	30	50	ns
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 9)	-	-	200	pF
Output Capacitance	C_{OSS}		-	-	80	pF
Reverse Transfer Capacitance	C_{RSS}		-	-	25	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-		^{o}C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^oC$, I_{SD} = 1A, V_{GS} = 0V	-	-	1.4	V
Reverse Recovery Time	t_{rr}	$T_J = 25^oC$, I_{SD} = 1A, dI_{SD}/dt = 100A/μs	-	100	-	ns

NOTES:

2. Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

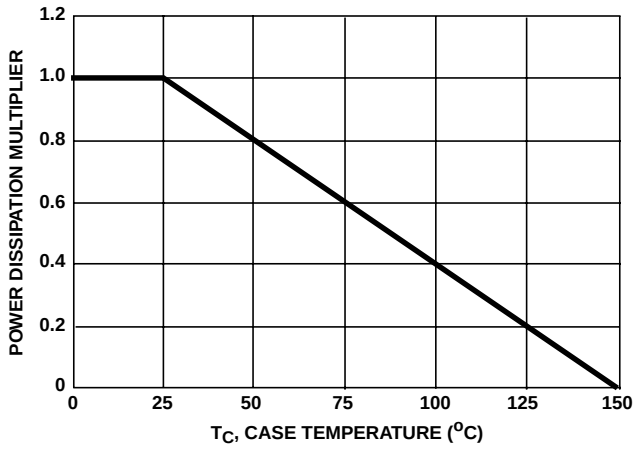


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

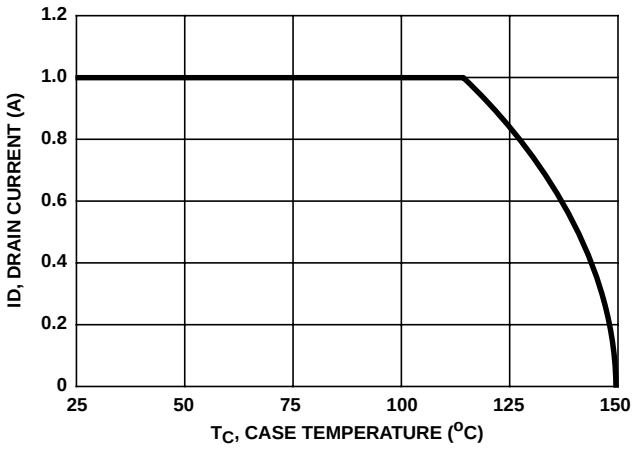


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

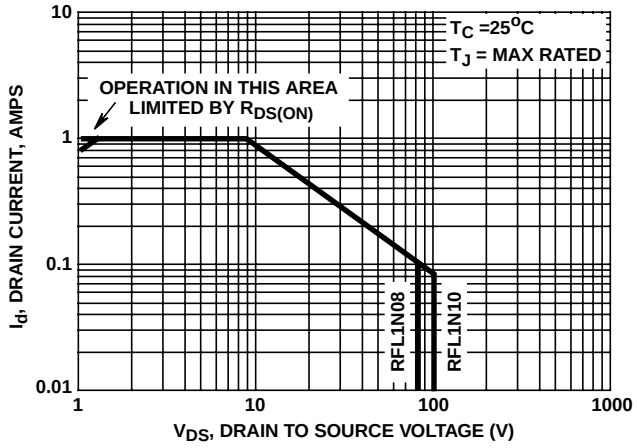


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

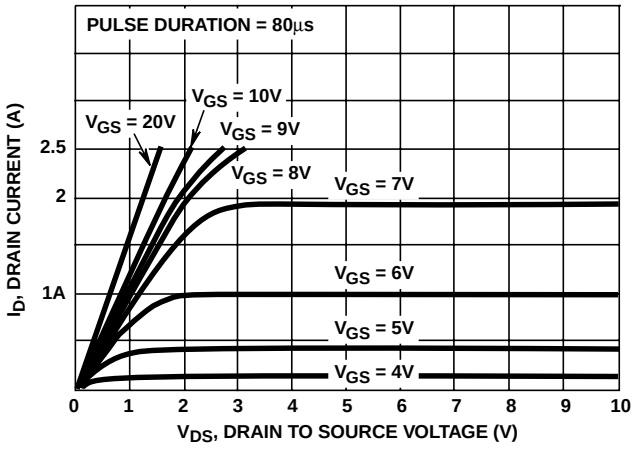


FIGURE 4. SATURATION CHARACTERISTICS

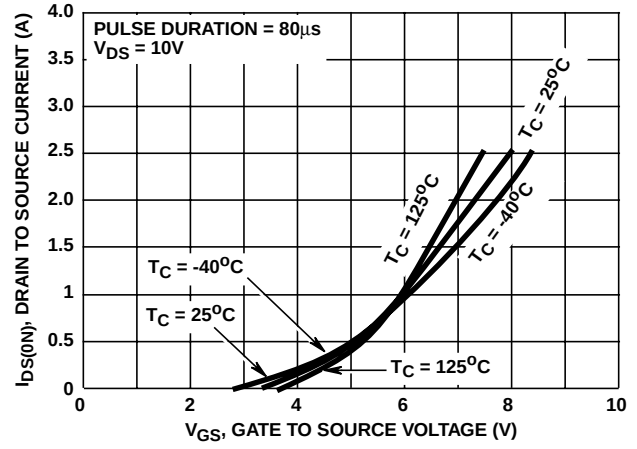


FIGURE 5. TRANSFER CHARACTERISTICS

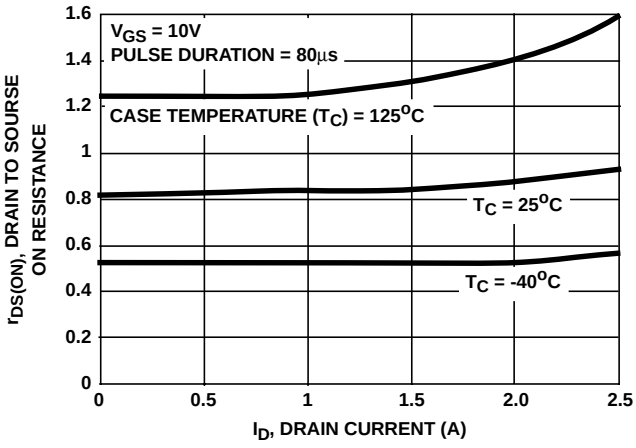


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

Typical Performance Curves Unless Otherwise Specified (Continued)

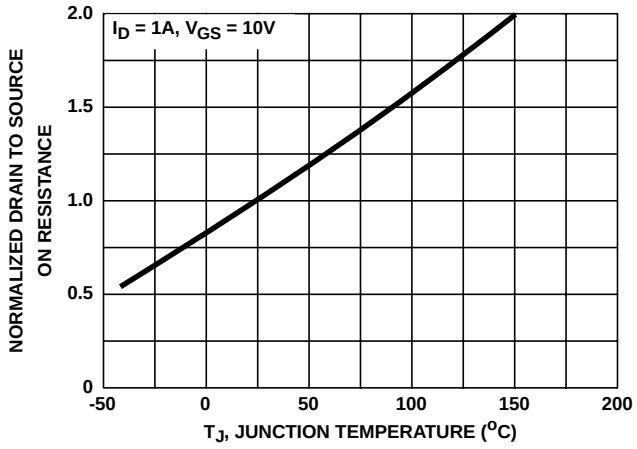


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

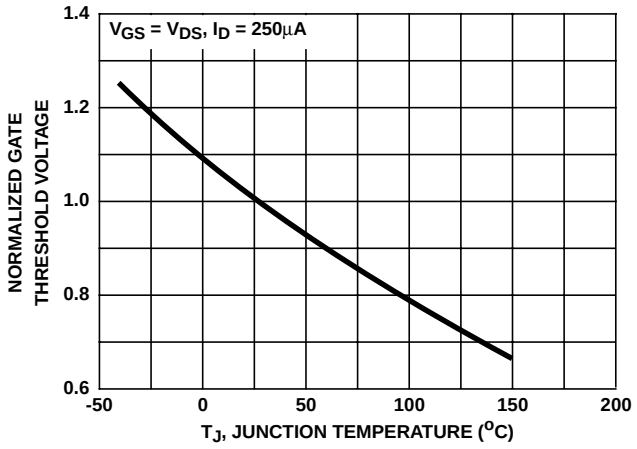


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

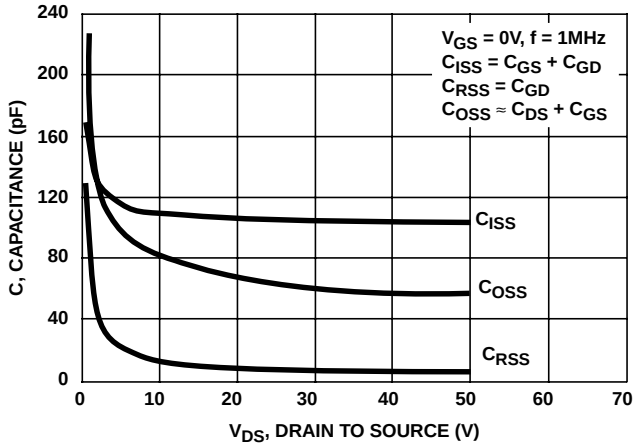
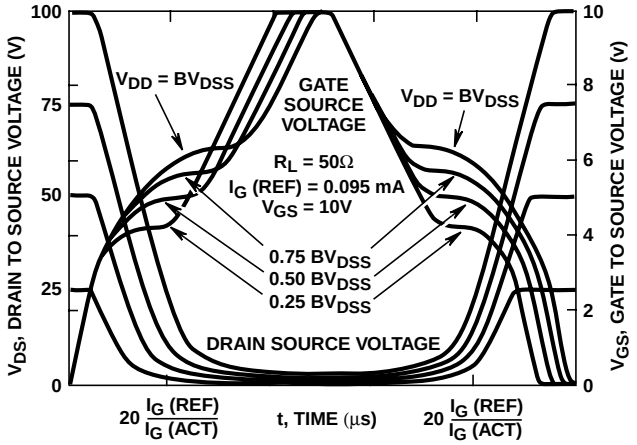


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

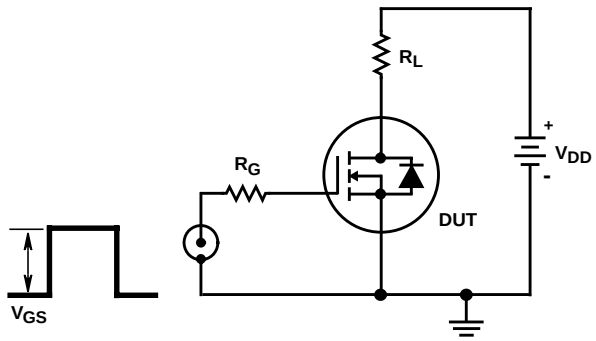


FIGURE 11. SWITCHING TIME TEST CIRCUIT

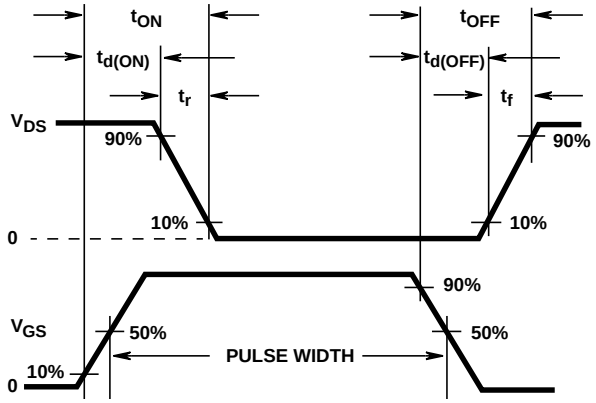


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS