AAT2782

Triple-Output PMIC: Dual Buck with Low-V_{IN} LDO

General Description

The AAT2782 provides three independently regulated DC outputs: two step-down (Buck) regulators and a single low input voltage, low drop-out (LDO) regulator. The input voltage range for the step-down regulators is 2.7V to 5.5V, while the LDO regulator allows inputs from 1.5V to 5.5V. The low input voltage LDO regulator allows high efficiency, step-down, low noise outputs. In addition, the LDO input may be connected to step-down outputs 1 or 2.

The Channel 1 and 2 step-down regulators can deliver up to 1200mA and 600mA output current, respectively. Step-down output voltages are set with external resistors. Switching frequency is set at 1.3MHz to ensure small external filtering components. Current mode control assures fast transient response and stable operation across the operating range. The Channel 3 LDO regulator can deliver up to 400mA with -80dB power supply rejection ratio (PSRR) and 65μV_{RMS} output noise with an optional bypass capacitor. The LDO output voltage is factory set with a default voltage of 1.20V. Independent enable and input pins are provided. The device consumes low quiescent current and provides high efficiency across the load range for maximum life in battery systems.

The AAT2782 is available in the Pb-free, 16-pin TDFN34 package and is rated over the -40°C to 85°C operating temperature range.

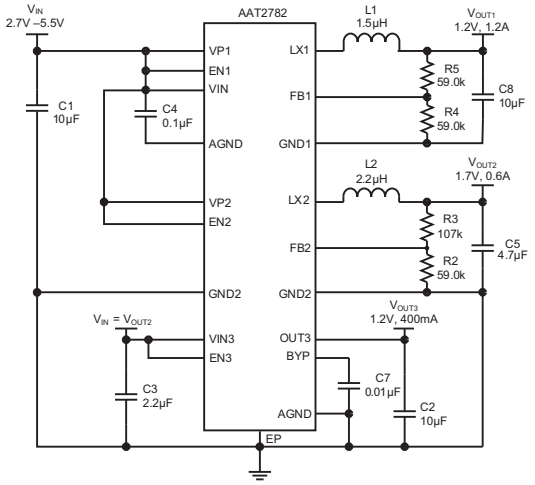
Features

- V_{IN} Range Step-Down (Buck): 2.7V to 5.5V
- V_{IN} Range Low Drop-Out (LDO): 1.5V to 5.5V
- Output Voltage Range: 0.6V to V_{IN}
- Step-Down Output Current:
  - Channel 1: 1200mA
  - Channel 2: 600mA
- LDO Output Current:
  - Channel 3: 400mA
- High Efficiency with Low $R_{DS(ON)}$ Switches
  - Step-Down up to 97%
  - LDO Regulator up to 80%
- Total Quiescent Current 170µA
- Shutdown Current: 1µA
- Step-Down Converters
  - 1.3MHz Switching Frequency
  - Current Mode Control
  - Cycle-by-Cycle Current Limit
  - High Efficiency Light-Load Mode Operation
- LDO Converter
  - Ultra Low Noise with Bypass Capacitor
  - Over-Current Protection
- 200µs Internal Soft Start
- Over-Temperature Protection
- TDFN34-16 Low Profile Package
- -40°C to 85°C Temperature Range

Applications

- Cellular and SmartPhones
- Microprocessor / DSP Core / IO Power
- PDAs and Handheld Computers
- Portable Media Players
- Wireless Data Systems

Typical Application

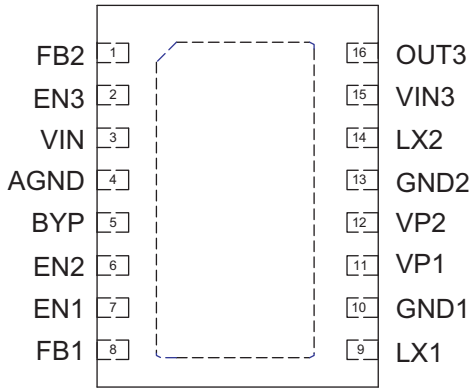


Pin Descriptions

Pin #	Symbol	Function
1	FB2	Feedback input pin for Channel 2. Connect an external resistor divider to this pin to program the output voltage to the desired value.
2	EN3	Enable Channel 3 input. Pull logic high to enable LDO Channel 3 converter. Pull logic low to disable. Channel 3 will turn on when EN3 is high and Channel 2 is in regulation.
3	VIN	Input voltage pin. Connect this pin to input voltage source.
4	AGND	Analog ground pin. Connect to ground plane.
5	BYP	LDO bypass pin. Connect a 10nF ceramic capacitor from this pin to ground plane for low output noise.
6	EN2	Enable Channel 2 input. Pull logic high to enable step-down Channel 2 converter. Pull logic low to disable.
7	EN1	Enable Channel 1 input. Pull logic high to enable step-down Channel 1 converter. Pull logic low to disable.
8	FB1	Channel 1 feedback pin internally set to 0.6V. Connect resistor divider and optional feed-forward capacitor to this pin to set the Channel 1 voltage and adjust transient load response (see Table 1).
9	LX1	Channel 1 converter switching pin. Connect Channel 1 inductor to this pin. Inductor value is determined by output voltage (see Table 2).
10	GND1	Power return pin for output 1 step-down converter. Connect returns of Channel 1 input and output capacitors close to this pin for best noise performance.
11	VP1	Input supply voltage pin for Channel 1 step-down converter. Connect the input capacitor close to this pin for best noise performance.
12	VP2	Input supply voltage pin for Channel 2 step-down converter. Connect the input capacitor close to this pin for best noise performance.
13	GND2	Power return pin for Channel 2 step-down converter. Connect returns of Channel 2 input and output capacitors close to this pin for best noise performance.
14	LX2	Channel 2 converter switching pin. Connect output 2 inductor to this pin. Inductor value is determined by output voltage (see Table 2).
15	VIN3	Input supply voltage pin for output 3 low-noise LDO converter. Connect the input capacitor close to this pin for best noise performance.
16	OUT3	Channel 3 LDO step-down converter output pin. Connect this pin to a 10µF ceramic capacitor.
	EP	Exposed pad. Connect to ground as close as possible to the device. Use properly sized vias for thermal coupling to the ground plane. See section on PCB layout guidelines.

Pin Configuration

TDFN34-16
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{IN}	VP1, VP2, VIN to GND1, GND2, AGND	-0.3 to 6.0	V
V_{IN3}	VIN3 to GND1, GND2, AGND	-0.3 to V_{IN}	V
V_{OUT3}	OUT3 to GND1, GND2, AGND	-0.3 to V_{IN3} + 0.3	V
V_{LX}	LX1, LX2 to GND1, GND2, AGND	-0.3 to V_{IN} + 0.3	V
V_{FB}	FB1, FB2, BYP to GND1, GND2, AGND	-0.3 to V_{IN} + 0.3	V
V_{EN}	EN1, EN2, EN3 to GND1, GND2, AGND	-0.3 to 6.0	V
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C

Thermal Information

Symbol	Description	Value	Units
P_D	Maximum Power Dissipation[2]	2.0	W
Θ_{JA}	Thermal Resistance[3]	50	°C/W

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Derate 20mW/°C above 25°C ambient temperature.
3. Mounted on an FR4 board with exposed paddle connected to ground plane.

Electrical Characteristics[1]

V_{P1} = V_{P2} = V_{IN} = V_{IN3} = 3.3V; V_{IN3} = 1.8V, T_A = -40°C to 85°C, unless noted otherwise. Typical values are at T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
General						
V_{IN}	Input Voltage		2.7		5.5	V
V_{UVLO}	UVLO Threshold	V_{P1} Rising			2.7	V
		V_{P1} Hysteresis		140		mV
		V_{P1} Falling	2.1			V
I_Q	Quiescent Current	No load; EN1 = EN2 = EN3 = V_{IN}			300	µA
I_{SHDN}	Shutdown Current	EN1 = EN2 =EN3 = GND			1.0	µA
T_{SD}	Over Temperature Shutdown Threshold			130		°C
T_{HYS}	Over Temperature Shutdown Hysteresis			20		°C
V_{IL}	Enable Threshold Low	For EN1, EN2, and EN3			0.6	V
V_{IH}	Enable Threshold High	For EN1, EN2, and EN3	1.4			V
I_{EN}	Enable Input Current	V_{IN} = V_{P1} = V_{P2} = V_{EN1} = V_{EN2} = V_{EN3} = 5.5V	-1.0		1.0	µA
Channel 1: 1200mA Step-down (Buck) Converter						
V_{P1}	Input Voltage		2.7		5.5	V
V_{OUT1}	Output Voltage Range		0.6		V_{P1}	V
$V_{OUT1(TOL)}$	Output Voltage Tolerance	I_{OUT1} = 0 to 1200mA; V_{P1} = 2.7 to 5.5V	-3.0		3.0	%
V_{FB1}	Feedback Pin Voltage		0.591	0.6	0.609	V
$\Delta V_{LOADREG1}$	Load Regulation	I_{OUT1} = 0 to 1200mA		0.2		%
$\Delta V_{LINEREG1}$	Line Regulation	V_{P1} = 2.7 to 5.5V		0.3		%
I_{Q1}	Quiescent Current	No load; EN1 = V_{IN}; EN2 = EN3 = GND		75		µA
I_{LIM1}	P-Channel Current Limit			1.7		A
$R_{DS(ON)H1}$	High Side Switch On-Resistance			250		mΩ
$R_{DS(ON)L1}$	Low Side Switch On-Resistance			190		mΩ
F_{OSC1}	Oscillator Frequency			1.3		MHz
T_{S1}	Start-Up Time	From Enable to Output Regulation		200		µs

1. The AAT2782 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range and is assured by design, characterization and correlation with statistical process controls.

Electrical Characteristics[1]

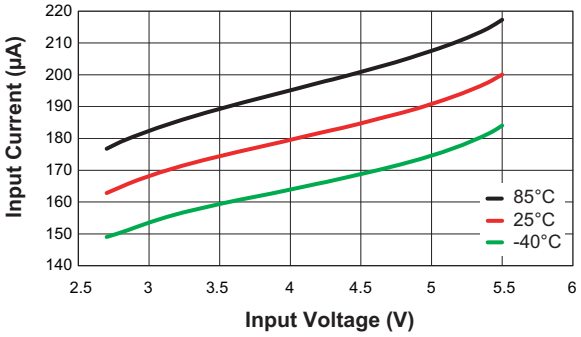
V_{P1} = V_{P2} = V_{IN} = V_{IN3} = 3.3V; V_{IN3} = 1.8V, T_A = -40°C to 85°C, unless noted otherwise. Typical values are at T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Channel 2: 600mA Step-down (Buck) Converter						
V_{P2}	Input Voltage		2.7		5.5	V
V_{OUT2}	Output Voltage Range		0.6		V_{P2}	V
$V_{OUT2(TOL)}$	Output Voltage Tolerance	I_{OUT2}= 0 to 600mA; V_{P1} = 2.7 to 5.5V	-3.0		3.0	%
V_{FB2}	Feedback Pin Voltage		0.591	0.6	0.609	V
$\Delta V_{LOADREG2}$	Load Regulation	I_{OUT2} = 0 to 600mA		0.5		%
$\Delta V_{LINEREG2}$	Line Regulation	V_{P2} = 2.7 to 5.5V		0.3		%
I_{Q2}	Quiescent Current	No Load; EN2 = V_{IN}; EN1 = EN3 = GND		75		µA
I_{LIM2}	P-Channel Current Limit			1.7		A
$R_{DS(ON)H2}$	High Side Switch On-Resistance			250		mΩ
$R_{DS(ON)L2}$	Low Side Switch On-Resistance			190		mΩ
F_{OSC2}	Oscillator Frequency			1.3		MHz
T_{S2}	Start-Up Time	From Enable to Output Regulation		200		µs
Channel 3: 400mA Low Dropout (LDO) Converter						
V_{IN3}	Input Voltage		1.7		V_{IN}	V
V_{DO3}	Dropout Voltage	I_{OUT3} = 150mA; V_{OUT3} > 1.20V		140		mV
		I_{OUT3} = 400mA; V_{OUT3} > 1.20V		300		
V_{OUT3}	LDO Output Voltage Tolerance	V_{IN3} = V_{OUT3} + V_{DO3} to 5.5V; I_{OUT3} = 0mA to 400mA	1.164	1.200	1.236	V
I_{OUT3}	Max Output Current	V_{OUT3} = 1.2V	400			mA
I_{SC}	Short-Circuit Current	V_{OUT3} < 0.4V		1.1		A
I_Q	Quiescent Current	No Load; EN1 = EN2 = GND; EN3 = V_{IN}		85		µA
T_S	Start-Up Time	From Enable to Output Regulation		200		µs
PSRR	Power Supply Rejection Ratio	10Hz, I_{OUT3} = 10mA		85		dB
		3kHz, I_{OUT3} = 10mA		80		dB
		30kHz, I_{OUT3} = 10mA		60		dB
		300kHz, I_{OUT3} = 10mA		55		dB
e_N	Output Noise	BW = 100Hz to 300kHz, C_{BYP} = 10nF, I_{OUT3} = 10mA		65		μV_{RMS}

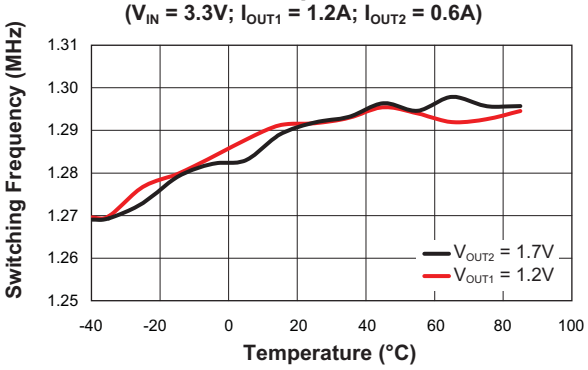
1. The AAT2782 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range and is assured by design, characterization and correlation with statistical process controls.

Typical Characteristics

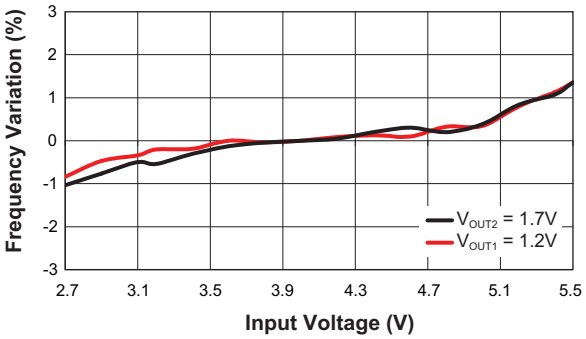
Step-Down Converters and LDO Input Current vs. Input Voltage
(V_{EN1} = V_{EN2} = V_{EN3} = V_{IN})



Step-Down Converter Switching Frequency vs. Temperature
(V_{IN} = 3.3V; I_{OUT1} = 1.2A; I_{OUT2} = 0.6A)

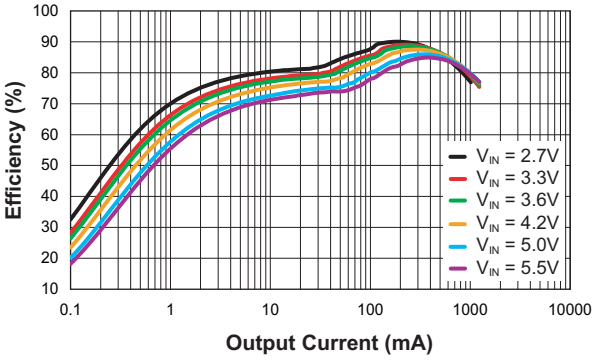


Step-Down Converter Switching Frequency vs. Input Voltage
(I_{OUT1} = 1.2A; I_{OUT2} = 0.6A)

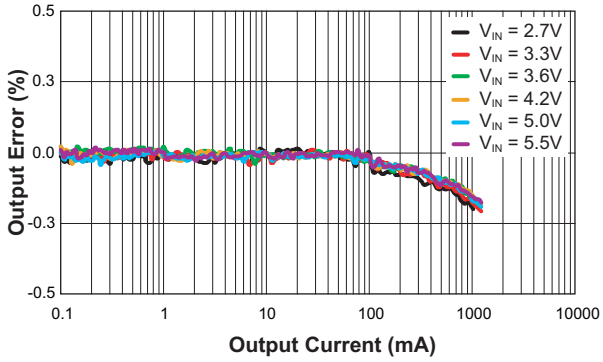


Typical Characteristics—Buck Converter 1

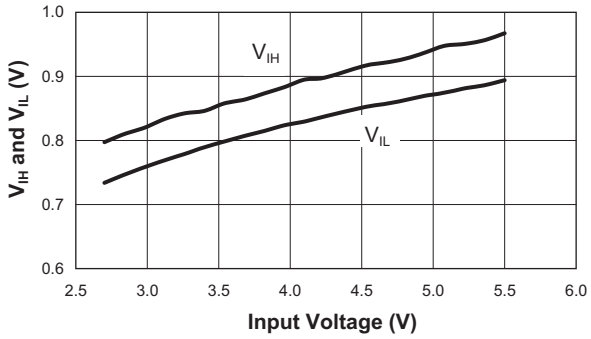
Step-Down Converter 1 Efficiency vs. Load
(V_{OUT1} = 1.2V; V_{IN} = 2.7V to 5.5V; L = 1.7µH)



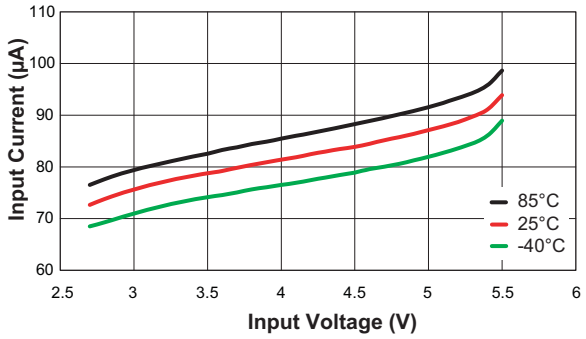
Step-Down Converter 1 DC Regulation
(V_{OUT1} = 1.2V; V_{IN} = 2.7 to 5.5V; L = 1.7µH)



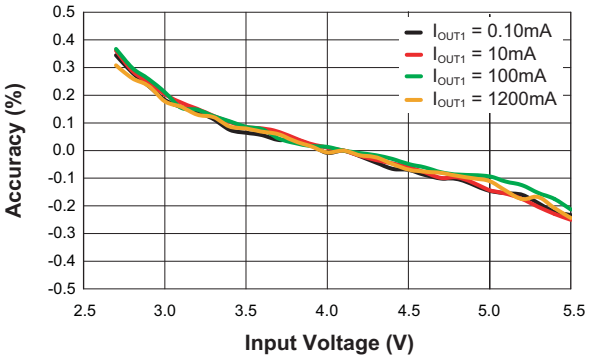
Step-Down Converter 1 V_{IH} and V_{IL} vs. Input Voltage
(V_{EN1} = V_{IN}; V_{EN2} = 0V; V_{EN3} = 0V)



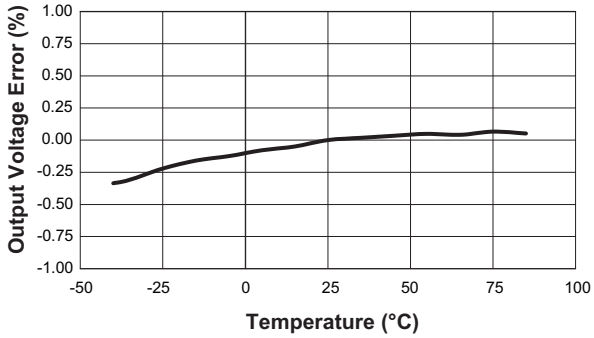
Step-Down Converter 1 Input Current vs. Input Voltage
(V_{EN1} = V_{IN}; V_{EN2} = V_{EN3} = 0V)



Step-Down Converter 1 Line Regulation
(V_{OUT1} = 1.2V; I_{OUT1} = 0.1mA to 1A; L = 1.7µH)

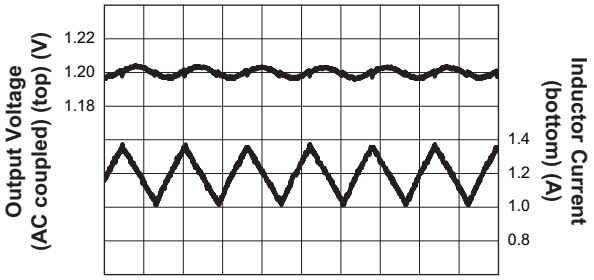


Step-Down Converter Output 1 Voltage Error vs. Temperature
(V_{IN} = 3.3V; V_{OUT1} = 1.2V; I_{OUT1} = 1.2A)

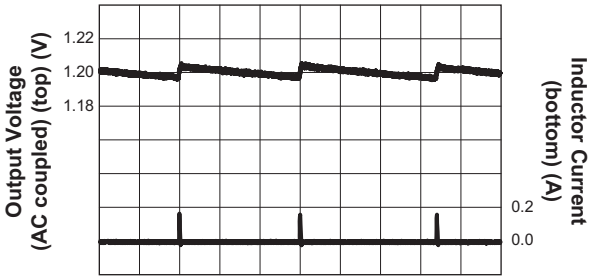


Typical Characteristics—Buck Converter 1

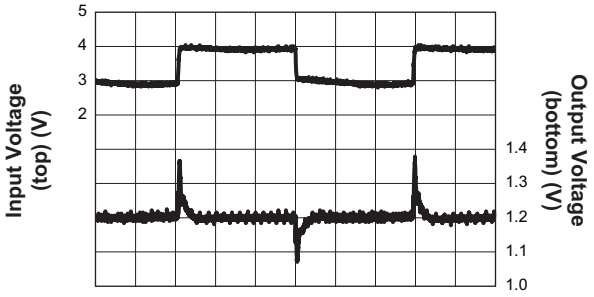
Step-Down Converter 1 Output Ripple
(V_{IN} = 3.3V; V_{OUT1} = 1.2V; I_{OUT1} = 1.2A)



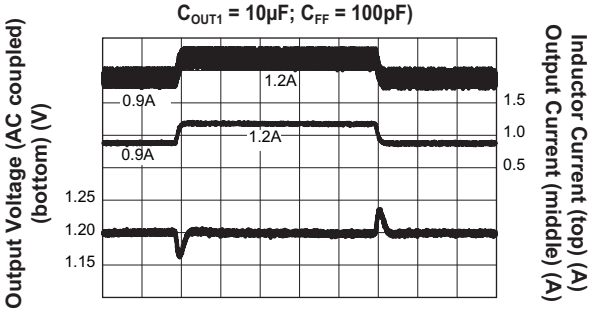
Step-Down Converter 1 Output Ripple
(V_{IN} = 3.3V; V_{OUT1} = 1.2V; I_{OUT1} = 1mA)



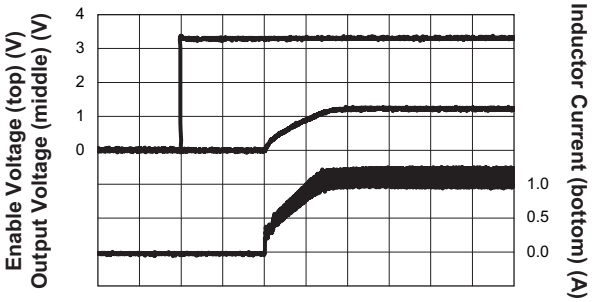
Step-Down Converter 1 Line Transient Response
(V_{IN} = 3V to 4V; V_{OUT1} = 1.2V; I_{OUT1} = 1.2A; C_{OUT} = 10µF)



Step-Down Converter 1 Load Transient Response
(I_{OUT1} = 0.9A to 1.2A; V_{IN} = 3.3V; V_{OUT1} = 1.2V; C_{OUT1} = 10µF; C_{FF} = 100pF)

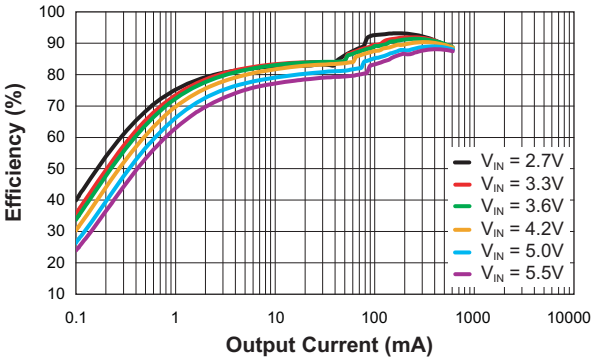


Step-Down Converter 1 Soft Start
(V_{IN} = 3.3V; V_{OUT1} = 1.2V; I_{OUT1} = 1.2A; C_{FF} = 100pF)

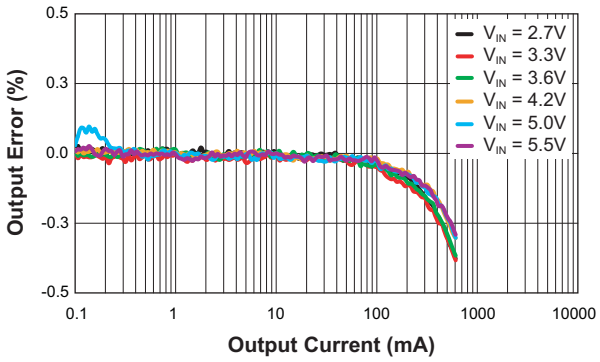


Typical Characteristics—Buck Converter 2

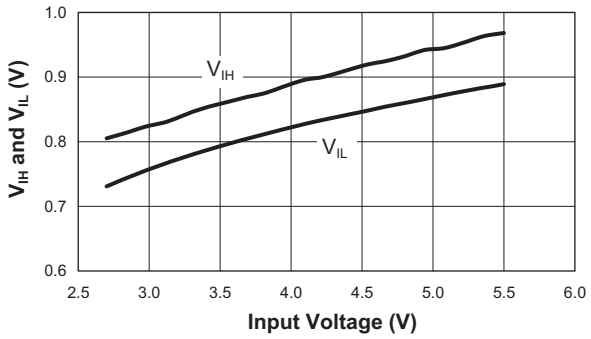
Step-Down Converter 2 Efficiency vs. Load
(V_{OUT2} = 1.7V; V_{IN} = 2.7V to 5.5V; L = 2.2µH)



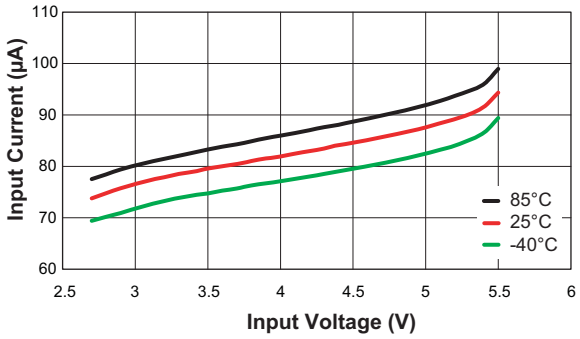
Step-Down Converter 2 DC Regulation
(V_{OUT2} = 1.7V; V_{IN} = 2.7V to 5.5V; L = 2.2µH)



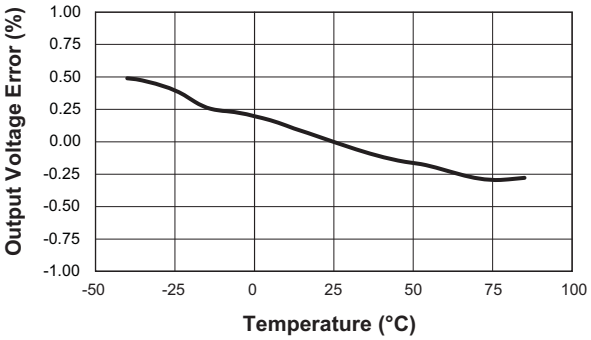
Step-Down Converter 2 V_{IH} and V_{IL} vs. Input Voltage
(V_{EN1} = 0V; V_{EN2} = V_{IN}; V_{EN3} = 0V)



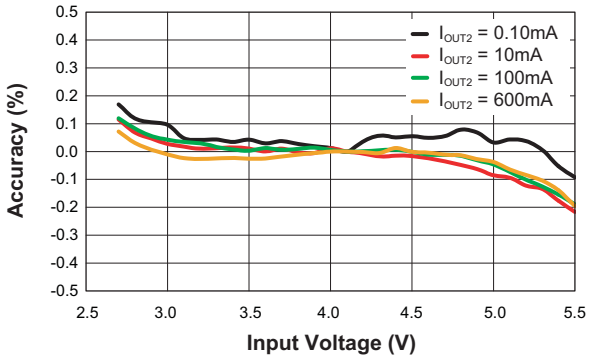
Step-Down Converter 2 Input Current vs. Input Voltage
(V_{EN1} = 0V; V_{EN2} = V_{IN}; V_{EN3} = 0V)



Step-Down Converter Output 2 Voltage Error vs. Temperature
(V_{IN} = 3.3V; V_{OUT2} = 1.7V; I_{OUT2} = 600mA)

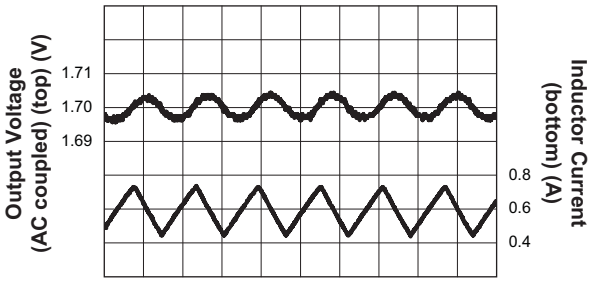


Step-Down Converter 2 Line Regulation
(V_{OUT2} = 1.7V; I_{OUT2} = 0.1mA to 600mA; L = 2.2µH)

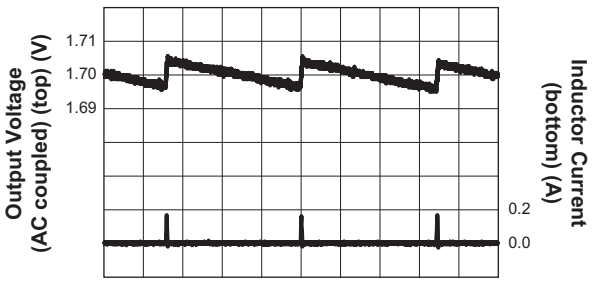


Typical Characteristics—Buck Converter 2

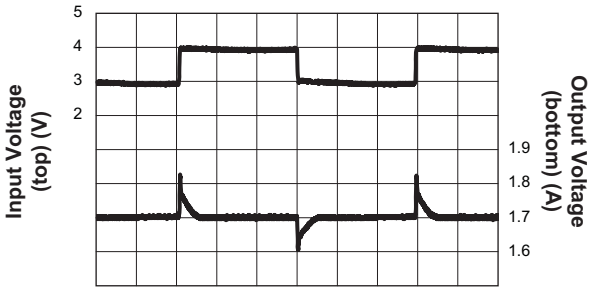
Step-Down Converter 2 Output Ripple
(V_{IN} = 3.3V; V_{OUT2} = 1.7V; I_{OUT2} = 600mA)



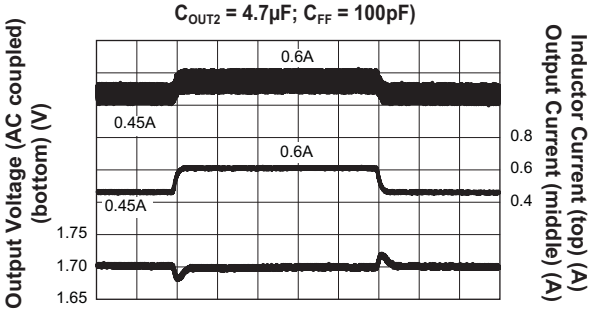
Step-Down Converter 2 Output Ripple
(V_{IN} = 3.3V; V_{OUT2} = 1.7V; I_{OUT2} = 1mA)



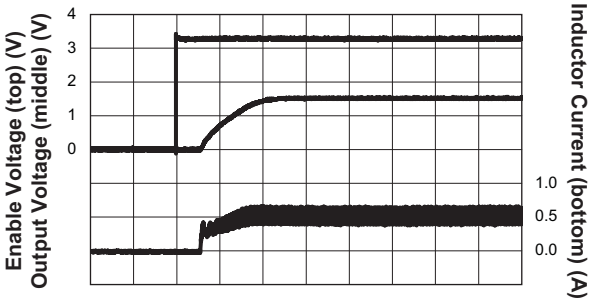
Step-Down Converter 2 Line Transient Response
(V_{IN} = 3V to 4V; V_{OUT2} = 1.7V; I_{OUT2} = 0.6A; C_{OUT2} = 10µF)



Step-Down Converter 2 Load Transient Response
(I_{OUT2} = 0.45A to 0.6A; V_{IN} = 3.3V; V_{OUT2} = 1.7V; C_{OUT2} = 4.7µF; C_{FF} = 100pF)

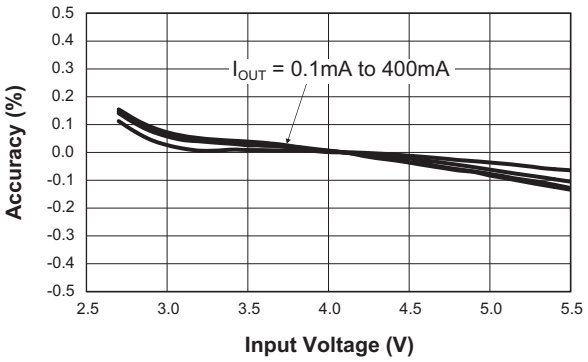


Step-Down Converter 2 Soft Start
(V_{IN} = 3.3V; V_{OUT2} = 1.7V; I_{OUT2} = 600mA; C_{FF} = 100pF)

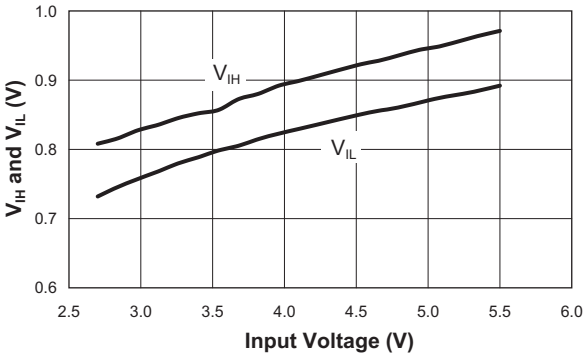


Typical Characteristics—LDO

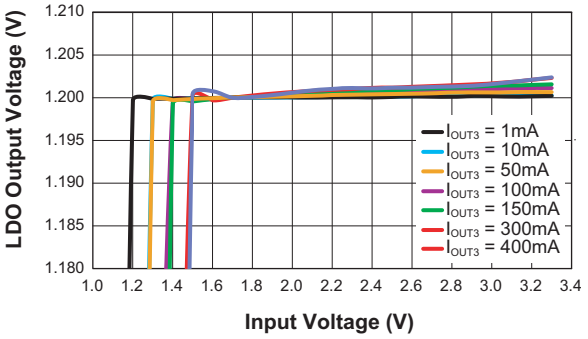
LDO Line Regulation
(V_{IN3} = V_{OUT2} = 1.7V; V_{OUT3} = 1.2V; Vary V_{IN})



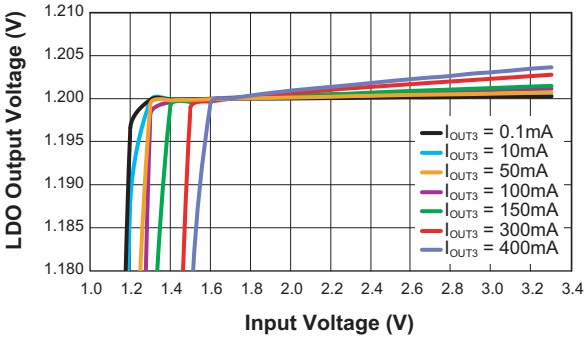
LDO V_{IH} and V_{IL} vs. Input Voltage
(V_{EN1} = 0V; V_{EN2} = V_{EN3} = V_{IN})



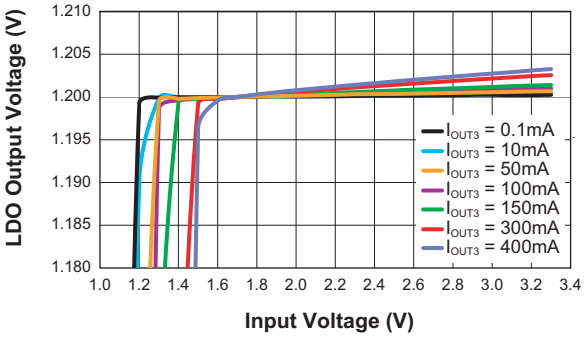
LDO Dropout Characteristics
(V_{IN} = 3.3V; Vary V_{IN3} from 3.3V to 1V; V_{OUT3} = 1.2V;
I_{OUT3} = 0.1mA to 400mA; -40°C)



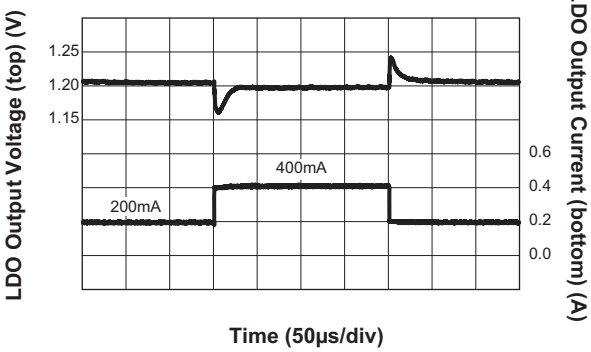
LDO Dropout Characteristics
(V_{IN} = 3.3V; V_{IN3} = 3.3V to 1V; V_{OUT3} = 1.2V;
I_{OUT3} = 0.1mA to 400mA; 85°C)



LDO Dropout Characteristics
(V_{IN} = 3.3V; V_{IN3} = 3.3V to 1V; V_{OUT3} = 1.2V;
I_{OUT3} = 0.1mA to 400mA; 25°C)

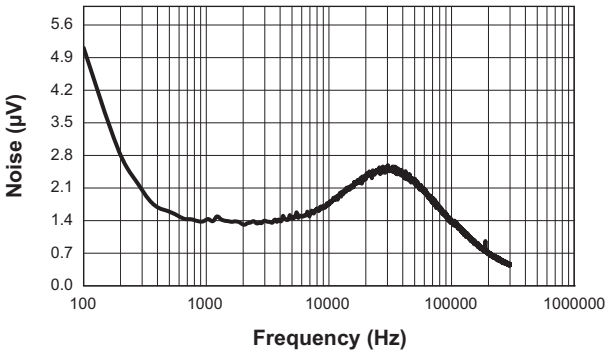


LDO Load Transient Response
(200mA to 400A; V_{IN} = 3.3V; V_{IN3} = V_{OUT2} = 1.7V)

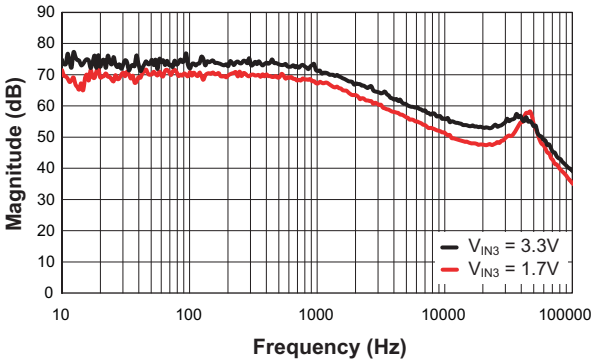


Typical Characteristics—LDO

LDO Output Voltage Noise
(I_{OUT3} = 10mA; Power BW: 100~300KHz)

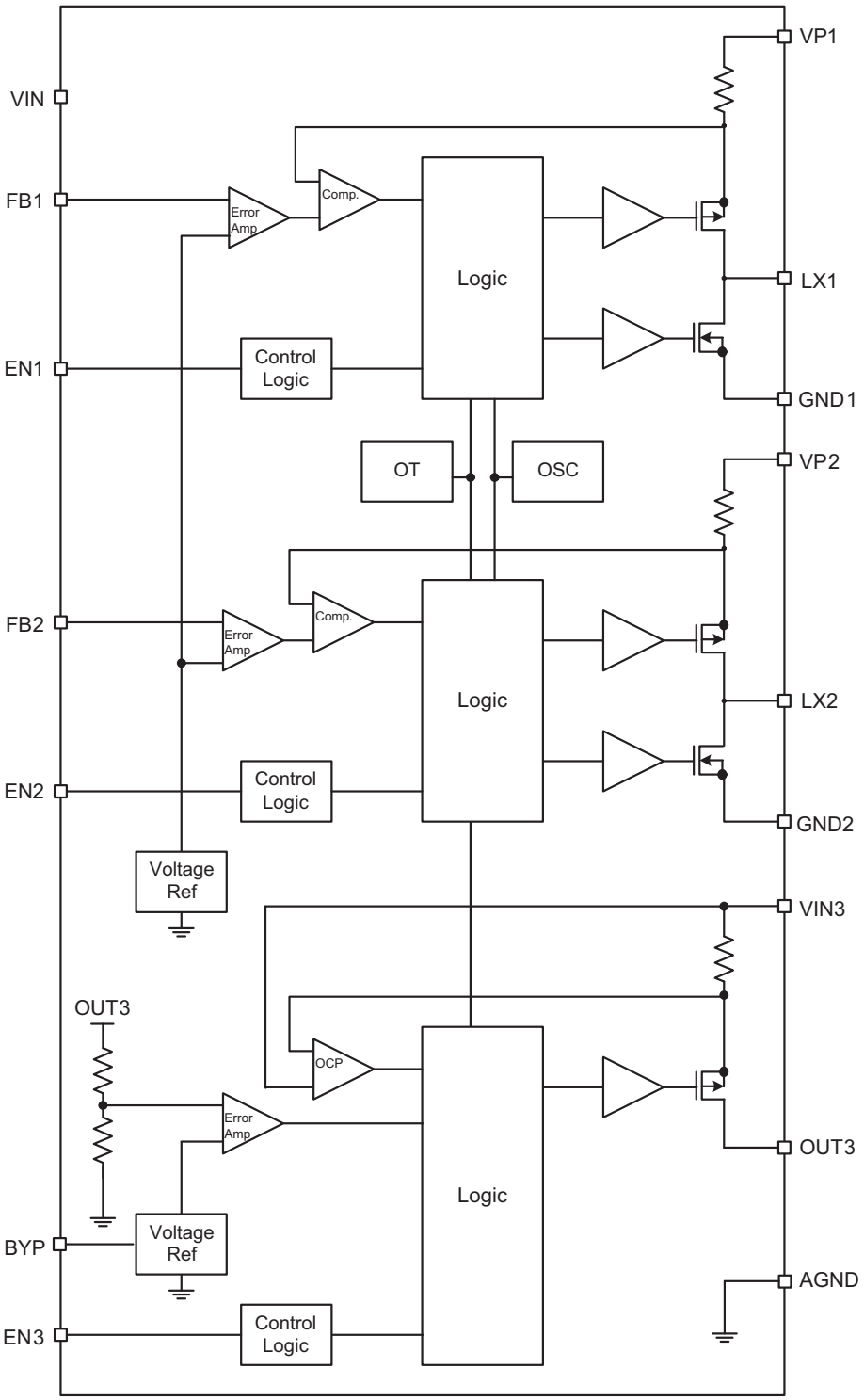


LDO Power Supply Rejection Ratio, PSRR
(I_{OUT3} = 10mA; BW: 100~300KHz)



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Functional Block Diagram



Functional Description

The AAT2782 is a 3-channel high performance power management IC. Channel 1 is a 1200mA step-down converter. Channel 2 is a 600mA step-down converter. Channel 3 is a 400mA LDO regulator with low-input voltage capability and low output noise for sensitive analog applications.

The low input voltage capability of the LDO regulator allows the step-down converter to be tied directly to the LDO input. This configuration provides the efficiency benefits of a switching converter plus the low noise benefits of a LDO (low drop-out) regulator.

Channel 1 and 2: 1200/600mA Step-Down (Buck) Converters

The AAT2782 Channel 1 and 2 step-down converters are peak current mode PWM converters operating at 1.3MHz frequency. The input voltage range is 2.7V to 5.5V. The output voltage range is 0.6V to V_{IN} and is adjustable with an external resistor divider. The converters provide internal compensation. Power devices are sized for 1A output current while maintaining over 85% efficiency at full load. Peak efficiency is above 95%. Light load efficiency is maintained at greater than 80% down to 85% of full load current. Channel 2 has excellent transient response and load and line regulation. Transient response time is typically less than 20µs.

The enable inputs, when pulled low, force the converter into a low power non-switching state consuming less than 1µA of current.

For overload conditions, the peak input current is limited. Also, thermal protection completely disables switching if internal dissipation becomes excessive, thus protecting the device from damage. The junction over-temperature threshold is 130°C with 20°C of hysteresis. Under-voltage lockout (UVLO) guarantees sufficient V_{IN} bias and proper operation of all internal circuits prior to activation.

Control Loop

The AAT2782 is a peak current mode step-down converter. The current through the P-channel MOSFET (high side) is sensed for current loop control, as well as short-circuit and overload protection. A fixed slope compensation signal is added to the sensed current to maintain stability for duty cycles greater than 50%. The peak current mode loop appears as a voltage-programmed current source in parallel with the output capacitor. The output of the voltage error amplifier programs the current mode loop for the necessary peak switch current to force a constant output voltage for all load and line conditions. Internal loop compensation terminates the transconductance voltage error amplifier output. The reference voltage is internally set to program the converter output voltage greater than or equal to 0.6V.

Soft Start/Enable

Soft start limits the current surge seen at the input and eliminates output voltage overshoot. When pulled low, the enable input forces the AAT2782 into a low-power, non-switching state. The total input current during shutdown is less than 1µA.

Low Dropout Operation

For conditions where the input voltage drops to the output voltage level, the converter duty cycle increases to 100%. As the converter approaches the 100% duty cycle, the minimum off-time initially forces the high side on-time to exceed the 1.3MHz clock cycle and reduces the effective switching frequency. Once the input drops below the level where the converter can regulate the output, the high side P-channel MOSFET is enabled continuously for 100% duty cycle. At 100% duty cycle the output voltage tracks the input voltage minus the I*R drop of the high side P-channel MOSFET.

Current Limit and Over-Temperature Protection

For overload conditions, the peak input current is limited. To minimize power dissipation and stresses under current limit and short-circuit conditions, switching is terminated after entering current limit for a series of pulses. Switching is terminated for seven consecutive clock cycles after a current limit has been sensed for a series of four consecutive clock cycles. Thermal protection completely disables switching when internal dissipation becomes excessive. The junction over-temperature threshold is 130°C with 20°C of hysteresis. Once an over-temperature or over-current fault conditions is removed, the output voltage automatically recovers.

Under-Voltage Lockout

Internal bias of all circuits is controlled via the VIN input. Under-voltage lockout (UVLO) guarantees sufficient V_{IN} bias and proper operation of all internal circuitry prior to activation.

Component Selection

Inductor Selection—Channel 1

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. The inductor should be set equal to the output voltage numeric value in µH. This guarantees that there is sufficient internal slope compensation. Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor. For Channel 1, the 1.5µH LQH32PN1R5NN0L series Murata inductor has a 57mΩ worst case DCR and a 1.75A DC current rating. At full 1.2A load, the inductor DC loss is 128mW which gives 9% loss in efficiency for a 1.2A, 1.2V output.

Inductor Selection—Channel 2

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. The internal slope compensation for the adjustable and low voltage fixed versions of the AAT2782 is 0.6A/µs. This equates to a slope compensation that is 75% of the inductor current down slope for a 1.8V output and 2.2µH inductor.

$$m = \frac{0.75 \cdot V_O}{L} = \frac{0.75 \cdot 1.8V}{2.2\mu H} = 0.6\frac{A}{\mu s}$$

$$L = \frac{0.75 \cdot V_O}{m} = \frac{0.75 \cdot V_O}{0.6\frac{A}{\mu s}} \quad 1.2\frac{\mu s}{A} \cdot V_O$$

$$= 1.2\frac{\mu s}{A}\,1.7V = 2.0\mu H$$

In this case a standard 2.2µH value is selected. Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the inductor's saturation characteristics. The inductor should not show any appreciable saturation under all normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

For Channel 2, the 2.2µH NLCV32T-2R2M series TDK inductor has a 130mΩ worst case DCR and a 770mA DC current rating. At full 600mA load, the inductor DC loss is 47mW which gives less than 3% loss in efficiency for a 600mA, 3.3V output.

Input Capacitor

Select a 10µF to 22µF X7R or X5R ceramic capacitor for the VP1 and VP2 inputs. To estimate the required input capacitor size, determine the acceptable input ripple level (V_{PP}) and solve for C. The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\frac{V_{PP}}{I_O} - ESR \cdot F_{OSC}}$$

$$\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1}{4} \text{ for } V_{IN} = 2 \cdot V_O$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_{OSC}}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10µF, 6.3V, X5R ceramic capacitor with 5.0V DC applied is actually about 6µF. The maximum input capacitor RMS current is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current.

$$\sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)} = \sqrt{D \cdot (1 - D)} = \sqrt{0.5^2} = \frac{1}{2}$$

for $V_{IN} = 2 \cdot V_O$

$$I_{RMS(MAX)} = \frac{I_O}{2}$$

The term $\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)$ appears in both the input voltage ripple and input capacitor RMS current equations and is a maximum when V_O is twice V_{IN}. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle. The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT2782. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple. The proper placement of the input capacitor (C1) can be seen in the evaluation board layout in the Layout section of this datasheet (see Figure 2). A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result. Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem. In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR/ESL bypass ceramic capacitor. This dampens the high Q network and stabilizes the system.

Output Capacitor—Channel 1

The output capacitor limits the output ripple and provides holdup during large load transitions. A 10µF to 22µF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple. The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within two or three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_{OSC}}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients. The internal voltage loop compensation also limits the minimum output capacitor value to 10µF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

Output Capacitor—Channel 2

The output capacitor limits the output ripple and limits droop during large load transitions. A 4.7µF to 10µF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple.

Adjustable Output Resistor Selection

The output voltages on the two AAT2782 buck converters are programmed with external feedback resistors R3, R5 and R2, R4. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R2, R4 is 59kΩ. Although a larger value will further

reduce quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Table 1 summarizes the resistor values for various output voltages with R2, R4 set to either 59kΩ for good noise immunity or 221kΩ for reduced no load input current.

$$V_{OUT} = 0.6V \cdot \left(1 + \frac{R3, R5}{R2, R4}\right)$$

V_{OUT} (V)	R2, R4 = 59kΩ R3, R5 (kΩ)	R2, R4 = 221kΩ R3, R5 (kΩ)
0.8	19.6	75
0.9	29.4	113
1.0	39.2	150
1.1	49.9	187
1.2	59.0	221
1.3	68.1	261
1.4	78.7	301
1.5	88.7	332
1.8	118	442
1.85	124	464
2.0	137	523
2.5	187	715
3.3	267	1000

Table 1: AAT2782 Resistor Values for Various Output Voltages.

Channel 3: 400mA Low Dropout (LDO) Converter

The Channel 3 LDO converter can operate independently or can be used to post-regulate one of the step-down buck converters and provide a quiet output voltage. The input voltage can be as low as 1.7V for an output voltage of 1.2V; 2.5V, 2.8V, and 3.3V versions are also available. The output current is 400mA. If the channel 2 buck converter efficiency at full load is 85% and the LDO efficiency is 70%, the combined post-regulated efficiency would be ~60%. If the LDO is used to post-regulate from a buck, then EN3 should be brought high after the buck comes into regulation.

Component Selection

Input Capacitor

Typically, a 10µF or larger capacitor is required for C_{IN} in most applications and capacitance value of greater than or equal to the value of the output capacitor is recommended. A C_{IN} capacitor is required for basic LDO regulator operation. If the AAT2782 is physically located more than three centimeters from an input power source, a C_{IN} capacitor will be needed for stable operation. C_{IN} should be located as closely to the device VIN3 pin as practically possible. C_{IN} values greater than 10µF will offer superior input line transient response and will assist in maximizing the highest possible power supply ripple rejection. Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{IN}. There is no specific capacitor ESR requirement for C_{IN}. However, for 400mA LDO regulator output operation, ceramic capacitors are recommended for C_{IN} due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices. Care should also be taken when choosing the voltage rating for the capacitors. A 6.3V rated capacitor should not be used to bypass a 5V input. In such cases, a 10V rated capacitor should be used.

Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required between pins VOUT3 and GND. The C_{OUT3} capacitor connection to the LDO regulator ground pin should be made as direct as practically possible for maximum device performance. The AAT2782 has been specifically designed to function with very low ESR ceramic capacitors. For best performance, ceramic capacitors are recommended. Typical output capacitor values for maximum output current conditions range from 4.7µF to 10µF. Applications utilizing the exceptionally low output noise and optimum power supply ripple rejection characteristics of the AAT2782 should use 10µF or greater for C_{OUT3}. If desired, C_{OUT3} may be increased without limit.

Thermal Calculations

There are three types of losses associated with the AAT2782 step-down converters: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the losses for each step-down is given by:

$$P_{TOTAL(Step\text{-}down)} = \frac{I_O^2 \cdot (R_{DS(ON)H} \cdot V_O + R_{DS(ON)L} \cdot [V_{IN} - V_O])}{V_{IN}}$$

$$+ [(t_{sw} \cdot F_{OSC} \cdot I_{OUT} + I_Q) \cdot V_{IN}]$$

I_Q is the step-down converter quiescent current. The term t_{sw} is used to estimate the full load step-down converter switching losses. For the condition where the step-down converter is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_{TOTAL(Step\text{-}down)} = I_O^2 \cdot R_{DSON(H)} + I_Q \cdot V_{IN}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

The AAT2782 LDO is designed to deliver a continuous output load current up to 400mA under normal operating conditions. The limiting characteristic for the maximum output load safe operating area is essentially package power dissipation and the internal preset thermal limit of the device. In order to obtain high operating currents, careful device layout and circuit operating conditions must be taken into account.

This calculation accounts for the total power dissipation of the LDO regulator, including that caused by ground current.

$$P_{TOTAL(LDO)} = (V_{IN3} - V_{OUT3})I_{OUT3} + (V_{IN3} - I_{Q3})$$

Add the total losses of the two step-down converters and the LDO to determine the max junctions temperature. The maximum junction temperature can be derived from the Θ_{JA} for the TDFN34-16 which is 50°C/W.

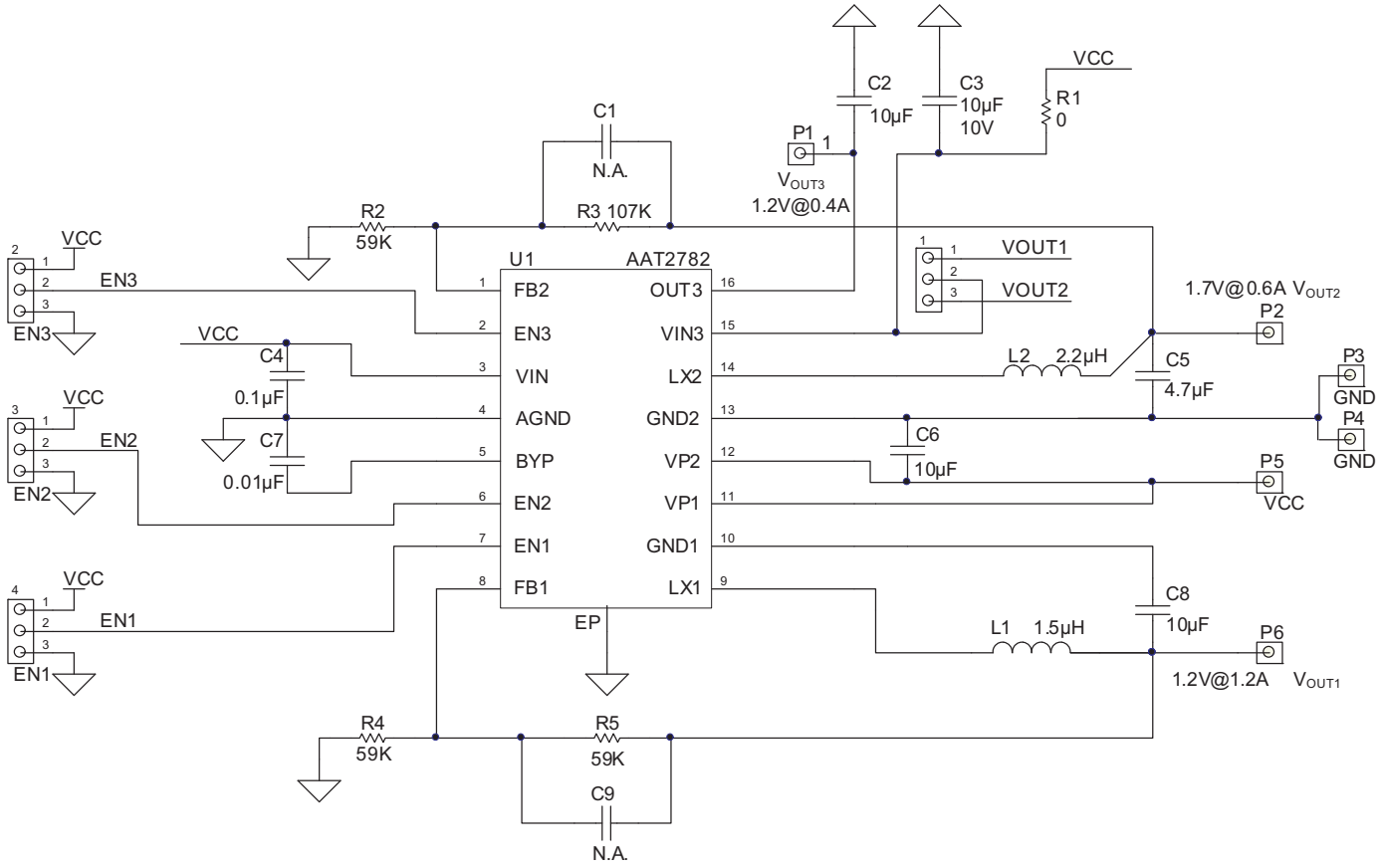
$$T_{J(MAX)} = P_{TOTAL} \cdot \Theta_{JA} + T_{AMB}$$

Layout

The suggested PCB layout for the AAT2782 is shown in Figures 2 and 3. The following guidelines should be used to help ensure a proper layout.

1. The power input capacitors (C6) should be connected as closely as possible to VP1 and VP2, The LDO input capacitor (C3) should be close to VIN3 as shown in Figure 2. Due to the pin placement of VP1, VP2 and VIN3 for all converters, proper decoupling is not possible with just one input capacitor.
2. C4 is a bypass capacitor for the VIN supply pin for the device.
3. C8 and L1, C5 and L2 should be connected as closely as possible. The connection of L1 and L2 to the LX1 and LX2 pins should be as short as possible.
4. The feedback trace or FB pin should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation.
5. The resistance of the trace from the load returns to GND1, GND2, and AGND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
6. Connect unused signal pins to ground to avoid unwanted noise coupling.
7. For good thermal coupling, PCB vias are required from the pad for the TDFN paddle to the ground plane. The via diameter should be 0.3mm to 0.33mm and positioned on a 1.2mm grid.

AAT2782 Schematic



Symbol	Part Number	Description	Quantity
U1	AAT2782	Skyworks AAT2782 Two Buck, One LDO 3x4 TDFN	1
L2	NLCV32T-2R2M	TDK 2.2µH Chip Inductor, I_{SAT} = 770mA, 3.2x2.5x2.2mm	1
	744028002	Wurth 2.2µH Inductor, I_{SAT} = 1A, 2.8x2.8x1.1mm	
	LQM2HPN2R2MG0	Murata 2.2µH Inductor, I_{SAT} = 1.3A, 2.5x2.0x0.9mm	
L1	LQH32PN1R5NN0L	Murata 1.5µH Inductor, I_{SAT} = 1.75A, 3.2x2.5x1.7mm	1
C2, C6, C8		Generic, MLC, 0603, 10µF/6.3V Cap	3
C3		Generic, MLC, 0603, 10µF/10V Cap	1
C5		Generic, MLC, 0603, 4.7µF/6.3V Cap	1
C9		Generic, MLC, 0402, 56pF/50V	1
R2-R6		Generic, 0402 Resistors	6

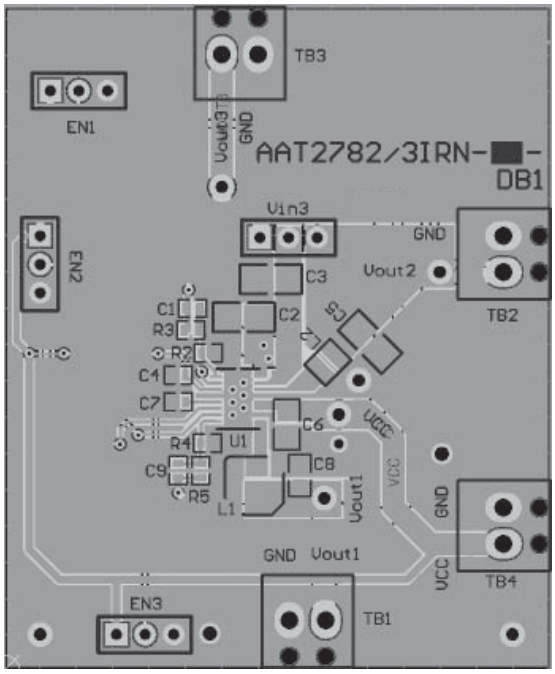


Figure 2: AAT2782 Evaluation Board Component Side Layout.

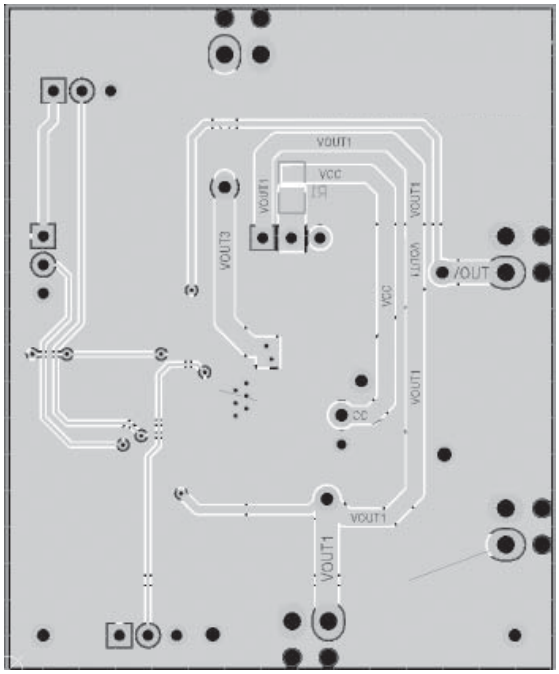


Figure 3: AAT2782 Evaluation Board Solder Side Layout.

Ordering Information

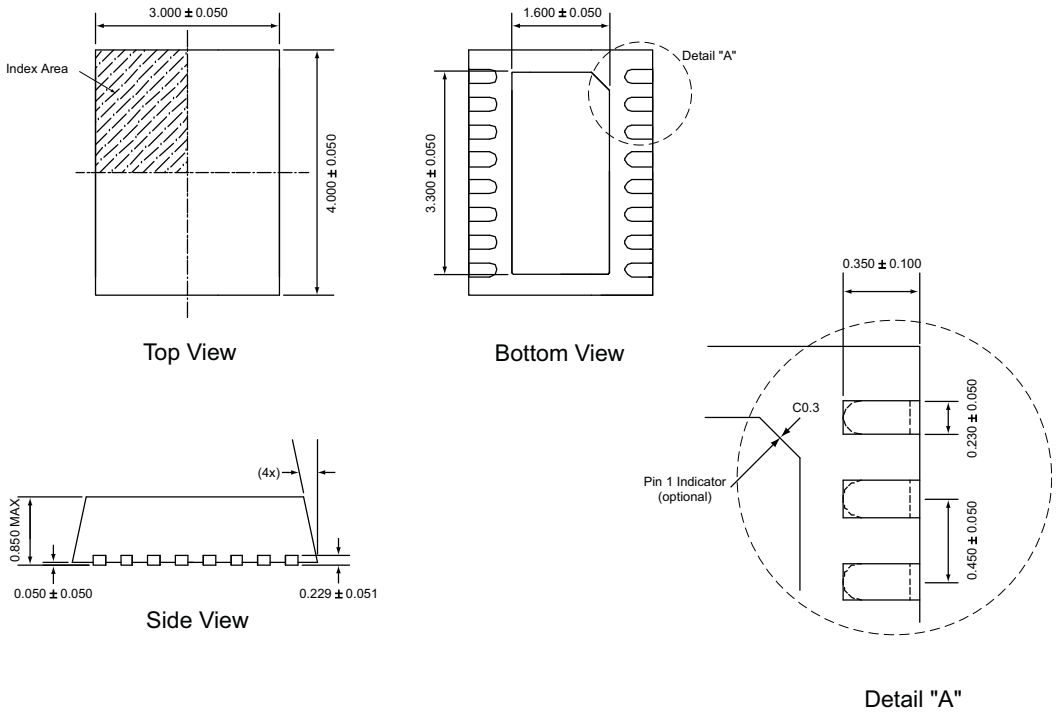
Package	Voltage			Marking[1]	Part Number (Tape and Reel)[2]
	Channel 1	Channel 2	Channel 3		
TDFN34-16	0.6	0.6	1.2	3ZXYY	**AAT2782IRN-AAE-T1**

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

Legend	
Voltage	**Code**
Adjustable (0.6)	A
1.2	E

Package Information

TDFN34-16



All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.
3. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

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