

TPS745-Q1 500-mA LDO With Power-Good in Small Wettable Flank WSON Packages

1 Features

- AEC-Q100 qualified for automotive applications:
 - Temperature grade 1: -40°C to $+125^{\circ}\text{C}$, T_A
- Device junction temperature: -40°C to 150°C
- Package:
 - 2-mm \times 2-mm wettable flank WSON
 - 3-mm \times 3-mm wettable flank WSON (preview)
- Input voltage range: 1.5 V to 6.0 V
- Output voltage range:
 - Fixed option: 0.65 V to 5.0 V
 - Adjustable option: 0.55 V to 5.5 V
- High PSRR: 45 dB at 100 kHz
- Output accuracy: $\pm 0.85\%$ (25°C), $\pm 1.5\%$ maximum
- Power-good output options:
 - Open-drain and push-pull
- Ultra-low dropout:
 - 160 mV (max) at 500 mA ($3.3 V_{OUT}$)
- Stable with a 1- μF or larger capacitor
- Low I_Q : 25 μA (typical), 1.5 μA (shutdown)
- Active output discharge
- Low thermal resistance:
 - DRV (6-pin WSON), $R_{\theta JA} = 80.3^{\circ}\text{C/W}$
 - DRB (8-pin WSON), $R_{\theta JA} = 62.0^{\circ}\text{C/W}$ (preview)

2 Applications

- Automotive head units
- Front and rear cameras
- Automotive cluster displays
- Telematics control units
- Medium, short range radar

3 Description

The TPS745-Q1 is a 500-mA ultra-low-dropout regulator (LDO) with power-good functionality. This device is available in a small 6-pin, 2-mm \times 2-mm and a small 8-pin, 3-mm \times 3-mm WSON package with wettable flanks to facilitate optical inspection. The TPS745-Q1 consumes low quiescent current and provides fast line and load transient performance.

The TPS745-Q1 is a flexible device for post-regulation by supporting an input voltage range from 1.5 V to 6.0 V and an externally adjustable output range of 0.55 V to 5.5 V. The device also features fixed output voltages for powering common voltage rails.

The TPS745-Q1 has a power-good (PG) output that monitors the voltage at the feedback pin to indicate the status of the output voltage. The EN input and PG output can be used for sequencing multiple power supplies in the system.

The TPS745-Q1 is stable with small ceramic output capacitors, allowing for a small overall solution size. A precision band-gap and error amplifier provides high accuracy of $\pm 0.85\%$ (max) at 25°C and $\pm 1.5\%$ (max) over temperature. This device includes integrated thermal shutdown, current limit, and undervoltage lockout (UVLO) features. The TPS745-Q1 has an internal foldback current limit that helps reduce the thermal dissipation during short-circuit events.

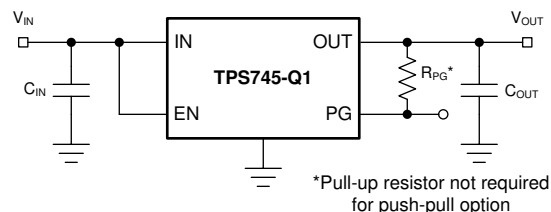
Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS745-Q1	Wettable flank WSON (6)	2.00 mm \times 2.00 mm
	Wettable flank WSON (8) ⁽²⁾	3.00 mm \times 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Preview package.

Typical Application: Fixed Voltage Version



Typical Application: Adjustable Voltage Version

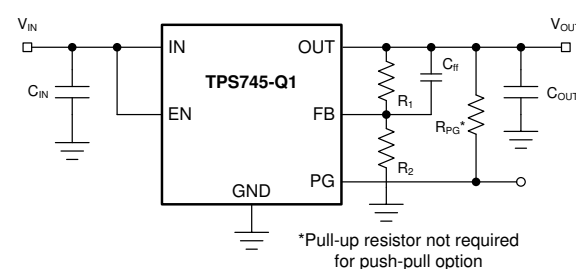


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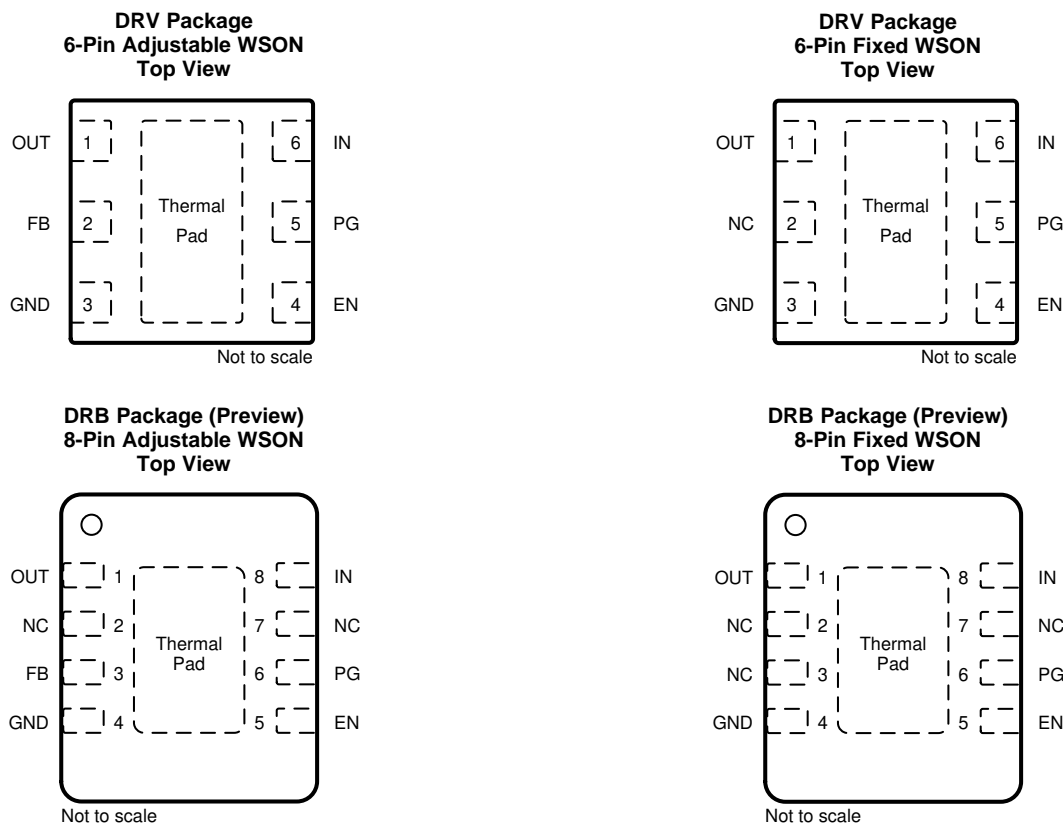
4 Revision History

Changes from Original (June 2019) to Revision A

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• Changed document status from advance information to production data.....	1
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5 Pin Configuration and Functions



Pin Functions

NAME	PIN				I/O	DESCRIPTION
	DRV (Fixed)	DRV (Adjust)	DRB (Fixed)	DRB (Adjust)		
EN	4	4	5	5	Input	Enable pin. Drive EN greater than $V_{EN(HI)}$ to turn on the regulator. Drive EN less than $V_{EN(LO)}$ to put the low-dropout regulator (LDO) into shutdown mode.
FB	—	2	—	3	—	This pin is used as an input to the control loop error amplifier and is used to set the output voltage of the LDO.
GND	3	3	4	4	—	Ground pin.
IN	6	6	8	8	Input	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the Recommended Operating Conditions table and the Input and Output Capacitor Selection section. Place the input capacitor as close to the output of the device as possible.
NC	2	—	2, 3, 7	2, 7	—	No internal connection. Ground this pin for better thermal performance.
OUT	1	1	1	1	Output	Regulated output voltage pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; see the Recommended Operating Conditions table and the Input and Output Capacitor Selection section. Place the output capacitor as close to output of the device as possible.
PG	5	5	6	6	Output	Power-good output. Available in open-drain and push-pull topologies. A pullup resistor is only required for the open-drain type. For the open-drain version, if the power-good functionality is not being used, ground this pin or leave floating. For the push-pull version, if the power-good functionality is not being used, leave this pin floating.

Pin Functions (continued)

PIN					I/O	DESCRIPTION
NAME	DRV (Fixed)	DRV (Adjust)	DRB (Fixed)	DRB (Adjust)		
Thermal Pad					—	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage	Supply, V_{IN}	−0.3	6.5	V
	Enable, V_{EN}	−0.3	6.5	
	Feedback, V_{FB}	−0.3	2.0	
	Power-good, V_{PG}	−0.3	6.5	
	Output, V_{OUT}	−0.3	$V_{IN} + 0.3^{(2)}$	
Current	Output, I_{OUT}	Internally limited		
	Power-good, I_{PG}		±10	mA
Temperature	Operating junction, T_J	−40	150	°C
	Storage, T_{stg}	−65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The absolute maximum rating is $V_{IN} + 0.3$ V or 6.0 V, whichever is smaller.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000
		Charged-device model (CDM), per AEC Q100-011, corner pins	±750
		Charged-device model (CDM), per AEC Q100-011, other pins	±500

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.5		6.0	V
V_{OUT}	Output voltage	Adjustable only		5.5	V
		Fixed only	0.65	5.0	
I_{OUT}	Output current	0		500	mA
C_{IN}	Input capacitor	1			μF
C_{OUT}	Output capacitor ⁽¹⁾	1		220	μF
C_{FF}	Feed-forward capacitor		10		nF
V_{EN}	Enable voltage	0		6.0	V
f_{EN}	Enable toggle frequency			10	kHz
V_{PG}	PG voltage	0		6.0	V
T_J	Junction operating temperature	−40		150	°C

- (1) Minimum derated capacitance of 0.47 μF is required for stability.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS745-Q1		UNIT
		DRV (WSON)	DRB (WSON) ⁽²⁾	
		6 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	80.3	62.0	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	98.7	73.1	°C/W
R _{θJB}	Junction-to-board thermal resistance	44.8	35.1	°C/W
ψ _{JT}	Junction-to-top characterization parameter	6.1	6.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	45.0	35.1	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	20.8	18.2	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) Preview package.

6.5 Electrical Characteristics

at operating temperature range ($T_J = -40^\circ\text{C}$ to $+150^\circ\text{C}$), $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 1.5 V (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$, unless otherwise noted. All typical values are at $T_J = 25^\circ\text{C}$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V _{FB}	Feedback voltage	Adjustable only	0.55		V	
Output accuracy ⁽¹⁾	T _J = 25°C	-40°C ≤ T _J ≤ 85°C	-0.85%	0.85%		
		-40°C ≤ T _J ≤ 150°C	-1.00%	1.00%		
		-40°C ≤ T _J ≤ 150°C	-1.50%	1.50%		
Line regulation	V _{OUT(NOM)} + 0.5 V ⁽²⁾ ≤ V _{IN} ≤ 6.0 V		2	7.5	mV	
Load regulation	0.1 mA ≤ I _{OUT} ≤ 500 mA, V _{IN} ≥ 2.0 V		0.030		V/A	
I _{GND}	Ground current	I _{OUT} = 0 mA	T _J = 25°C	25	32	μA
			-40°C ≤ T _J ≤ 150°C	25	36	
I _{SHDN}	Shutdown current	V _{EN} ≤ 0.3 V, 1.5 V ≤ V _{IN} ≤ 6.0 V	-40°C ≤ T _J ≤ 125°C	0.1	1	μA
			-40°C ≤ T _J ≤ 150°C	0.1	1.55	
I _{FB}	Feedback Pin Current	Adjustable only	0.01	0.1	μA	
I _{CL}	Output current limit	V _{OUT(NOM)} < 1.0 V, V _{OUT} = V _{OUT(NOM)} - 0.2 V, V _{IN} = 2.0 V	515	720	865	mA
		V _{OUT(NOM)} ≥ 1.0 V, V _{OUT} = V _{OUT(NOM)} × 0.85, V _{IN} = V _{OUT(NOM)} + 1.0 V				
I _{SC}	Short-circuit current limit	V _{OUT} = 0 V	V _{OUT(NOM)} < 1.0 V, V _{IN} = 2.0 V	350	400	mA
			V _{OUT(NOM)} ≥ 1.0 V, V _{IN} = V _{OUT(NOM)} + 1.0 V			
V _{DO}	Dropout voltage	I _{OUT} = 500 mA, V _{OUT} = 0.95 × V _{OUT(NOM)}	0.65 V ≤ V _{OUT} < 0.8 V ⁽³⁾	720	910	mV
			0.8 V ≤ V _{OUT} < 1.0 V	585	780	
			1.0 V ≤ V _{OUT} < 1.2 V	420	600	
			1.2 V ≤ V _{OUT} < 1.5 V	285	430	
			1.5 V ≤ V _{OUT} < 1.8 V	180	265	
			1.8 V ≤ V _{OUT} < 2.5 V	140	215	
			2.5 V ≤ V _{OUT} < 3.3 V	105	170	
			3.3 V ≤ V _{OUT} < 5.5 V	95	160	
PSRR	Power-supply rejection ratio	V _{OUT} = 1.8 V, V _{IN} = 2.8 V, I _{OUT} = 500 mA, C _{OUT} = 2.2 μF	f = 1 kHz	57	dB	
			f = 100 kHz	42		
			f = 1 MHz	35		
V _N	Output noise voltage	BW = 10 Hz to 100 kHz, V _{OUT} = 0.9 V, V _{IN} = 1.9 V	53		μV _{RMS}	
V _{UVLO}	Undervoltage lockout	V _{IN} falling	1.17	1.30	1.42	V
		V _{IN} rising	1.21	1.34	1.47	

(1) When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.

(2) V_{IN} = 1.5 V for V_{OUT} < 1.0 V.

(3) Dropout is not tested for nominal output voltages below 0.65 V since the input voltage may be below UVLO.

Electrical Characteristics (continued)

at operating temperature range ($T_J = -40^\circ\text{C}$ to $+150^\circ\text{C}$), $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 1.5 V (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1\ \mu\text{F}$, unless otherwise noted. All typical values are at $T_J = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{UVLO,HYST}$	Undervoltage lockout hysteresis	V_{IN} hysteresis		40		mV
t_{STR}	Startup time	From EN low-to-high transition to $V_{OUT} = V_{OUT(NOM)} \times 0.95$		500	650	μs
$V_{EN(HI)}$	EN pin high voltage (enabled)		1.0			V
$V_{EN(LO)}$	EN pin low voltage (disabled)				0.3	V
I_{EN}	Enable pin current	$V_{IN} = V_{EN} = 6.0\text{ V}$		10		nA
$R_{PULLDOWN}$	Pulldown resistance	$V_{IN} = 6.0\text{ V}$		95		Ω
PG_{HTH}	PG high threshold	V_{OUT} increasing	89	92	96	$\%V_{OUT}$
PG_{LTH}	PG low threshold	V_{OUT} decreasing	86	90	93	$\%V_{OUT}$
PG_{HYST}	PG hysteresis			2		$\%V_{OUT}$
$V_{OL(PG)}$	PG pin low-level output voltage	$V_{OUT} \geq 1.5\text{V}$, $I_{SINK} = 1.0\text{ mA}$ $V_{OUT} \geq 2.75\text{V}$, $I_{SINK} = 2.0\text{ mA}$			300	mV
$V_{OH(PG)}$	PG pin high-level output voltage ⁽⁴⁾	$V_{OUT} \geq 1.0\text{V}$, $I_{SOURCE} = 0.04\text{ mA}$ $V_{OUT} \geq 1.4\text{V}$, $I_{SOURCE} = 0.2\text{ mA}$ $V_{OUT} \geq 2.5\text{V}$, $I_{SOURCE} = 0.5\text{ mA}$ $V_{OUT} \geq 4.5\text{V}$, $I_{SOURCE} = 1.0\text{ mA}$		$0.8 \times V_{OUT}$		V
$I_{IKG(PG)}$	PG pin leakage current ⁽⁵⁾	$V_{OUT} > PG_{HTH}$, $V_{PG} = 6.0\text{ V}$		7	50	nA
T_{SD}	Thermal shutdown	Shutdown, temperature increasing Reset, temperature decreasing		170		$^\circ\text{C}$
				155		

(4) Push-pull version only. The push-pull option is supported only for $V_{OUT} \geq 1.0\text{ V}$.

(5) Open-drain version only.

6.6 Timing Requirements

		MIN	TYP	MAX	UNIT
t_{PGDH}	PG delay time rising, time from 92% V_{OUT} to 20% of $PG^{(1)}$	135	165	178	μs
	'B' version ⁽²⁾	4.5	5	5.5	ms
t_{PGDL}	PG delay time falling, time from 90% V_{OUT} to 80% of $PG^{(1)}$	1.5	7	10	μs

(1) Output overdrive = 10%.

(2) See the Device Nomenclature table for more information on available PG timings.

6.7 Typical Characteristics

at operating temperature range $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 1.5 V (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1\ \mu\text{F}$ (unless otherwise noted)

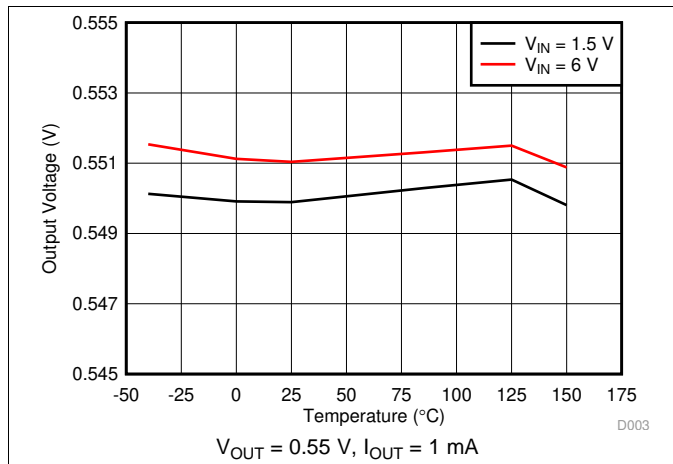


Figure 1. Output Voltage vs Ambient Temperature

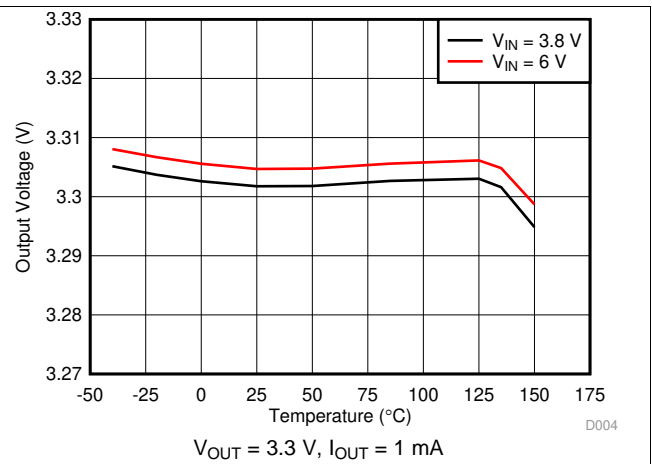


Figure 2. Output Voltage vs Ambient Temperature

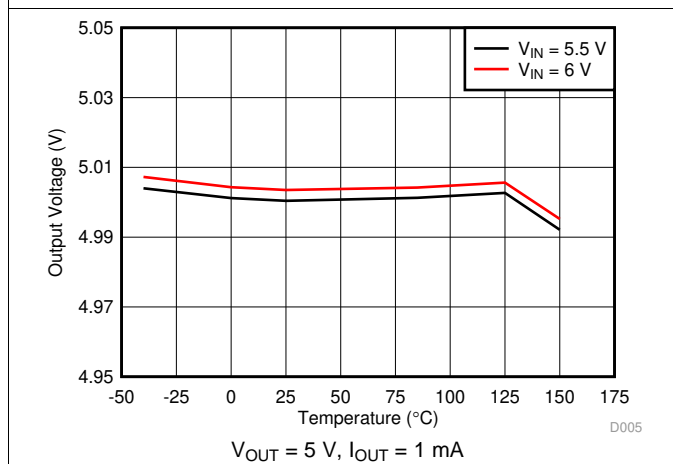


Figure 3. Output Voltage vs Ambient Temperature

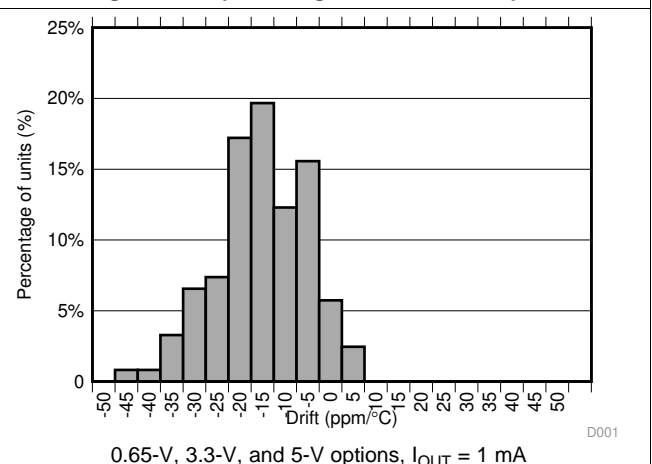


Figure 4. Temperature Drift Histogram (-40°C to +25°C)

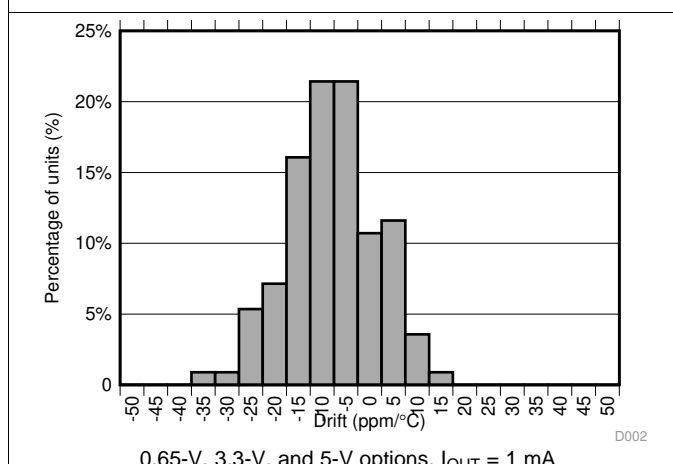


Figure 5. Temperature Drift Histogram (25°C to 150°C)

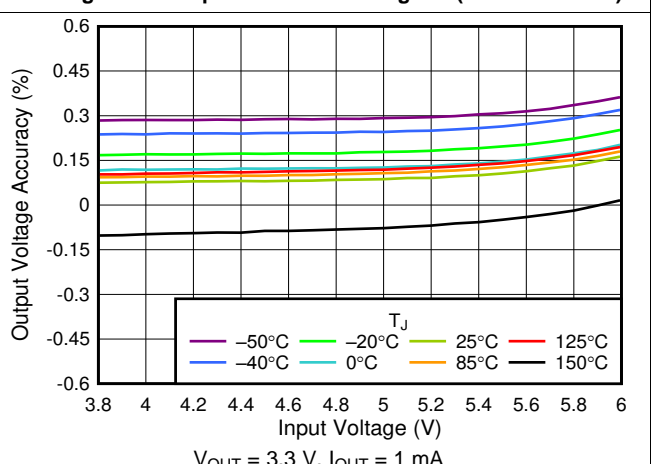


Figure 6. 3.3-V Line Regulation vs V_{IN}

Typical Characteristics (continued)

at operating temperature range $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 1.5 V (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$ (unless otherwise noted)

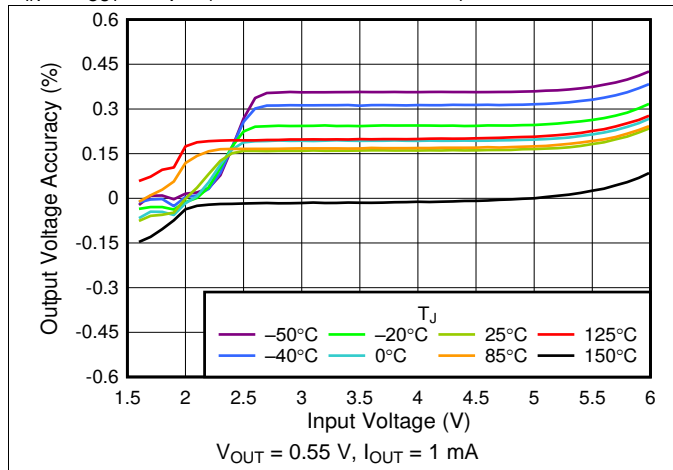


Figure 7. 0.55-V Line Regulation vs V_{IN}

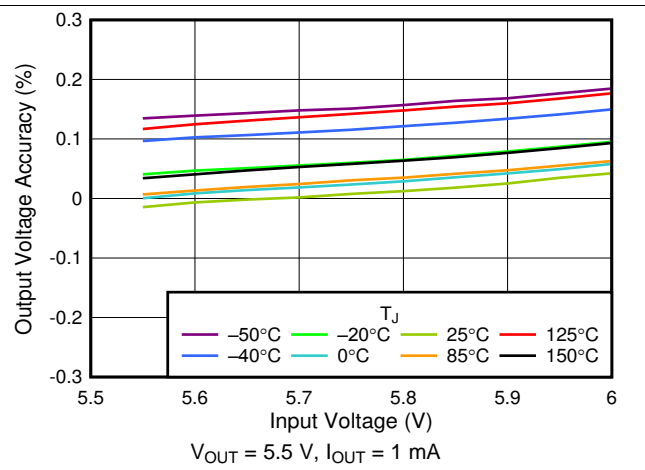


Figure 8. 5.5-V Line Regulation vs V_{IN}

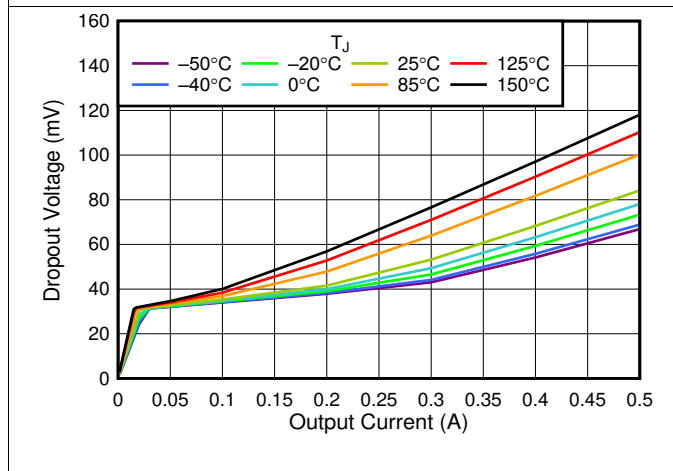


Figure 9. 3.3-V Dropout Voltage vs I_{OUT}

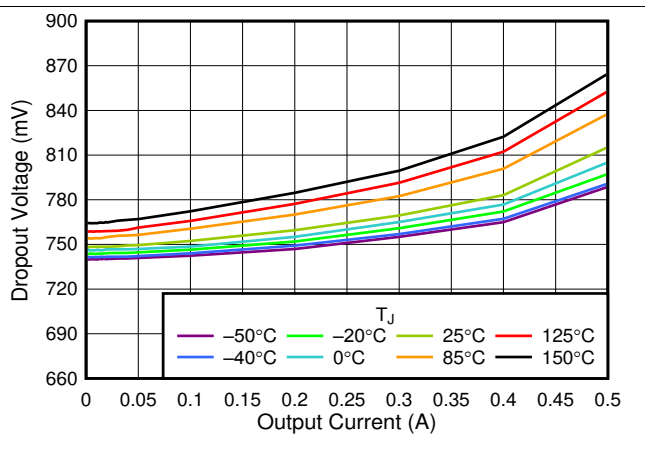


Figure 10. 0.55-V Dropout Voltage vs I_{OUT}

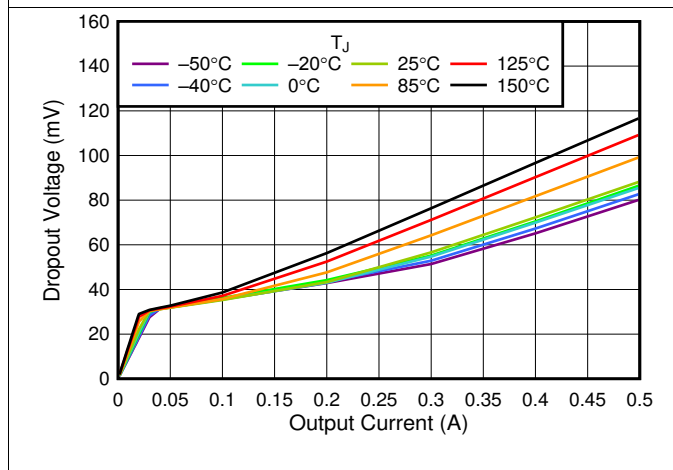


Figure 11. 5.5-V Dropout Voltage vs I_{OUT}

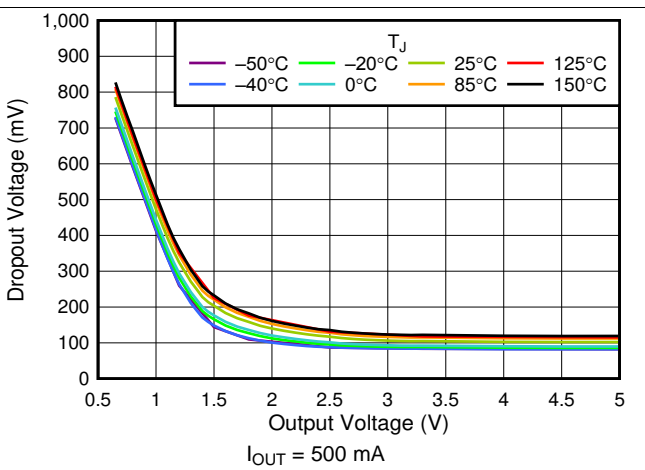
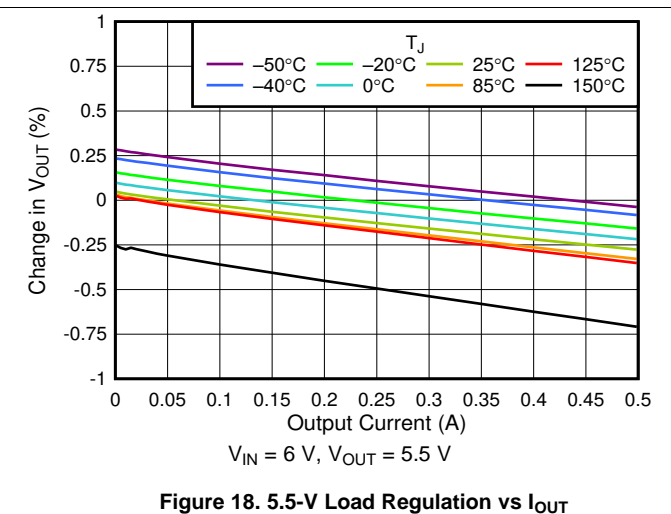
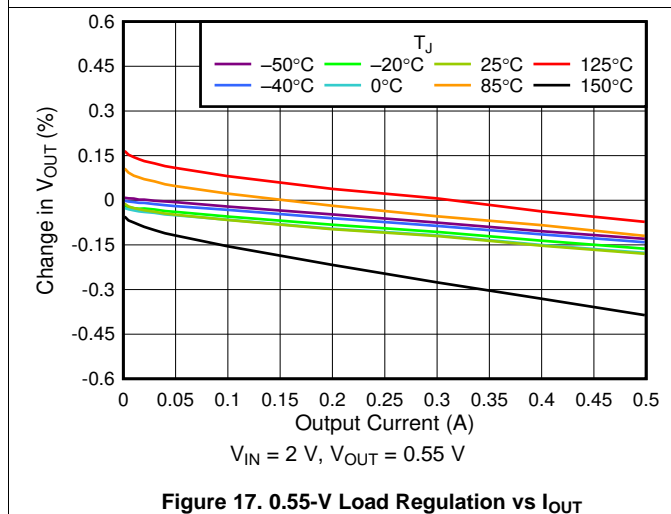
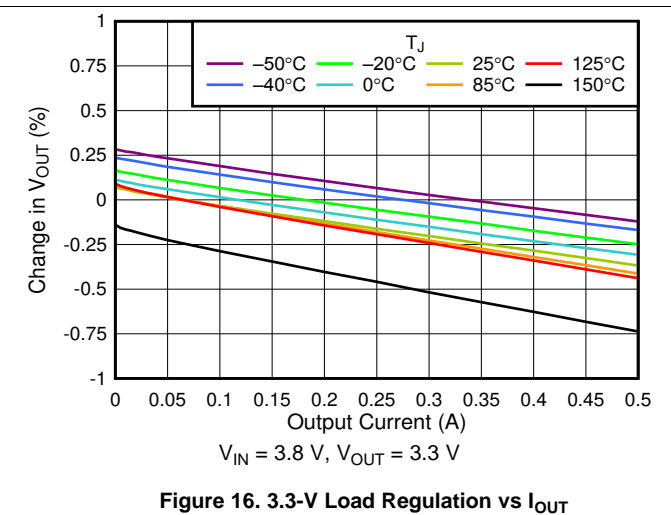
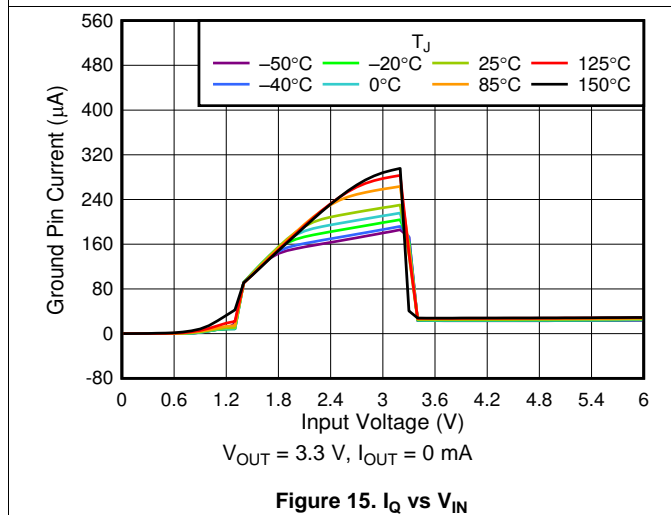
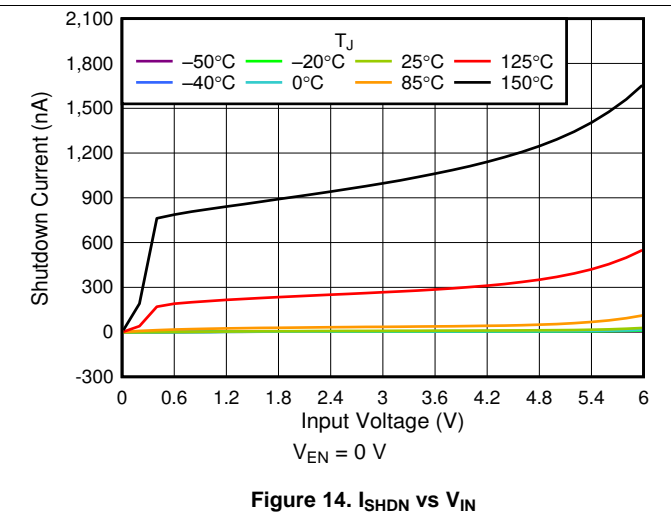
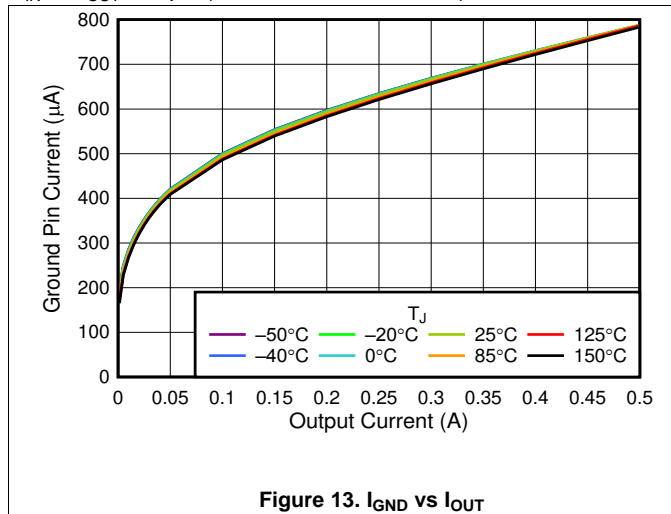


Figure 12. V_{DO} vs V_{OUT}

Typical Characteristics (continued)

at operating temperature range $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 1.5 V (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$ (unless otherwise noted)



Typical Characteristics (continued)

at operating temperature range $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 1.5 V (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$ (unless otherwise noted)

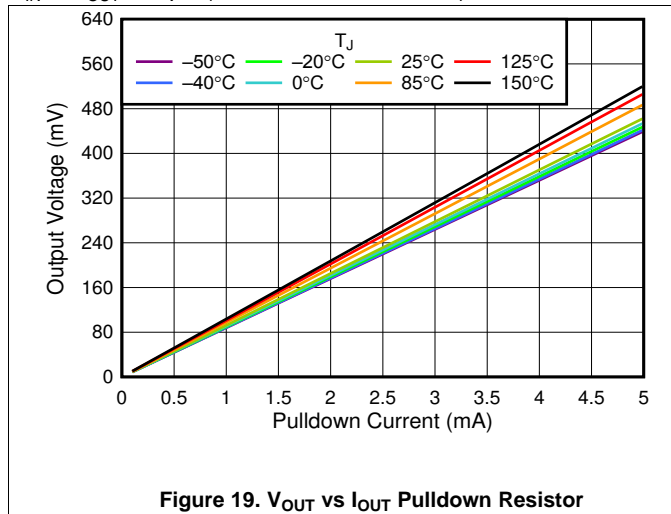


Figure 19. V_{OUT} vs I_{OUT} Pulldown Resistor

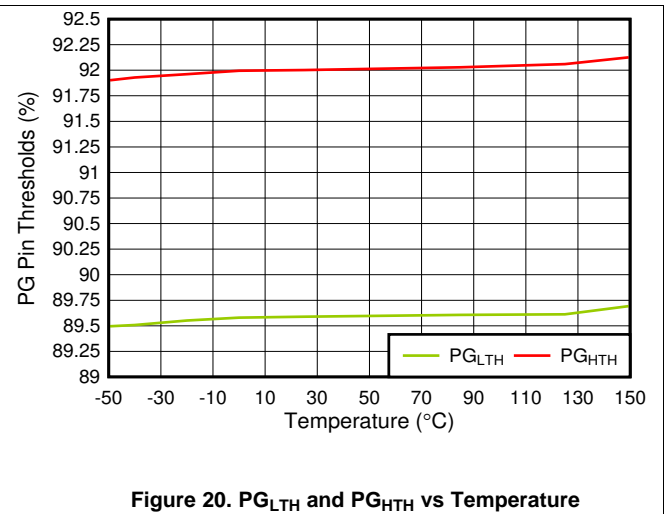


Figure 20. PGL_{TH} and PGH_{TH} vs Temperature

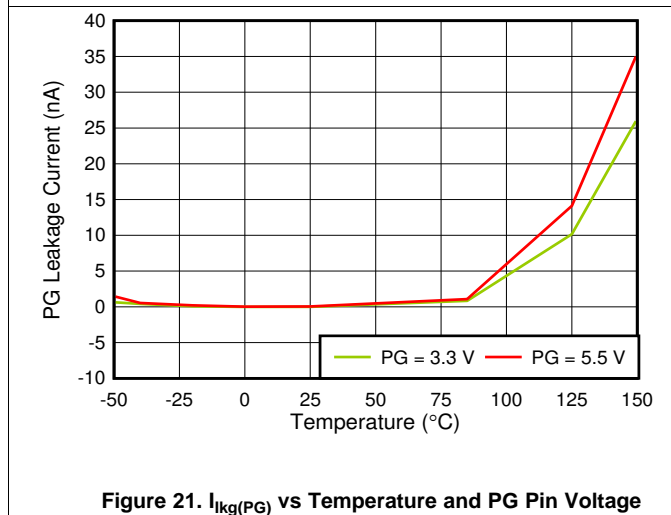


Figure 21. $I_{kg(PG)}$ vs Temperature and PG Pin Voltage

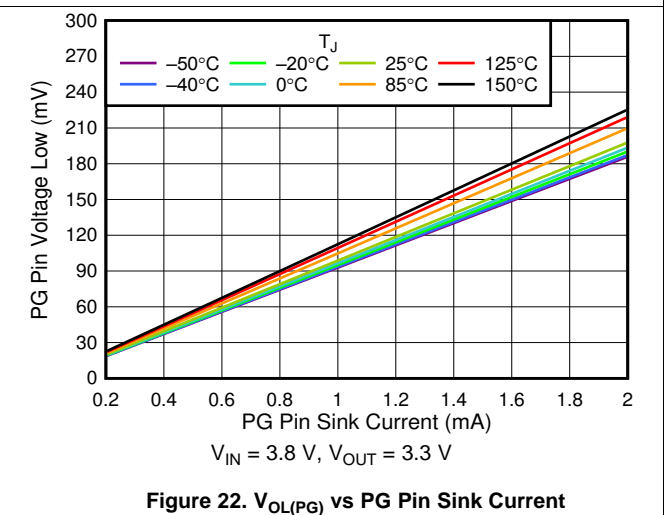


Figure 22. $V_{OL(PG)}$ vs PG Pin Sink Current

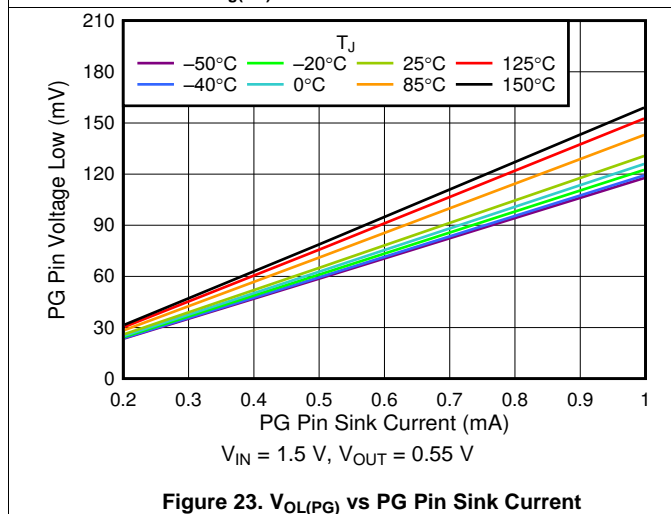


Figure 23. $V_{OL(PG)}$ vs PG Pin Sink Current

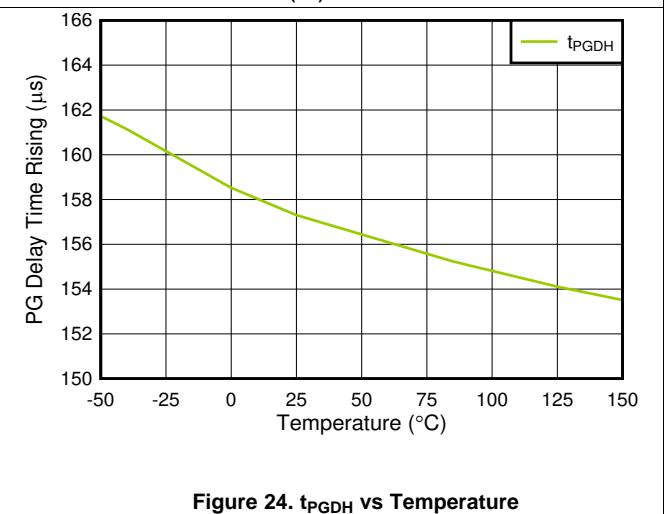


Figure 24. t_{PGDH} vs Temperature

Typical Characteristics (continued)

at operating temperature range $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 1.5 V (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$ (unless otherwise noted)

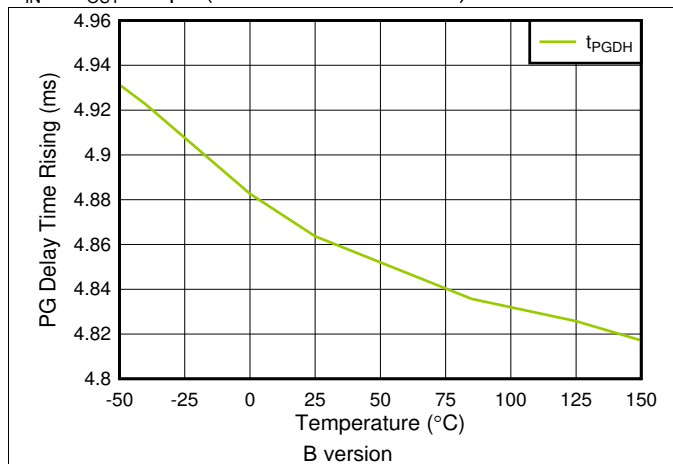


Figure 25. t_{PGDH} vs Temperature (For TPS746B Only)

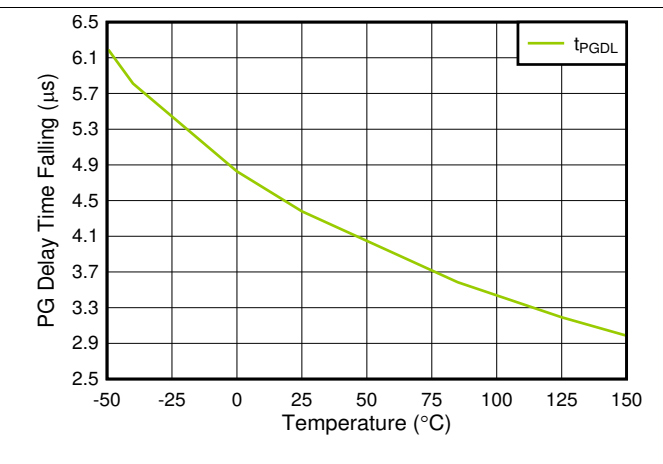


Figure 26. t_{PGDL} vs Temperature

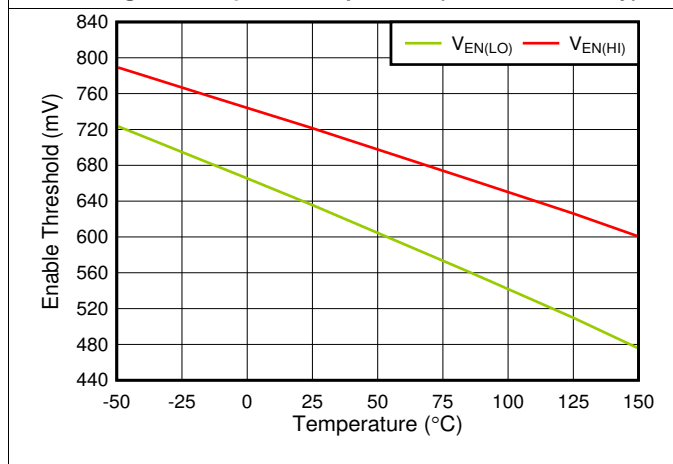


Figure 27. $V_{EN(HI)}$ and $V_{EN(LO)}$ vs Temperature

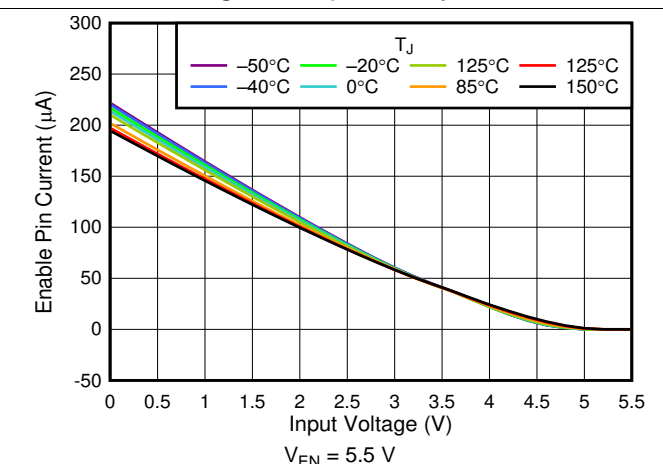


Figure 28. I_{EN} vs V_{IN}

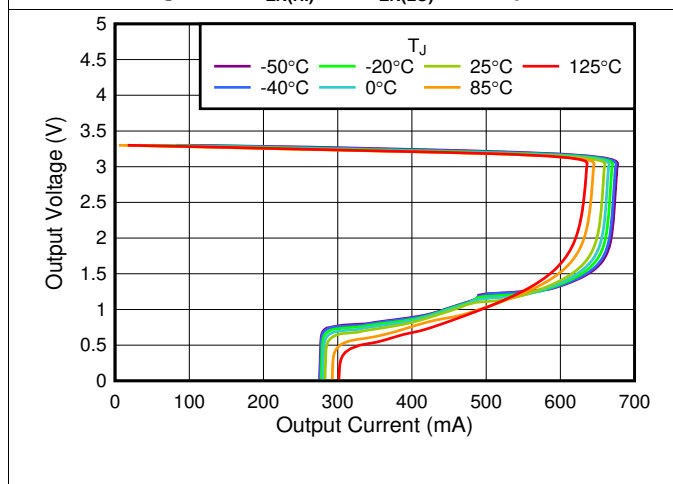


Figure 29. 3.3-V V_{OUT} vs I_{OUT}

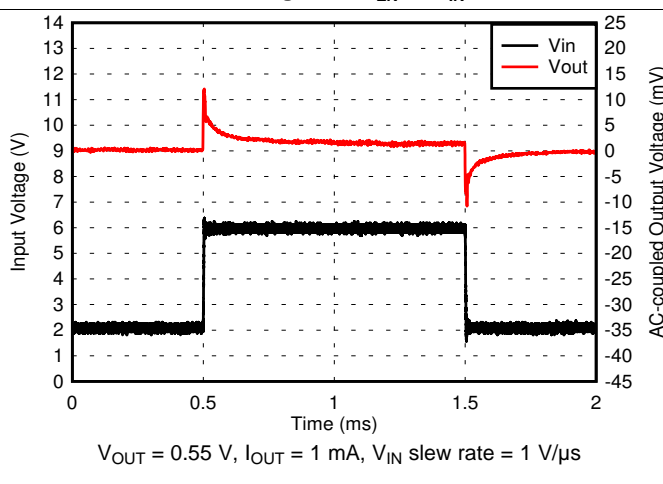


Figure 30. 0.55-V Line Transient

Typical Characteristics (continued)

at operating temperature range $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 1.5 V (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$ (unless otherwise noted)

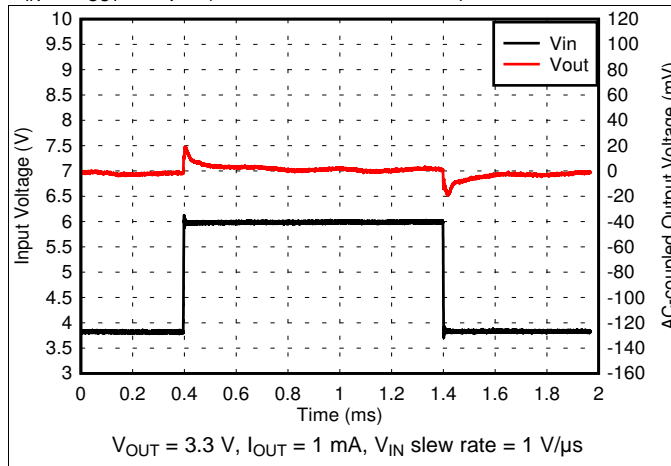


Figure 31. 3.3-V Line Transient

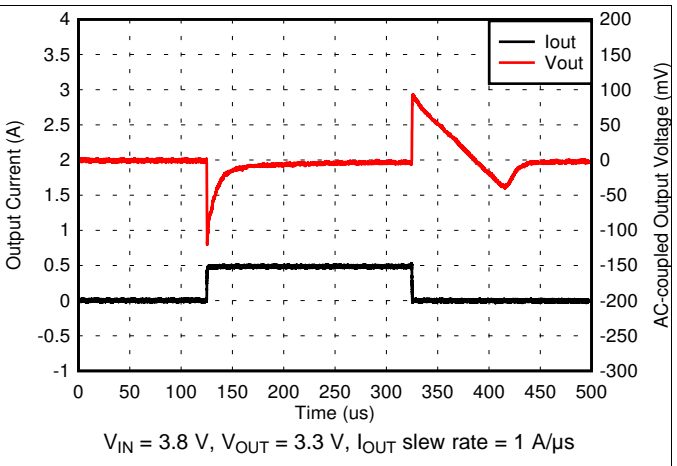


Figure 32. 3.3-V, 1-mA to 500-mA Load Transient

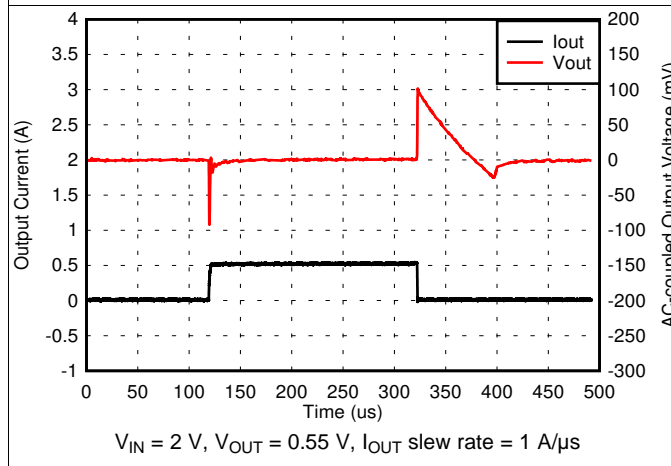


Figure 33. 0.55-V, 1-mA to 500-mA Load Transient

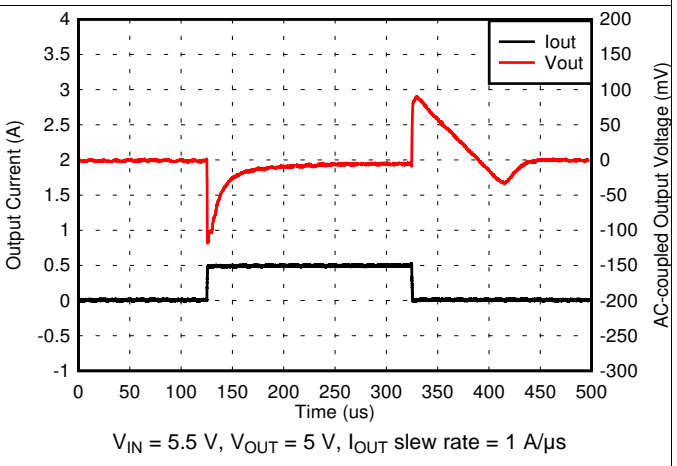


Figure 34. 5-V, 1-mA to 500-mA Load Transient

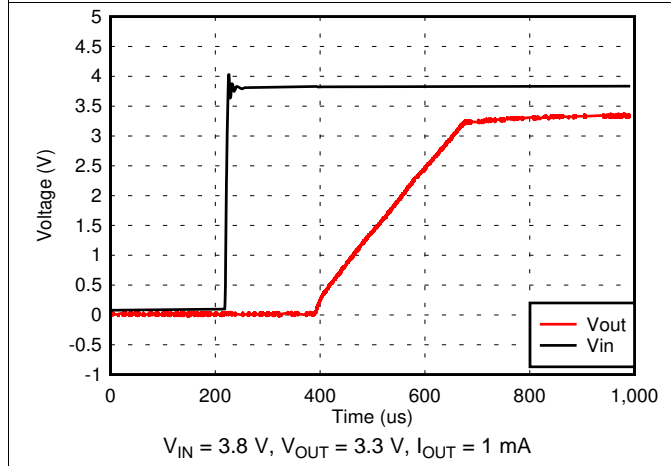


Figure 35. V_{IN} Power-Up

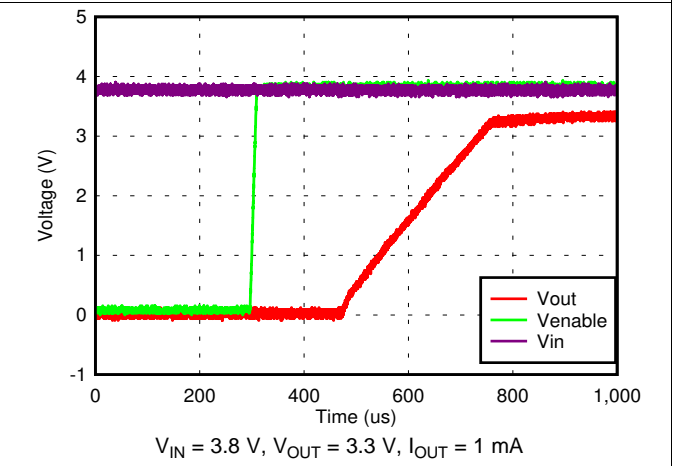
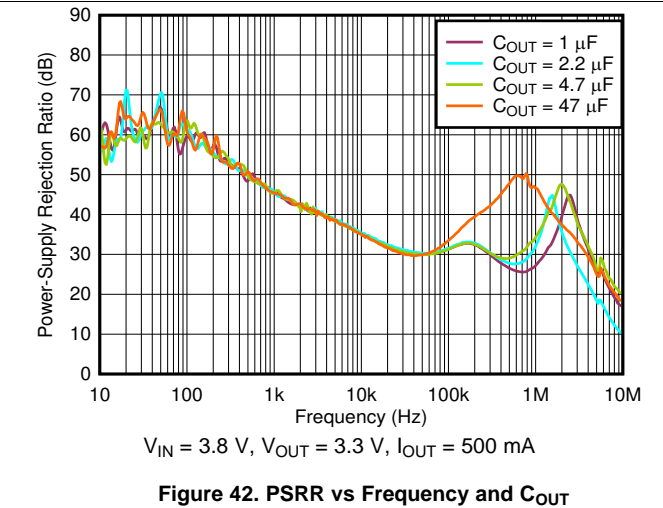
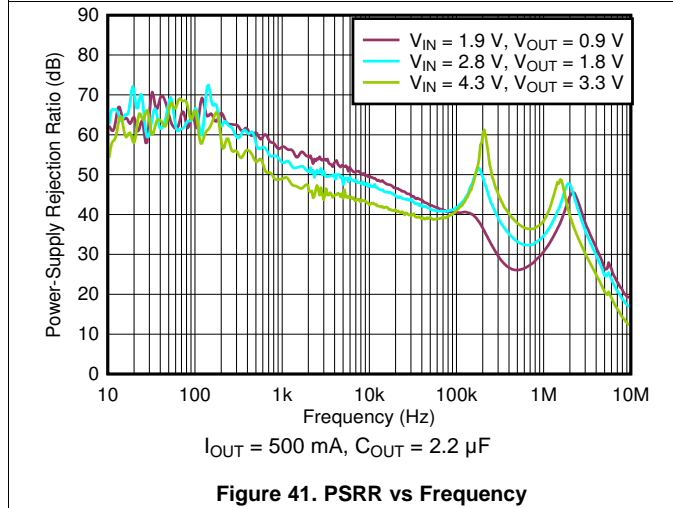
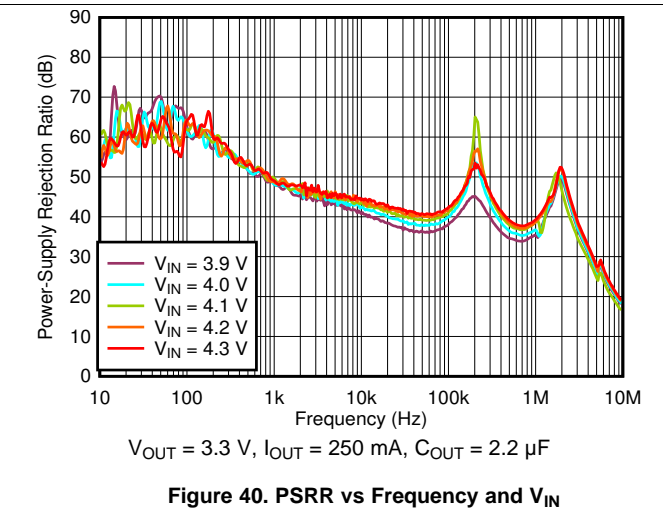
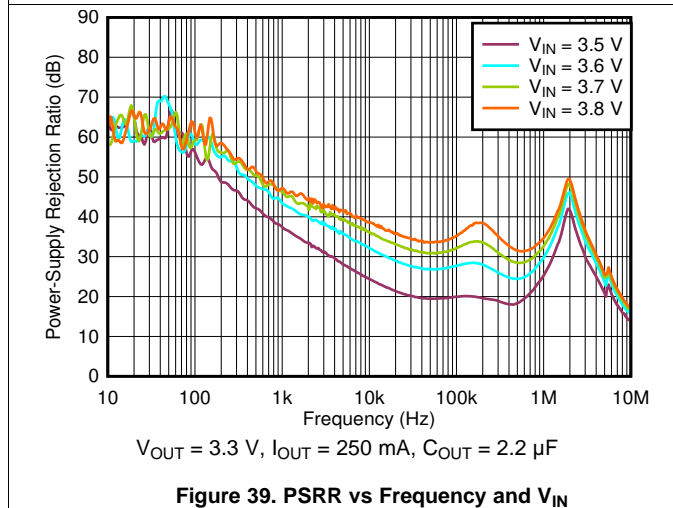
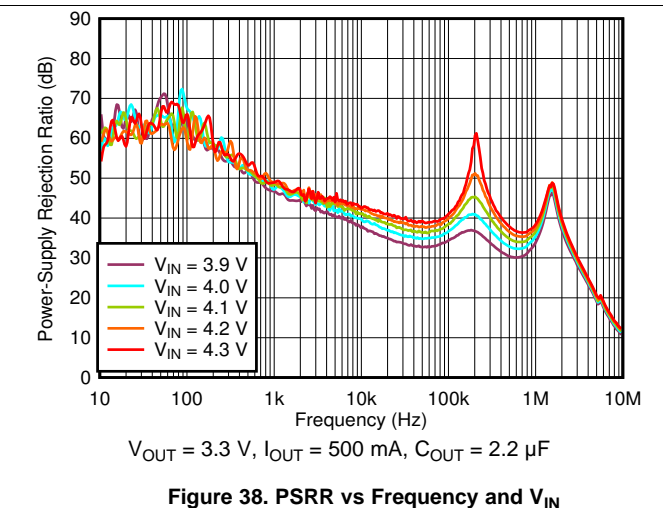
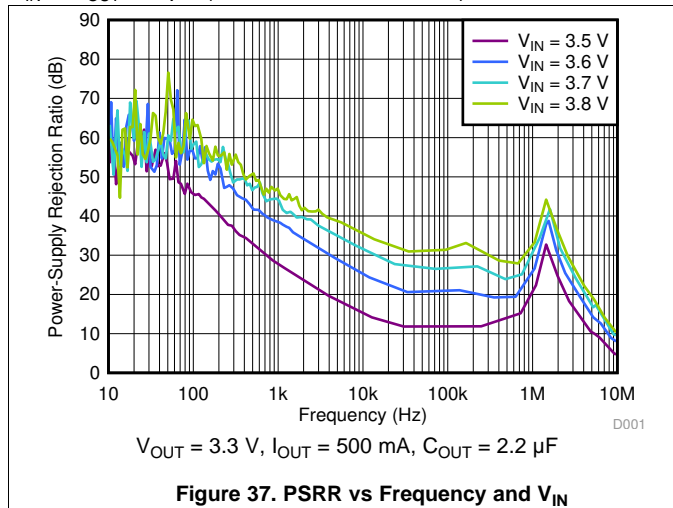


Figure 36. Start-Up With EN

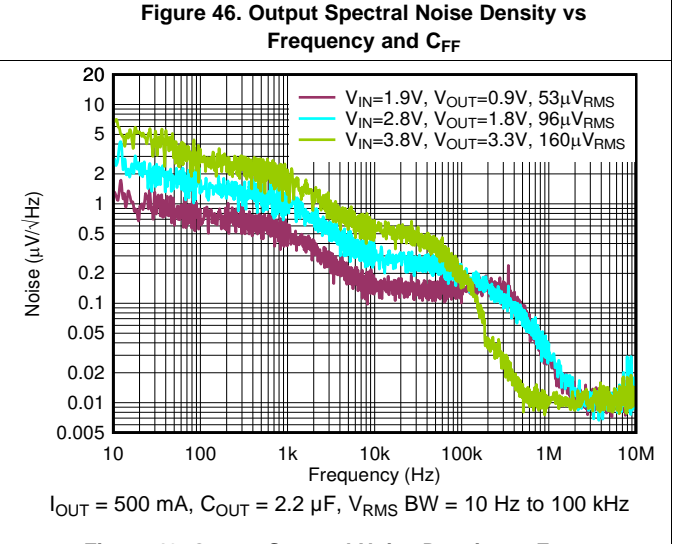
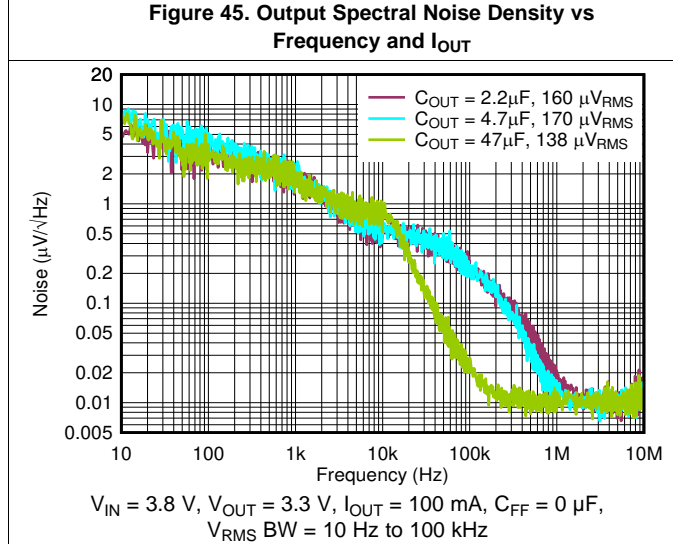
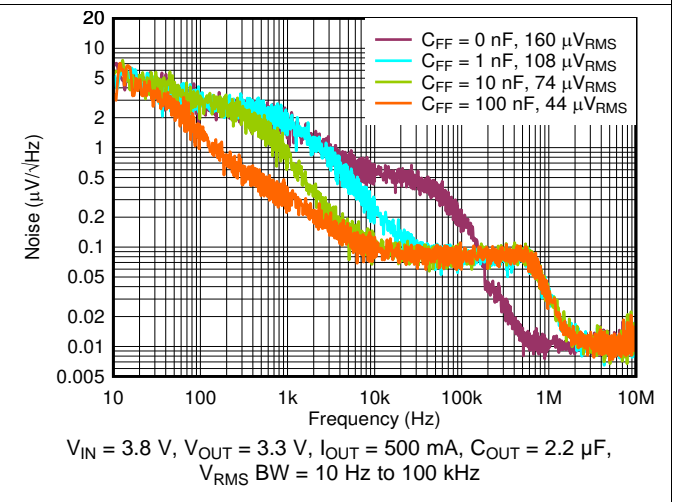
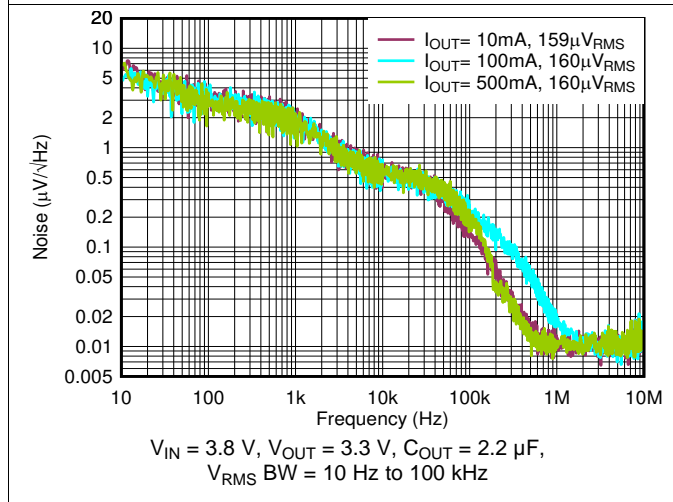
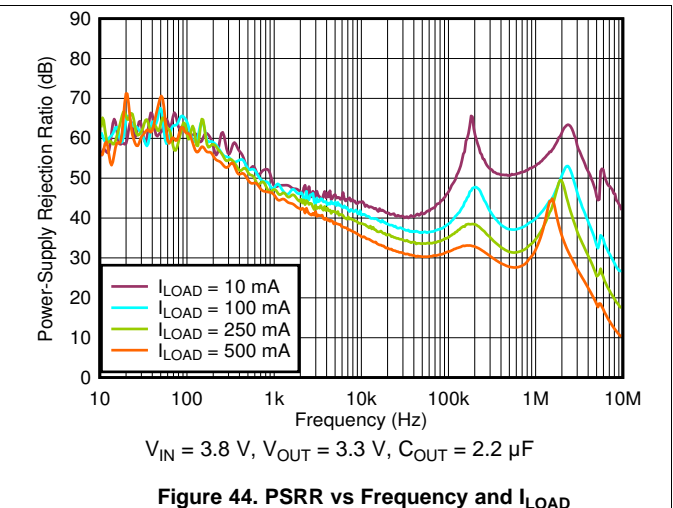
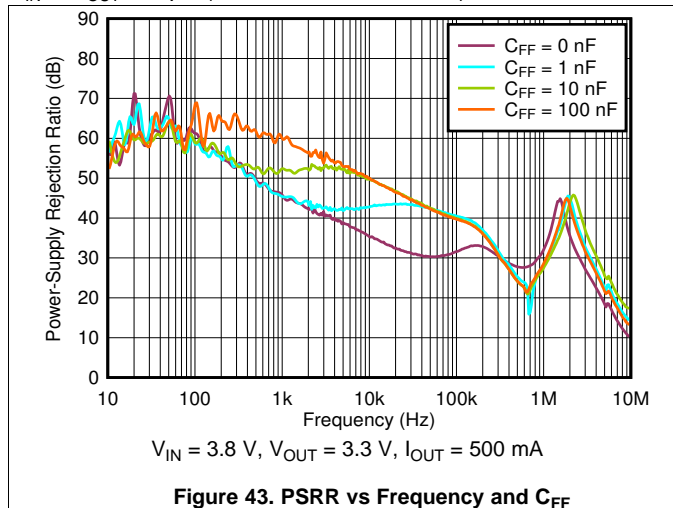
Typical Characteristics (continued)

at operating temperature range $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 1.5 V (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$ (unless otherwise noted)



Typical Characteristics (continued)

at operating temperature range $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 1.5 V (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$ (unless otherwise noted)



7 Detailed Description

7.1 Overview

The TPS745-Q1 is a low-dropout regulator (LDO) that consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise, good PSRR with low dropout voltage, make this device ideal for automotive applications.

This regulator offers foldback current limit, shutdown, and thermal protection. The operating junction temperature for this device is -40°C to $+150^{\circ}\text{C}$.

7.2 Functional Block Diagrams

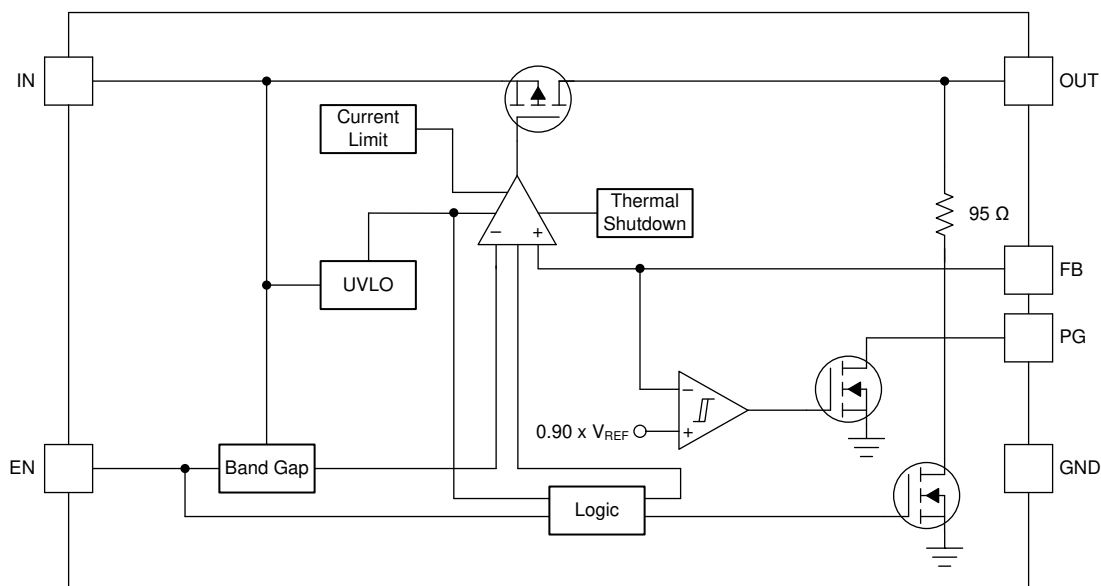


Figure 49. Adjustable Version With Open-Drain Power-Good

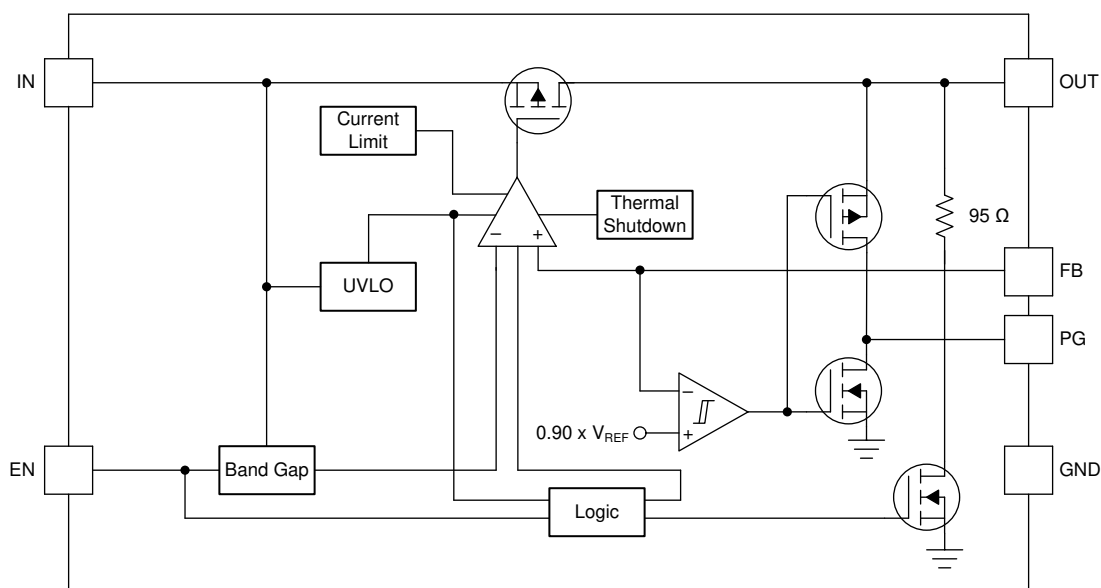


Figure 50. Adjustable Version With Push-Pull Power-Good

Functional Block Diagrams (continued)

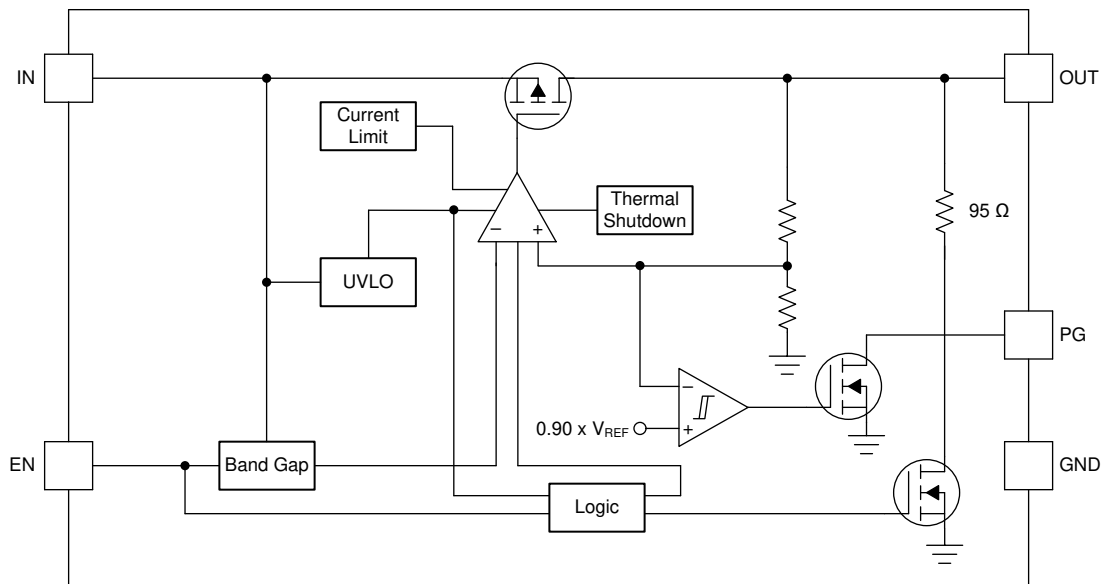


Figure 51. Fixed Voltage Version With Open-Drain Power-Good

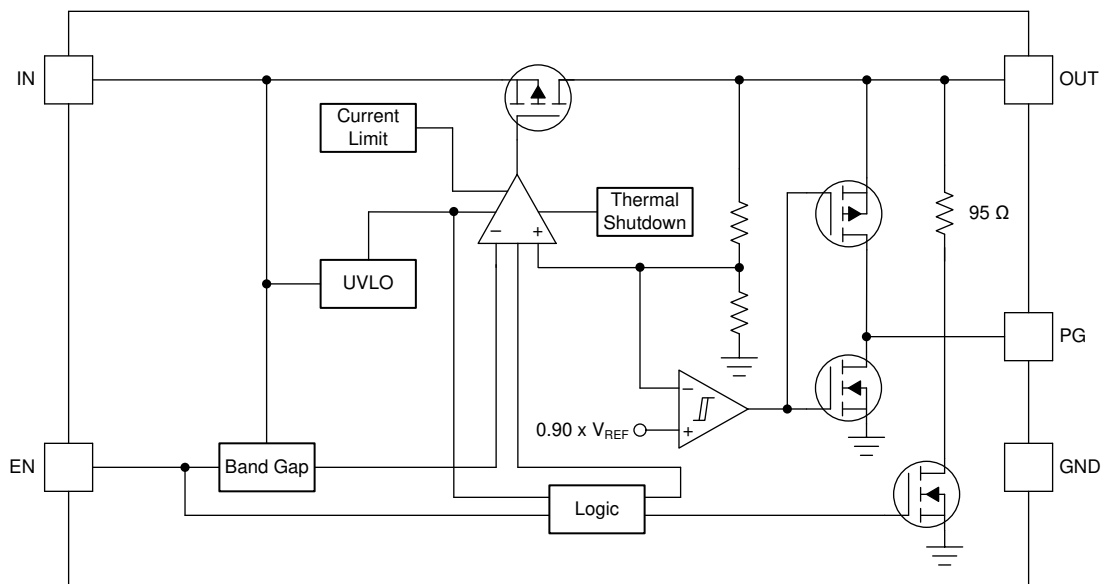


Figure 52. Fixed Voltage Version With Push-Pull Power-Good

7.3 Feature Description

7.3.1 TPS745-Q1 Comparison

Table 1 lists the three different power-good (PG) options for the TPS745-Q1.

Table 1. TPS745-Q1 Comparison Table

DEVICE	POWER-GOOD DELAY	POWER-GOOD TYPE
TPS745xxPQWDRVRQ1, TPS745xxPQWDRBRQ1	150 μ s	Open-drain
TPS745xxPBQWDRVRQ1	5 ms	Open-drain
TPS745xxPCQWDRVRQ1	150 μ s	Push-pull

7.3.2 Undervoltage Lockout (UVLO)

The TPS745-Q1 uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage (V_{UVLO}). This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry. When V_{IN} is less than V_{UVLO} , the output is connected to ground with a pulldown resistor ($R_{PULLDOWN}$). When the device enters UVLO, the PG output is pulled low.

7.3.3 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(HI)}$. Turn off the device by forcing the EN pin to drop below $V_{EN(LO)}$. If shutdown capability is not required, connect EN to IN. When the device is disabled, the PG output pin is pulled low.

The TPS745-Q1 has an internal pulldown MOSFET that connects an $R_{PULLDOWN}$ resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the pulldown resistor ($R_{PULLDOWN}$). Equation 1 calculates the time constant:

$$\tau = (R_{PULLDOWN} \times R_L) / (R_{PULLDOWN} + R_L) \times C_{OUT} \quad (1)$$

7.3.4 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK} = 0.4 \text{ V} \times V_{OUT(NOM)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power $[(V_{IN} - V_{OUT}) \times I_{CL}]$. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power $[(V_{IN} - V_{OUT}) \times I_{SC}]$. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the [Know Your Limits application report](#).

Figure 53 shows a diagram of the foldback current limit.

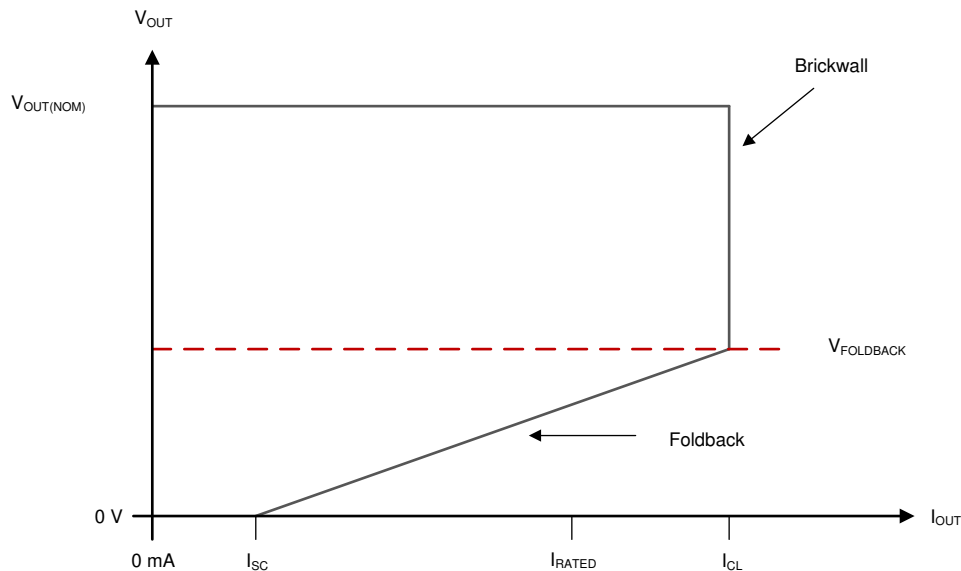


Figure 53. Foldback Current Limit

7.3.5 Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 170°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 155°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the regulator from damage as a result of overheating.

Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the $(V_{IN} - V_{OUT})$ voltage and the load current. For reliable operation, limit junction temperature to 150°C maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TPS745-Q1 internal protection circuitry protects against overload conditions but is not intended to be activated in normal operation. Continuously running the TPS745-Q1 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 2. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Adjustable Device Feedback Resistors

Figure 54 shows that the output voltage of the TPS745P-Q1 can be adjusted from 0.55 V to 5.5 V by using a resistor divider network.

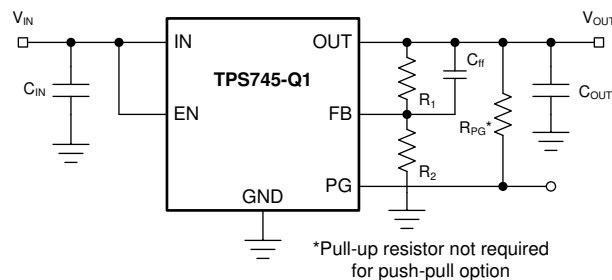


Figure 54. Adjustable Operation

The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2 , according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (2)$$

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100x the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (3)$$

8.1.2 Input and Output Capacitor Selection

The TPS745-Q1 requires an output capacitance of 0.47 μF or larger for stability. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. When choosing a capacitor for a specific application be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitance is 220 μF .

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

8.1.3 Dropout Voltage

The TPS745-Q1 uses a PMOS pass transistor to achieve low dropout. When $(V_{IN} - V_{OUT})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as $(V_{IN} - V_{OUT})$ approaches dropout operation.

Application Information (continued)

8.1.4 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on V_{IN} during start-up. As with other LDOs, the output can overshoot on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up, as shown in Figure 55, when the slew rate and voltage levels are in the correct range. Use an enable signal to avoid this condition.

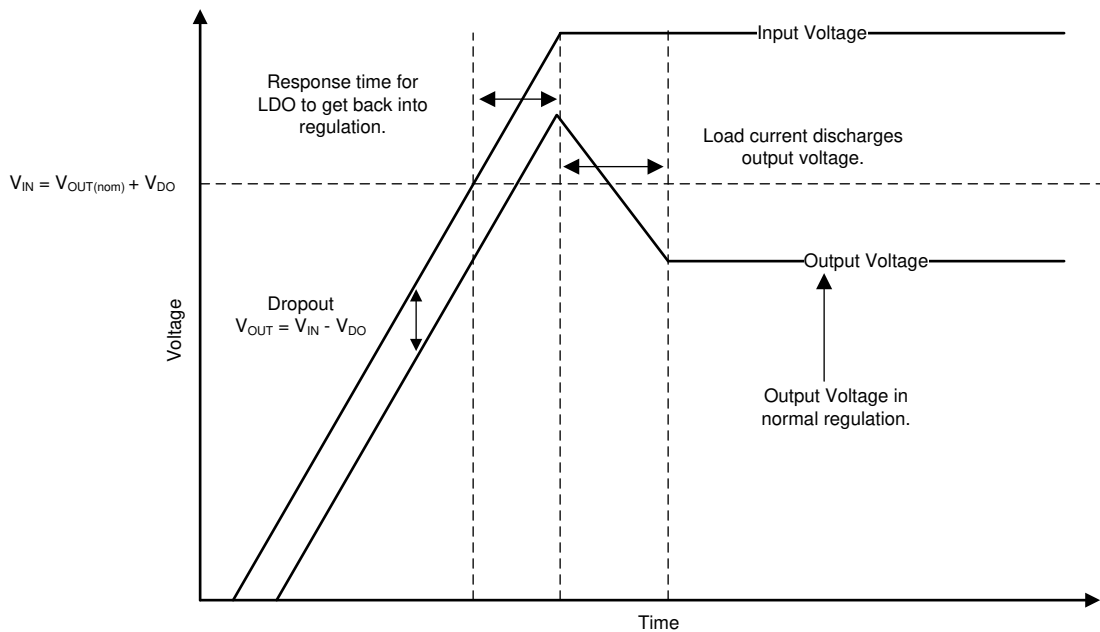
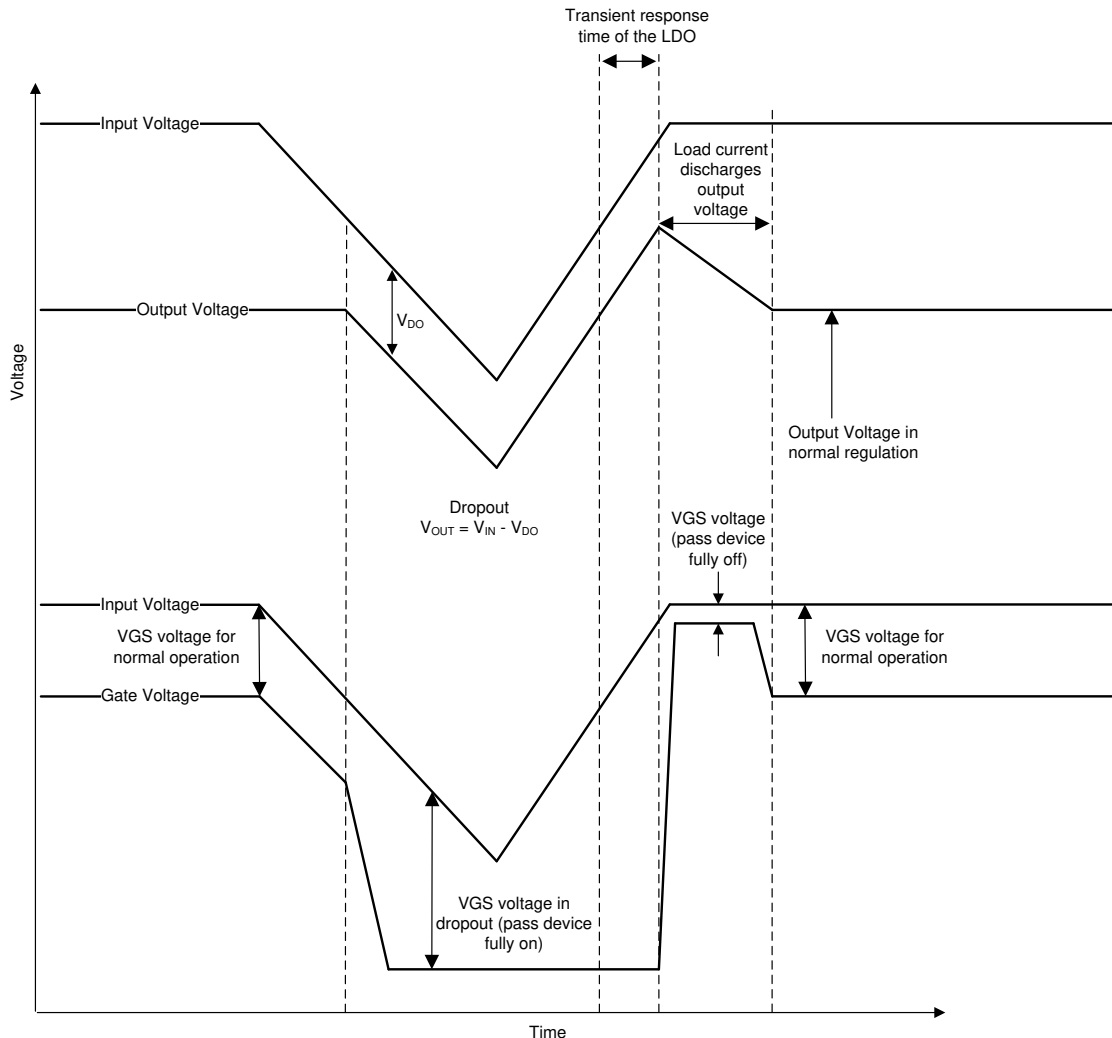


Figure 55. Start-Up Into Dropout

Line transients out of dropout can also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass element and bring the gate back to the correct voltage for proper regulation. Figure 56 illustrates what is happening internally with the gate voltage and how overshoot can be caused during operation. When the LDO is placed in dropout, the gate voltage (V_{GS}) is pulled all the way down to ground to give the pass device the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation and can cause the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.

Application Information (continued)

Figure 56. Line Transients From Dropout
8.1.5 Reverse Current

As with most LDOs, excessive reverse current can damage this device.

Reverse current flows through the body diode on the pass element instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device, as a result of one of the following conditions:

- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3\text{ V}$:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

Application Information (continued)

If reverse current flow is expected in the application, external protection must be used to protect the device. Figure 57 shows one approach of protecting the device.

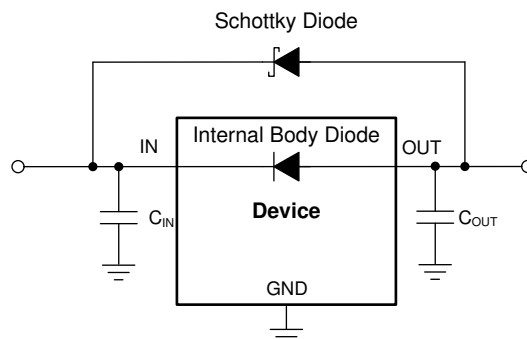


Figure 57. Example Circuit for Reverse Current Protection Using a Schottky Diode

8.1.6 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Equation 4 calculates power dissipation (P_D).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

NOTE

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to Equation 5, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (5)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

Figure 58 and Figure 59 illustrate the functions of $R_{\theta JA}$ and ψ_{JB} versus copper (Cu) area and thickness. These plots are generated with a 101.6-mm x 101.6-mm x 1.6-mm printed circuit board (PCB) of two and four layers. For the four-layer board, the inner planes use a 1-oz copper thickness. Outer layers are simulated with both 1-oz and 2-oz copper thickness. A 2 x 1 array of thermal vias of 300- μ m drill diameter and 25- μ m Cu plating is located beneath the thermal pad of the device. The thermal vias connect the top layer, the bottom layer and, in the case of the 4-layer board, the first inner GND plane.

Application Information (continued)

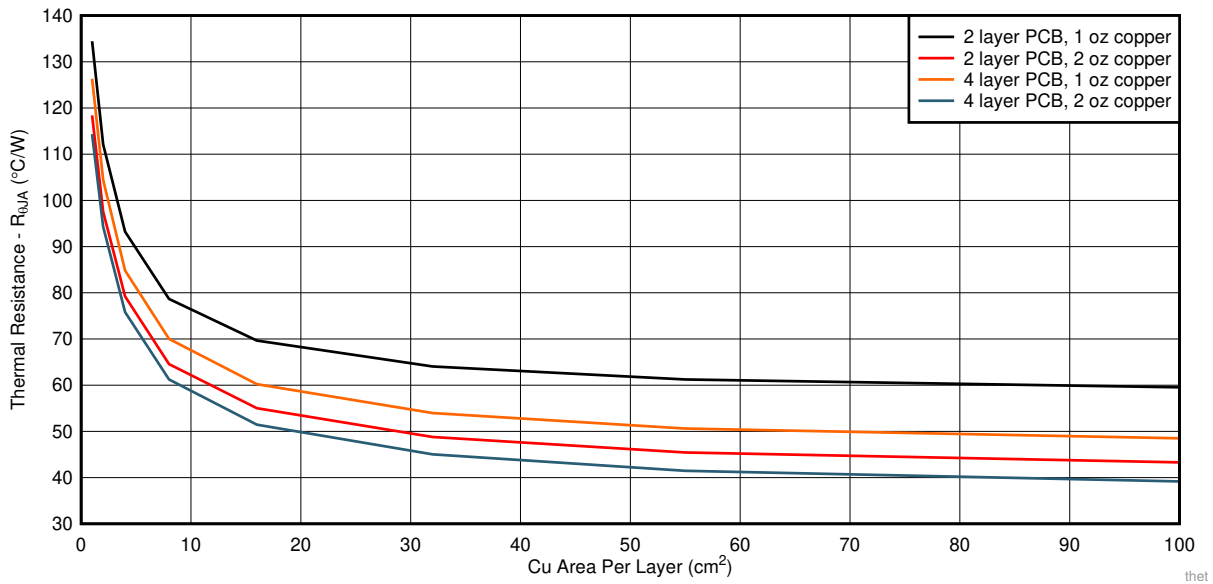


Figure 58. $R_{\theta JA}$ versus Cu Area for the WSON (DRV) Package

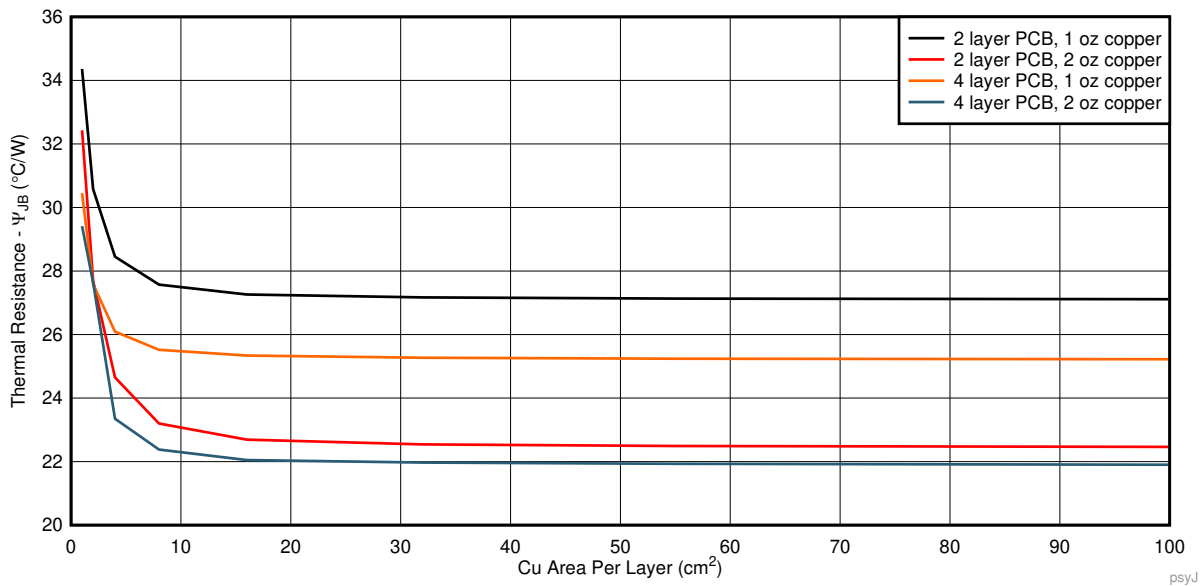
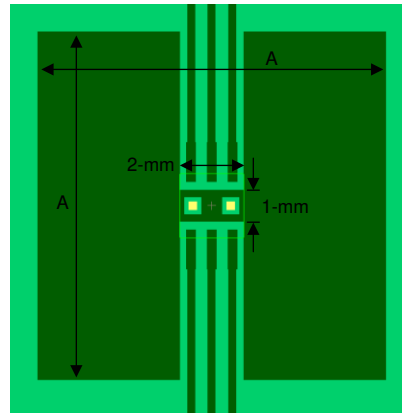


Figure 59. ψ_{JB} versus Cu Area for the WSON (DRV) Package

Application Information (continued)

As shown in Figure 60, each layer has a copper plane of equal area.



Buried plane and bottom layer Cu ground planes are modeled with Area = AxA

Figure 60. Board parameters used for simulation

For a more comprehensive study of how thermal resistance varies with copper area and thickness, see the [An empirical analysis of the impact of board layout on LDO thermal performance application report](#). As shown in Figure 61, modifying board layout to be more thermally enhanced can lower the $R_{\theta JA}$ value from 80.3°C/W to 46.8°C/W or better.

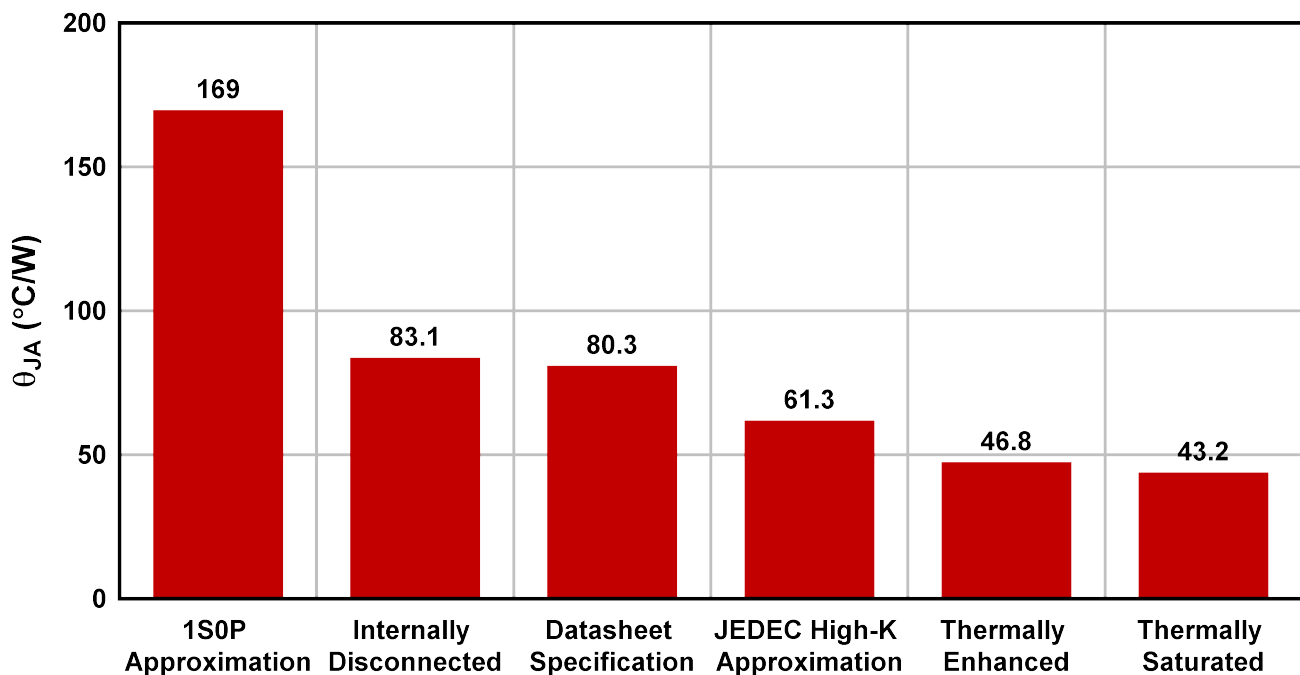


Figure 61. TPS745-Q1 (WSN) $R_{\theta JA}$ versus Board Layout

Application Information (continued)

8.1.7 Power-Good Function

The power-good circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. When the output voltage falls below the PG threshold voltage (PG_{LTH}), the PG pin open-drain output engages and pulls the PG pin close to GND. When the output voltage exceeds PG_{HTH} , the PG pin becomes high impedance. The open-drain output requires a pullup resistor. By connecting a pullup resistor to an external supply, any downstream device can receive power-good as a logic signal that can be used for sequencing. Additionally, the open-drain output can be tied to other open-drain outputs to implement AND logic. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device. Using a pullup resistor from 10 k Ω to 100 k Ω is recommended. The push-pull power-good option does not require the pullup resistor and instead has a high logic signal that correlates with the output voltage of the device. The push-pull option is supported only for $V_{OUT} \geq 1.0$ V. The push-pull option is supported only for $V_{OUT} \geq 1.0$ V. Do not tie the push-pull output to other logic outputs.

When using a feed-forward capacitor (C_{FF}), the time constant for the LDO start-up is increased whereas the power-good output time constant stays the same, possibly resulting in an invalid status of the power-good output. To avoid this issue, and to receive a valid PG output, make sure that the time constant of both the LDO start-up and the power-good output match, which can be done by adding a capacitor in parallel with the power-good pullup resistor. For more information, see the [Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator application report](#).

The state of PG is only valid when the TPS745-Q1 operates above the minimum input voltage of the device and power-good is asserted, regardless of the output voltage state when the input voltage falls below the UVLO threshold minus the UVLO hysteresis. When the input voltage falls below approximately 0.8 V, there is not enough gate drive voltage to keep the open-drain, power-good device turned on and the power-good output pulled high. Connecting the power-good pullup resistor to the output voltage can help minimize this effect.

8.1.8 Feed-Forward Capacitor (C_{FF})

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. A higher capacitance C_{FF} can be used; however, the startup time increases. For a detailed description of C_{FF} tradeoffs, see the [Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator application report](#).

8.1.9 Start-Up Sequencing

If V_{EN} is greater than V_{UVLO} rising (min), the input pin (IN) must sink 1 mA of current to avoid the device being turned on with a floating input pin.

8.2 Typical Application

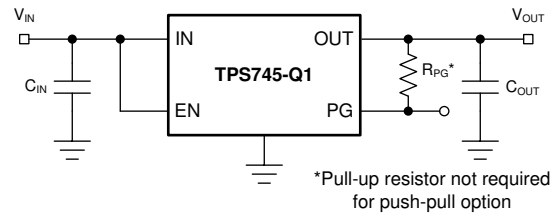


Figure 62. TPS745-Q1 Typical Application

8.2.1 Design Requirements

Table 3 summarizes the design requirements for Figure 62.

Table 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.3 V
Output voltage	1.8 V, ±1%
Input current	300 mA, maximum
Output load	300-mA DC
Maximum ambient temperature	105°C

8.2.2 Detailed Design Procedure

Input and output capacitors are required to achieve the output voltage transient requirements. Capacitance values of 2.2 µF are selected to give the maximum output capacitance in a small, low-cost package; see the [Input and Output Capacitor Selection](#) section for details.

8.2.2.1 Input Current

During normal operation, the input current to the LDO is approximately equal to the output current of the LDO. During start-up, the input current is higher as a result of the inrush current charging the output capacitor. Use Equation 6 to calculate the current through the input.

$$I_{OUT(t)} = \left(\frac{C_{OUT} \times dV_{OUT}(t)}{dt} \right) + \left(\frac{V_{OUT}(t)}{R_{LOAD}} \right)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t) / dt$ is the slope of the V_{OUT} ramp
- R_{LOAD} is the resistive load impedance

(6)

8.2.2.2 Thermal Dissipation

The junction temperature can be determined using the junction-to-ambient thermal resistance ($R_{\theta JA}$) and the total power dissipation (P_D). Use Equation 7 to calculate the power dissipation. Multiply P_D by $R_{\theta JA}$ as Equation 8 shows and add the ambient temperature (T_A) to calculate the junction temperature (T_J).

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} - V_{OUT}) \tag{7}$$

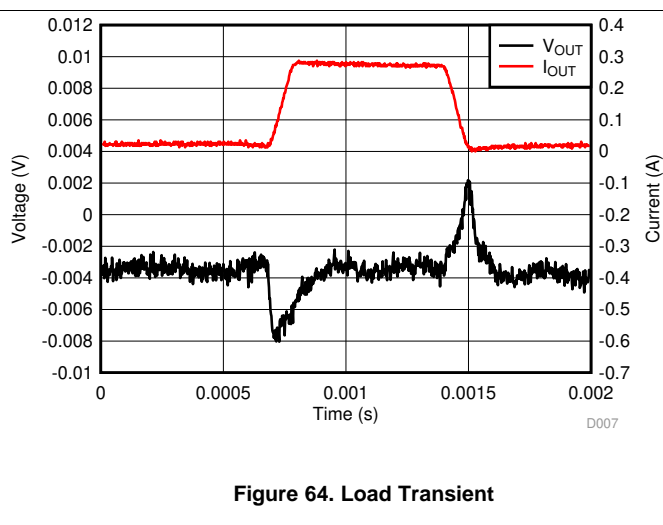
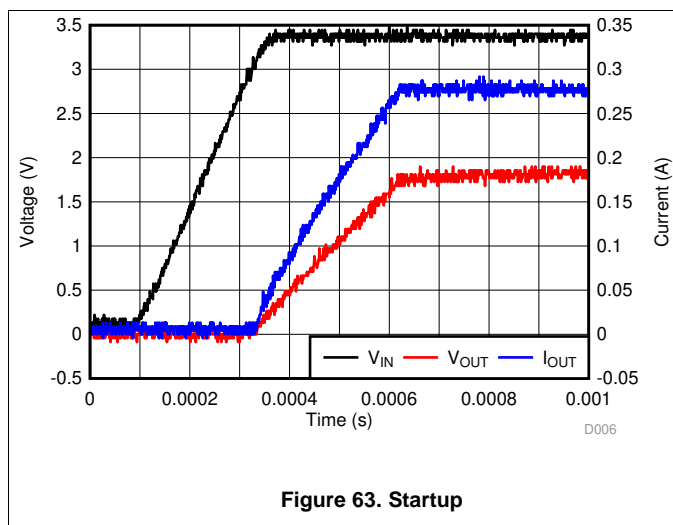
$$T_J = R_{\theta JA} \times P_D + T_A \tag{8}$$

Calculate the maximum ambient temperature according to Equation 9 and Equation 10. The maximum ambient temperature is 113.86°C for the example conditions.

$$T_{A(MAX)} = T_{J(MAX)} - R_{\theta JA} \times P_D \tag{9}$$

$$T_{A(MAX)} = 150^\circ\text{C} - 80.3^\circ\text{C/W} \times (3.3\text{ V} - 1.8\text{ V}) \times (0.3\text{ A}) = 113.86^\circ\text{C} \tag{10}$$

8.2.3 Application Curves



9 Power Supply Recommendations

The TPS745-Q1 is designed to operate from an input voltage supply range from 1.5 V to 6.0 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve output noise performance. Connect a low output impedance power supply directly to the IN pin of the TPS745-Q1.

10 Layout

10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute heat.
- Only place tented thermal vias directly beneath the thermal pad of the DRV or DRB package. An untented via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

10.2 Layout Examples

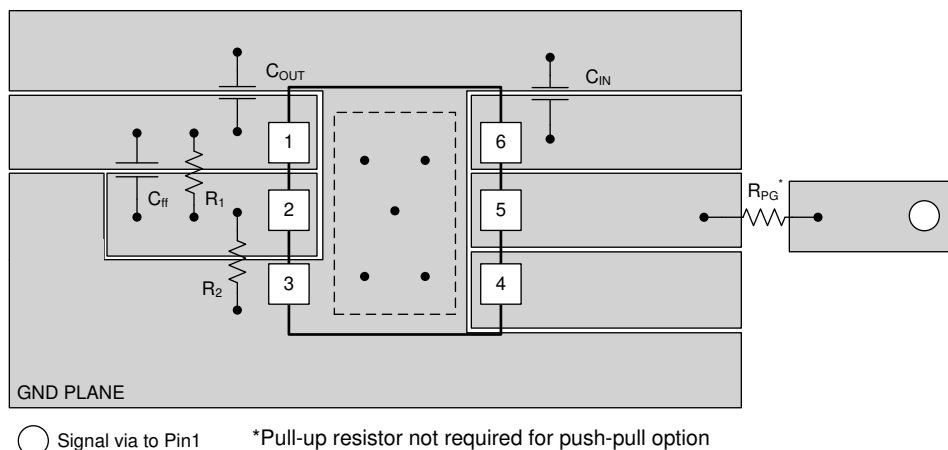


Figure 65. Layout Example for the DRV Package

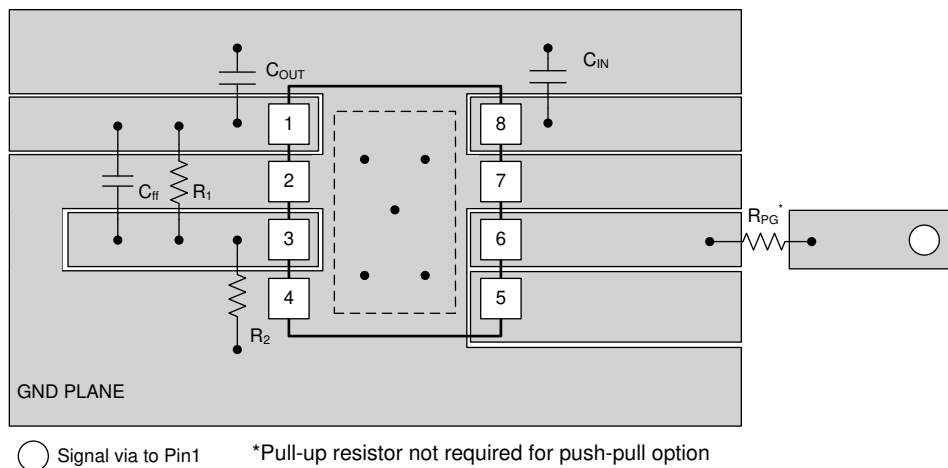


Figure 66. Layout Example for the DRB Package

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Table 4. Device Nomenclature⁽¹⁾⁽²⁾

PRODUCT	V _{OUT}
TPS745xx(x)PvQWyyyZQ1	<p>xx(x) is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V; 01 = adjustable).</p> <p>P indicates an active output discharge feature. All members of the TPS745-Q1 family actively discharge the output when the device is disabled.</p> <p>v indicates the topology of the power-good output and the timing associated with the power-good delay.</p> <ul style="list-style-type: none"> If unused, indicates an open-drain power-good output with a 150-μs delay. If B, indicates a open-drain power-good output with a 5-ms delay. If C, indicates a push-pull power-good output with a 150-μs delay. <p>Q indicates that this device is a Grade-1 device in accordance with the AEC-Q100 standard.</p> <p>W indicates the package has wettable flanks.</p> <p>yyy is the package designator.</p> <p>z is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).</p> <p>Q1 indicates that this device is an automotive grade (AEC-Q100) device.</p>

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
- (2) Output voltages from 0.65 V to 5.0 V in 50-mV increments are available. Contact the factory for details and availability.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [An empirical analysis of the impact of board layout on LDO thermal performance application report](#)
- Texas Instruments, [Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator application report](#)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

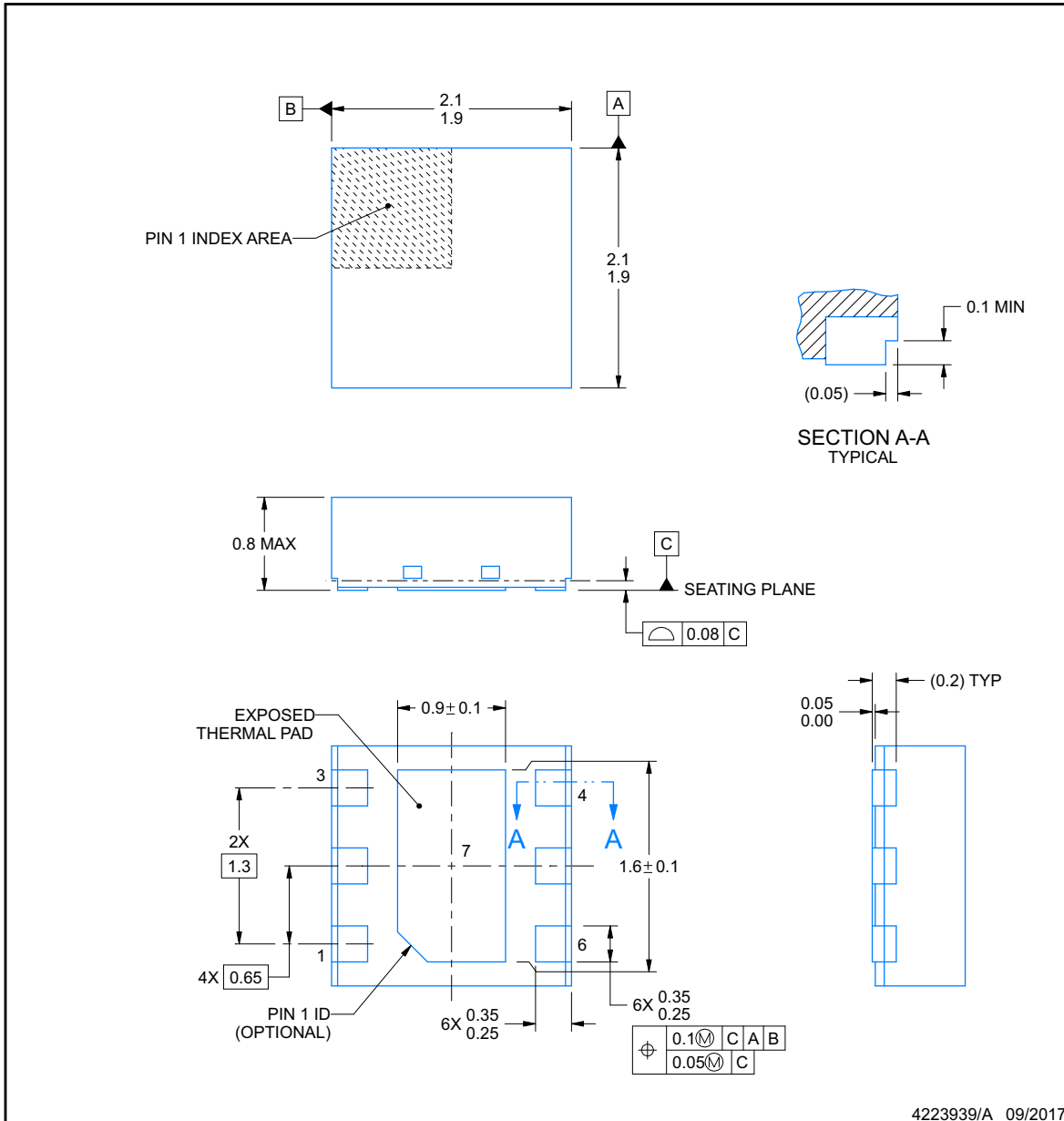


DRV0006C

PACKAGE OUTLINE

WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

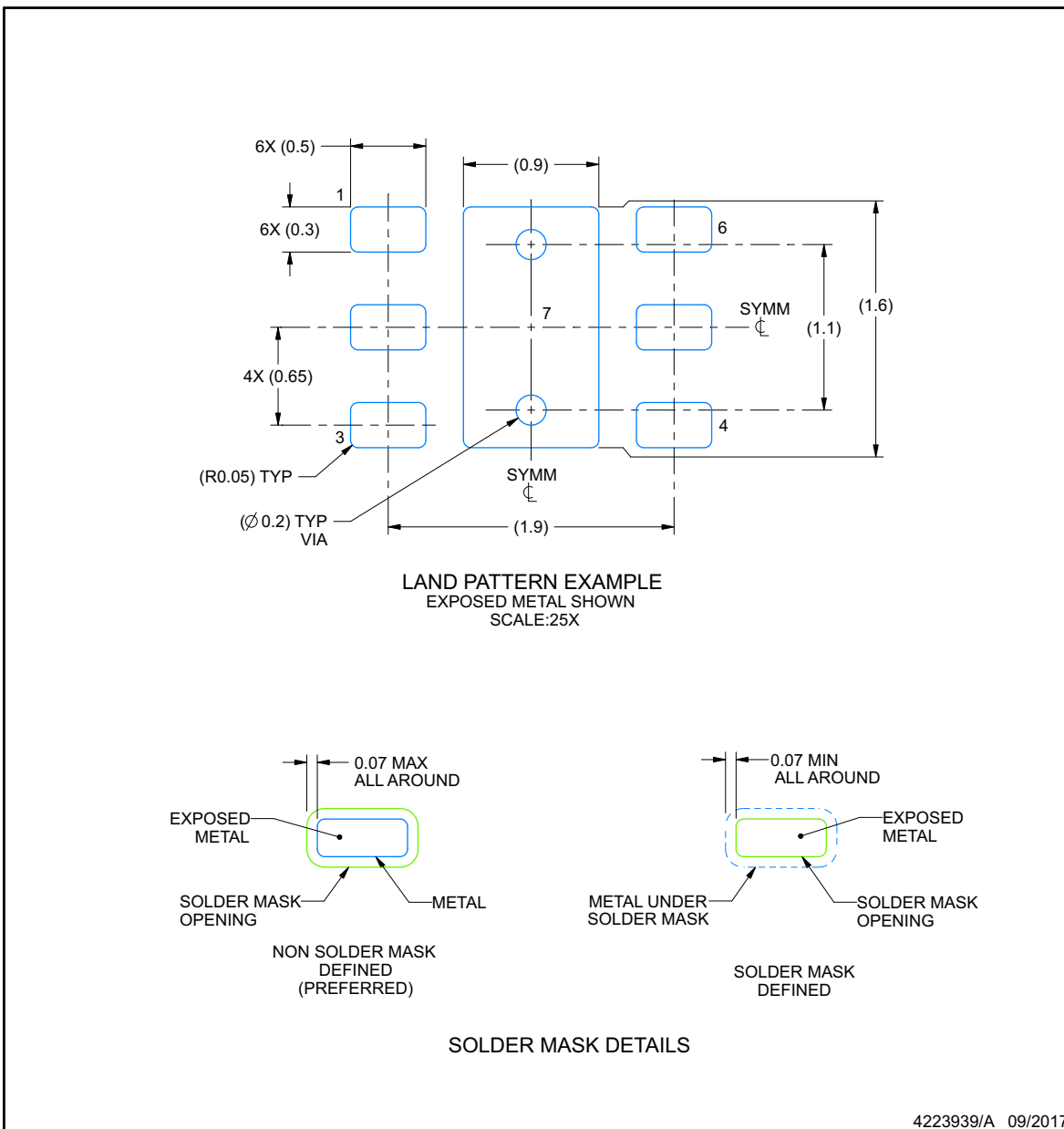
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

DRV0006C

WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

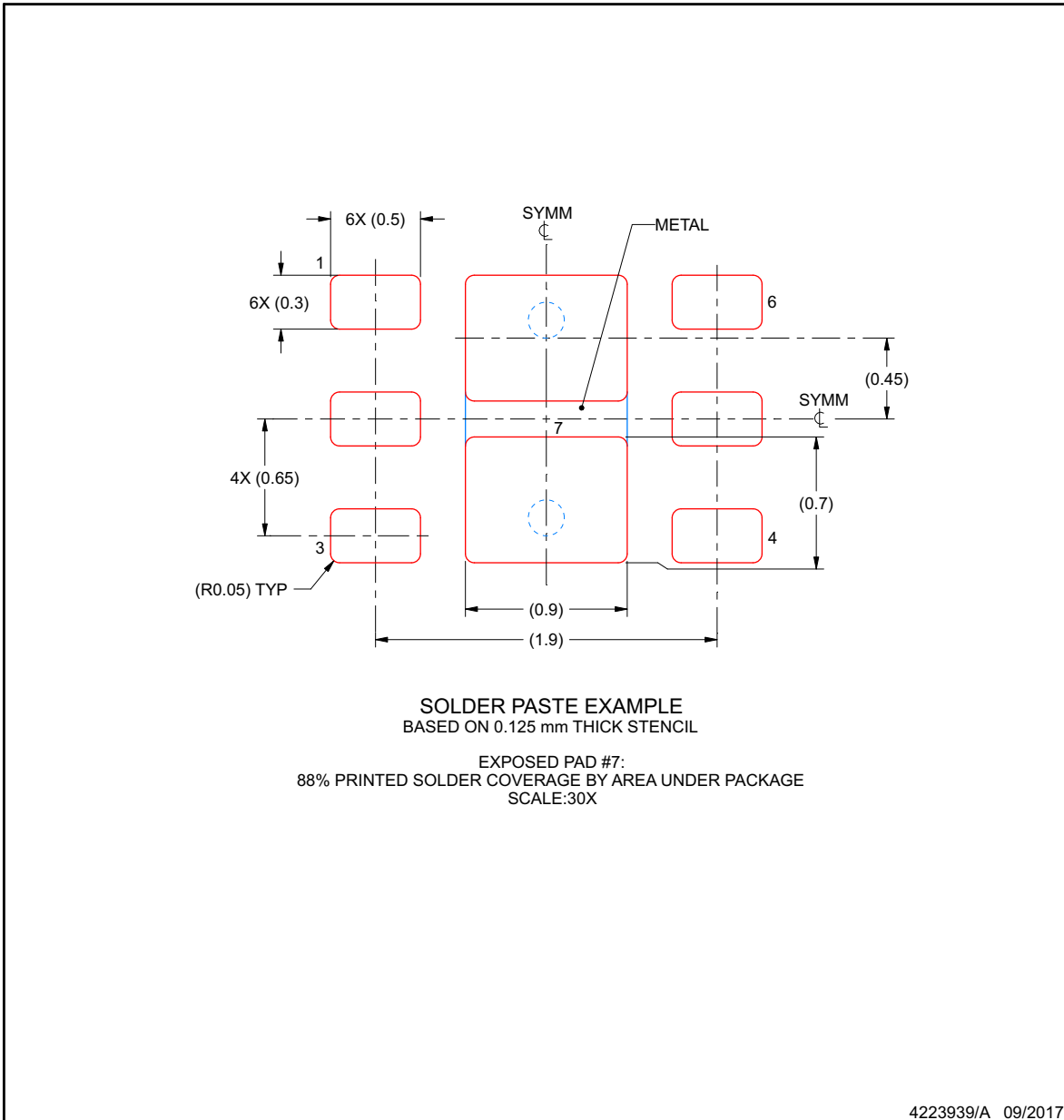
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRV0006C

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

- 5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PPS74501PQWDRBRQ1	ACTIVE	SON	DRB	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TPS74501PBQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	1S36	Samples
TPS74501PCQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	1ZF6	Samples
TPS74501PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	1S26	Samples
TPS745105PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	1S66	Samples
TPS74510PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	1S56	Samples
TPS74511PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	1S76	Samples
TPS74512PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	1S86	Samples
TPS74515PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	1S96	Samples
TPS74518PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	1SA6	Samples
TPS74522PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	1SB6	Samples
TPS74525PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	1SC6	Samples
TPS74528PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	1SD6	Samples
TPS74529PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	1SE6	Samples
TPS74533PCQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	1ZE6	Samples
TPS74533PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	1SF6	Samples
TPS74550PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	1T36	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS745-Q1 :

- Catalog: [TPS745](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

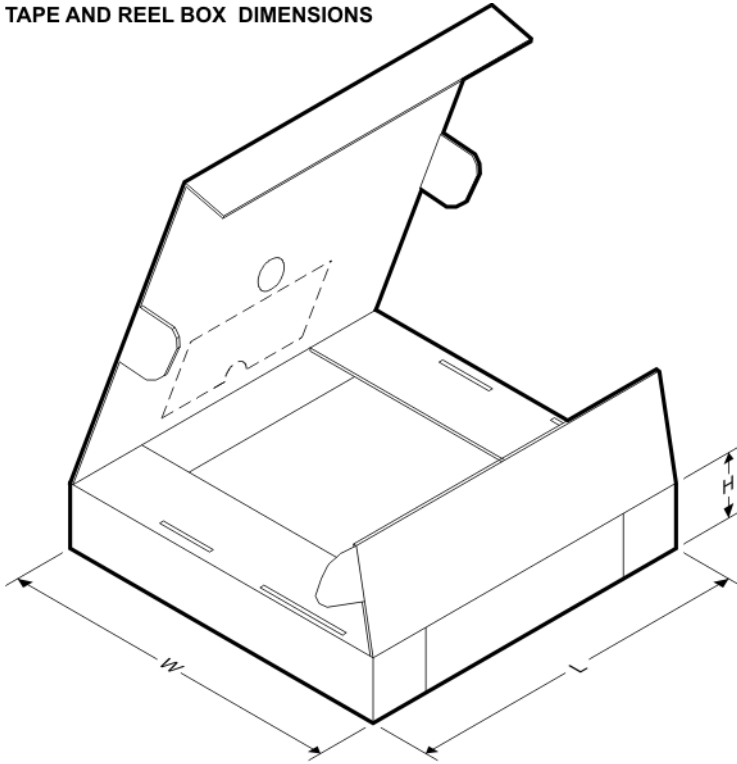


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74501PBQWDRVRQ1	WSO	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74501PCQWDRVRQ1	WSO	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74501PQWDRVRQ1	WSO	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS745105PQWDRVRQ1	WSO	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74510PQWDRVRQ1	WSO	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74511PQWDRVRQ1	WSO	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74512PQWDRVRQ1	WSO	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74515PQWDRVRQ1	WSO	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74518PQWDRVRQ1	WSO	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74522PQWDRVRQ1	WSO	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74525PQWDRVRQ1	WSO	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74528PQWDRVRQ1	WSO	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74529PQWDRVRQ1	WSO	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74533PCQWDRVRQ1	WSO	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74533PQWDRVRQ1	WSO	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74550PQWDRVRQ1	WSO	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74501PBQWDRVRQ1	WSO	DRV	6	3000	203.0	203.0	35.0
TPS74501PCQWDRVRQ1	WSO	DRV	6	3000	203.0	203.0	35.0
TPS74501PQWDRVRQ1	WSO	DRV	6	3000	203.0	203.0	35.0
TPS745105PQWDRVRQ1	WSO	DRV	6	3000	203.0	203.0	35.0
TPS74510PQWDRVRQ1	WSO	DRV	6	3000	203.0	203.0	35.0
TPS74511PQWDRVRQ1	WSO	DRV	6	3000	203.0	203.0	35.0
TPS74512PQWDRVRQ1	WSO	DRV	6	3000	203.0	203.0	35.0
TPS74515PQWDRVRQ1	WSO	DRV	6	3000	203.0	203.0	35.0
TPS74518PQWDRVRQ1	WSO	DRV	6	3000	203.0	203.0	35.0
TPS74522PQWDRVRQ1	WSO	DRV	6	3000	203.0	203.0	35.0
TPS74525PQWDRVRQ1	WSO	DRV	6	3000	203.0	203.0	35.0
TPS74528PQWDRVRQ1	WSO	DRV	6	3000	203.0	203.0	35.0
TPS74529PQWDRVRQ1	WSO	DRV	6	3000	203.0	203.0	35.0
TPS74533PCQWDRVRQ1	WSO	DRV	6	3000	203.0	203.0	35.0
TPS74533PQWDRVRQ1	WSO	DRV	6	3000	203.0	203.0	35.0
TPS74550PQWDRVRQ1	WSO	DRV	6	3000	203.0	203.0	35.0

DRB 8

GENERIC PACKAGE VIEW

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

GENERIC PACKAGE VIEW

DRV 6

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4206925/F

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