LMC6032 CMOS Dual Operational Amplifier

Check for Samples: LMC6032

FEATURES

- Specified for 2 kΩ and 600 Ω Loads
- High Voltage Gain: 12 dB
- Low Offset Voltage Drift: 2.3 μV/°C
- Ultra Low Input Bias Current: 40 fA
- Input Common-mode Range Includes V^-
- Operating Range From +5V to +15V Supply
- I_{SS} = 400 μA/Amplifier; Independent of V^+
- Low Distortion: 0.01% at 10 kHz
- Slew Rate: 1.1 V/μs
- Improved Performance Over TLC272

APPLICATIONS

- High-Impedance Buffer or Preamplifier
- Current-to-Voltage Converter
- Long-Term Integrator
- Sample-and-Hold Circuit
- Medical Instrumentation

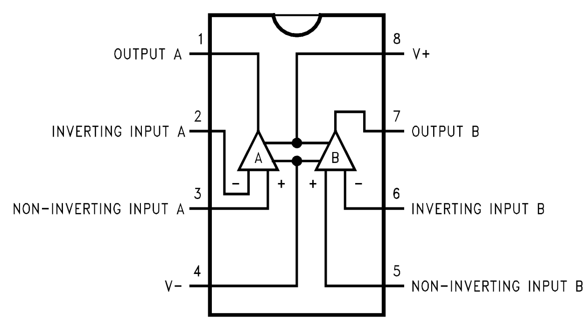
DESCRIPTION

The LMC6032 is a CMOS dual operational amplifier which can operate from either a single supply or dual supplies. Its performance features include an input common-mode range that reaches ground, low input bias current, and high voltage gain into realistic loads, such as 2 kΩ and 600 Ω.

This chip is built with TI's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6034 datasheet for a CMOS quad operational amplifier with these same features. For higher performance characteristics refer to the LMC662.

CONNECTION DIAGRAMS



8-Pin PDIP/SOIC
Top View

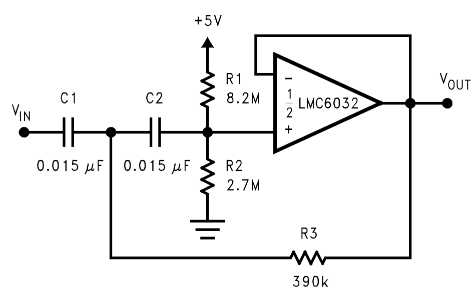


Figure 1. 10 Hz High-Pass Filter

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1]

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	See[2]
Output Short Circuit to V^-	See[3]
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance[4]	1000V
Power Dissipation	See[5]
Voltage at Output/Input Pin	(V^+) + 0.3V
	(V^-) − 0.3V
Current at Output Pin	±18 mA
Current at Input Pin	±5 mA
Current at Power Supply Pin	35 mA

(1) Absolute Maximum Ratings indicate limits beyond which damage to component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.
(2) Do not connect output to V^+, when V^+ is greater than 13V or reliability may be adversely affected.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(4) Human body model, 100 pF discharged through a 1.5 kΩ resistor.
(5) The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Operating Ratings[1]

Temperature Range		$-40°C \leq T_J \leq +85°C$
Supply Voltage Range		4.75V to 15.5V
Power Dissipation		[2]
Thermal Resistance (θ_{JA})[3]	8-Pin PDIP	101°C/W
	8-Pin SOIC	165°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.
(2) For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.
(3) All numbers apply for packages soldered directly into a PC board.

DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = GND = 0V, V_{CM} = 1.5V, V_{OUT} = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions		Typical (1)	LMC6032I Limit (2)	Units
V_{OS}	Input Offset Voltage			1	9	mV
					11	max
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Average Drift			2.3		μV/°C
I_B	Input Bias Current			0.04		pA
					200	max
I_{OS}	Input Offset Current			0.01		pA
					100	max
R_{IN}	Input Resistance			>1		TeraΩ
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 12V V^+ = 15V		83	63	dB
					60	min
+PSRR	Positive Power Supply Rejection Ratio	5V ≤ V^+ ≤ 15V V_O = 2.5V		83	63	dB
					60	min
−PSRR	Negative Power Supply Rejection Ratio	0V ≤ V^- ≤ −10V		94	74	dB
					70	min
V_{CM}	Input Common-Mode Voltage Range	V^+ = 5V & 15V For CMRR ≥ 50 dB		−0.4	−0.1	V
					0	max
				V^+ − 1.9	V^+ − 2.3	V
					V^+ − 2.6	min
A_V	Large Signal Voltage Gain	R_L = 2 kΩ (3)	Sourcing	2000	200	V/mV
					100	min
			Sinking	500	90	V/mV
					40	min
		R_L = 600Ω (3)	Sourcing	1000	100	V/mV
					75	min
			Sinking	250	50	V/mV
					20	min

(1) Typical values represent the most likely parametric normal.
(2) All limits are specified at room temperature (standard type face) or at operating temperature extremes (bold type face).
(3) V^+ = 15V, V_{CM} = 7.5V, and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = GND = 0V, V_{CM} = 1.5V, V_{OUT} = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typical (1)	LMC6032I Limit (2)	Units
V_O	Output Voltage Swing	V^+ = 5V R_L = 2 kΩ to 2.5V	4.87	4.20	V
				4.00	min
			0.10	0.25	V
				0.35	max
		V^+ = 5V R_L = 600Ω to 2.5V	4.61	4.00	V
				3.80	min
			0.30	0.63	V
				0.75	max
		V^+ = 15V R_L = 2 kΩ to 7.5V	14.63	13.50	V
				13.00	min
			0.26	0.45	V
				0.55	max
		V^+ = 15V R_L = 600Ω to 7.5V	13.90	12.50	V
				12.00	min
			0.79	1.45	V
				1.75	max
I_O	Output Current	V^+ = 5V Sourcing, V_O = 0V Sinking, V_O = 5V	22	13	mA
				9	min
			21	13	mA
				9	min
		V^+ = 15V Sourcing, V_O = 0V Sinking, V_O = 13V(4)	40	23	mA
				15	min
			39	23	mA
				15	min
I_S	Supply Current	Both Amplifiers V_O = 1.5V	0.75	1.6	mA
				1.9	max

(4) Do not connect output to V^+, when V^+ is greater than 13V or reliability may be adversely affected.

AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = GND = 0V, V_{CM} = 1.5V, V_{OUT} = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typical (1)	LMC6032I Limit (2)	Units
SR	Slew Rate	See (3)	1.1	0.8	V/μs
				0.4	min
GBW	Gain-Bandwidth Product		1.4		MHz
$φ_M$	Phase Margin		50		Deg
G_M	Gain Margin		17		dB
	Amp-to-Amp Isolation	See (4)	130		dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	22		$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002		$pA/\sqrt{Hz}$
THD	Total Harmonic Distortion	F = 10 kHz, A_V = −10 R_L = 2 kΩ, V_O = 8 V_{PP} ±5V Supply	0.01		%

(1) Typical values represent the most likely parametric normal.
(2) All limits are specified at room temperature (standard type face) or at operating temperature extremes (bold type face).
(3) V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.
(4) Input referred. V^+ = 15V and R_L = 10 kΩ connected to V^+/2. Each amp excited in turn with 1 kHz to produce V_O = 13 V_{PP}.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±7.5V, T_A = 25°C unless otherwise specified

Supply Current vs Supply Voltage

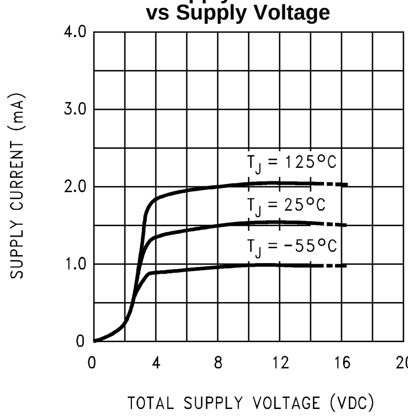


Figure 2.

Input Bias Current

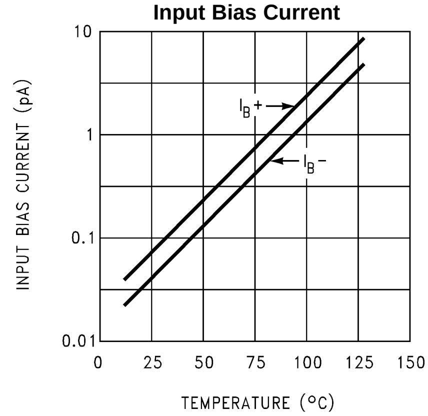


Figure 3.

Output Characteristics Current Sinking

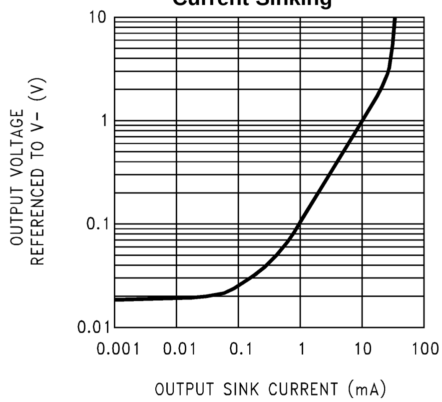


Figure 4.

Output Characteristics Current Sourcing

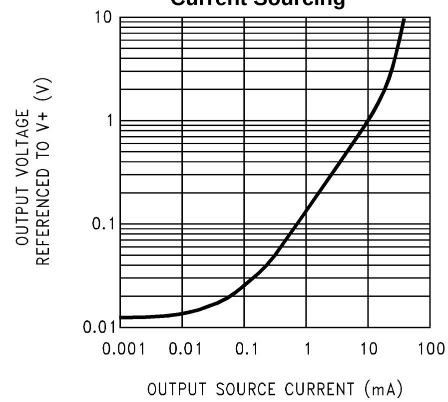


Figure 5.

Input Voltage Noise vs Frequency

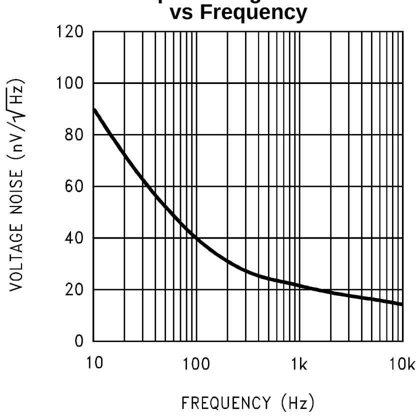


Figure 6.

CMRR vs Frequency

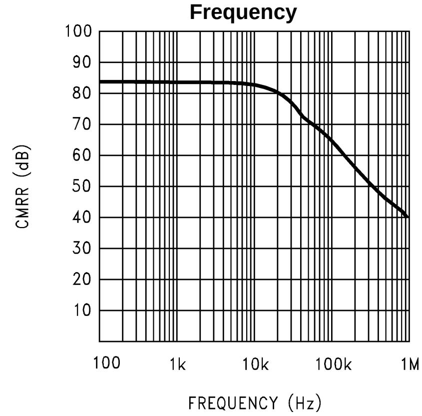


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_S = ±7.5V, T_A = 25°C unless otherwise specified

Open-Loop Frequency Response

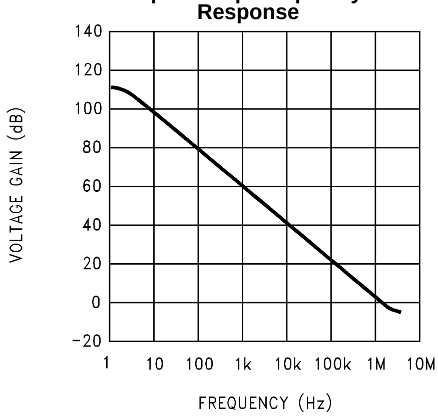


Figure 8.

Frequency Response vs Capacitive Load

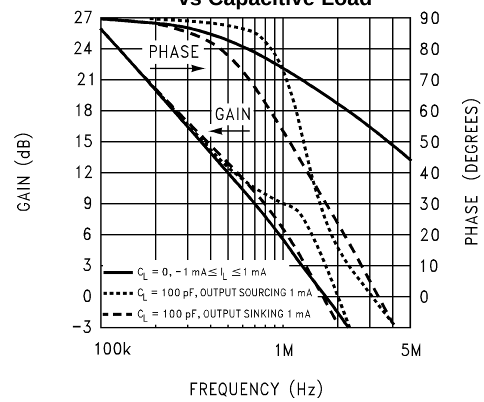


Figure 9.

Non-Inverting Large Signal Pulse Response

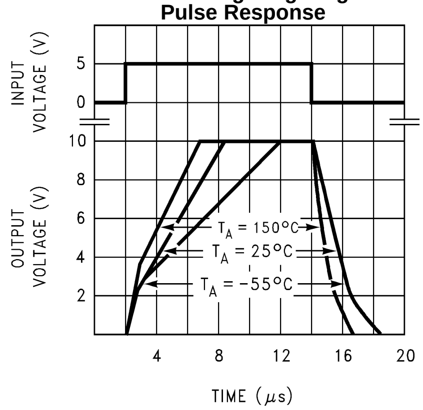


Figure 10.

Stability vs Capacitive Load

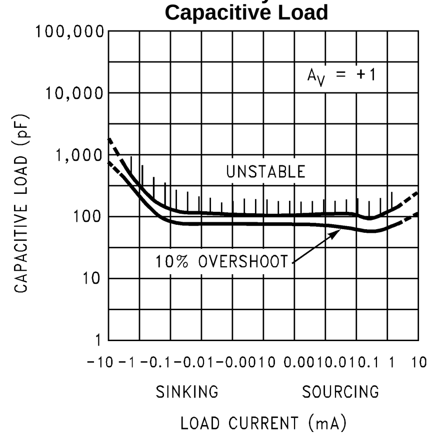


Figure 11.

Stability vs Capacitive Load

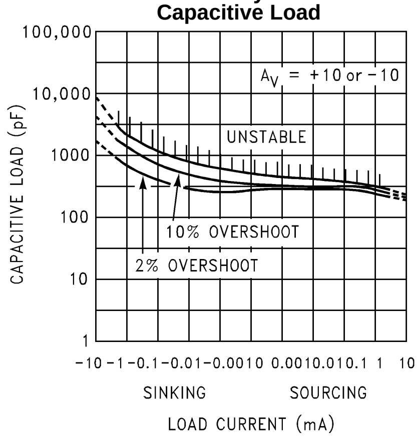


Figure 12.

Stability vs Capacitive Load

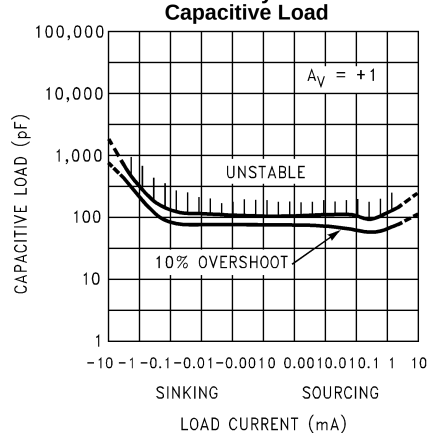
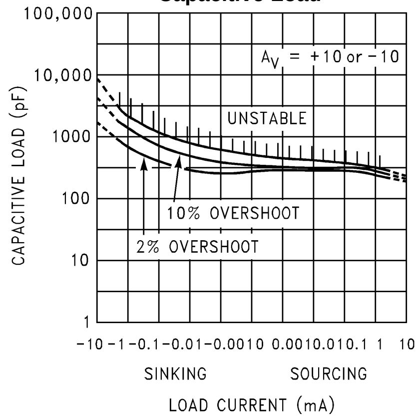


Figure 13.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_S = ±7.5V, T_A = 25°C unless otherwise specified

Stability vs Capacitive Load



Avoid resistive loads of less than 500Ω, as they may cause instability.

Figure 14.

APPLICATION HINTS

AMPLIFIER TOPOLOGY

The topology chosen for the LMC6032, shown in Figure 15, is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow a larger output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

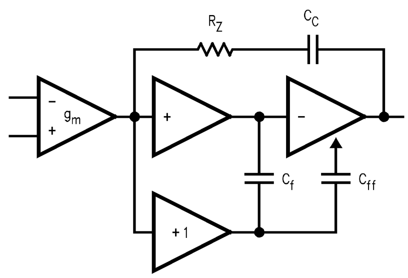


Figure 15. LMC6032 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, even with a 600Ω load. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, under heavy load (600Ω) the gain will be reduced as indicated in the Electrical Characteristics.

COMPENSATING INPUT CAPACITANCE

The high input resistance of the LMC6032 op amps allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. In the following General Operational Amplifier Circuit, Figure 16, the frequency of this pole is

$$f_P = \frac{1}{2\pi C_S R_P}$$

where C_S is the total capacitance at the inverting input, including amplifier input capacitance and any stray capacitance from the IC socket (if one is used), circuit board traces, etc., and $R_P$is the parallel combination of R_F and R_{IN}. This formula, as well as all formulae derived below, apply to inverting and non-inverting op-amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole will be quite high, since $C_S$is generally less than 10 pF. If the frequency of the feedback pole is much higher than the “ideal” closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of C_S), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the “ideal” −3 dB frequency, a feedback capacitor, C_F, should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier's low-frequency noise gain: To maintain stability, a feedback capacitor will probably be needed if

$$\left(\frac{R_F}{R_{IN}} + 1\right) \leq \sqrt{6 \times 2\pi \times GBW \times R_F \times C_S}$$

where

$$\left(\frac{R_F}{R_{IN}} + 1\right)$$

is the amplifier's low-frequency noise gain and GBW is the amplifier's gain bandwidth product. An amplifier's low-frequency noise gain is represented by the formula

$$\left(\frac{R_F}{R_{IN}} + 1\right)$$

regardless of whether the amplifier is being used in an inverting or non-inverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \geq 2\sqrt{GBW \times R_F \times C_S}\ ,$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1\right)}$$

If

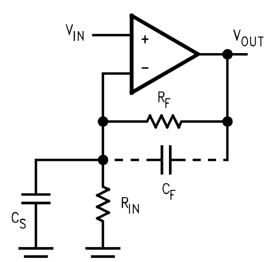
$$\left(\frac{R_F}{R_{IN}} + 1\right) < 2\sqrt{GBW \times R_F \times C_S}\ ,$$

the feedback capacitor should be:

$$C_F = \sqrt{\frac{C_S}{GBW \times R_F}}$$

Note that these capacitor values are usually significantly smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F}.$$



C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistor.

Figure 16. General Operational Amplifier Circuit

Using the smaller capacitors will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the value of C_F should be checked on the actual circuit, starting with the computed value.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC6032 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in Figure 17, the addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

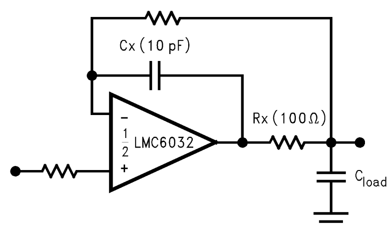


Figure 17. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 18). Typically a pull up resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see DC Electrical Characteristics).

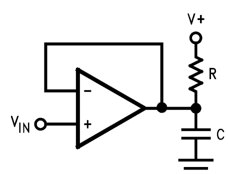


Figure 18. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6032, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6032's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See Figure 19. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of 10^{12}Ω, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC6032's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of 10^{11}Ω would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See Figure 20, Figure 21, Figure 22 for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 23.

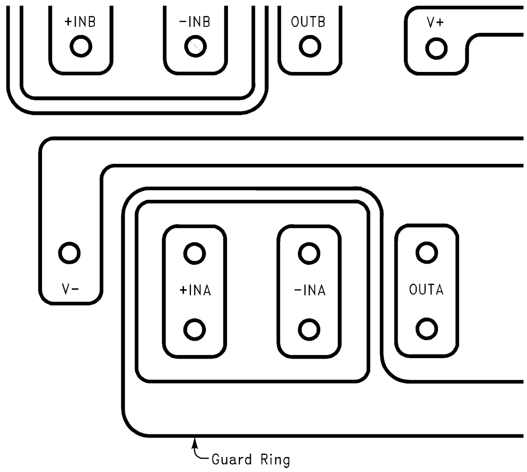


Figure 19. Example of Guard Ring in P.C. Board Layout

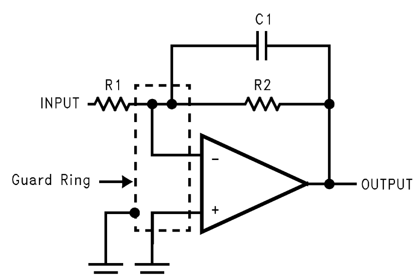


Figure 20. Inverting Amplifier Guard Ring Connections

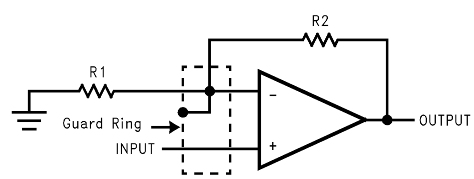


Figure 21. Non-Inverting Amplifier Guard Ring Connections

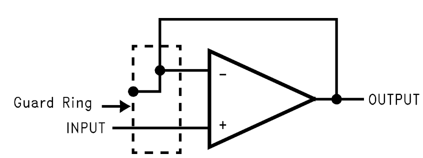


Figure 22. Follower Guard Ring Connections

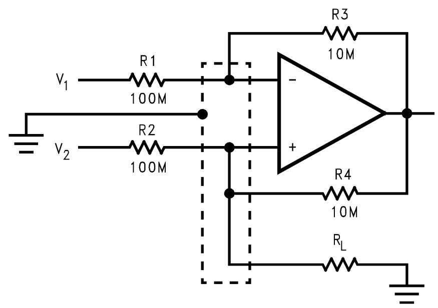
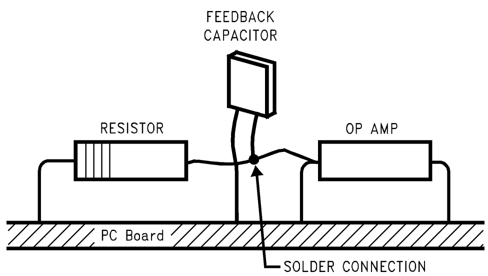


Figure 23. Howland Current Pump Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 24.



Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.

Figure 24. Air Wiring

BIAS CURRENT TESTING

The test method of Figure 25 is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I_b^- = \frac{dV_{OUT}}{dt} \times C2.$$

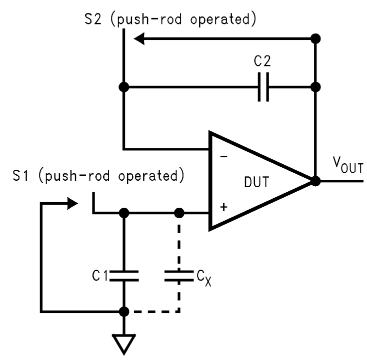


Figure 25. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I_b-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

$$I_b^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_x)$$

where C_x is the stray capacitance at the + input.

TYPICAL SINGLE-SUPPLY APPLICATIONS

($V^+ = 5.0\ V_{DC}$)

Additional single-supply applications ideas can be found in the LM358 datasheet. The LMC6032 is pin-for-pin compatible with the LM358 and offers greater bandwidth and input resistance over the LM358. These features will improve the performance of many existing single-supply applications. Note, however, that the supply voltage range of the LMC6032 is smaller than that of the LM358.

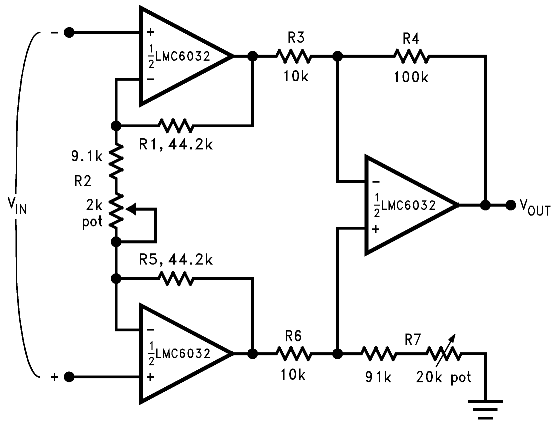


Figure 26. Instrumentation Amplifier

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

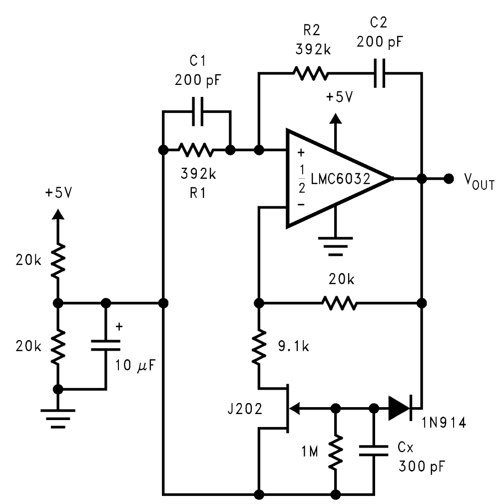
if R1 = R5;

R3 = R6,

and R4 = R7.

= 100 for circuit shown.

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affects CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.



Oscillator frequency is determined by R1, R2, C1, and C2:

$f_{OSC} = 1/2\pi RC$

where R = R1 = R2 and C = C1 = C2.

Figure 27. Sine-Wave Oscillator

This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.0V.

TYPICAL SINGLE-SUPPLY APPLICATIONS (continued)

($V^+ = 5.0\ V_{DC}$)

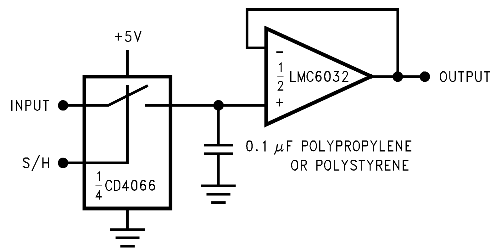


Figure 28. Low-Leakage Sample-and-Hold

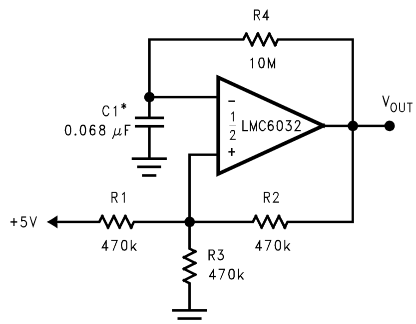


Figure 29. 1 Hz Square-Wave Oscillator

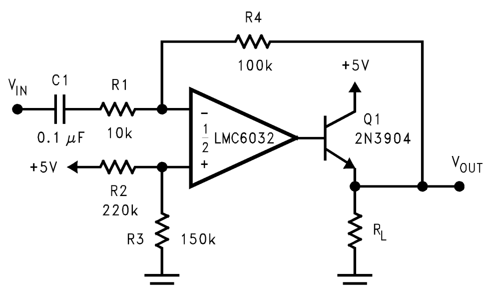
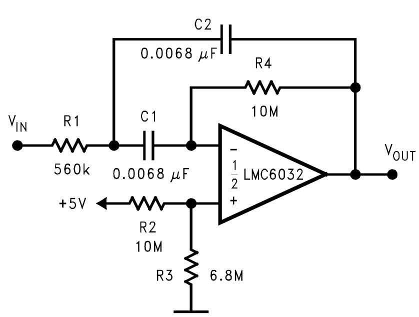


Figure 30. Power Amplifier



f_O = 10 Hz
Q = 2.1
Gain = −8.8

Figure 31. 10 Hz Bandpass Filter

TYPICAL SINGLE-SUPPLY APPLICATIONS (continued)

($V^+ = 5.0\ V_{DC}$)

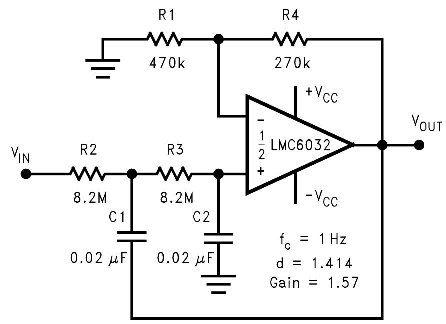
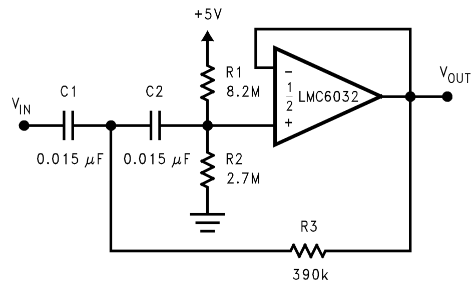
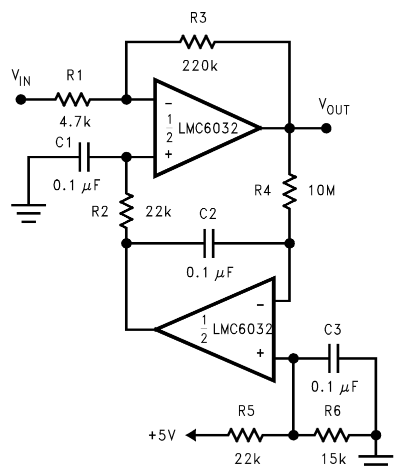


Figure 32. 1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



f_c = 10 Hz
d = 0.895
Gain = 1
2 dB passband ripple

Figure 33. 10 Hz High-Pass Filter



Gain = −46.8
Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV).

Figure 34. High Gain Amplifier with Offset Voltage Reduction

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6032IM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMC60 32IM	
LMC6032IM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC60 32IM	Samples
LMC6032IMX	NRND	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	LMC60 32IM	
LMC6032IMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC60 32IM	Samples
LMC6032IN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	LMC 6032IN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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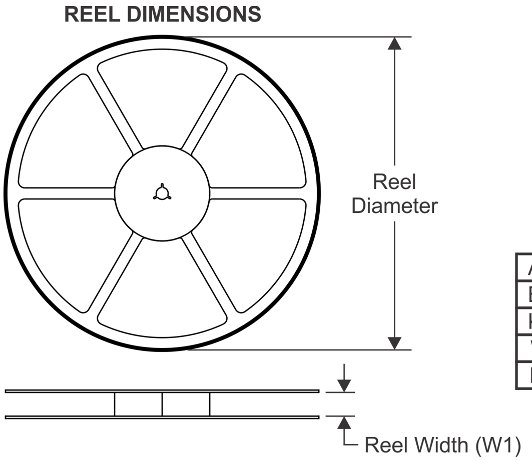
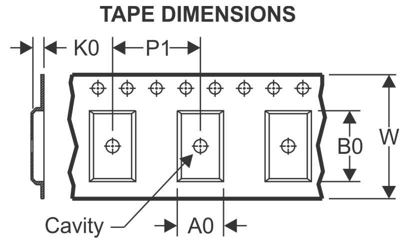
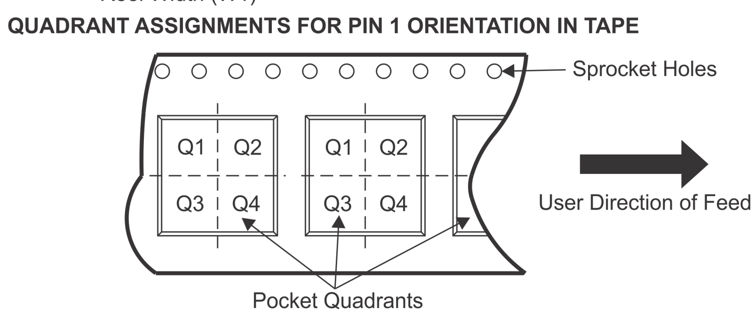




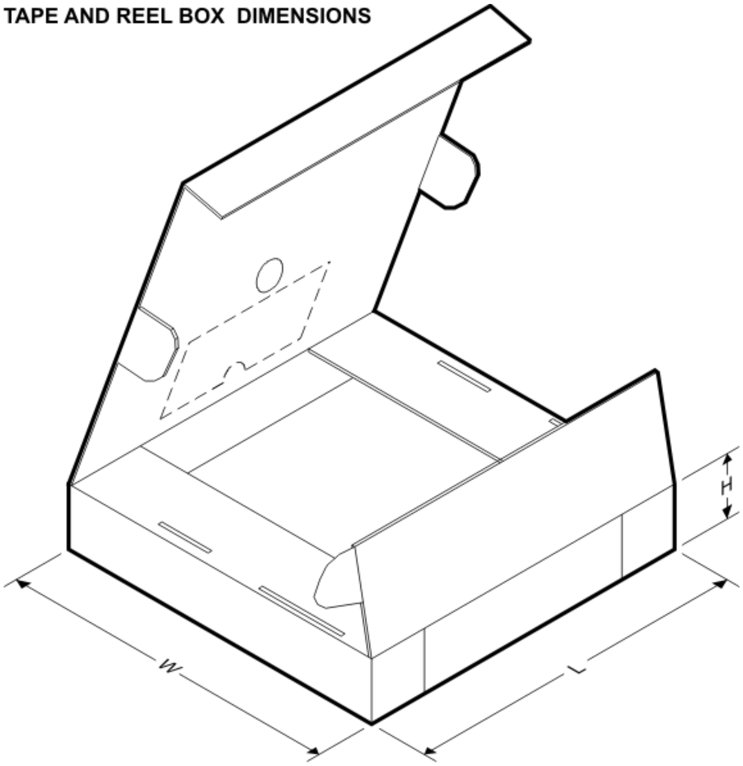
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6032IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

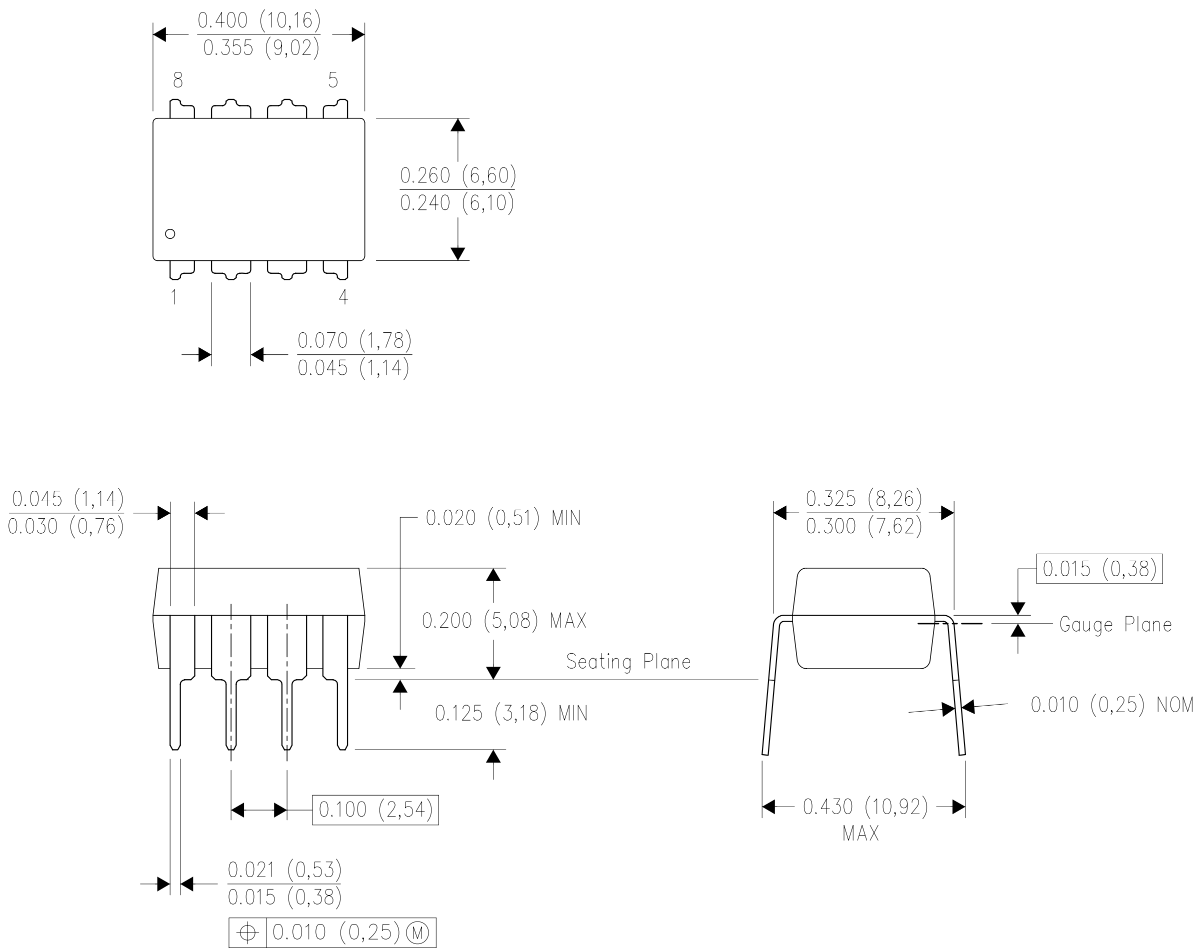
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6032IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



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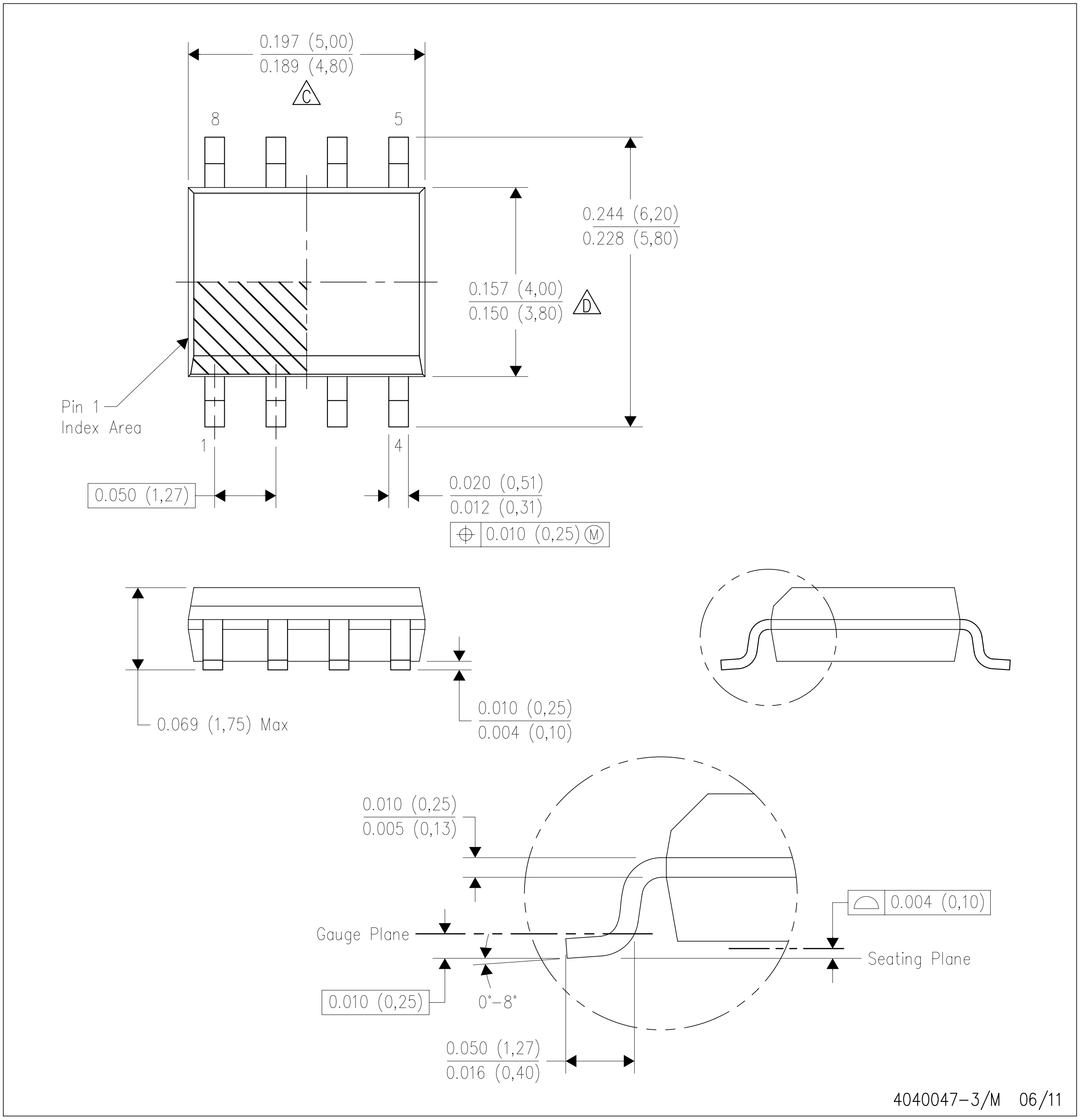
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

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