PROCESS CP710V

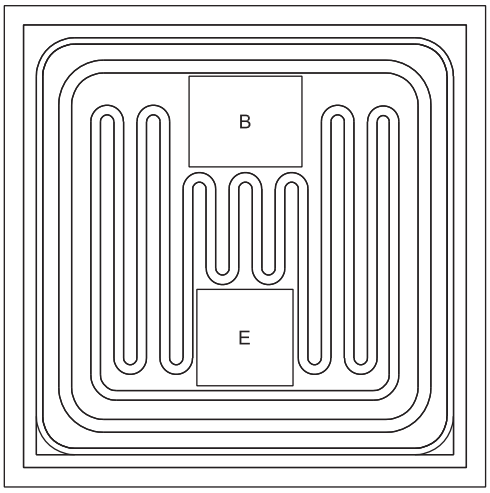
Small Signal Transistor

PNP - High Voltage Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	26 x 26 MILS
Die Thickness	7.1 MILS
Base Bonding Pad Area	6.1 x 4.9 MILS
Emitter Bonding Pad Area	5.2 x 5.2 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



BACKSIDE COLLECTOR R2

GROSS DIE PER 5 INCH WAFER

25,214

PRINCIPAL DEVICE TYPES

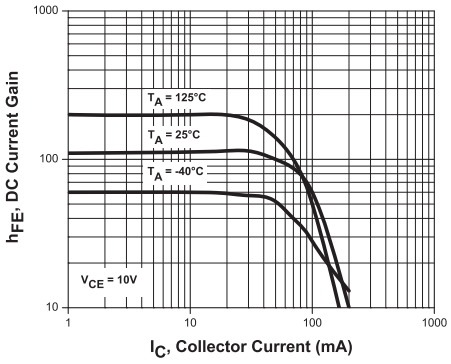
CMLTA94
CMPTA94
CMPTA92E
CXTA92
CZTA92
CZTA94

R0 (5-August 2010)

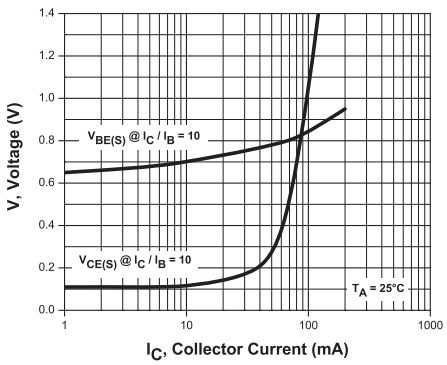
PROCESS CP710V

Typical Electrical Characteristics

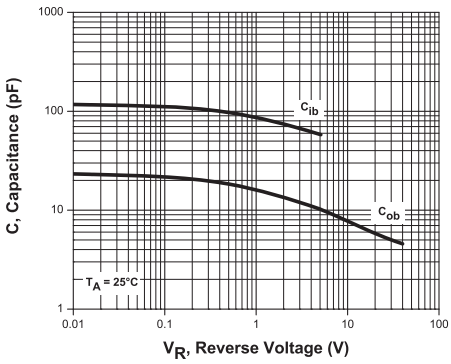
DC Current Gain



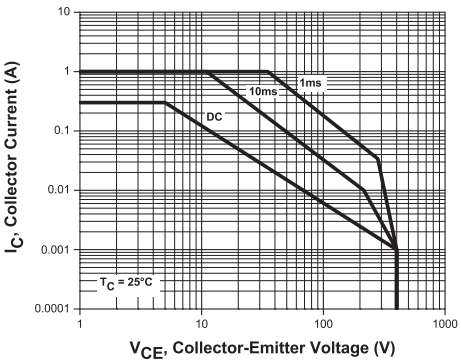
"ON" Voltage



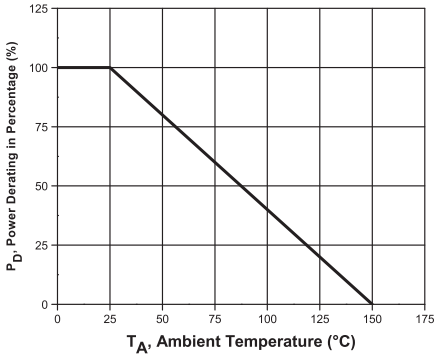
Capacitance



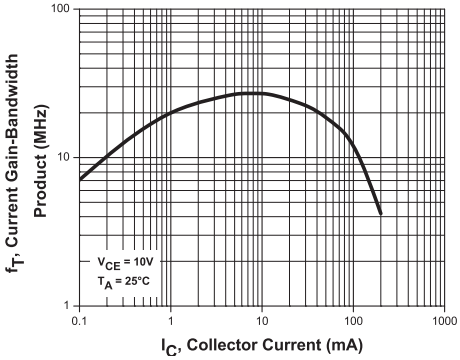
Safe Operating Area



Normalized Power Derating



Current Gain-Bandwidth Product



R0 (5-August 2010)