AC/DC Drivers

AC/DC controller IC for LED lighting

BD521GOFJ

General Description

BD521GOFJ is an AC/DC converter for LED lighting. This IC can be applied to quasi-resonant typed high-side LED driver application, and the high current precision and low EMI noise can be achieved. Moreover, owing to the built-in PFC (Power Factor Correction) converter, the harmonic is improved.

By choosing the external MOSFET, the LED drivers for from low power to high power can be achieved. So that, it can be widely used on from the low power lighting such as spotlight to the high power lighting such as base light.

Owing to the external current setting resistance, a power supply design with a high degree of freedom can be achieved.

Features

- Quasi-resonant Switching Mode + PFC Circuit
- Non-isolated Application
- Maximum Frequency 300kHz
- VCC Pin: Under Voltage Protection
- VCC Pin: Over Voltage Protection (Latch)
- CS Pin: Leading-Edge-Blanking Function
- CS Pin: OPEN Protection Function
- LED Over Current Detection Function

Package

SOP-J8

W(Typ) x D(Typ) x H(Max)

4.90mm x 6.00mm x 1.65mm



Key Specifications

- Operating Power Supply Voltage Range: VCC 8.9V to 25.0V
- Operating Current: Normal Operation: 400μA (Typ)
- Operating Temperature Range: - 40°C to +105°C

Application

LED Bulb, Down-light, Tube Light etc.
Electrical Machineries for LED Lighting

Typical Application Circuit

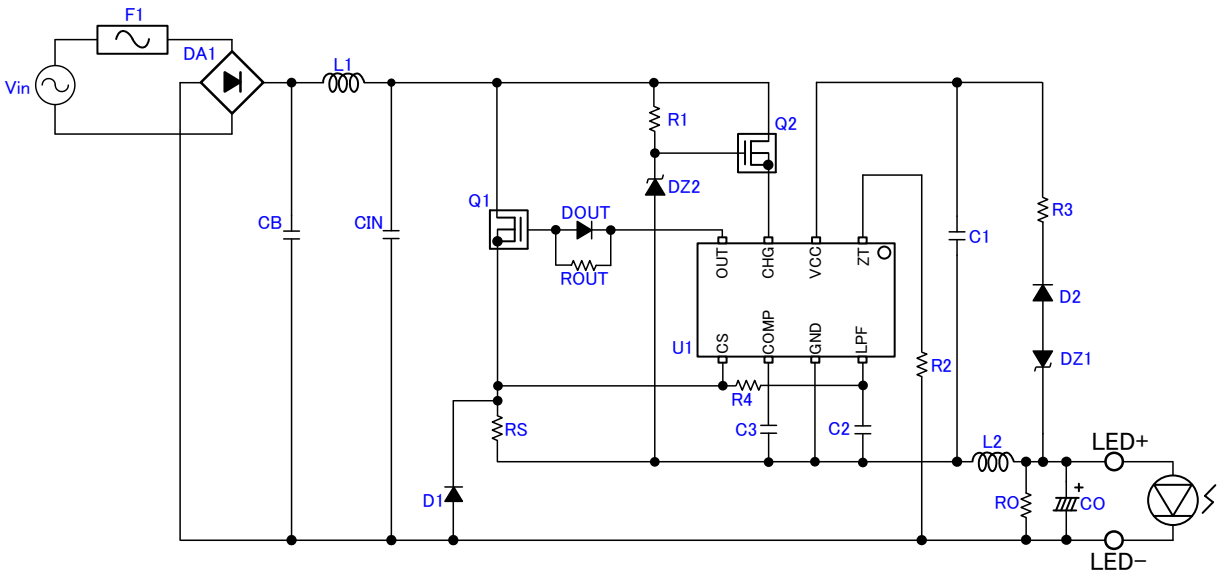


Figure 1. Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit	Condition
Input Voltage Range 1	Vmax1	-0.3 to 30	V	VCC, CHG
Input Voltage Range 2	Vmax2	-0.3 to 6.5	V	CS, COMP, LPF, ZT
Input Voltage Range 3	Vmax3	-0.3 to 15.5	V	OUT
Operating Temperature Range	Topr	-40 to +105	°C	
Maximum Junction Temperature	Tjmax	150	°C	
Storage Temperature Range	Tstg	-55 to+150	°C	

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
SOP-J8				
Junction to Ambient	θ_{JA}	149.3	76.9	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	18	11	°C/W

*(Note 1)*Based on JESD51-2A(Still-Air)
*(Note 2)*The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
*(Note 3)*Using a PCB board based on JESD51-3.
*(Note 4)*Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

Recommended Operating Condition (Ta=25°C)

Item	Symbol	Range	Unit	Condition
Input Voltage Range	Vcc	8.9 to 25.0	V	VCC Voltage

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Electrical Characteristics (Unless otherwise specified V_{CC}=15 V Ta = 25°C)

Item	Symbol	Specification			Unit	Condition
		Min	Typ	Max		
[Circuit Current]						
Circuit Current (ON)	I_{ON}	-	400	800	μA	ZT=0V(Pulse Operating)
Circuit Current (OFF)	I_{OFF}	-	300	600	μA	ZT=1V(Pulse OFF)
[CHG Pin Charge Circuit]						
CHG Charge Current 1	I_{START1}	0.25	0.35	0.45	mA	VCC= 0V,CHG=15V
CHG Charge Current 2	I_{START2}	2	6	12	mA	VCC=10V,CHG=15V
CHG OFF Current	I_{START3}	3	6	9	μA	VCC UVLO Released CHG Pin Sink Current CHG=15V
CHG Charge Current Switching Voltage	V_{SC}	0.4	0.8	1.6	V	VCC Pin
[VCC Pin Protection]						
VCC UVLO Voltage 1	V_{UVLO1}	12.5	13.5	14.5	V	VCC Rising Up
VCC UVLO Voltage 2	V_{UVLO2}	7.5	8.2	8.9	V	VCC Falling Down
VCC UVLO Hysteresis	V_{UVLO3}	-	5.3	-	V	$V_{UVLO3} = V_{UVLO1} - V_{UVLO2}$
VCC OVP Trigger Voltage	V_{OVP1}	25.0	27.5	30.0	V	VCC Rising Up
VCC OVP Release Voltage	V_{OVP2}	21.0	23.5	26.0	V	VCC Falling Down
Latch Released VCC Voltage	V_{LATCH}	-	V_{UVLO2}-0.5	-	V	VCC Falling Down
VCC Recharge Start Voltage	V_{CHG1}	7.7	8.7	9.7	V	VCC Falling Down
VCC Recharge End Voltage	V_{CHG2}	12	13	14	V	VCC Rising Up
Latch Mask Time	T_{LATCH}	75	150	300	μs	
[DC/DC Converter Block (Turn-on)]						
ZT Comparator Voltage 1	V_{ZT1}	30	110	190	mV	ZT Falling Down
ZT Comparator Voltage 2	V_{ZT2}	100	200	300	mV	ZT Rising Up
ZT Comparator Hysteresis	V_{ZTHYS}	40	90	140	mV	$V_{ZTHYS} = V_{ZT2} - V_{ZT1}$
ZT Trigger Timeout	T_{ZTOUT}	9	18	36	μs	
[DC/DC Converter Block (Turn-off)]						
Current Trigger Voltage	V_{CS}	2.60	2.95	3.30	V	
Maximum Frequency	F_{SW}	255	300	345	kHz	
Leading Edge Blank Time	T_{LEB}	0.1	0.2	0.4	μs	
Error Amplifier Reference Voltage	V_{REF}	0.582	0.600	0.618	V	
[Driver Block]						
OUT Pin High Voltage	V_{OUTH}	10.5	12.0	14.5	V	
OUT High ON Resistance	R_{OUTH}	23	45	76	Ω	I_{OUT} = -2mA
OUT Low ON Resistance	R_{OUTL}	33	65	110	Ω	I_{OUT} = +2mA

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Pin Configuration

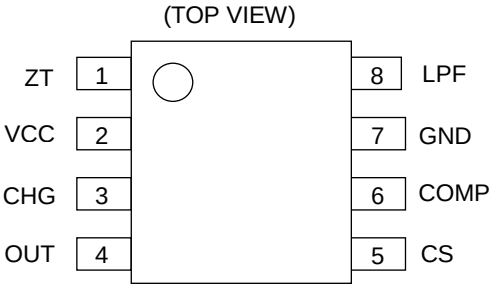


Figure 2. Pin Configuration

Pin Descriptions

Table 1. PIN Functions

NO.	Pin Name	Function
1	ZT	Zero current detecting pin
2	VCC	Power supply pin
3	CHG	Input pin of the charge circuit
4	OUT	GATE pin of the external MOSFET
5	CS	Inductor current sensing pin
6	COMP	Error amplifier output pin
7	GND	GND pin
8	LPF	Error amplifier input pin

I/O Equivalence Circuits

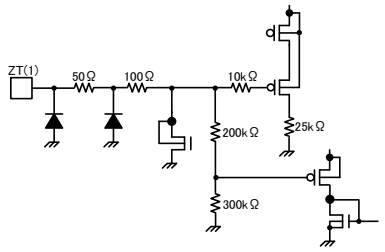
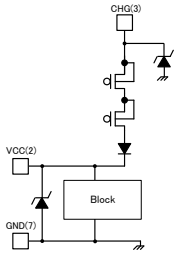
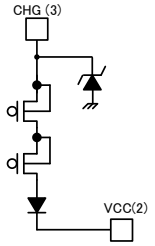
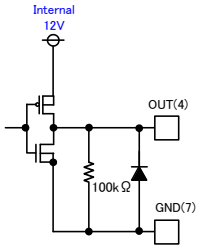
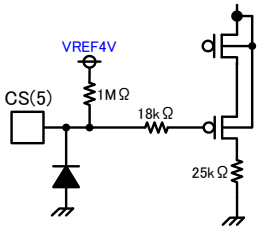
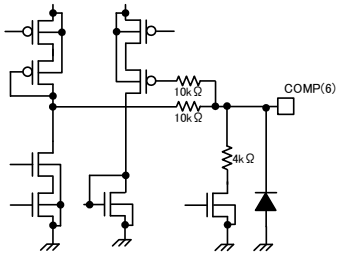
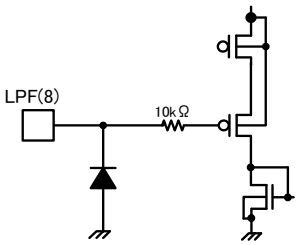
1PIN : ZT	2PIN : VCC / 7PIN : GND	3PIN : CHG
		
4PIN : OUT	**5PIN : CS**	**6PIN : COMP**
		
8PIN : LPF		
		

Figure 3. I/O Equivalent Circuits

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Block Diagram

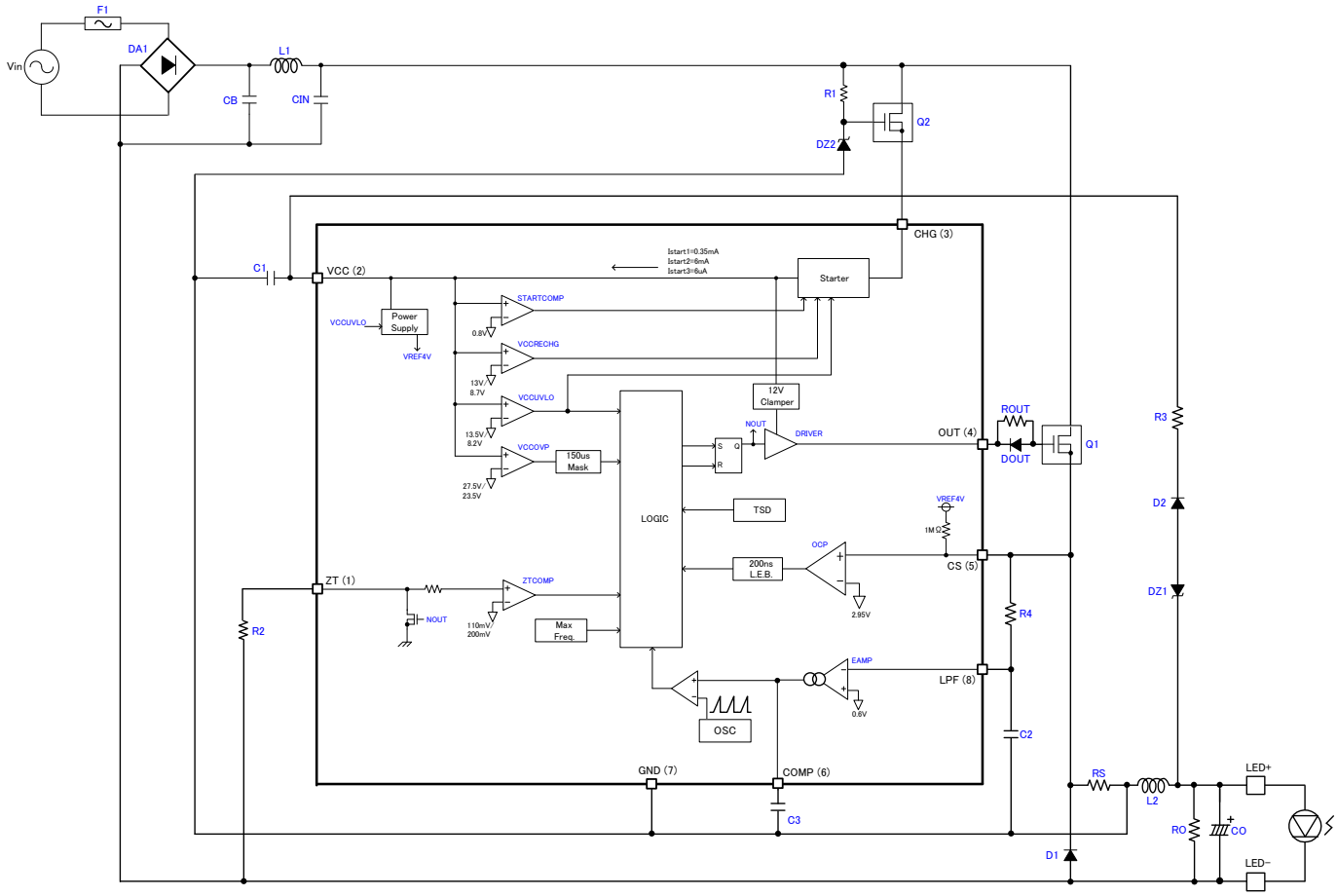


Figure 4. Block Diagram

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Description of Blocks

(1) Charge Circuit Block (VCC: 2pin, CHG: 3pin)

(1.1)Block Description

A charge circuit is built in this IC. After the IC starts up, the power consumption becomes only the idling current I_{START3} (Typ=6μA).

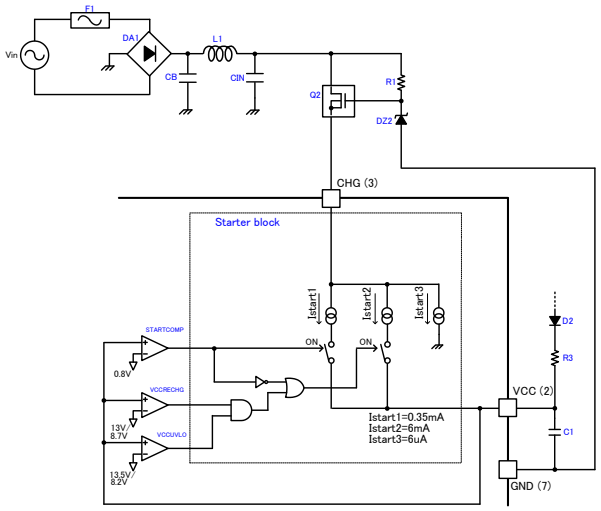


Figure 5. Charge Circuit Block Diagram

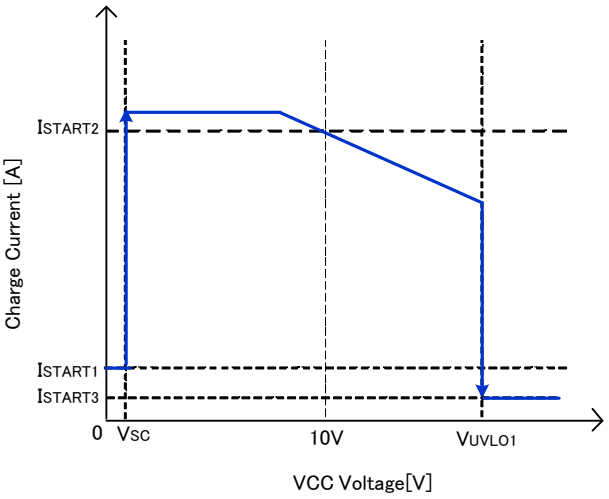


Figure 6. Charge Current－VCC Voltage Curve

For reducing the number of the components, the application schematic which consists by the starter resistor RSTR and the protection zener diode DZ3 is showed in Figure7.

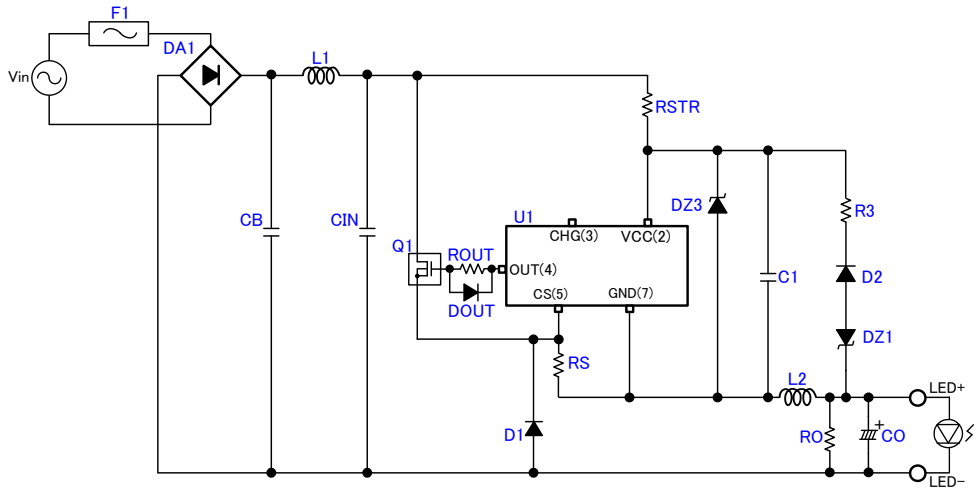


Figure 7. Application Circuit Example for DCDC (The internal charge circuit is not used)

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(1.2)Start Sequences

The time chart of the start sequences are showed in Figure 8.

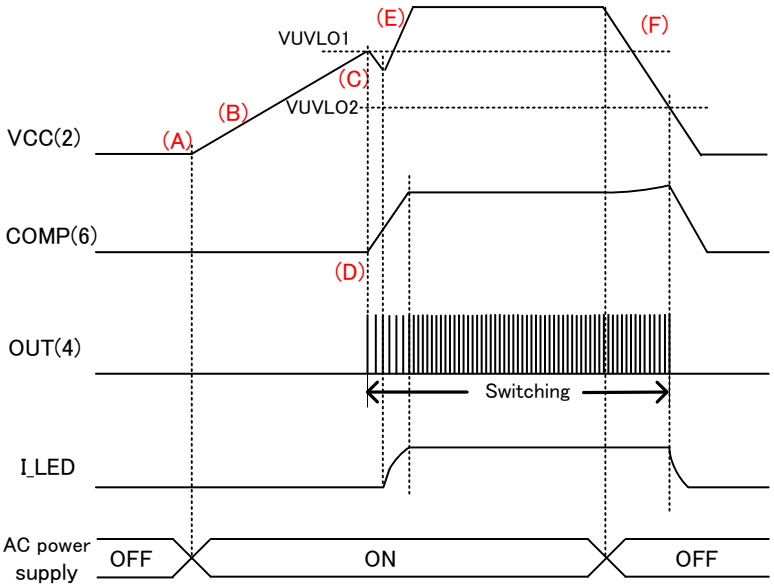


Figure 8. ON/OFF Sequences

ON/OFF Sequences

A: Input voltage is applied to CHG pin when the AC power supply turns ON.

B: The capacitor connected to the VCC pin is charged by the start-up current from the CHG pin, and the VCC rises up.

C: The IC starts operating when $V_{CC} > V_{UVLO1}$ (Typ=13.5V)

D: By the increase of the COMP pin voltage, the IC starts up with the soft-start operation.

E: The current is supplied to VCC pin from LED+ and D2 by the switching operation of OUT pin.

※The power is supplied from LED+, and the VCC voltage is determined by the V_{DZ1}(the breakdown voltage of DZ1).

$V_{CC}=V_{LED}-V_{DZ1}-Vf_{D2}$

(V_{LED}: the Vf of LED, V_{DZ1}: the breakdown voltage of DZ1, Vf_{D2}: the Vf of D2)

F: When the power supply turns OFF, VCC voltage falls down due to the drop of the power supply.

The IC turns OFF when the V_{UVLO2} (Typ=8.2V) is triggered.

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(1.3) VCC Pin Protection Functions

The VCC under voltage protection function VCC UVLO (Under Voltage Lock Out), over voltage protection function VCC OVP (Over Voltage Protection), and a VCC recharge function which operates when a voltage drop occurs at VCC pin are built in this IC. The VCC UVLO and VCC OVP functions are used for preventing from the destructions of the switching MOSFET which occurs when the VCC voltage gets too high or too low.

Owing to the VCC charge function, the VCC pin is charged by the charge circuit when the VCC voltage drops.

VCC UVLO / VCC OVP Function

VCC UVLO and VCC OVP are comparators which have voltage hysteresis.

(The comparator of VCC UVLO is auto recovery type, and the comparator of VCC OVP is latch type.)

VCC OVP has a built-in mask time T_{LATCH} (Typ=150μs).

When the VCC voltage is over V_{OVP1} (Typ=27.5V), and this state lasts T_{LATCH}, the detection is executed.

Owing to this function, the surge which occurs at VCC pin can be masked.

VCC Charge Function

When the VCC pin voltage is over V_{UVLO1} (Typ=13.5V), the IC starts up. In this case, if the VCC pin voltage drops below V_{CHG1} (Typ=8.7V), VCC charge function operates. At this time, the VCC pin is charged from the CHG pin through the charge circuit. Owing to this operation, the failure of start-up can be prevented.

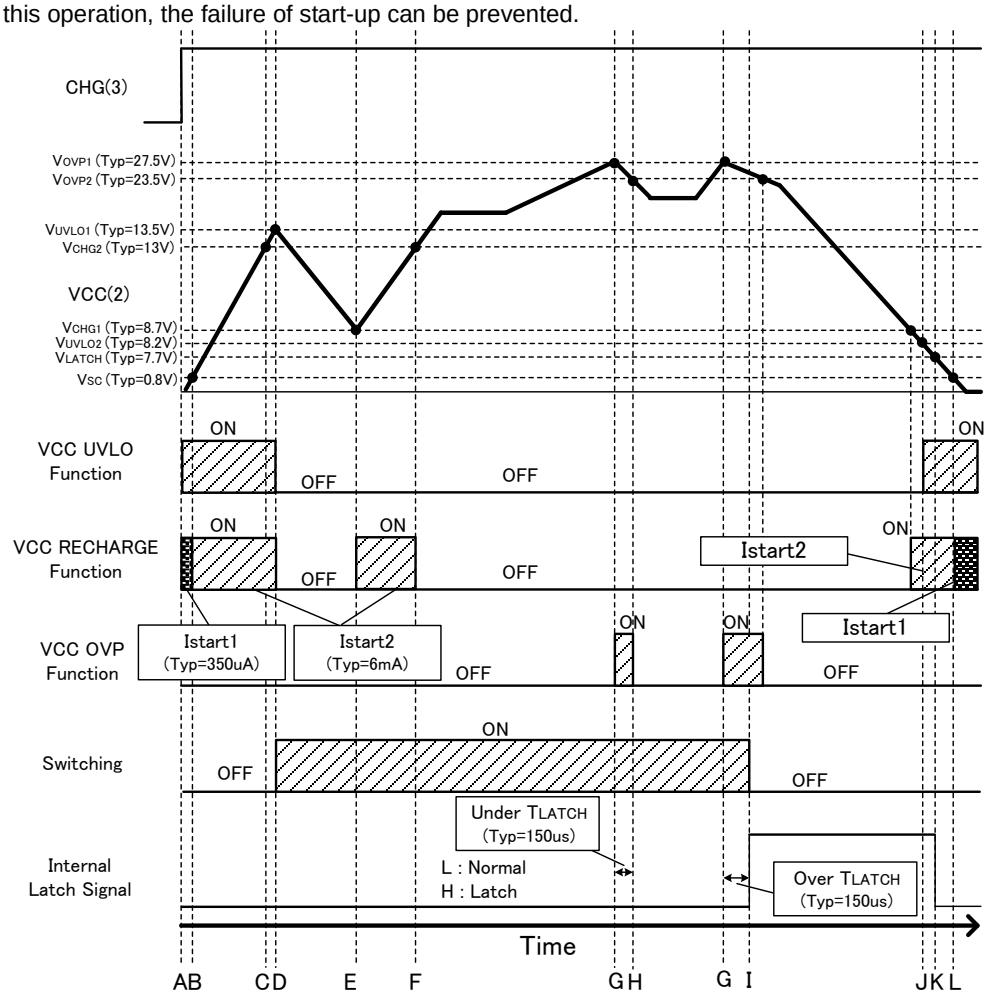


Figure 9. Timing Chart of VCC UVLO/ VCC OVP / VCC Charge Function

A: CHG pin voltage is applied, VCC voltage rises by the charging current Istart1 (Typ=350μA).
B: VCC voltage> V_{SC}(Typ=0.8V), the charging current to VCC changes from Istart1 to Istart2(Typ=6mA)
C: VCC voltage> V_{CHG2}(Typ=13V), though VCC charge function reacts, due to VCC UVLO is detected, the charge continues.
D: VCC voltage> V_{UVLO1}, the VCC UVLO is released, the DC/DC operation starts, and the VCC charge operation stops.
E: VCC voltage< V_{CHG1}, the VCC charge operation restarts.
F: VCC voltage> V_{CHG2}, the VCC charge operation stops.
G: VCC voltage> V_{OVP1}, VCC OVP is detected.
H: VCC voltage< V_{OVP2}(Typ=23.5V), if VCC voltage drops below V_{OVP2} in T_{LATCH}, VCC OVP is released, and the latch will not be activated.
I: VCC voltage > V_{OVP2}, if this state is kept longer than T_{LATCH}, the switching stops by latch.
J: VCC voltage< V_{UVLO2}(Typ=8.2V), VCC UVLO is detected.
K: VCC voltage< V_{LATCH}(Typ=7.7V), the latch state is released.
L: VCC voltage< V_{SC}, the charge current to VCC changes from Istart2 to Istart1

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(2)Error Amplifier Block (CS: 5pin, COMP: 6 pin, LPF: 8pin)

(2.1)Block Description

An error amplifier is built in this IC, the High time of the OUT pin changes by controlling the output of the error amplifier.

The voltage which occurs on the current sensing resistor RS (CS Pin Voltage) is inputted to the RC filter circuit which is composed by R4, C2. The output of the low pass filter circuit (LPF Pin Voltage) is used as the input voltage of the error amplifier, and the summation of the current which flows through the inductor L2 while the MOSFET is ON, and the current which flows through the inductor L2 from the flywheel diode D1 while the MOSFET is OFF flows through the RS.

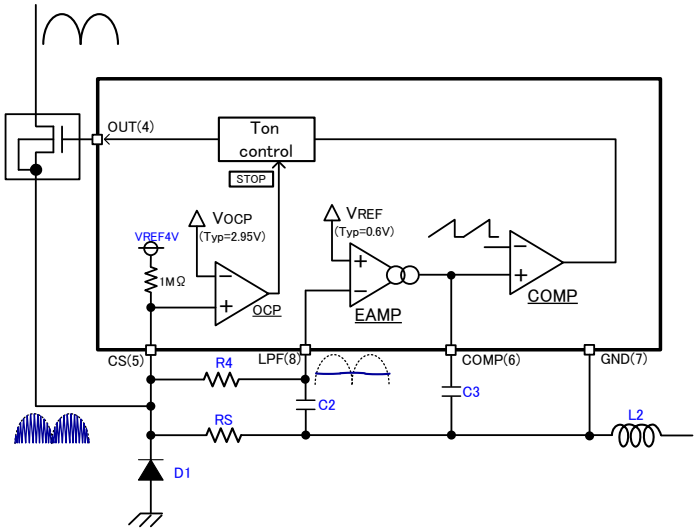


Figure 10. Error Amplifier Block Diagram

(2.2) CS Pin OCP Protection

An OCP (Over Current Protection) function is built in the CS pin. While the voltage of CS pin rises up to the trigger voltage V_{OCP} (Typ=2.95V), the MOSFET is forced to turn OFF. (Automatic Recovery Protection)

(2.3) L.E.B Blanking Period

When the MOSFET is turned ON, surge current occurs by the capacitive components and drive current. In this case, if the CS pin voltage rises temporarily, the false detections may occur in the over current limiter circuit. For preventing from the false detections, an L.E.B (Leading Edge Blanking) function which masks the CS voltage during a constant time T_{LEB} (Typ=200ns) after the OUT pin switches form Low to High is built in.

(2.4) CS Pin Open Protection

When the CS pin becomes open, this function stops the switching operation for protection. (Automatic Recovery Protection)

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(3)Zero current detection block (ZT : 1pin)

(3.1)Block Description

ZT pin (1pin) controls the Low time of the output of OUT pin. While the output is Low (MOSFET: OFF), the current flows from the flywheel diode D1 to the inductor L2. While the current I_L is close to zero, the voltage of ZT pin falls down. While the voltage becomes lower than V_{ZT1} (Typ=110mV), it is detected by the ZT comparator, and the output of OUT pin turns to High (MOSFET: ON).

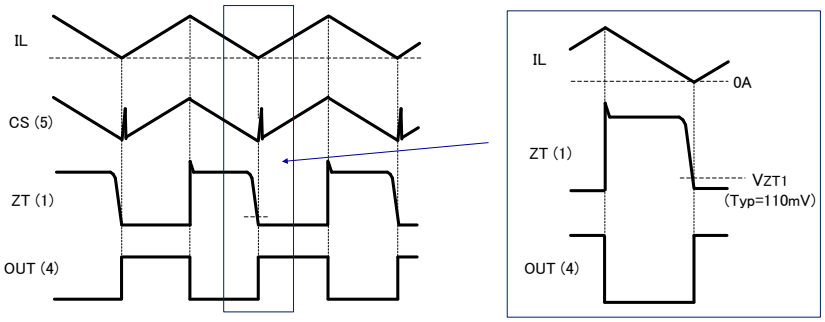


Figure 11. Zero-cross Detection by ZT Pin

(3.2) ZT Tigger Timeout

In case of the ZT pin is locked at low voltage which is caused by some malfunctions of the components on the application, and the quasi-resonant switching operation stops, the output of OUT pin turns to High after T_{ZTOUT} (Typ=18μs).

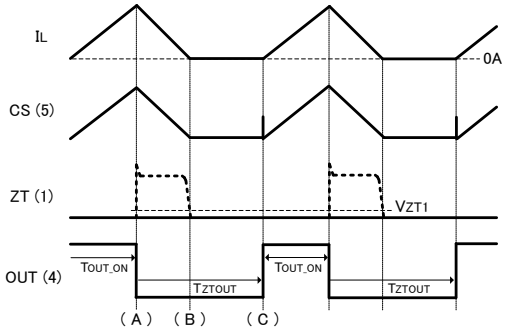


Figure 12. ZT Trigger Timeout Operation

(A)…When the ON time (T_{OUT_ON}) which is determined by the voltage of COMP pin passed, the output of OUT pin turns to Low.
(B)…The ZT pin is locked at a low voltage, the output of OUT pin keeps Low.
(C)…When T_{ZTOUT} passed after the output of OUT pin turns to Low, the output of OUT pin turns to High.

(3.3) Maximum Frequency

The maximum frequency is a function which is designed for preventing from the overheating of the IC, and it limits the IC to operate under the F_{MAX} (Typ=300kHz).

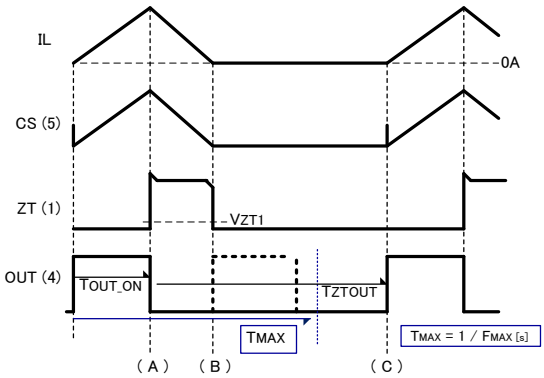


Figure 13. Maximum Frequency Operation

(A)…When the ON time (T_{OUT_ON}) which is determined by the voltage of COMP pin passed, the output of OUT pin turns to Low.
(B)…If the switching frequency exceeds the F_{MAX}, the output of OUT pin cannot turn to High.
(C)…When T_{ZTOUT} passed after the output of OUT pin turns to Low, the output of OUT pin is forced to turn to High.

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Operation Mode of Protection Circuit

Operation mode of protection functions are shown in Table 2.

Table 2. Operation Mode of Protection Circuit

Abnormal State Detection		Detection	Release	Protection Operations
VCC	UVLO	<= 8.2V(Typ)	>= 13.5V (Typ)	IC Stops (Automatic Recovery)
	OVP	>=27.5V(Typ)	Before Latch：<= 23.5V (Typ) Latched：Vcc<= 7.7V (Typ)	150μs(Typ) Timer Latch
CS	OCP	>=2.95V(Typ)	<2.95V (Typ)	Output Stops (Automatic Recovery)
TSD		>=175 °C (Typ)	Before Latch：<= 155 °C (Typ) Latched：Vcc<= 7.7V (Typ)	150μs(Typ) Timer Latch

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors**.**

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

11. Unused Input Terminals

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

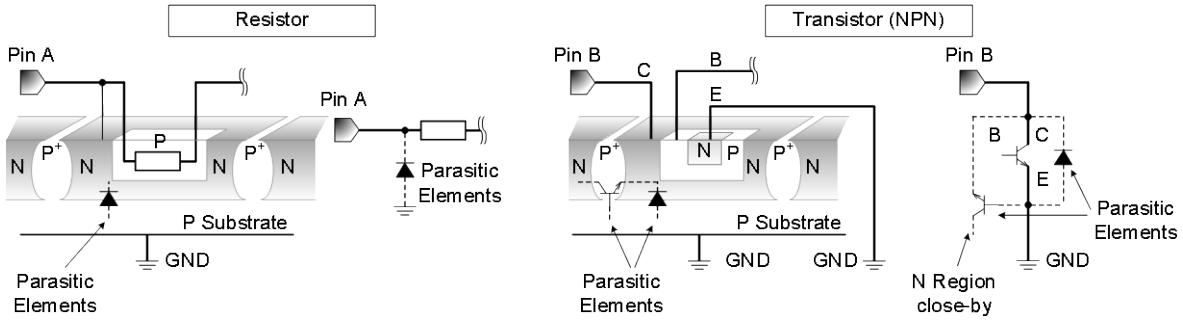


Figure 14. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

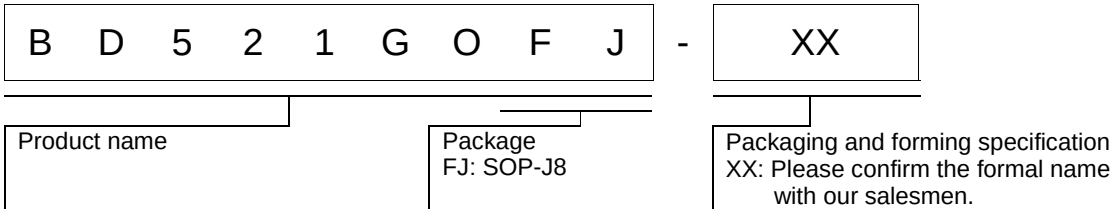
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. The IC should be powered down and turned ON again to resume normal operation because the TSD circuit keeps the outputs at the OFF state even if the TJ falls below the TSD threshold.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

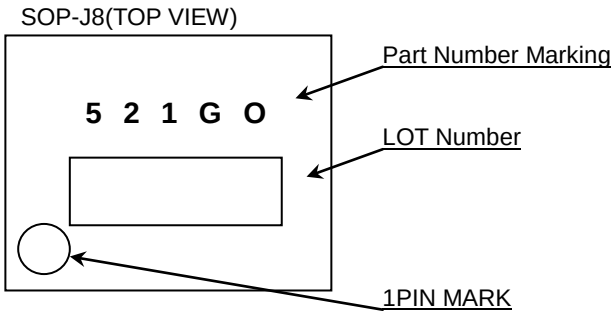
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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Ordering Information



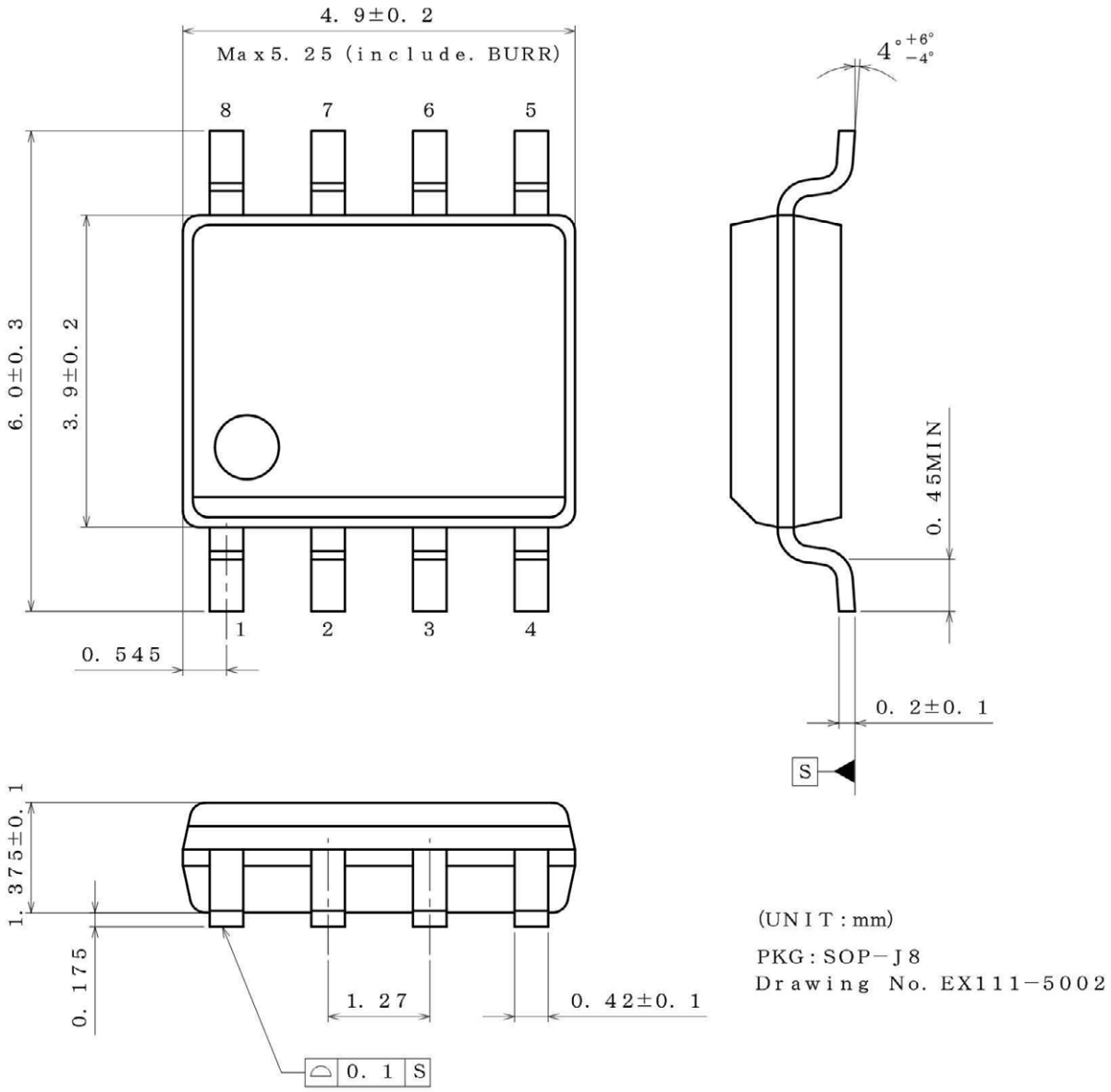
Marking Diagram



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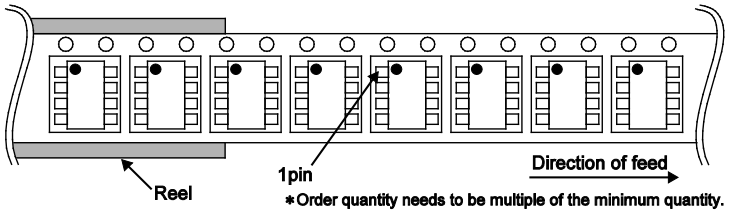
Physical Dimension, Tape and Reel Information

Package Name	SOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
18.Jan.2016	001	New Release
20.Apr.2016	002	P2 Footprints and Traces Changed the representation of the units. $74.2mm^2$ (Square) ⇒ 74.2mm x 74.2mm

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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BD521GOFJ - Web Page

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Distribution Inventory

Part Number	BD521GOFJ
Package	SOP-J8
Unit Quantity	2500
Minimum Package Quantity	2500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes