DATA SHEET

GPCD9341A

Multi-Channel Sound Controller (OTP)

Jul. 27, 2017

Version 1.1

Table of Contents

MULTI-CHANNEL SOUND CONTROLLER (OTP)

1.GENERAL DESCRIPTION

GPCD9341A(OTP) features 1M-byte internal OTP ROM, 512 bytes working SRAM, three sets of 12-bit timer, 32 general I/Os with selectable 8+1 channels input and one 14-bit DAC with push-pull amplifier. The microprocessor implements software based on audio processing, functional control and others. For audio processing, melody and speech can be mixed into one output. GPCD9341A also outfits up to two software channels and a high performance SPU voice engine for voice playback function in ADPCM or PCM format. It is designed to operate over a wide voltage range with a low voltage reset function to assure the capability of operating at an extremely low voltage condition. In addition, GPCD9341A features sleep mode for power savings. While in standby mode, it can be rapidly awaked from sleep mode by interrupt sources or IO state alterations. A Serial Peripheral Interface (SPI) controller is also available in certain GPCD9341A to facilitate communications with other devices and components.

2.FEATURES

- Working Voltage: 2.3V - 5.5V
- CPU speed: Max. 8MHz
- F_{OSC} = Max. 16MHz (2 x CPU clock)
- ROM size: 1M bytes
- RAM size: Max. 512 bytes
- Three 12-bit timers/counters; TMA with capture and comparison function; TMB/ TMC with comparison function only (Programmable and Auto Reload)
- Sleep mode to reduce power consumption
- Key change wake-up function
- Clock source with ROSC or XTAL (option)

- IRQs & NMI interrupts
- Watchdog function (option)
- 5.5V to 3.3V regulator
- Low Voltage Reset
- 32 bit-programmable general I/Os
- Eight I/Os with high sink current for LED application
- All general IOs with 1M pull-low function to prevent current leakage from error key touch
- One 14-bit DAC with push-pull amplifier for direct drive speaker
- SPU (Sound Processing Unit) engine can output audio data with 14-bit resolution to perform high quality voice/melody
- IR PWM Output
- Hardware PWMIO supports four LED outputs with 256-level brightness control
- Real-time clock
- 8-channel SPU engine with ADPCM/PCM wavetable
- Up to two 14-bit software channels with noise filter to playback high quality sound
- SPI master interface

3.APPLICATION FIELD

- Talking instrument controller
- General music synthesizer
- General purpose controller
- High end toy controller
- Intelligent education toy
- And more

4. BLOCK DIAGRAM

GPCD9341A

XI	8-Bit controller	512 Bytes SRAM
XO		

12- Bit Timer / Counter A
12- Bit Timer / Counter B
12- Bit Timer / Counter C

8 Bit X 8 Bit Multiplier

1MB OTP ROM

8-CH SPU
2-CH Software

RESETB — Regulator/LVR/Porst

Digital Mixer

IOD0~3 — SPI

IOB0~3 — PWMIO

14-Bit Push-Pull DAC — AUDP / AUDN

Max. 32 General I/O,IOA,IOB,IOC,IOD
(IOB with Special Function)

IOA 0~7   IOB 0~7   IOC0~7   IOD 0~7
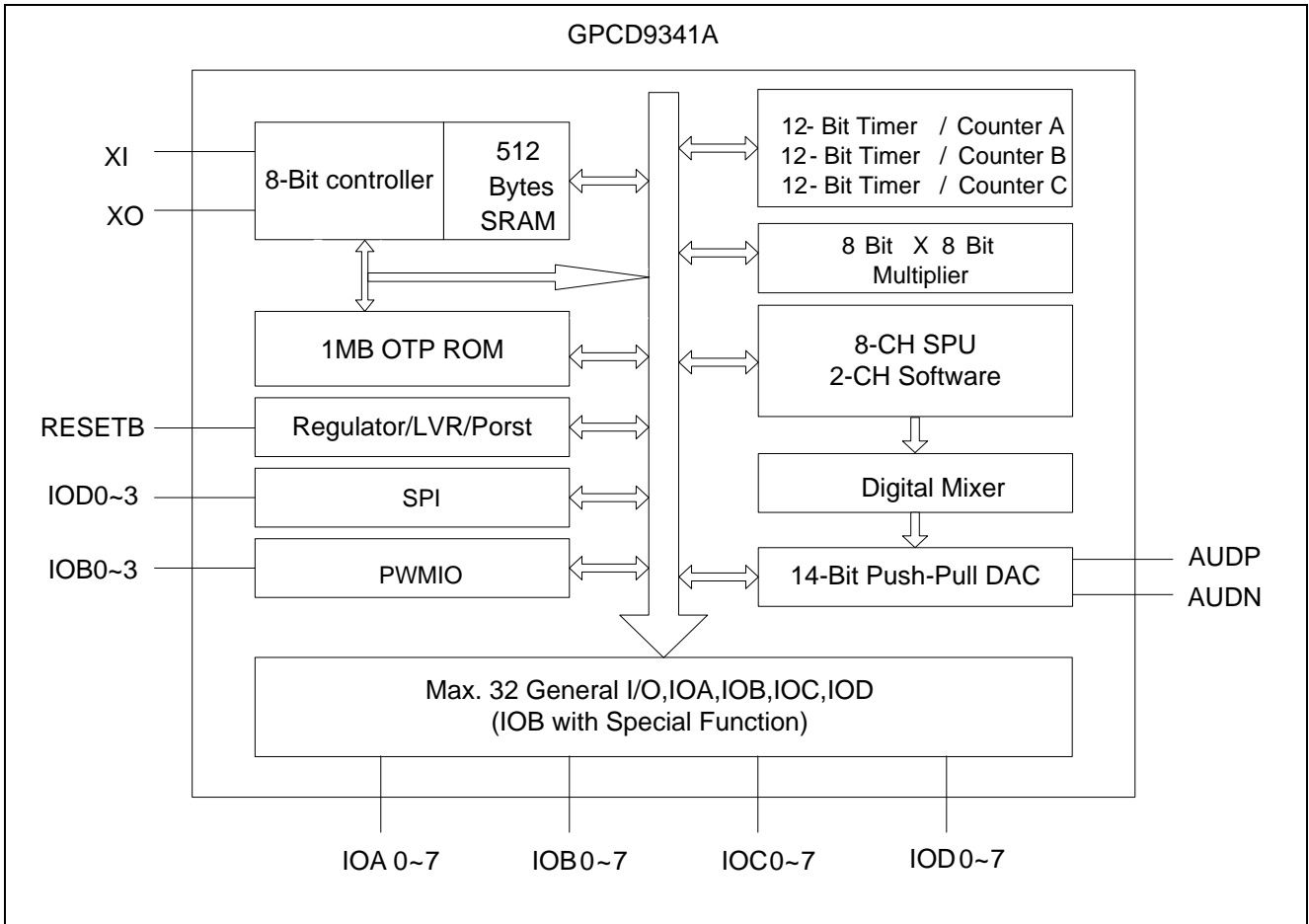
5. SIGNAL DESCRIPTIONS

5.1. Signal Description for GPCD9341A

Name	Pin No. (LQFP64)	Type	Description	Note
IO PORT				
IOA0~IOA7	9~5,2~1,64	I/O	Bi-directional IO ports with wakeup capability	IOA0~3 high sink
IOB0~IOB7	11~18	I/O	Bi-directional IO ports with wakeup capability	IOB0~3 high sink
IOC0~IOC7	19~26	I/O	Bi-directional IO ports with wakeup capability	-
IOD0~IOD7	63~56	I/O	Bi-directional IO ports with wakeup capability	-
Clock Related				
XO	52	O	Oscillator crystal output	-
XI	53	I	Oscillator crystal input./R_{OSC} input	Floating
POWER PAD				
VDD_REG	29	P	Positive power supply for regulator (2.3~5.5V)	-
VDD_DAC1	38	P	Positive power supply for amplifier (2.3~5.5V)	-
VDD_DAC2	40	P	Positive power supply for DAC (2.3~5.5V)	-
VDD_IO1	27	P	Positive power supply for IOB,IOC (2.3~5.5V)	-
VDD_IO2	55	P	Positive power supply for IOA,IOD (2.3~5.5V)	-
VDD/VDD_2*	54	P	Core power from regulator and recommended connecting to VDD33 via PCB	Shorted to VDD33 internally
VDD33	30	P	Core power output from regulator	External components power source not allowed. Shorted to VDD internally
VSS_REG	28	G	Ground reference for regulator	-
VSS	10	G	Ground reference for GPIO and core circuit	-
VSS_2*	NC	G	Ground reference for OTP_SCK and OTP_SDA	Shorted to VSS internally
VSS_DAC1/2	34,44	G	Ground reference for amplifier	-
VSS_DAC3	45	G	Ground reference for DAC	-
VPP	49	P	OTP high voltage source for program	-
Others				
RESETB	3	I	External reset pin(active low)	Internal pull-high
TEST	4	I	For test mode, NC for normal application	Internal pull-low
SIFEN	46	I	Serial interface enable control	Internal pull-high
OTP_SCK	47	I	Serial clock for OTP read/write via serial interface	Internal pull-low
OTP_SDA	48	I/O	Serial data for OTP read/write via serial interface	-
AUDP	42	O	Audio output of push-pull DAC	-
AUDN	36	O	Audio output of push-pull DAC	-

*Note: (1) VDD pad is recommended being bonded for stability issue even VDD33 is shorted to VDD internally. VDD_2 and VSS_2 could not be bonded in case of dedicated PCB design for GPCD9340A.

(2) For IO special function and allocation, please refer to 6.6.1 IO configuration.

(3) For more details about pad information, please refer to GPCD9341A "Pad Assignment and Locations" document.

(4) VDD33 and VDD/VDD2 are dedicated to GPCD9341A internal circuits, not allowed for external component power source.

5.2. Signal Description

IOA[6]	1	48	OTP_SDA
IOA[5]	2	47	OTP_SCK
RESETB	3	46	SIFEN
TEST	4	45	VSS_DAC3
IOA[4]	5	44	VSS_DAC2
IOA[3]	6	43	NC
IOA[2]	7	42	AUDP
IOA[1]	8	41	NC
IOA[0]	9	40	VDD_DAC2
VSS	10	39	NC
IOB[0]	11	38	VDD_DAC1
IOB[1]	12	37	NC
IOB[2]	13	36	AUDN
IOB[3]	14	35	NC
IOB[4]	15	34	VSS_DAC1
IOB[5]	16	33	NC

GPCD9341A
LQFP64

Top pins (64–49): IOA[7], IOD[0], IOD[1], IOD[2], IOD[3], IOD[4], IOD[5], IOD[6], IOD[7], VDD_IO2, VDD, IX, OX, NC, NC, VPP

Bottom pins (17–32): IOB[6], IOB[7], IOC[0], IOC[1], IOC[2], IOC[3], IOC[4], IOC[5], IOC[6], IOC[7], VDD_IO1, VSS_REG, VDD_REG, VDD33, NC, NC

6. FUNCTIONAL DESCRIPTIONS

6.1. SRAM

The 512-byte SRAM (including Stack) area is located in $000000~$0002FF.

6.2. ROM

GPCD9341A is capable of accessing internal 1MB OTP ROM. The ROM size is as following table:

Body	ROM Size	ROM Address
GPCD9341A	1MB	0x00840~0xFFFFF

6.3. Low Voltage Reset

The GPCD9341A provides another important feature - Low Voltage Reset (LVR). With the LVR function, a reset signal is generated to reset system when the operating voltage drops below LVR. Without LVR, CPU becomes unstable and malfunction when working voltage is too low.

6.4. Interrupt

The GPCD9341A has two interrupt (INT) modes: IRQ (interrupt Request) and NMI (Non-Mask Interrupt Request). The interrupt controller controls fifteen IRQs and seven NMIs. A NMI cannot be interrupted by any other IRQs.

Interrupt Source	Interrupt Name	Priority
Timer A	NMI_TIMER_A	NMI
Timer B	NMI_TIMER_B	NMI
Timer C	NMI_TIMER_C	NMI
CPU_CLOCK/1024	NMI_D1024	NMI
CPU_CLOCK/4096	NMI_D4096	NMI
KEY	NMI_KEY	NMI
EXT	NMI_EXT	NMI
TIMER A	IRQ_TIMER_A	IRQ1
TIMER B	IRQ_TIMER_B	IRQ2
TIMER C	IRQ_TIMER_C	IRQ3
CPU_CLOCK/1024	IRQ_D1024	IRQ4
CPU_CLOCK/4096	IRQ_D4096	IRQ5
16 Hz	IRQ_16Hz	IRQ6
2 Hz	IRQ_2 Hz	IRQ7
KEY	IRQ_KEY	IRQ8
EXT	IRQ_EXT	IRQ9
SPU	IRQ_SPU	IRQ10
SPI	IRQ_SPI	IRQ11

Interrupt Source	Interrupt Name	Priority
QD1_F	IRQ_QD1_F	IRQ12
QD1_B	IRQ_QD1_B	IRQ13
QD2_F	IRQ_QD2_F	IRQ14
QD2_B	IRQ_QD2_B	IRQ15

6.5. Hardware PWMIO

Hardware PWMIO supports four LED outputs from IOB0~3 with brightness control of 256 levels. The clock source of PWMIO is selected on user's demand.

6.6. I/O

The purpose of input and output port is to communicate with other devices. Maximum 32 programmable I/O ports are built-in for GPCD9341A series, including Port A, B, C, and D. All ports are general I/Os with programmable wake-up capability and 1M pull-low function. In addition, these ports also provide some special functions in certain pins. PortA0~3 and PortB0~3 provide large sink current for LED application. The Port D0~3 is sharing with SPI function. Please refer to following figure for more information about **IO Sharing**.

6.6.1. I/O Configuration

The following diagram represents the I/O schematic.

I/O A, B, C, D Schematic:
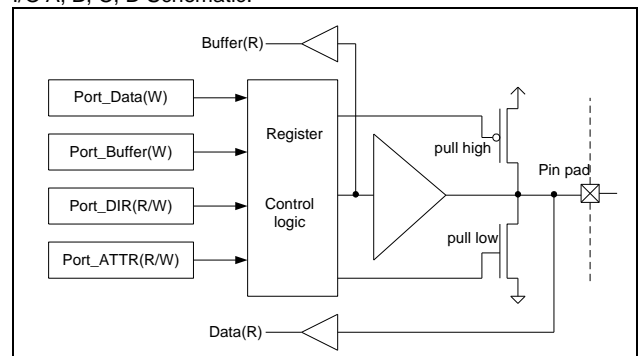
Port_Data and Port_Buffer are written into the same register but reading from different node. To activate key wakeup function, user should latch data on IOX_Data and enable the key wakeup function. Wakeup is triggered when the port's state is different from the latched data.

A summary of IO sharing is listed as following.

IO Sharing

	IOA								IOB							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Auto Wake up								V								
Wake up	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
High Sink					V	V	V	V					V	V	V	V
PWMIO													V	V	V	V
IR(Output)									V							
External INT										V						
External Clock		V(TMC)	V(TMB)	V(TMA)												
RTC											V	V				
IIS Out/In	V(in)	V(in)	V(in)			V(out)	V(out)	V(out)								
QD					V(qd2)	V(qd2)	V(qd1)	V(qd1)								
CC		TMC	TMB	TMA						TMC	TMB	TMA				
1M Pull low	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V

	IOC								IOD							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Wake up	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
SPI													V(rx)	V(tx)	V(ck)	V(cs)
1M Pull low	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V

*Note: QD means quadrature decoder; CC means Capture/Comparison.**

6.7. Timer/Counter (Timer A/Timer B/Timer C)

Three 12-bit timers are outfitted in GPCD9341A: Timer A, Timer B, and Timer C. These timers all have a 12-bit up-counter, a preloaded register, and programmable clock sources. Timer A/B can also be the clock source of the software channel 1/2 respectively. The clock source of each timer can be set individually. Two clock sources including CPU clock and external clock can be selected individually or their combination to be timer's clock source. Besides, capture and comparison function are supported by TMA. Comparison is supported by TMB and TMC.
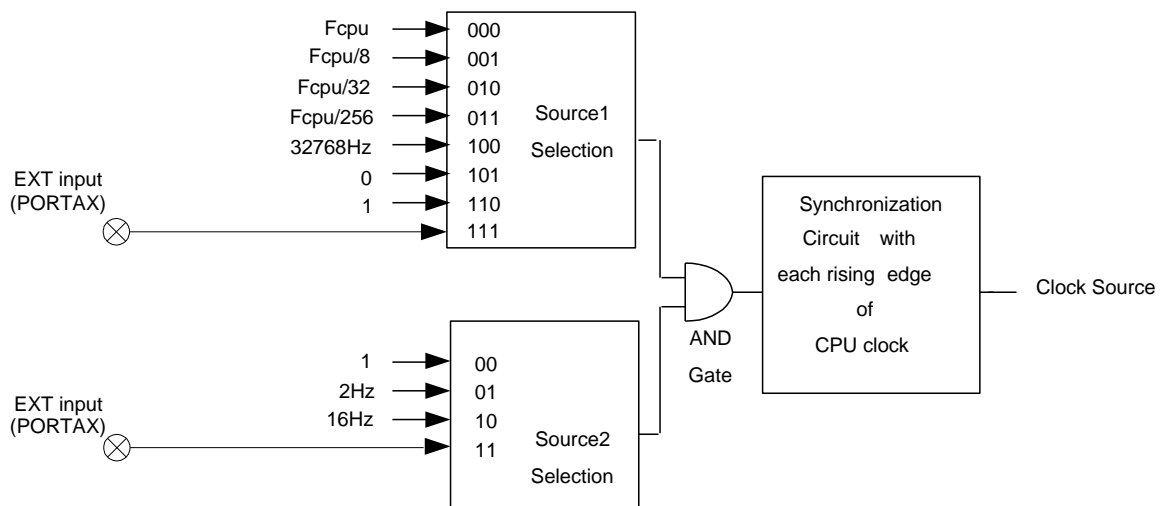
6.8. Sleep, Wakeup and Watchdog

6.8.1. Sleep and Wakeup

Sleep mode saves power by stopping clock while device is not in use. When entering into sleep mode, the device runs from operating mode to standby mode. Wake-up from sleep mode is to turn back to operating mode.

1). Sleep: after power-on reset, IC starts working until a sleep command is given. When a sleep signal is accepted, IC will turn off system clock and enter into sleep mode.

2). Wake-up: while an IRQ/NMI interrupt signal is generated, GPCD9341A wakes up from sleep mode. While wake-up is completed, program counter will continue to execute the next command.

6.8.2. Watchdog

The purpose of watchdog is to monitor whether the system operates normally. Within a certain period, watchdog must be cleared. It prevents the system from incorrect code execution by generating a system reset when software is failed to clear watchdog flag within 0.75 seconds. Watchdog function can be removed by option in GPCD9341A.

6.9. Speech and DAC

The GPCD9341A uses a high performance SPU voice engine to achieve 8-channel voice with ADPCM/PCM. The SPU also supports automatic zero-crossing concatenate function. A hardware multiplier is also embedded in this SPU for software usage. The fixed address of RAM area $0000 - $007F is designed as address pointer and a data buffer for the 8-channel speech/melody generation. Moreover, up to two 14-bit software channels with noise filter included and one 14-bit DAC with push-pull amplifier for direct audio output.

6.10. SPI Controller

A Serial Peripheral Interface (SPI) controller is built-in GPCD9341A to facilitate communicating with other devices and components. There are four control signals on SPI including SPICSN, SPICLK (SCK), SPIRX (SDI), and SPITX (SDO); these four signals are shared with PortD0, PortD1, PortD2, and PortD3. While SPI module is enabled by corresponding control bits, these four pins cannot be GPIOs and any setting on corresponding GPIO control register will have no effect. Four types of timing are presented as follows:
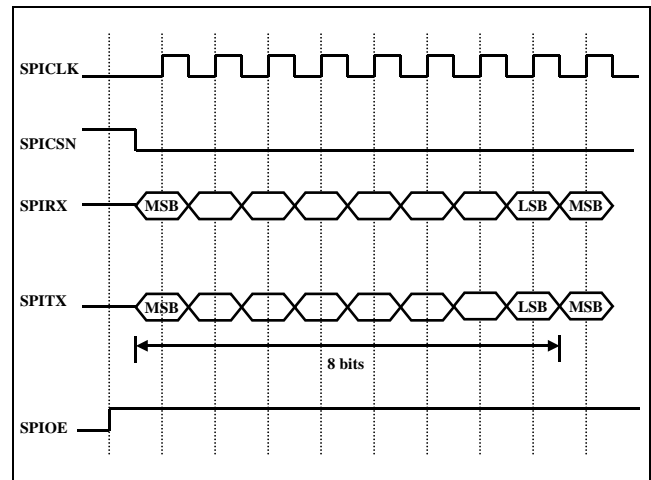
Master Mode, SPO = 0, SPH=0
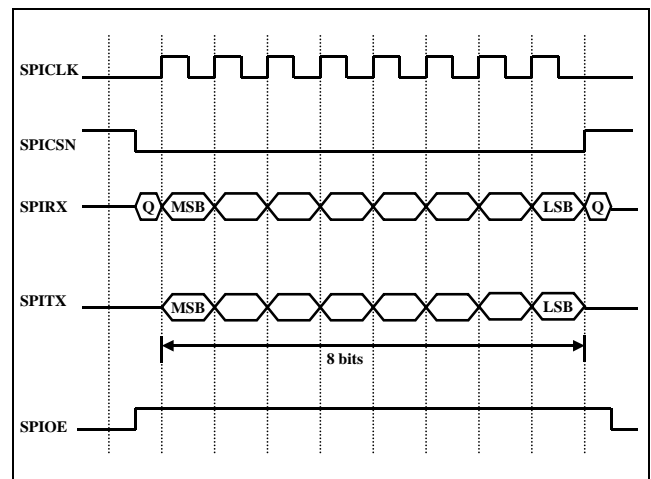
Master Mode, SPO = 0, SPH=1
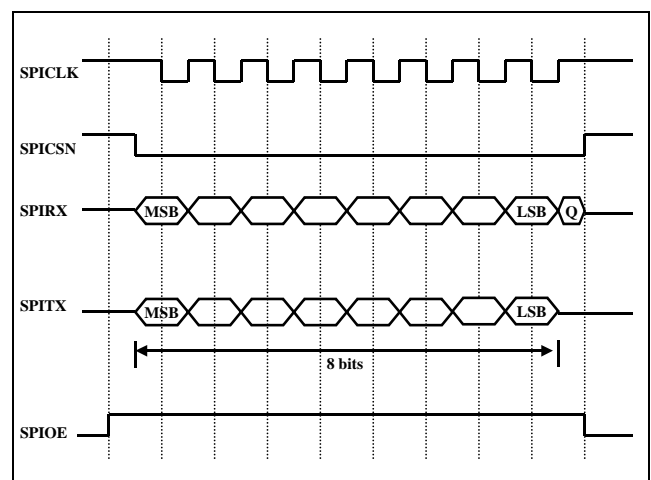
Master Mode, SPO = 1, SPH=0
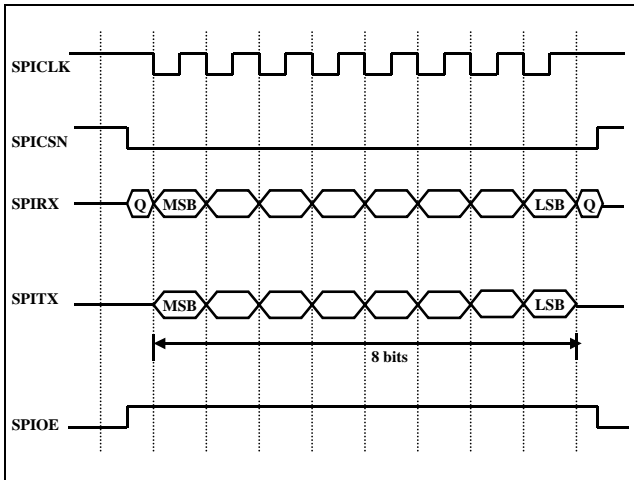
Master Mode, SPO = 1, SPH=1

6.11. OTP Serial Interface

GPCD9341A offers an easy way to read/write OTP ROM by serial interface.   It could be easily implemented via pins OTP_SCK and OTP_SDA.   In order to protect user's code development, the OTP interface also provides security function to prevent code reading through serial interface.   Moreover, the serial read/write OTP ROM must bond VDD_DAC2 and VSS_DAC3 or there is no power/ground source for OTP_SCK and OTP_SDA pins.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions, please refer to DC Electrical Characteristics.

7.2. DC Characteristics (VDD_IO/VDD_REG=3.0V, TA=25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.3	-	3.6	V	For 2-battery
Operating Current-1	I_{OP-1}	-	8	-	mA	VDD_IO/VDD_ADC/VDD_REG=3.0V F_{CPU} = 8MHz , DAC on, no load
Operating Current-2	I_{OP-2}	-	5	-	mA	VDD_IO/VDD_ADC/VDD_REG=3.0V F_{CPU} = 8MHz , DAC off, no load
Standby Current	I_{STBY}	-	-	3	μA	VDD_IO/VDD_ADC/VDD_REG=3.0V
OSC Frequency	F_{OSC}	-	-	16	MHz	VDD_IO/VDD_ADC/VDD_REG=3.0V
Input High Level	V_{IH}	0.7*VDD	-	VDD	V	-
Input Low Level	V_{IL}	VSS	-	0.3*VDD	V	-
Output High Current (IOA/B/C/D[7:0])	I_{OH}	-	5	-	mA	VDD_IO/VDD_ADC/VDD_REG=3.0V, V_{OH} =2.1V
Output Low Sink Current (IOA/B[7:4], IOC/D[7:0])	I_{OL1}	-	10	-	mA	VDD_IO/VDD_ADC/VDD_REG=3.0V, V_{OL} =0.9V
Output Low Sink Current (IOA/B[3:0])	I_{OL2}	-	20	-	mA	VDD_IO/VDD_ADC/VDD_REG=3.0V, V_{OL} =0.9V
Input Pull-Low Resistor (IOA/B/C/D[7:0])	R_{PL}	-	1600	-	Kohm	VDD_IO/VDD_ADC/VDD_REG=3.0V, Vin=3.0V
Input Pull-High Resistor (IOA/B/C/D[7:0])	R_{PL}	-	160	-	Kohm	VDD_IO/VDD_ADC/VDD_REG=3.0V, Vin=VSS

7.3. DC Characteristics (VDD_IO/VDD_REG=4.5V, TA=25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current-1	I_{OP-1}	-	10	-	mA	VDD_IO/VDD_ADC/VDD_REG=4.5V F_{CPU} = 8MHz , DAC on, no load
Operating Current-2	I_{OP-2}	-	6	-	mA	VDD_IO/VDD_ADC/VDD_REG=4.5V F_{CPU} = 8MHz , DAC off, no load
Standby Current	I_{STBY}	-	-	4	μA	VDD_IO/VDD_ADC/VDD_REG=4.5V
OSC Frequency	F_{OSC}	-	-	16	MHz	VDD_IO/VDD_ADC/VDD_REG=4.5V
Input High Level	V_{IH}	0.7*VDD	-	VDD	V	-
Input Low Level	V_{IL}	VSS	-	0.3*VDD	V	-

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Output High Current (IOA/B/C/D[7:0])	I_{OH}	-	12	-	mA	VDD_IO/VDD_ADC/VDD_REG=4.5V, V_{OH} =3.15V
Output Low Sink Current (IOA/B[7:4], IOC/D[7:0])	I_{OL1}	-	20	-	mA	VDD_IO/VDD_ADC/VDD_REG=4.5V, V_{OL} =1.35V
Output Low Sink Current (IOA/B[3:0])	I_{OL2}	-	38	-	mA	VDD_IO/VDD_ADC/VDD_REG=4.5V, V_{OL} =1.35V
Input Pull-Low Resistor (IOA/B/C/D[7:0])	R_{PL}	-	960	-	Kohm	VDD_IO/VDD_ADC/VDD_REG=4.5V, Vin=4.5V
Input Pull-High Resistor (IOA/B/C/D[7:0])	R_{PH}	-	97	-	Kohm	VDD_IO/VDD_ADC/VDD_REG=4.5V, Vin=VSS

7.4. DAC Characteristics (VDD_IO/VDD_REG/VDD_DAC=4.5V, R_L=8Ω, f=1KHz, TA=25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
DAC Resolution	RESO	-	-	14	bit
THD+n (4.5V@0.45W)	-	-	0.4	-	%
Noise at No Signal	-	-	-97	-	dBr A
Dynamic Range(-60dB)	-	-	-81	-	dBr A

7.5. Regulator Characteristics (TA=25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	2.3	4.5	5.5	V
Maximum Current Output	IREGO	-	-	30	mA
Output Voltage	VREGO	2.3	3.3	3.6	V
Standby Current	IREGS	-	-	2.0	uA

8.APPLICATION CIRCUITS

8.1. GPCD9341A Application Circuit without IO Output Driving Application (R_{OSC}-mode)
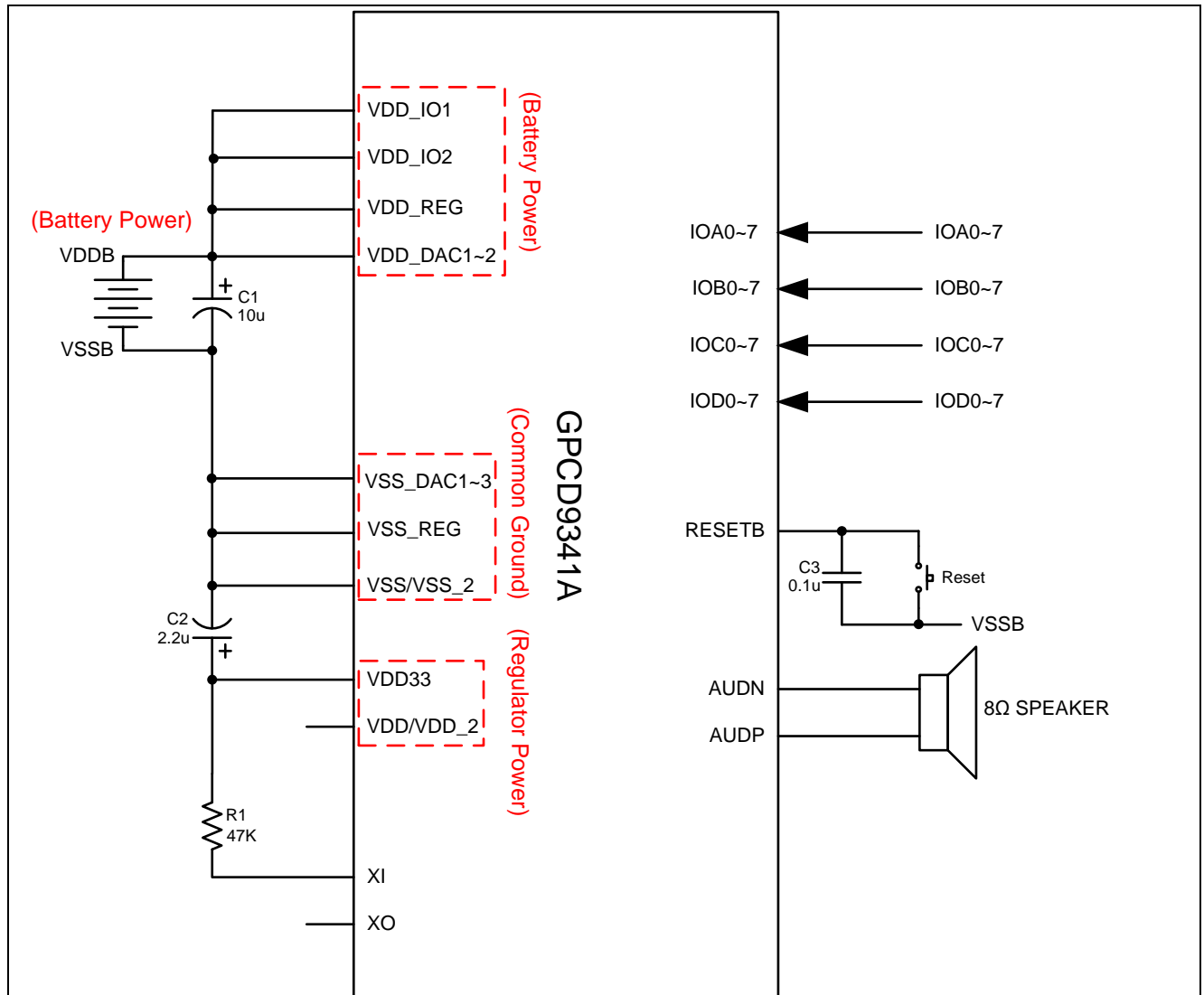
Note:

1. 4Ω speaker application is not allowed in GPCD9341A.

2. Above illustration only suggested for no IO heavy driving output, such as only key input trigger and no LED or motor driver output.

3. C1/C2 value may vary with system application.

4. VDD could be not bonded due to internally connect to VDD33.

5. If system is not stable, it is suggested to refer to following 9.3~9.6 circuits.
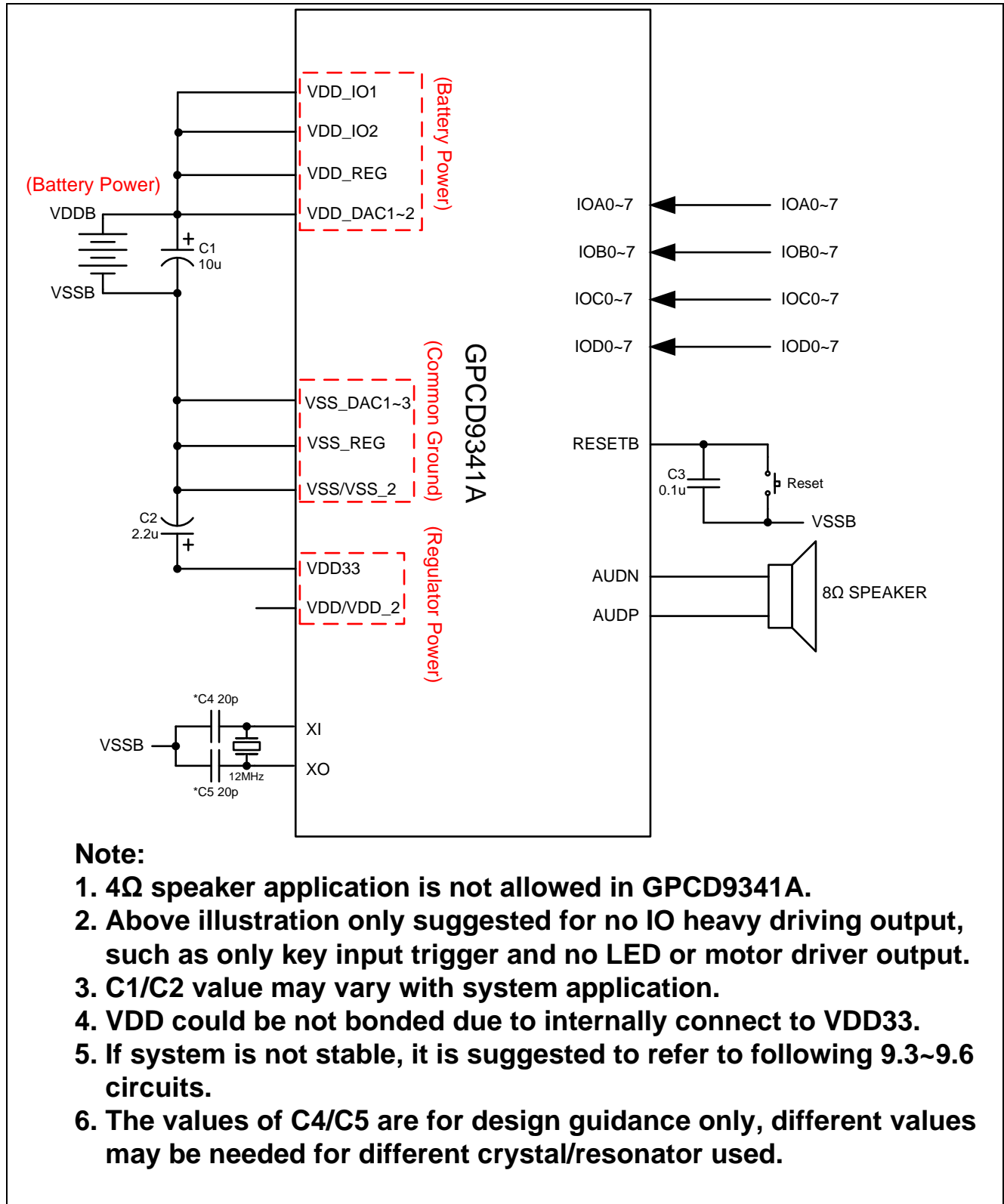
8.2. GPCD9341A Application Circuit without IO Output Driving Application (XTAL-mode)
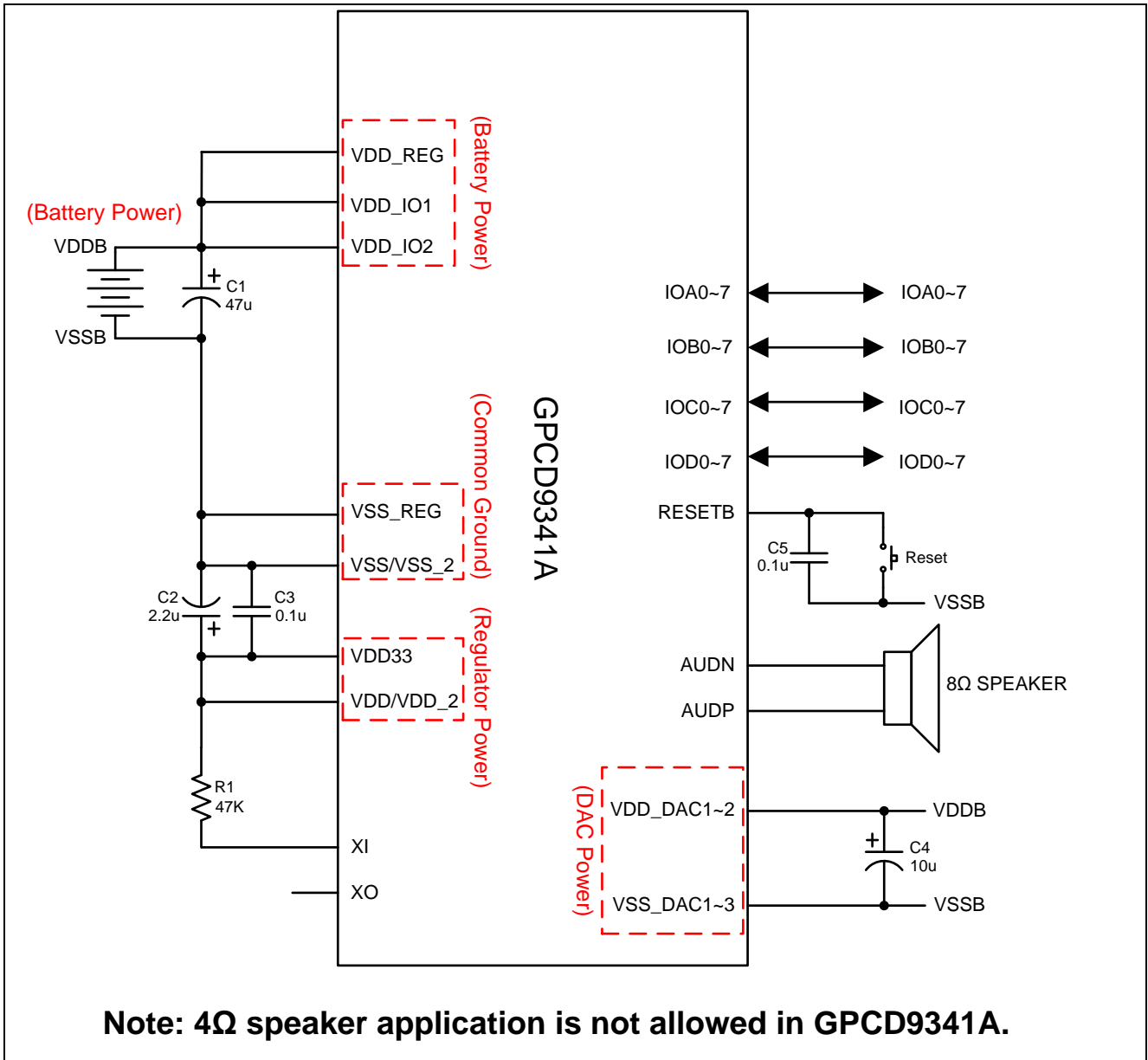

Note:

1. **4Ω speaker application is not allowed in GPCD9341A.**
2. **Above illustration only suggested for no IO heavy driving output, such as only key input trigger and no LED or motor driver output.**
3. **C1/C2 value may vary with system application.**
4. **VDD could be not bonded due to internally connect to VDD33.**
5. **If system is not stable, it is suggested to refer to following 9.3~9.6 circuits.**
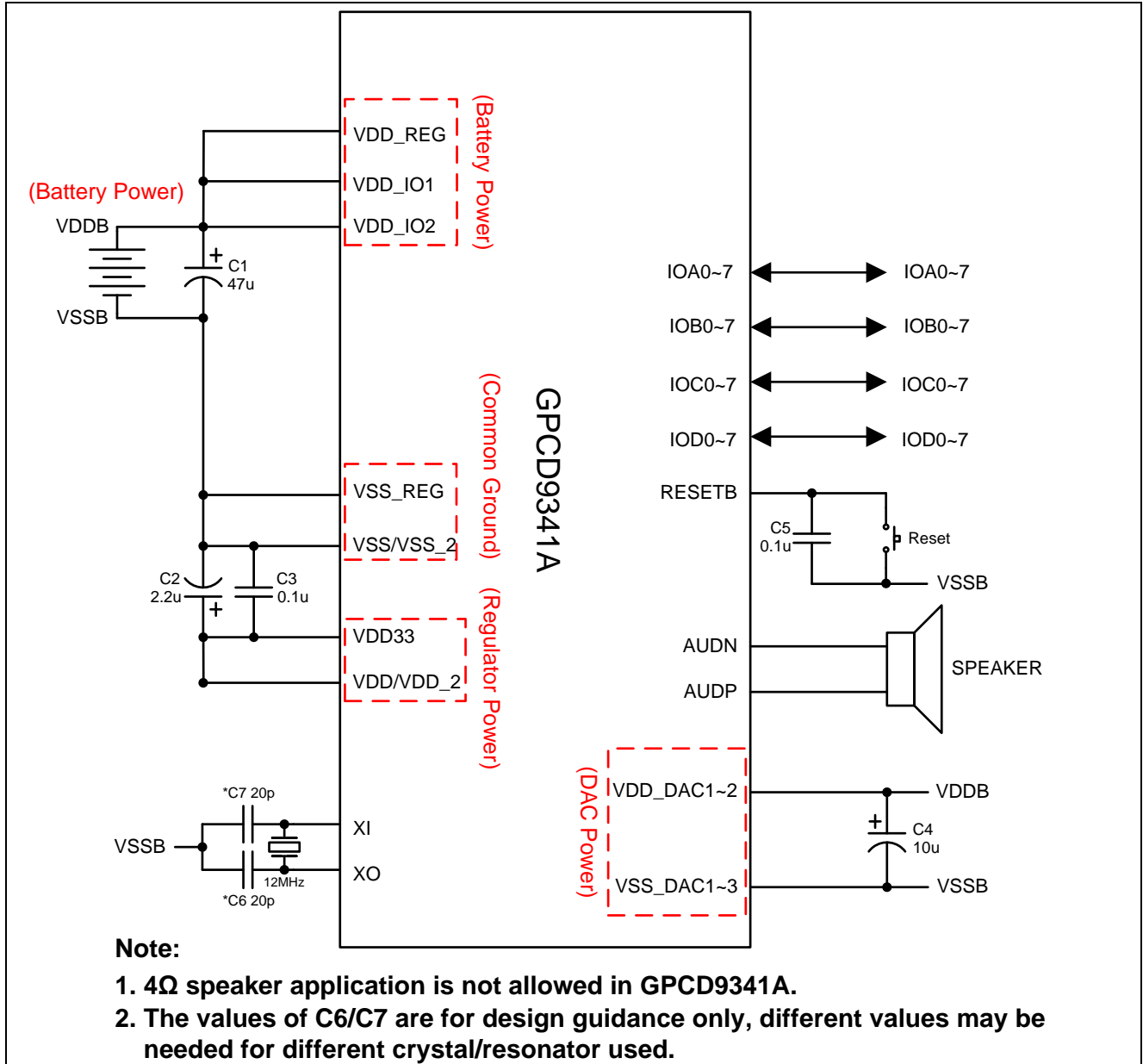6. **The values of C4/C5 are for design guidance only, different values may be needed for different crystal/resonator used.**

8.3. GPCD9341A Application Circuit with R$_{OSC}$ Option

Note: 4Ω speaker application is not allowed in GPCD9341A.

8.4. GPCD9341A Application Circuit with Crystal Option

Note:

1. 4Ω speaker application is not allowed in GPCD9341A.

2. The values of C6/C7 are for design guidance only, different values may be needed for different crystal/resonator used.

8.5. GPCD9341A Application Circuit with IO Heavy Loading(1):High Sourcing

Note:

1. 4Ω speaker application is not allowed in GPCD9341A.

2. For system stability and performance, it is recommended to add R1/C8 for the applications that IOs toggle with high current sourcing, such as LEDs or motor drivers.

3. The value of R2~R9/C8 depends on applications. Basically, the more IO toggles, the larger C8 is suggested.

4. The values of C6/C7 are for design guidance only, different values may be needed for different crystal/resonator used.

8.6. GPCD9341A Application Circuit with IO Heavy Loading(2): High Sinking

Note:

1. **4Ω speaker application is not allowed in GPCD9341A.**
2. **For system stability and performance, it is recommended to add R1~R9/C8 for the applications that IOs toggle with high current sinking, such as LEDs or motor drivers.**
3. **The value of R2~R9/C8 depends on the system application.**
4. **Basically, the more IO toggles, the larger C8 is suggested.**
5. **The values of C6/C7 are for design guidance only, different values may be needed for different crystal/resonator used.**

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9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

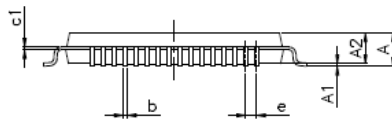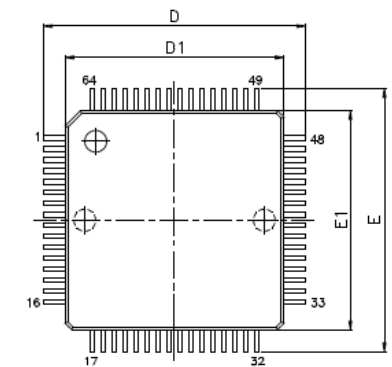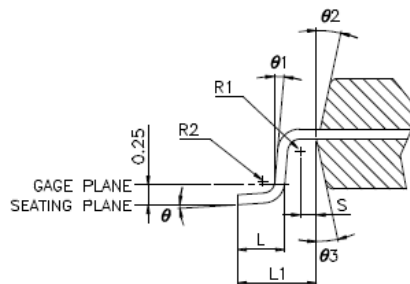| Product Number	Package Type
GPCD9341A-NnnV-QL02x	Green Package – LQFP64

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

9.2. Package Information

LQFP 64 Outline Dimensions

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c1	0.09	–	0.16
D	11.75	12.00	12.25
D1	9.90	10.00	10.10
E	11.75	12.00	12.25
E1	9.90	10.00	10.10
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20 REF		
θ	3.5° REF		
θ1	5.0° REF		
θ2	12° REF		
θ3	12° REF		
R1	0.16 REF		
R2	0.15 REF		

THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2 MIN.	E2 MAX.	D2 MIN.	D2 MAX.
210X21E	4.27	5.33	4.27	5.33
260X26E	5.28	6.60	5.28	6.60

NOTES:
1. JEDEC OUTLINE : MS-026 BCD MS-026 BCD-HD(THERMALLY ENHANCED VARIATIONS ONLY)
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
Jul. 27, 2017	1.1	Modify "software channel" description.	3,4,9,
Mar. 07, 2017	1.0	Release to 1.0	21
MAR. 31, 2011	0.2	1. Modify "Signal Description" in section 5.	5~6
		2. Modify "DC Characteristics" in section 7.	11~12
JAN. 27, 2011	0.1	Original	21