720p 24-bit Color FPD-Link III Serializer with HDCP

General Description

The DS90UH925Q serializer, in conjunction with the DS90UH926Q deserializer, provides a solution for secure distribution of content-protected digital video within automotive entertainment systems. This chipset translates a parallel RGB Video Interface into a single pair high-speed serialized interface. The digital video data is protected using the industry standard HDCP copy protection scheme. The serial bus scheme, FPD-Link III, supports video and audio data transmission and full duplex control including I2C communication over a single differential link. Consolidation of video data and control over a single differential pair reduces the interconnect size and weight, while also eliminating skew issues and simplifying system design.

The DS90UH925Q serializer embeds the clock, content protects the data payload, and level shifts the signals to high-speed low voltage differential signaling. Up to 24 RGB data bits are serialized along with three video control signals and up to two I2S data inputs.

The DS90UH925Q serializer has a 31-bit parallel LVCMOS input interface to accommodate the RGB, video control, and I2S audio data.

EMI is minimized by the use of low voltage differential signaling, data scrambling and randomization and spread spectrum clocking compatibility.

The HDCP cipher engine is implemented in the serializer and deserializer. HDCP keys are stored in on-chip memory.

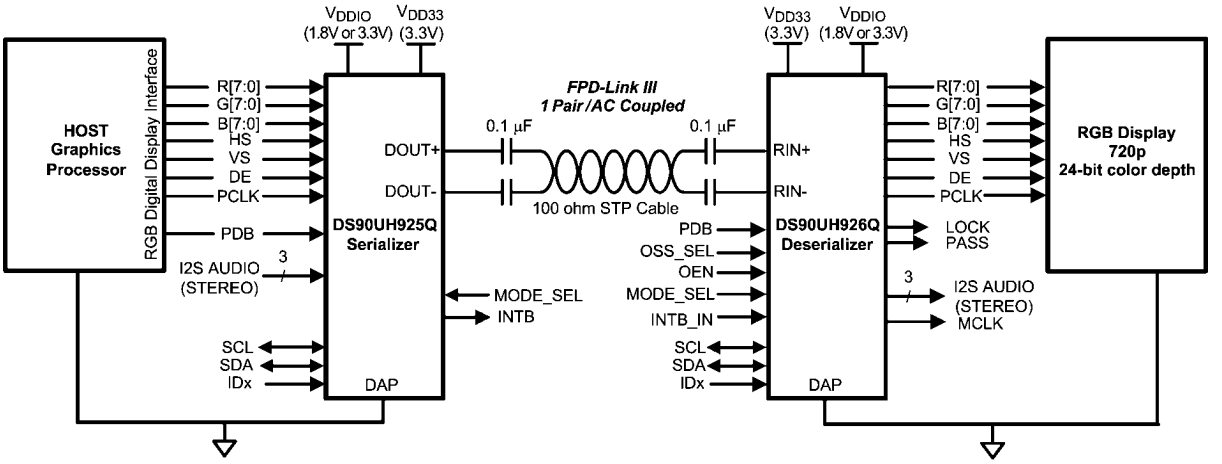
Features

- Integrated HDCP cipher engine with on-chip key storage
- Bidirectional control interface channel interface with I2C compatible serial control bus
- Supports high definition (720p) digital video format
- RGB888 + VS, HS, DE and I2S audio supported
- 5 – 85MHz PCLK supported
- Single 3.3V Operation with 1.8V or 3.3V compatible LVCMOS I/O interface
- AC-coupled STP Interconnect up to 10 meters
- Parallel LVCMOS video inputs
- DC-balanced & scrambled Data w/ Embedded Clock
- HDCP Content protected
- Supports HDCP repeater application
- Internal pattern generation
- Low power modes minimize power dissipation
- Automotive grade product: AEC-Q100 Grade 2 qualified
- >8kV HBM and ISO 10605 ESD rating
- Backward compatible modes

Applications

- Automotive Display for Navigation
- Rear Seat Entertainment Systems

Applications Diagram



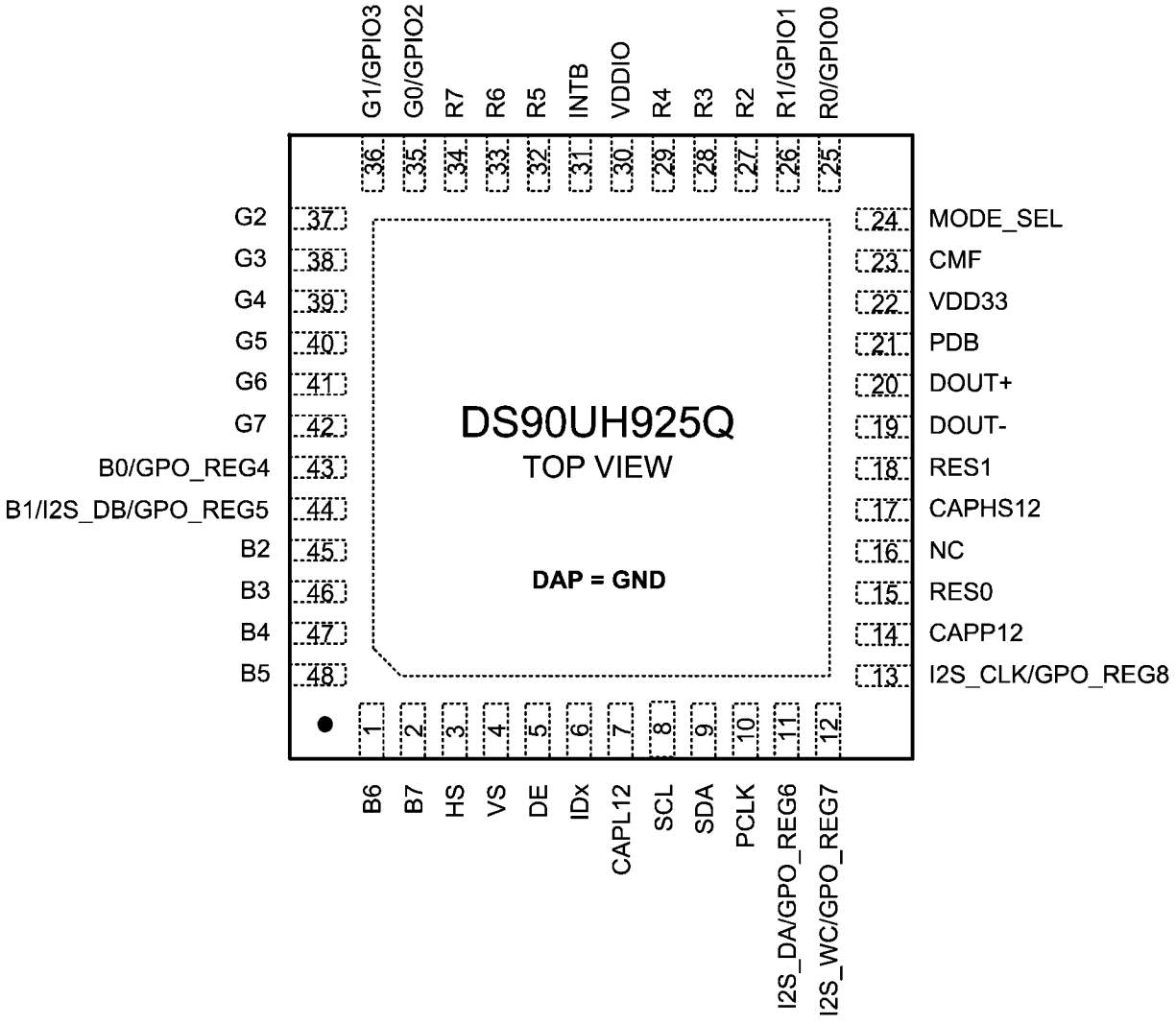
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DS90UH925Q Pin Diagram



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DS90UH925Q — Top View

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Pin Descriptions

Pin Name	Pin #	I/O, Type	Description
LVCMOS Parallel Interface			
R[7:0]	34, 33, 32, 29, 28, 27, 26, 25	I, LVCMOS w/ pull down	RED Parallel Interface Data Input Pins Leave open if unused R0 can optionally be used as GPIO0 and R1 can optionally be used as GPIO1.
G[7:0]	42, 41, 40, 39, 38, 37, 36, 35	I, LVCMOS w/ pull down	GREEN Parallel Interface Data Input Pins Leave open if unused G0 can optionally be used as GPIO2 and G1 can optionally be used as GPIO3.
B[7:0]	2, 1, 48, 47, 46, 45, 44, 43	I, LVCOS w/ pull down	BLUE Parallel Interface Data Input Pins Leave open if unused B0 can optionally be used as GPO_REG4 and B1 can optionally be used as GPO_REG5.
HS	3	I, LVCMOS w/ pull down	Horizontal Sync Input Pin Video control signal pulse width must be 3 PCLKs or longer to be transmitted when the Control Signal Filter is enabled. There is no restriction on the minimum transition pulse when the Control Signal Filter is disabled. The signal is limited to 2 transitions per 130 PCLKs. See *Table 6*
VS	4	I, LVCMOS w/ pull down	Vertical Sync Input Pin Video control signal is limited to 1 transition per 130 PCLKs. Thus, the minimum pulse width is 130 PCLKs.
DE	5	I, LVCMOS w/ pull down	Data Enable Input Pin Video control signal pulse width must be 3 PCLKs or longer to be transmitted when the Control Signal Filter is enabled. There is no restriction on the minimum transition pulse when the Control Signal Filter is disabled. The signal is limited to 2 transitions per 130 PCLKs. See *Table 6*
PCLK	10	I, LVCMOS w/ pull down	Pixel Clock Input Pin. Strobe edge set by RFB configuration register. See *Table 6*
I2S_CLK, I2S_WC, I2S_DA	13, 12, 11	I, LVCMOS w/ pull down	Digital Audio Interface Data Input Pins Leave open if unused I2S_CLK can optionally be used as GPO_REG8, I2S_WC can optionally be used as GPO_REG7, and I2S_DA can optionally be used as GPO_REG6.
Optional Parallel Interface			
I2S_DB	44	I, LVCMOS w/ pull down	Second Channel Digital Audio Interface Data Input pin at 18–bit color mode and set by MODE_SEL pin or configuration register Leave open if unused I2S_DB can optionally be used as B1 or GPO_REG5.
GPIO[3:0]	36, 35, 26, 25	I/O, LVCMOS w/ pull down	General Purpose IOs. Available only in 18-bit color mode, and set by MODE_SEL pin or configuration register. See *Table 6* Leave open if unused Shared with G1, G0, R1 and R0.
GPO_REG [8:4]	13, 12, 11, 44, 43	O, LVCMOS w/ pull down	General Purpose Outputs and set by configuration register. See *Table 6* Share with I2S_CLK, I2S_WC, I2S_DA, I2S_DB or B1, B0.
Control			
PDB	21	I, LVCMOS w/ pull-down	Power-down Mode Input Pin PDB = H, device is enabled (normal operation) Refer to ”Power Up Requirements and PDB Pin” in the Applications Information Section. PDB = L, device is powered down. When the device is in the powered down state, the Driver Outputs are both HIGH, the PLL is shutdown, and IDD is minimized. Control Registers are **RESET**.
MODE_SEL	24	I, Analog	Device Configuration Select. See *Table 1*

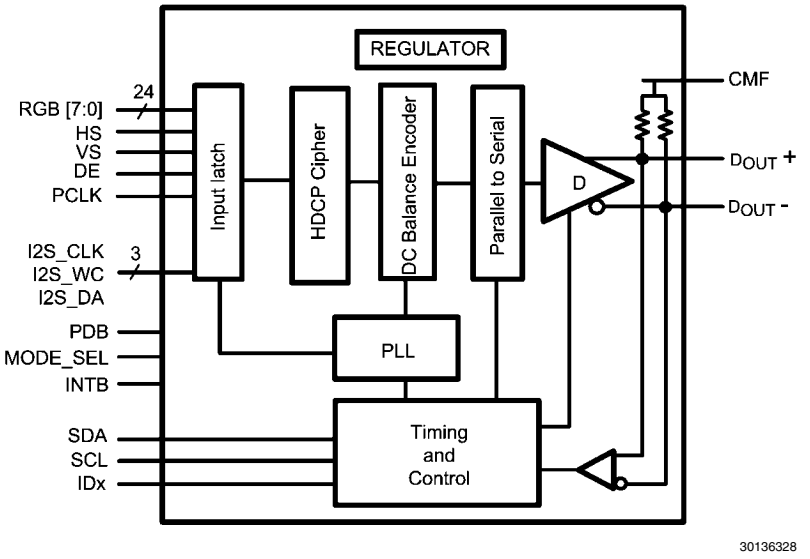
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Pin Name	Pin #	I/O, Type	Description
I2C			
IDx	6	I, Analog	I2C Serial Control Bus Device ID Address Select External pull-up to V_{DD33} is required under all conditions, DO NOT FLOAT. Connect to external pull-up and pull-down resistor to create a voltage divider. See *Figure 17*
SCL	8	I/O, LVCMOS Open Drain	I2C Clock Input / Output Interface Must have an external pull-up to V_{DD33}, DO NOT FLOAT. Recommended pull-up: 4.7kΩ.
SDA	9	I/O, LVCMOS Open Drain	I2C Data Input / Output Interface Must have an external pull-up to V_{DD33}, DO NOT FLOAT. Recommended pull-up: 4.7kΩ.
Status			
INTB	31	O, LVCMOS Open Drain	HDCP Interrupt INTB = H, normal INTB = L, Interrupt request Recommended pull-up: 4.7kΩ to V_{DDIO}
FPD-Link III Serial Interface			
DOUT+	20	O, LVDS	True Output The output must be AC-coupled with a 0.1µF capacitor.
DOUT-	19	O, LVDS	Inverting Output The output must be AC-coupled with a 0.1µF capacitor.
CMF	23	Analog	Common Mode Filter. Connect 0.1µF to GND
Power* and Ground			
V_{DD33}	22	Power	Power to on-chip regulator **3.0 V - 3.6 V**. Requires 4.7 uF to GND
V_{DDIO}	30	Power	LVCMOS I/O Power **1.8 V ±5% OR 3.0 V - 3.6 V**. Requires 4.7 uF to GND
GND	DAP	Ground	DAP is the large metal contact at the bottom side, located at the center of the LLP package. **Connect to the ground plane** (GND) with at least 9 vias.
Regulator Capacitor			
CAPHS12, CAPP12	17, 14	CAP	Decoupling capacitor connection for on-chip regulator. Requires a 4.7uF to GND at each CAP pin.
CAPL12	7	CAP	Decoupling capacitor connection for on-chip regulator. Requires two 4.7uF to GND at this CAP pin.
Others			
NC	16	NC	Do not connect.
RES[1:0]	18, 15	GND	Reserved. Tie to Ground.

*The VDD (V_{DD33} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise.

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Block Diagram



Ordering Information

PART NUMBER	PACKAGE DESCRIPTION	QUANTITY	SPEC	PACKAGE ID
DS90UH925QSQE	48-pin LLP, 7.0 X 7.0 X 0.8 mm, 0.5 mm pitch	250	NOPB	SQA48A
DS90UH925QSQ	48-pin LLP, 7.0 X 7.0 X 0.8 mm, 0.5 mm pitch	1000	NOPB	SQA48A
DS90UH925QSQX	48-pin LLP, 7.0 X 7.0 X 0.8 mm, 0.5 mm pitch	2500	NOPB	SQA48A

Note: Automotive Grade (Q) product incorporates enhanced manufacturing and support processes for the automotive market, including defect detection methodologies. Reliability qualification is compliant with the requirements and temperature grades defined in the AEC Q100 standard. Automotive Grade products are identified with the letter Q. For more information go to http://www.ti.com/automotive.

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Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Supply Voltage – V_{DD33}	−0.3V to +4.0V
Supply Voltage – V_{DDIO}	−0.3V to +4.0V
LVCMOS I/O Voltage	−0.3V to (V_{DDIO} + 0.3V)
Serializer Output Voltage	−0.3V to +2.75V
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
48L LLP Package Maximum Power Dissipation Capacity at 25°C	
Derate above 25°C	1/ θ_{JA}°C/W
θ_{JA}	35 °C/W
θ_{JC}	5.2 °C/W
ESD Rating (IEC, powered-up only), R_D = 330Ω, C_S = 150pF	
Air Discharge (D_{OUT+}, D_{OUT-})	≥±15 kV
Contact Discharge (D_{OUT+}, D_{OUT-})	≥±8 kV
ESD Rating (ISO10605), R_D = 330Ω, C_S = 150pF	
Air Discharge (D_{OUT+}, D_{OUT-})	≥±15 kV
Contact Discharge(D_{OUT+}, D_{OUT-})	≥±8 kV
ESD Rating (ISO10605), R_D = 2kΩ, C_S = 150pF or 330pF	
Air Discharge (D_{OUT+}, D_{OUT-})	≥±15 kV
Contact Discharge (D_{OUT+}, D_{OUT-})	≥±8 kV
ESD Rating (HBM)	≥±8 kV
ESD Rating (CDM)	≥±1.25 kV
ESD Rating (MM)	≥±250 V
For soldering specifications: see product folder at www.ti.com and www.ti.com/lit/an/snoa549c/snoa549c.pdf	

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{DD33})	3.0	3.3	3.6	V
LVCMOS Supply Voltage (V_{DDIO})	3.0	3.3	3.6	V
OR				
LVCMOS Supply Voltage (V_{DDIO})	1.71	1.8	1.89	V
Operating Free Air Temperature (T_A)	−40	+25	+105	°C
PCLK Frequency	5		85	MHz
Supply Noise (*Note 7*)			100	mV_{P-P}

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DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (*Note 2*, *Note 3*, *Note 4*)

Symbol	Parameter	Conditions		Pin/Freq.	Min	Typ	Max	Units
LVCMOS I/O DC SPECIFICATIONS								
V_{IH}	High Level Input Voltage	V_{DDIO} = 3.0 to 3.6V		PDB	2.0		V_{DDIO}	V
V_{IL}	Low Level Input Voltage	V_{DDIO} = 3.0 to 3.6V			GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO} = 3.0 to 3.6V			−10	±1	+10	µA
V_{IH}	High Level Input Voltage	V_{DDIO} = 3.0 to 3.6V		R[7:0], G[7:0], B[7:0], HS, VS, DE, PCLK, I2S_CLK, I2S_WC, I2S_DA, I2S_DB	2.0		V_{DDIO}	V
		V_{DDIO} = 1.71 to 1.89V			0.65* V_{DDIO}		V_{DDIO}	V
V_{IL}	Low Level Input Voltage	V_{DDIO} = 3.0 to 3.6V			GND		0.8	V
		V_{DDIO} = 1.71 to 1.89V			GND		0.35* V_{DDIO}	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}	V_{DDIO} = 3.0 to 3.6V		−10	±1	+10	µA
			V_{DDIO} = 1.71 to 1.89V		−10	±1	+10	µA
V_{OH}	High Level Output Voltage	I_{OH} = −4mA	V_{DDIO} = 3.0 to 3.6V	GPIO[3:0], GPO_REG[8:4]	2.4		V_{DDIO}	V
			V_{DDIO} = 1.71 to 1.89V		V_{DDIO} - 0.45		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	I_{OL} = +4mA	V_{DDIO} = 3.0 to 3.6V		GND		0.4	V
			V_{DDIO} = 1.71 to 1.89V		GND		0.35	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				−50		mA
I_{OZ}	TRI-STATE® Output Current	V_{OUT} = 0V or V_{DDIO}, PDB = L,			−10		+10	µA
FPD-LINK III CML DRIVER DC SPECIFICATIONS								
V_{ODp-p}	Differential Output Voltage (DOUT+) – (DOUT-)	R_L = 100Ω, *Figure 1*		DOUT+, DOUT-	1160	1250	1340	mVp-p
ΔV_{OD}	Output Voltage Unbalance					1	50	mV
V_{OS}	Offset Voltage – Single-ended	R_L = 100Ω, *Figure 1*				2.5-0.25*V_{ODp-p} (TYP)		V
ΔV_{OS}	Offset Voltage Unbalance Single-ended					1	50	mV
I_{OS}	Output Short Circuit Current	DOUT+/- = 0V, PDB = L or H				−38		mA
R_T	Internal Termination Resistor - Single ended				40	52	62	Ω

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Symbol	Parameter	Conditions		Pin/Freq.	Min	Typ	Max	Units
SUPPLY CURRENT								
I_{DD1}	Supply Current (includes load current) R_L = 100Ω, f = 85MHz	Checker Board Pattern, *Figure 2*	V_{DD33}= 3.6V	V_{DD33}		148	170	mA
I_{DDIO1}			V_{DDIO} = 3.6V	V_{DDIO}		90	180	µA
			V_{DDIO} = 1.89V			1	1.6	mA
I_{DDS1}	Supply Current Remote Auto Power Down Mode	0x01[7] = 1, deserializer is powered down	V_{DD33} = 3.6V	V_{DD33}		1.2	2.4	mA
I_{DDIOS1}			V_{DDIO} = 3.6V	V_{DDIO}		65	150	µA
			V_{DDIO} = 1.89V			55	150	µA
I_{DDS2}	Supply Current Power Down	PDB = L, All LVCMOS inputs are floating or tied to GND	V_{DD33} = 3.6V	V_{DD33}		1	2	mA
I_{DDIOS2}			V_{DDIO} = 3.6V	V_{DDIO}		65	150	µA
			V_{DDIO} = 1.89V			50	150	µA

AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (*Note 2*, *Note 3*, *Note 4*)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
GPIO BIT RATE							
B_R	Forward Channel Bit Rate	(*Note 8*, *Note 9*)	f = 5 – 85 MHz GPIO[3:0]		0.25* f		Mbps
	Back Channel Bit Rate				75		kbps
RECOMMENDED TIMING FOR PCLK							
t_{TCP}	PCLK Period	(*Note 8*, *Note 9*)	PCLK	11.76	T	200	ns
t_{CIH}	PCLK Input High Time			0.4*T	0.5*T	0.6*T	ns
t_{CIL}	PCLK Input Low Time			0.4*T	0.5*T	0.6*T	ns
t_{CLKT}	PCLK Input Transition Time *Figure 3* (*Note 8*, *Note 9*)		f = 5 MHz	4.0			ns
			f = 85 MHz	0.5			ns
t_{IJIT}	PCLK Input Jitter Tolerance, Bit Error Rate ≤10^{-10}	f / 40 < Jitter Freq < f / 20 (*Note 10*, *Note 8*)	f = 5 – 78MHz	0.4	0.6		UI
SWITCHING CHARACTERISTICS							
t_{LHT}	CML Output Low-to-High Transition Time	See *Figure 4*	DOUT+, DOUT-		80	130	ps
t_{HLT}	CML Output High-to-Low Transition Time				80	130	ps
t_{DIS}	Data Input Setup to PCLK	See *Figure 5*	R[7:0], G[7:0], B[7:0], HS, VS, DE, PCLK, I2S_CLK, I2S_WC, I2S_DA, I2S_DB	2.0			ns
t_{DIH}	Data Input Hold from PCLK			2.0			ns
t_{PLD}	Serializer PLL Lock Time	*Figure 6* (*Note 5*)	f = 5 – 85 MHz		131*T		ns
t_{SD}	Delay — Latency		f = 5 – 85 MHz		145*T		ns
t_{TJIT}	Output Total Jitter, Bit Error Rate ≥10^{-10} *Figure 7* (*Note 6*, *Note 8*, *Note 9*)	R_L = 100Ω f = 85MHz, LFMODE = L	DOUT+, DOUT-		0.25	0.30	UI
		R_L = 100Ω f = 5MHz, LFMODE = H			0.25	0.30	UI

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Recommended Timing for the Serial Control Bus

Over 3.3V supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency	Standard Mode	0		100	kHz
		Fast Mode	0		400	kHz
t_{LOW}	SCL Low Period	Standard Mode	4.7			us
		Fast Mode	1.3			us
t_{HIGH}	SCL High Period	Standard Mode	4.0			us
		Fast Mode	0.6			us
$t_{HD;STA}$	Hold time for a start or a repeated start condition *Figure 8*	Standard Mode	4.0			us
		Fast Mode	0.6			us
$t_{SU:STA}$	Set Up time for a start or a repeated start condition *Figure 8*	Standard Mode	4.7			us
		Fast Mode	0.6			us
$t_{HD;DAT}$	Data Hold Time *Figure 8*	Standard Mode	0		3.45	us
		Fast Mode	0		0.9	us
$t_{SU;DAT}$	Data Set Up Time *Figure 8*	Standard Mode	250			ns
		Fast Mode	100			ns
$t_{SU;STO}$	Set Up Time for STOP Condition, *Figure 8*	Standard Mode	4.0			us
		Fast Mode	0.6			us
t_{BUF}	Bus Free Time Between STOP and START, *Figure 8*	Standard Mode	4.7			us
		Fast Mode	1.3			us
t_r	SCL & SDA Rise Time, *Figure 8*	Standard Mode			1000	ns
		Fast Mode			300	ns
t_f	SCL & SDA Fall Time, *Figure 8*	Standard Mode			300	ns
		Fast mode			300	ns

DC and AC Serial Control Bus Characteristics

Over 3.3V supply and temperature ranges unless otherwise specified. (*Note 2*, *Note 3*, *Note 4*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Level	SDA and SCL	0.7* V_{DD33}		V_{DD33}	V
V_{IL}	Input Low Level Voltage	SDA and SCL	GND		0.3* V_{DD33}	V
V_{HY}	Input Hysteresis			>50		mV
V_{OL}		SDA, IOL = 1.25mA	0		0.36	V
I_{in}		SDA or SCL, Vin = V_{DD33} or GND	-10		+10	µA
t_R	SDA RiseTime – READ	SDA, RPU = 10kΩ, Cb ≤ 400pF, *Figure 8*		430		ns
t_F	SDA Fall Time – READ			20		ns
$t_{SU;DAT}$	Set Up Time — READ	*Figure 8*		560		ns
$t_{HD;DAT}$	Hold Up Time — READ	*Figure 8*		615		ns
t_{SP}	Input Filter			50		ns
C_{in}	Input Capacitance	SDA or SCL		<5		pF

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Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 2: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: Typical values represent most likely parametric norms at V_{DD} = 3.3V, Ta = +25 degC, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 4: Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD and ΔVOD, which are differential voltages.

Note 5: t_{PLD} is the time required by the device to obtain lock when exiting power-down state with an active PCLK.

Note 6: UI – Unit Interval is equivalent to one serialized data bit width (1UI = 1 / 35*PCLK). The UI scales with PCLK frequency.

Note 7: Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the V_{DD33} and V_{DDIO}supplies with amplitude = 100 mVp-p measured at the device V_{DD33} and V_{DDIO} pins. Bit error rate testing of input to the Ser and output of the Des with 10 meter cable shows no error when the noise frequency on the Ser is less than 50MHz. The Des on the other hand shows no error when the noise frequency is less than 50 MHz.

Note 8: Specification is guaranteed by characterization and is not tested in production.

Note 9: Specification is guaranteed by design and is not tested in production.

Note 10: Jitter Frequency is specified in conjunction with DS90UH926 PLL bandwidth.

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AC Timing Diagrams and Test Circuits

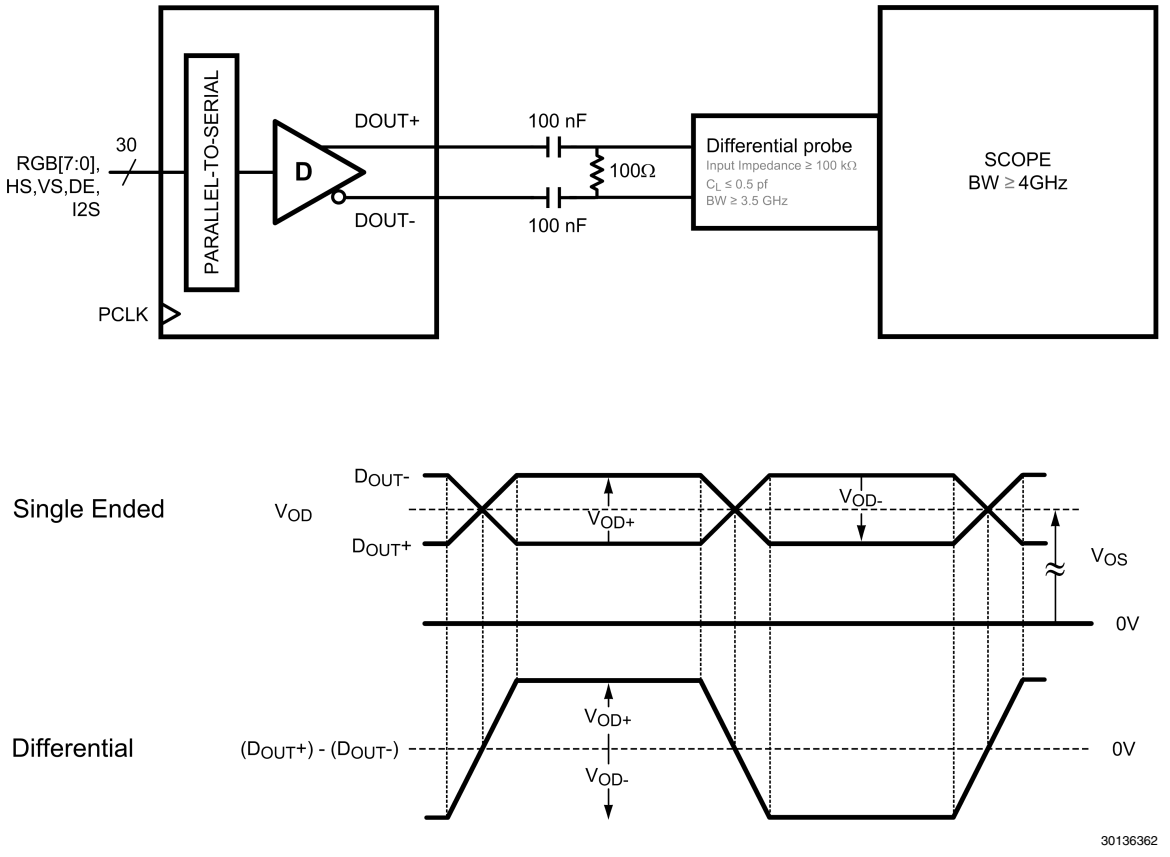


FIGURE 1. Serializer VOD DC Output

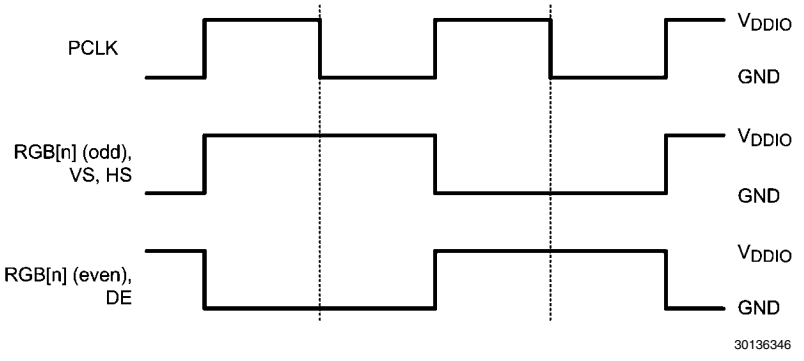


FIGURE 2. Checkboard Data Pattern

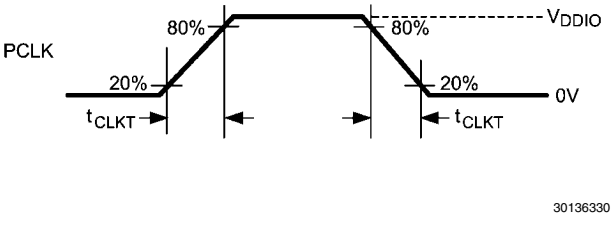


FIGURE 3. Serializer Input Clock Transition Time

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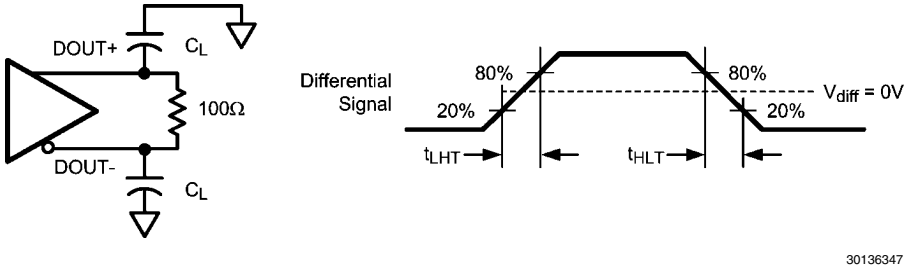


FIGURE 4. Serializer CML Output Load and Transition Time

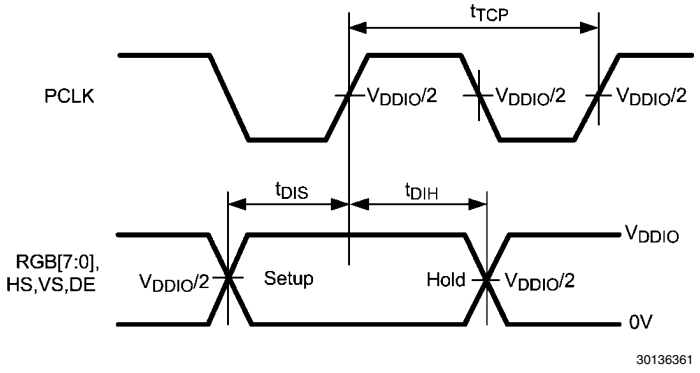


FIGURE 5. Serializer Setup and Hold Times

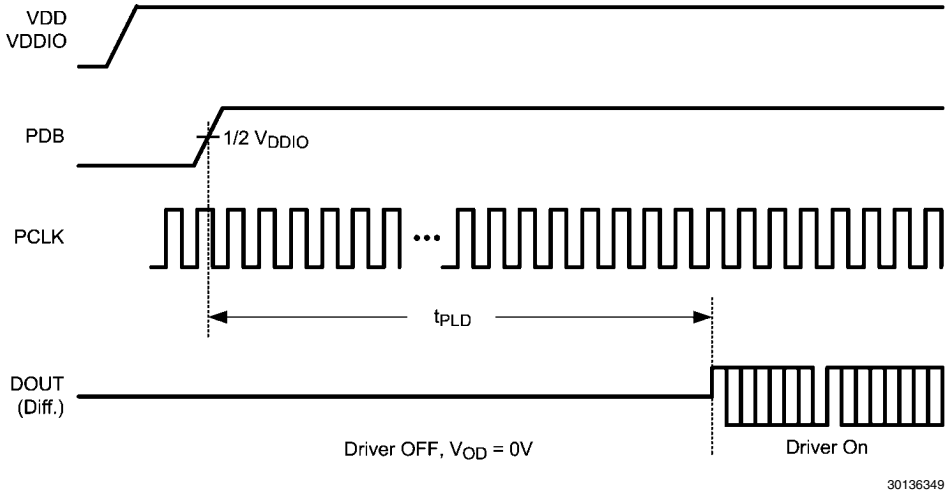


FIGURE 6. Serializer Lock Time

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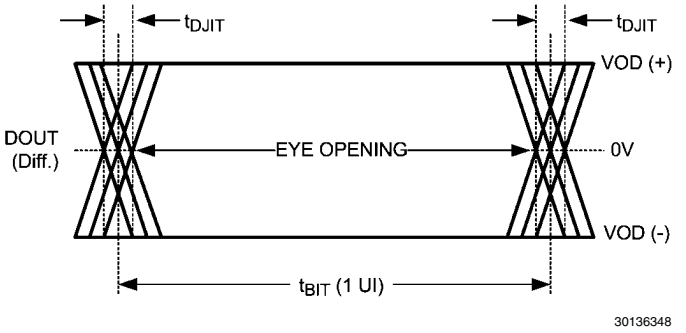


FIGURE 7. Serializer CML Output Jitter

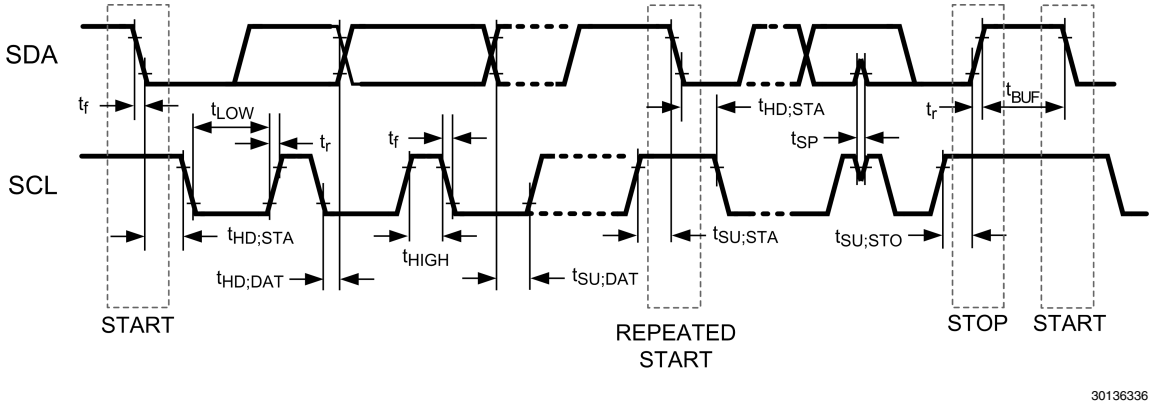


FIGURE 8. Serial Control Bus Timing Diagram

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Functional Description

The DS90UH925Q serializer transmits a 35-bit symbol over a single serial FPD-Link III pair operating up to 2.975 Gbps line rate. The serial stream contains an embedded clock, video control signals and DC-balanced video data and audio data which enhance signal quality to support AC coupling. The DS90UH925Q serializes video and audio data then applies encryption through a High-Bandwidth Digital Content Protection (HDCP) Cipher and transmits out through the FPD-Link III interface. Audio encryption is supported. The serializer also includes the HDCP cipher. On board non-volatile memory stores the HDCP keys. All key exchange is conducted over the FPD-Link III bidirectional control interface. The serializer is intended for use with the DS90UH926Q deserializer, but is also backward compatible with DS90UR906Q or DS90UR908Q FPD-Link II deserializer.

HIGH SPEED FORWARD CHANNEL DATA TRANSFER

The High Speed Forward Channel (HS_FC) is composed of 35 bits of data containing RGB data, sync signals, HDCP, I2C, and I2S audio transmitted from Serializer to Deserializer. *Figure 9* illustrates the serial stream per PCLK cycle. This data payload is optimized for signal transmission over an AC coupled link. Data is randomized, balanced and scrambled.

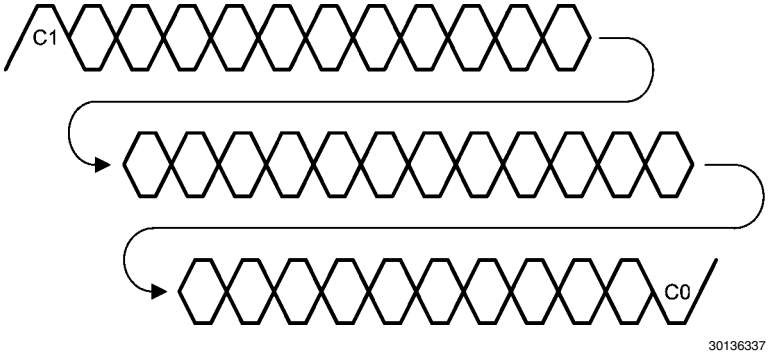


FIGURE 9. FPD-Link III Serial Stream

The device supports clocks in the range of 5 MHz to 85 MHz. The application payload rate is 2.975 Gbps maximum (175 Mbps minimum) with the actual line rate of 2.975 Gbps maximum and 525 Mbps Minimum.

LOW SPEED BACK CHANNEL DATA TRANSFER

The Low-Speed Backward Channel (LS_BC) of the DS90UH925Q provides bidirectional communication between the display and host processor. The information is carried back from the Deserializer to the Serializer per serial symbol. The back channel control data is transferred over the single serial link along with the high-speed forward data, DC balance coding and embedded clock information. This architecture provides a backward path across the serial link together with a high speed forward channel. The back channel contains the I2C, HDCP, CRC and 4 bits of standard GPIO information with 10 Mbps line rate.

BACKWARD COMPATIBLE MODE

The DS90UH925Q is also backward compatible to DS90UR906Q and DS90UR908Q FPD Link II deserializers at 5-65 MHz of PCLK. It transmits 28-bits of data over a single serial FPD-Link II pair operating at the line rate of 140 Mbps to 1.82 Gbps. The backward configuration mode can be set via MODE_SEL pin (*Table 1*) or the configuration register (*Table 6*). Note: frequency range = 15 - 65MHz when LFMODE = 0 and frequency range = 5 - <15MHz when LFMODE = 1.

COMMON MODE FILTER PIN (CMF)

The serializer provides access to the center tap of the internal termination. A capacitor must be placed on this pin for additional common-mode filtering of the differential pair. This can be useful in high noise environments for additional noise rejection capability. A 0.1 µF capacitor must be connected to this pin to Ground.

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VIDEO CONTROL SIGNAL FILTER

When operating the devices in Normal Mode, the Video Control Signals (DE, HS, VS) have the following restrictions:

- Normal Mode with Control Signal Filter Enabled: DE and HS — Only 2 transitions per 130 clock cycles are transmitted, the transition pulse must be 3 PCLK or longer.
- Normal Mode with Control Signal Filter Disabled: DE and HS — Only 2 transitions per 130 clock cycles are transmitted, no restriction on minimum transition pulse.
- VS — Only 1 transition per 130 clock cycles are transmitted, minimum pulse width is 130 clock cycles.

Video Control Signals are defined as low frequency signals with limited transitions. Glitches of a control signal can cause a visual display error. This feature allows for the chipset to validate and filter out any high frequency noise on the control signals. See *Figure 10*.

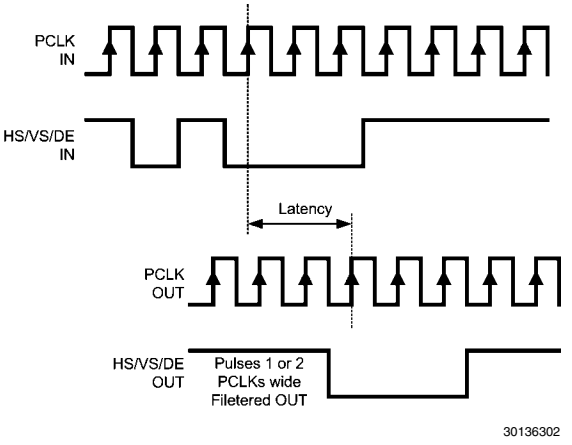


FIGURE 10. Video Control Signal Filter Waveform

EMI REDUCTION FEATURES

Input SSC Tolerance (SSCT)

The DS90UH925Q serializer is capable of tracking a triangular input spread spectrum clocking (SSC) profile up to +/-2.5% amplitude deviations (center spread), up to 35 kHz modulation at 5–85 MHz, from a host source.

LVCMOS V_{DDIO} OPTION

1.8V or 3.3V Inputs and Outputs are powered from a separate V_{DDIO} supply to offer compatibility with external system interface signals. Note: When configuring theV_{DDIO} power supplies, all the single-ended data and control input pins for device need to scale together with the same operating V_{DDIO} levels.

POWER DOWN (PDB)

The Serializer has a PDB input pin to ENABLE or POWER DOWN the device. This pin can be controlled by the host or through the V_{DDIO}, where V_{DDIO} = 3.0V to 3.6V or V_{DD33}. To save power disable the link when the display is not needed (PDB = LOW). When the pin is driven by the host, make sure to release it after V_{DD33} and V_{DDIO} have reached final levels; no external components are required. In the case of driven by the V_{DDIO} = 3.0V to 3.6V or V_{DD33} directly, a 10 kohm resistor to the V_{DDIO} = 3.0V to 3.6V or V_{DD33} , and a >10uF capacitor to the ground are required (See *Figure 21* Typical Connection Diagram).

REMOTE AUTO POWER DOWN MODE

The Serializer features a remote auto power down mode. During the power down mode of the pairing deserializer, the Serializer enters the remote auto power down mode. In this mode, the power dissipation of the Serializer is reduced significantly. When the Deserializer is powered up, the Serializer enters the normal power on mode automatically. This feature is enabled through the register bit 0x01[7] *Table 6*.

INPUT PCLK LOSS DETECT

The serializer can be programmed to enter a low power SLEEP state when the input clock (PCLK) is lost. A clock loss condition is detected when PCLK drops below approximately 1MHz. When a PCLK is detected again, the serializer will then lock to the incoming PCLK. Note – when PCLK is lost, the Serial Control Bus Registers values are still RETAINED.

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SERIAL LINK FAULT DETECT

The serial link fault detection is able to detect any of following seven (7) conditions

1) cable open
2) “+” to “-“ short
3) “+” short to GND
4) “-“ short to GND
5) “+” short to battery
6) “-“ short to battery
7) Cable is linked correctly

If any one of the fault conditions occurs, The Link Detect Status is 0 (cable is not detected) on bit 0 of address 0x0C *Table 6*.

PIXEL CLOCK EDGE SELECT (RFB)

The RFB control register bit selects which edge of the Pixel Clock is used. For the serializer, this pin determines the edge that the data is latched on. If RFB is HIGH (‘1’), data is latched on the Rising edge of the PCLK. If RFB is LOW (‘0’), data is latched on the Falling edge of the PCLK.

LOW FREQUENCY OPTIMIZATION (LFMODE)

The LFMODE is set via register (0x04[1:0]) or MODE_SEL Pin 24 (*Table 1*). It controls the operating frequency of the serializer. If LFMODE is Low (default), the PCLK frequency is between 15 MHz and 85 MHz. If LFMODE is High, the PCLK frequency is between 5 MHz and <15 MHz. Please note when the device LFMODE is changed, a PDB reset is required.

INTERRUPT PIN — FUNCTIONAL DESCRIPTION AND USAGE (INTB)

1. On DS90UH925, set register 0xC6[5] = 1 and 0xC6[0] = 1
2. DS90UH926Q deserializer INTB_IN (pin 16) is set LOW by some downstream device.
3. DS90UH925Q serializer pulls INTB (pin 31) LOW. The signal is active low, so a LOW indicates an interrupt condition.
4. External controller detects INTB = LOW; to determine interrupt source, read HDCP_ISR register .
5. A read to HDCP_ISR will clear the interrupt at the DS90UH925, releasing INTB.
6. The external controller typically must then access the remote device to determine downstream interrupt source and clear the interrupt driving INTB_IN. This would be when the downstream device releases the INTB_IN (pin 16) on the DS90UH926Q. The system is now ready to return to step (1) at next falling edge of INTB_IN.

CONFIGURATION SELECT (MODE_SEL)

Configuration of the device may be done via the MODE_SEL input pin, or via the configuration register bit. A pull-up resistor and a pull-down resistor of suggested values may be used to set the voltage ratio of the MODE_SEL input (V_{R4}) and V_{DD33} to select one of the other 10 possible selected modes. See *Figure 11* and *Table 1*.

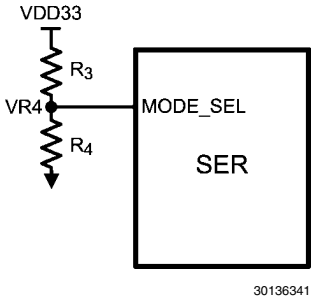


FIGURE 11. MODE_SEL Connection Diagram

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TABLE 1. Configuration Select (MODE_SEL)

#	Ideal Ratio V_{R4}/V_{DD33}	Ideal V_{R4} (V)	Suggested Resistor R3 kΩ (1% tol)	Suggested Resistor R4 kΩ (1% tol)	LFMODE	Repeater	Backward Compatible	I2S Channel B (18–bit Mode)
1	0	0	Open	40.2 or Any	L	L	L	L
2	0.121	0.399	294	40.2	L	L	L	H
3	0.152	0.502	280	49.9	L	H	L	L
4	0.242	0.799	240	76.8	L	H	L	H
5	0.311	1.026	226	102	H	L	L	L
6	0.402	1.327	196	130	H	L	L	H
7	0.492	1.624	169	165	H	H	L	L
8	0.583	1.924	137	191	H	H	L	H
9	0.629	2.076	124	210	L	L	H*	L
10	0.727	2.399	90.9	243	H	L	H*	L

LFMODE:
L = frequency range is 15 – 85 MHz (Default)
H = frequency range is 5 – <15 MHz
Repeater:
L = Repeater *OFF* (Default)
H = Repeater *ON*
Backward Compatible:
L = Backward Compatible is *OFF* (Default)
H = Backward Compatible is *ON*; DES = DS90UR906Q or DS90UR916Q or DS90UR908Q
– frequency range = 15 - 65MHz when LFMODE = 0
– frequency range = 5 - <15MHz when LFMODE = 1
I2S Channel B:
L = I2S Channel B is *OFF*, Normal 24-bit RGB Mode (Default)
H = I2S Channel B is *ON*, 18-bit RGB Mode with I2S_DB Enabled. Note: use of GPIO(s) on unused inputs must be enabled by register.

GPIO[3:0] and GPO_REG[8:4]

In 18-bit RGB operation mode, the optional R[1:0] and G[1:0] of the DS90UH925Q can be used as the general purpose IOs GPIO [3:0] in either forward channel (Inputs) or back channel (Outputs) application.

GPIO[3:0] Enable Sequence

See *Table 2* for the GPIO enable sequencing.

Step 1: Enable the 18-bit mode either through the configuration register bit *Table 6* on DS90UH925Q only. DS90UH926Q is automatically configured as in the 18-bit mode.

Step 2: To enable GPIO3 forward channel, write 0x03 to address 0x0F on DS90UH925Q, then write 0x05 to address 0x1F on DS90UH926Q.

TABLE 2. GPIO Enable Sequencing Table

#	Description	Device	Forward Channel	Back Channel
1	Enable 18-bit mode	DS90UH925Q	0x12 = 0x04	0x12 = 0x04
		DS90UH926Q	Auto Load from DS90UH925Q	Auto Load from DS90UH925Q
2	GPIO3	DS90UH925Q	0x0F = 0x03	0x0F = 0x05
		DS90UH926Q	0x1F = 0x05	0x1F = 0x03
3	GPIO2	DS90UH925Q	0x0E = 0x30	0x0E = 0x50
		DS90UH926Q	0x1E = 0x50	0x1E = 0x30
4	GPIO1	DS90UH925Q	0x0E = 0x03	0x0E = 0x05
		DS90UH926Q	0x1E = 0x05	0x0E = 0x05
5	GPIO0	DS90UH925Q	0x0D = 0x93	0x0D = 0x95
		DS90UH926Q	0x1D = 0x95	0x1D = 0x93

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GPO_REG[8:4] Enable Sequence

GPO_REG[8:4] are the outputs only pins. They must be programmed through the local register bits. See *Table 3* for the GPO_REG enable sequencing.

Step 1: Enable the 18-bit mode either through the configuration register bit on DS90UH925Q only. DS90UH926Q is automatically configured as in the 18-bit mode.

Step 2: To enable GPO_REG8 outputs an "1", write 0x90 to address 0x11 on DS90UH925Q.

TABLE 3. GPO_REG Enable Sequencing Table

#	Description	Device	Local Access	Local Output
1	Enable 18-bit mode	DS90UH925Q	0x12 = 0x04	
2	GPO_REG8	DS90UH925Q	0x11 = 0x90	"1"
			0x11 = 0x10	"0"
3	GPO_REG7	DS90UH925Q	0x11 = 0x09	"1"
			0x11 = 0x01	"0"
4	GPO_REG6	DS90UH925Q	0x10 = 0x90	"1"
			0x10 = 0x10	"0"
5	GPO_REG5	DS90UH925Q	0x10 = 0x09	"1"
			0x10 = 0x01	"0"
6	GPO_REG4	DS90UH925Q	0x0F = 0x90	"1"
			0x0F = 0x10	"0"

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I2S TRANSMITTING

In normal 24-bit RGB operation mode, the DS90UH925Q supports 3 bits of I2S. They are I2S_CLK, I2S_WC and I2S_DA. The optionally encrypted and packetized audio information can be transmitted during the video blanking (data island transport) or during active video (forward channel frame transport). Note: The bit rates of any I2S bits must maintain one fourth of the PCLK rate. The audio encryption capability is supported per HDCP v1.3.

Secondary I2S Channel

In I2S Channel B operation mode, the secondary I2S data (I2S_DB) can be used as the additional I2S audio in addition to the 3–bit of I2S. The I2S_DB input must be synchronized to I2S_CLK and aligned with I2S_DA and I2S_WC at the input to the serializer. This operation mode is enabled through either the MODE_SEL pin (*Table 1*) or through the register bit 0x12[0] (*Table 6*).

Table 4 below covers the range of I2S sample rates.

TABLE 4. Audio Interface Frequencies

Sample Rate (kHz)	I2S Data Word Size (bits)	I2S CLK (MHz)
32	16	1.024
44.1	16	1.411
48	16	1.536
96	16	3.072
192	16	6.144
32	24	1.536
44.1	24	2.117
48	24	2.304
96	24	4.608
192	24	9.216
32	32	2.048
44.1	32	2.822
48	32	3.072
96	32	6.144
192	32	12.288

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HDCP

The Cipher function is implemented in the serializer per HDCP v1.3 specification. The DS90UH925Q provides HDCP encryption of audiovisual content when connected to an HDCP capable FPD-Link III deserializer such as the DS90UH926Q. HDCP authentication and shared key generation is performed using the HDCP Control Channel which is embedded in the forward and backward channels of the serial link. An on-chip Non-Volatile Memory (NVM) is used to store the HDCP keys. The confidential HDCP keys are loaded by TI during the manufacturing process and are not accessible external to the device.

The DS90UH925Q uses the Cipher engine to encrypt the data as per HDCP v1.3. The encrypted data is transmitted through the FPD-Link III interface.

HDCP REPEATER

When DS90UH925Q and DS90UH926Q are configured as the HDCP Repeater application, it provides a mechanism to extend HDCP transmission over multiple links to multiple display devices. This repeater application provides a mechanism to authenticate all HDCP Receivers in the system and distribute protected content to the HDCP Receivers using the encryption mechanisms provided in the HDCP specification.

Repeater Configuration

In HDCP repeater application, In this document, the DS90UH925Q is referred to as the HDCP Transmitter or transmit port (TX), and the DS90UH926Q is referred to as the HDCP Receiver (RX). *Figure 12* shows the maximum configuration supported for HDCP Repeater implementations using the DS90UH925Q (TX) and DS90UH926Q (RX). Two levels of HDCP Repeaters are supported with a maximum of three HDCP Transmitters per HDCP Receiver.

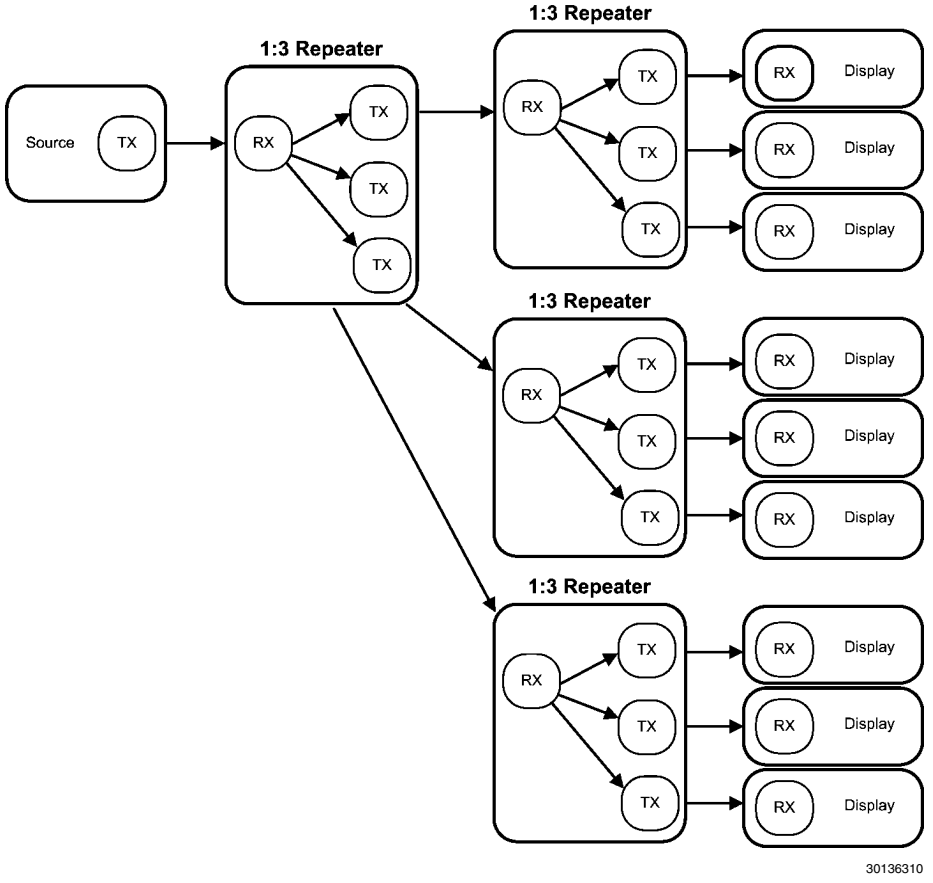


FIGURE 12. HDCP Maximum Repeater Application

To support HDCP Repeater operation, the DS90UH926Q Deserializer includes the ability to control the downstream authentication process, assemble the KSV list for downstream HDCP Receivers, and pass the KSV list to the upstream HDCP Transmitter. An I2C master within the DS90UH926Q communicates with the I2C slave within the DS90UH925Q Serializer. The DS90UH925Q Serializer handles authenticating with a downstream HDCP Receiver and makes status available through the I2C interface. The DS90UH926Q monitors the transmit port status for each DS90UH925Q and reads downstream KSV and KSV list values from the DS90UH925Q.

In addition to the I2C interface used to control the authentication process, the HDCP Repeater implementation includes two other interfaces. A parallel LVCMOS interface provides the unencrypted video data in 24-bit RGB format and includes the DE/VS/HS control signals. In addition to providing the RGB video data, the parallel LVCMOS interface communicates control information and

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packetized audio data during video blanking intervals. A separate I2S audio interface may optionally be used to send I2S audio data between the HDCP Receiver and HDCP Transmitter in place of using the packetized audio over the parallel LVCMOS interface. All audio and video data is decrypted at the output of the HDCP Receiver and is re-encrypted by the HDCP Transmitter.

Figure 13 provides more detailed block diagram of a 1:2 HDCP repeater configuration.

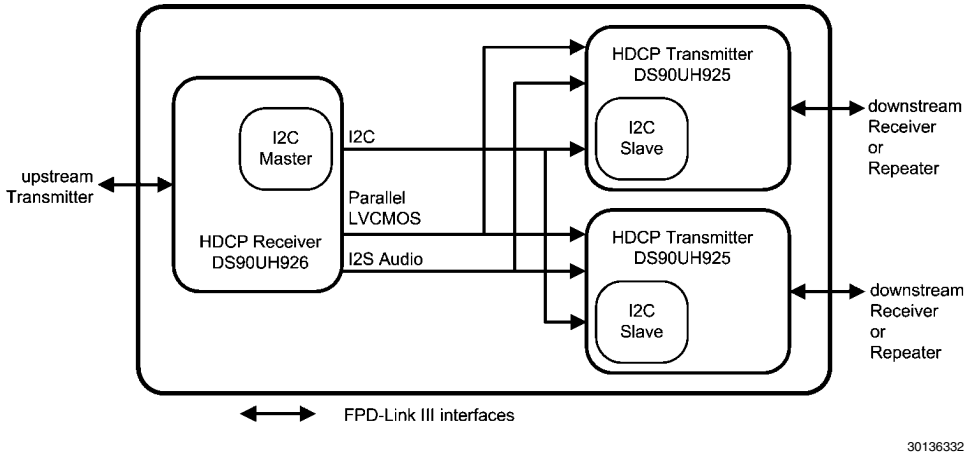


FIGURE 13. HDCP 1:2 Repeater Configuration

Repeater Connections

The HDCP Repeater requires the following connections between the HDCP Receiver and each HDCP Transmitter *Figure 14*.

1) Video Data – Connect PCLK, RGB and control signals (DE, VS, HS).

2) I2C – Connect SCL and SDA signals. Both signals should be pulled up to V_{DD33} with 4.7 kΩ resistors.

3) Audio – Connect I2S_CLK, I2S_WC, and I2S_DA signals.

4) IDx pin – Each HDCP Transmitter and Receiver must have an unique I2C address.

5) MODE_SEL pin – All HDCP Transmitter and Receiver must be set into the Repeater Mode.

6) Interrupt pin – Connect DS90UH926Q INTB_IN pin to DS90UH925Q INTB pin. The signal must be pulled up to V_{DDIO}.

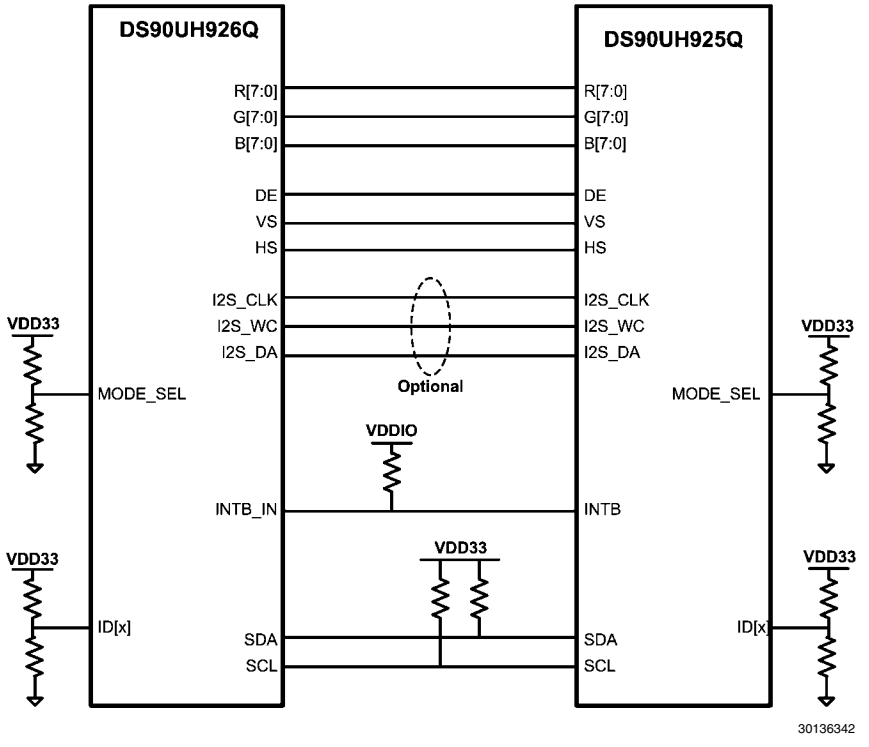


FIGURE 14. HDCP Repeater Connection Diagram

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BUILT IN SELF TEST (BIST)

An optional At-Speed Built In Self Test (BIST) feature supports the testing of the high speed serial link and the low- speed back channel. This is useful in the prototype stage, equipment production, in-system test and also for system diagnostics. Note: BIST not available in backwards compatible mode.

BIST Configuration and Status

The BIST mode is enabled at the deserializer by the Pin select (Pin 44 BISTEN and Pin 16 BISTC) or configuration register (*Table 6*) through the deserializer. When LFMODE = 0, the pin based configuration defaults to external PCLK or 33 MHz internal Oscillator clock (OSC) frequency. In the absence of PCLK, the user can select the desired OSC frequency (default 33 MHz or 25MHz) through the register bit. When LFMODE = 1, the pin based configuration defaults to external PCLK or 12.5MHz MHz internal Oscillator clock (OSC) frequency.

When BISTEN of the deserializer is high, the BIST mode enable information is sent to the serializer through the Back Channel. The serializer outputs a test pattern and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The PASS output pin toggles to flag any payloads that are received with 1 to 35 bit errors.

The BIST status is monitored real time on PASS pin. The result of the test is held on the PASS output until reset (new BIST test or Power Down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the deserializer BISTEN pin. This BIST feature also contains a Link Error Count and a Lock Status. If the connection of the serial link is broken, then the link error count is shown in the register. When the PLL of the deserializer is locked or unlocked, the lock status can be read in the register. See *Table 6*.

Sample BIST Sequence

See *Figure 15* for the BIST mode flow diagram.

Step 1: For the DS90UH925Q and DS90UH926Q FPD-Link III chipset, BIST Mode is enabled via the BISTEN pin of DS90UH926Q FPD-Link III deserializer. The desired clock source is selected through BISTC pin.

Step 2: The DS90UH925Q serializer is woken up through the back channel if it is not already on. The all zero pattern on the data pins is sent through the FPD-Link III to the deserializer. Once the serializer and the deserializer are in BIST mode and the deserializer acquires Lock, the PASS pin of the deserializer goes high and BIST starts checking the data stream. If an error in the payload (1 to 35) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3: To Stop the BIST mode, the deserializer BISTEN pin is set Low. The deserializer stops checking the data. The final test result is held on the PASS pin. If the test ran error free, the PASS output will be High. If there was one or more errors detected, the PASS output will be Low. The PASS output state is held until a new BIST is run, the device is RESET, or Powered Down. The BIST duration is user controlled by the duration of the BISTEN signal.

Step 4: The Link returns to normal operation after the deserializer BISTEN pin is low. *Figure 16* shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission etc.), thus they may be introduced by greatly extending the cable length, faulting the interconnect, reducing signal condition enhancements (Rx Equalization).

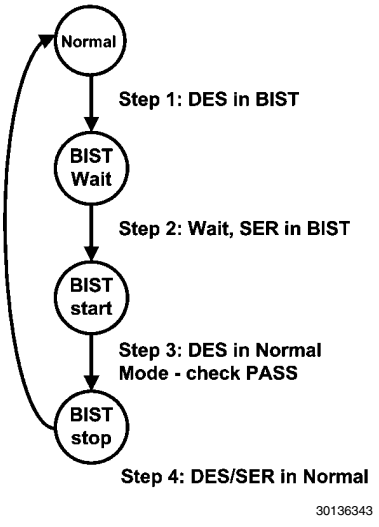


FIGURE 15. BIST Mode Flow Diagram

Forward Channel and Back Channel Error Checking

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While in BIST mode, the serializer stops sampling RGB input pins and switches over to an internal all-zero pattern. The internal all-zeroes pattern goes through scrambler, dc-balancing etc. and goes over the serial link to the deserializer. The deserializer on locking to the serial stream compares the recovered serial stream with all-zeroes and records any errors in status registers and dynamically indicates the status on PASS pin. The deserializer then outputs a SSO pattern on the RGB output pins.

The back-channel data is checked for CRC errors once the serializer locks onto back-channel serial stream as indicated by link detect status (register bit 0x0C[0]). The CRC errors are recorded in an 8-bit register. The register is cleared when the serializer enters the BIST mode. As soon as the serializer exits BIST mode, the functional mode CRC register starts recording the CRC errors. The BIST mode CRC error register is active in BIST mode only and keeps the record of last BIST run until cleared or enters BIST mode again.

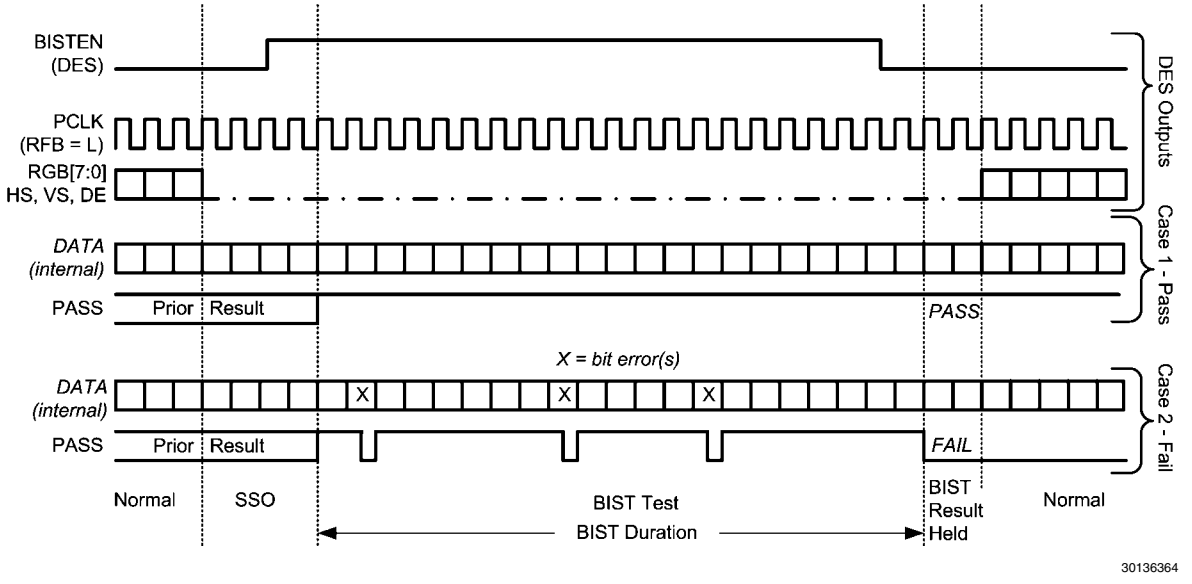


FIGURE 16. BIST Waveforms

Internal Pattern Generation

The DS90UH925Q serializer supports the internal pattern generation feature. It allows basic testing and debugging of an integrated panel through the FPD-Link III output stream. The test patterns are simple and repetitive and allow for a quick visual verification of panel operation. As long as the device is not in power down mode, the test pattern will be displayed even if no parallel input is applied. If no PCLK is received, the test pattern can be configured to use a programmed oscillator frequency. For detailed information, refer to Application Note *AN-2198*.

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Serial Control Bus

The DS90UH925Q is configured by the use of a serial control bus that is I2C protocol compatible. This bus is also used by the Host source to control and monitor status of the HDCP function. Multiple serializer devices may share the serial control bus since 16 device addresses are supported. Device address is set via R_1 and R_2 values on IDx pin. See *Figure 17* below.

The serial control bus consists of two signals and a configuration pin. The SCL is a Serial Bus Clock Input / Output. The SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pull-up resistor to V_{DD33}. For most applications a 4.7 k pull-up resistor to V_{DD33} may be used. The resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.

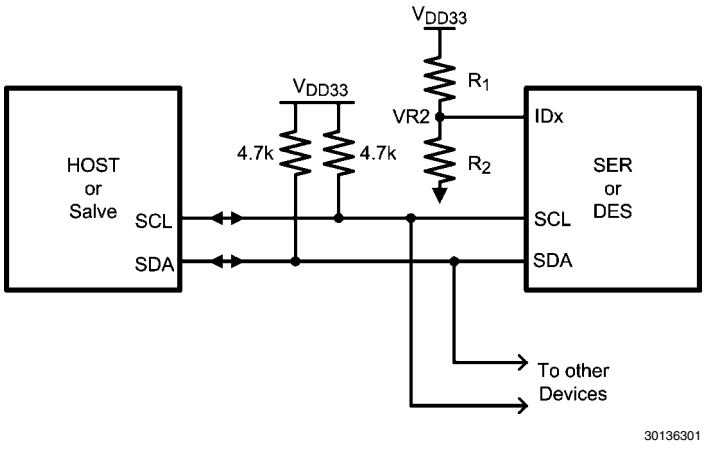


FIGURE 17. Serial Control Bus Connection

The configuration pin is the IDx pin. This pin sets one of 16 possible device addresses. A pull-up resistor and a pull-down resistor of suggested values may be used to set the voltage ratio of the IDx input (V_{R2}) and V_{DD33} to select one of the other 16 possible addresses. See *Table 6*.

TABLE 5. Serial Control Bus Addresses for IDx

#	Ideal Ratio V_{R2} / V_{DD33}	Ideal V_{R2} (V)	Suggested Resistor R1 kΩ (1% tol)	Suggested Resistor R2 kΩ (1% tol)	Address 7'b	Address 8'b Appended
1	0	0	Open	40.2 or Any	0x0C	0x18
2	0.121	0.399	294	40.2	0x0D	0x1A
3	0.152	0.502	280	49.9	0x0E	0x1C
4	0.182	0.601	270	60.4	0x0F	0x1E
5	0.212	0.700	267	71.5	0x10	0x20
6	0.242	0.799	240	76.8	0x11	0x22
7	0.273	0.901	243	90.9	0x12	0x24
8	0.310	1.023	226	102	0x13	0x26
9	0.356	1.175	210	115	0x14	0x28
10	0.402	1.327	196	130	0x15	0x2A
11	0.447	1.475	182	147	0x16	0x2C
12	0.492	1.624	169	165	0x17	0x2E
13	0.538	1.775	154	180	0x18	0x30
14	0.583	1.924	137	191	0x19	0x32
15	0.629	2.076	124	210	0x1A	0x34
16	0.727	2.399	90.9	243	0x1B	0x36

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The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transition High while SCL is also HIGH. See *Figure 18*.

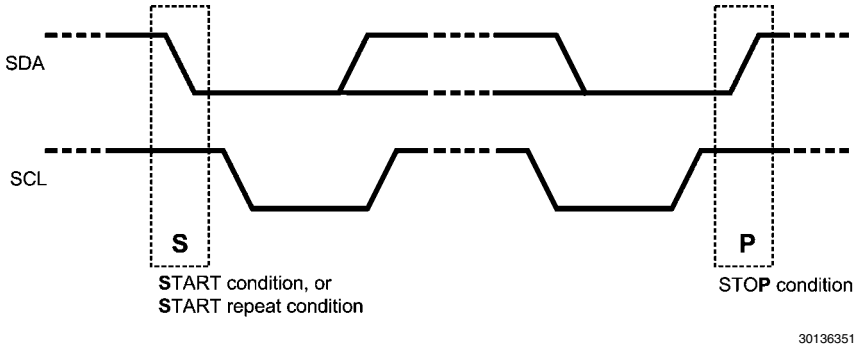


FIGURE 18. START and STOP Conditions

To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match a device's slave address, it Not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in *Figure 19* and a WRITE is shown in *Figure 20*.

If the Serial Bus is not required, the three pins may be left open (NC).

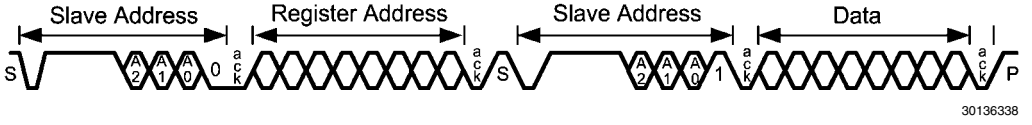


FIGURE 19. Serial Control Bus — READ

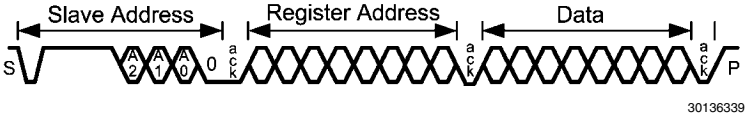


FIGURE 20. Serial Control Bus — WRITE

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TABLE 6. Serial Control Bus Registers

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
0	0x00	I2C Device ID	7:1	RW		Device ID	7–bit address of Serializer
			0	RW		ID Setting	I2C ID Setting 1: Register I2C Device ID (Overrides IDx pin) 0: Device ID is from IDx pin
1	0x01	Reset	7	RW	0x00	Remote Auto Power Down	Remote Auto Power Down 1: Power down when no Bidirectional Control Channel link is detected 0: Do not power down when no Bidirectional Control Channel link is detected
			6:2				***Reserved***.
			1	RW		Digital RESET1	Reset the entire digital block including registers This bit is self-clearing. 1: Reset 0: Normal operation
			0	RW		Digital RESET0	Reset the entire digital block except registers This bit is self-clearing 1: Reset 0: Normal operation
3	0x03	Configuration [0]	7	RW	0xD2	Back channel CRC Checker Enable	Back Channel Check Enable 1: Enable 0: Disable
			6				***Reserved***.
			5	RW		I2C Remote Write Auto Acknowledge	Automatically Acknowledge I2C Remote Write When enabled, I2C writes to the Deserializer (or any remote I2C Slave, if I2C PASS ALL is enabled) are immediately acknowledged without waiting for the Deserializer to acknowledge the write. This allows higher throughput on the I2C bus 1: Enable 0: Disable
			4	RW		Filter Enable	HS, VS, DE two clock filter When enabled, pulses less than two full PCLK cycles on the DE, HS, and VS inputs will be rejected 1: Filtering enable 0: Filtering disable
			3	RW		I2C Pass-through	I2C Pass-Through Mode 1: Pass-Through Enabled 0: Pass-Through Disabled
			2				***Reserved***
			1	RW		PCLK Auto	Switch over to internal OSC in the absence of PCLK 1: Enable auto-switch 0: Disable auto-switch
			0	RW		TRFB	Pixel Clock Edge Select 1: Parallel Interface Data is strobed on the Rising Clock Edge. 0: Parallel Interface Data is strobed on the Falling Clock Edge.

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ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
4	0x04	Configuration [1]	7	RW	0x80	Failsafe State	Input Failsafe State 1: Failsafe to Low 0: Failsafe to High
			6				***Reserved***
			5	RW		CRC Error Reset	Clear back channel CRC Error Counters This bit is NOT self-clearing 1: Clear Counters 0: Normal Operation
			4				***Reserved***
			3	RW		Backward Compatible select by pin or register control	Backward Compatible (BC) mode set by MODE_SEL pin or register 1: BC is set by register bit. Use register bit reg_0x04[2] to set BC Mode 0: BC is set by MODE_SEL pin.
			2	RW		Backward Compatible Mode Select	Backward compatible (BC) mode to DS90UR906Q or DS90UR908Q, if reg_0x04[3] = 1 1: Backward compatible with DS90UR906Q or DS90UR908Q 0: Backward Compatible is *OFF* (default)
			1	RW		LFMODE select by pin or register control	Frequency range is set by MODE_SEL pin or register 1: Frequency range is set by register. Use register bit reg_0x04[0] to set LFMODE 0: Frequency range is set by MODE_SEL pin.
			0	RW		LFMODE	Frequency range select 1: PCLK range = 5MHz - <15 MHz), if reg_0x04[1] = 1 0: PCLK range = 15MHz - 85MHz (default)

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ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
5	0x05	I2C Control	7:5		0x00		***Reserved***
			4:3	RW		SDA Output Delay	SDA output delay Configures output delay on the SDA output. Setting this value will increase output delay in units of 40ns. Nominal output delay values for SCL to SDA are 00: 240ns 01: 280ns 10: 320ns 11: 360ns
			2	RW		Local Write Disable	Disable remote writes to local registers Setting the bit to a 1 prevents remote writes to local device registers from across the control channel. It prevents writes to the Serializer registers from an I2C master attached to the Deserializer. Setting this bit does not affect remote access to I2C slaves at the Serializer
			1	RW		I2C Bus Timer Speedup	Speed up I2C bus watchdog timer 1: Watchdog timer expires after ~50 ms. 0: Watchdog Timer expires after ~1 s
			0	RW		I2C Bus timer Disable	Disable I2C bus watchdog timer When the I2C watchdog timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signalling occurs for ~1 s, the I2C bus assumes to be free. If SDA is low and no signaling occurs, the device attempts to clear the bus by driving 9 clocks on SCL
6	0x06	DES ID	7:1	RW	0x00	DES Device ID	7-bit Deserializer Device ID Configures the I2C Slave ID of the remote Deserializer. A value of 0 in this field disables I2C access to the remote Deserializer. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but should also assert the FREEZE DEVICE ID bit to prevent overwriting by the Bidirectional Control Channel.
			0	RW		Device ID Frozen	Freeze Deserializer Device ID Prevents autoloading of the Deserializer Device ID by the Bidirectional Control Channel. The ID will be frozen at the value written.
7	0x07	Slave ID	7:1	RW	0X00	Slave Device ID	7-bit Remote Slave Device ID Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Device Alias ID, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer
			0				***Reserved***

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ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
8	0x08	Slave Alias	7:1	RW	0x00	Slave Device Alias ID	7-bit Remote Slave Device Alias ID Assigns an Alias ID to an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID register. A value of 0 in this field disables access to the remote I2C Slave.
			0				***Reserved***
10	0x0A	CRC Errors	7:0	R	0x00	CRC Error LSB	Number of back channel CRC errors – 8 least significant bits
11	0x0B		7:0	R	0x00	CRC Error MSB	Number of back channel CRC errors – 8 most significant bits
12	0x0C	General Status	7:4		0x00		***Reserved***
			3	R		BIST CRC Error	Back channel CRC error during BIST communication with Deserializer. The bit is cleared upon loss of link, restart of BIST, or assertion of CRC ERROR RESET in register 0x04.
			2	R		PCLK Detect	PCLK Status 1: Valid PCLK detected 0: Valid PCLK not detected
			1	R		DES Error	Back channel CRC error during communication with Deserializer. The bit is cleared upon loss of link or assertion of CRC ERROR RESET in register 0x04.
			0	R		LINK Detect	LINK Status 1: Cable link detected 0: Cable link not detected (Fault Condition)
13	0x0D	Revision ID and GPIO0 Configuration	7:4	R	0xA0	Rev-ID	Revision ID: 1010 Production Device
			3	RW		GPIO0 Output Value	Local GPIO output value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
			2	RW		GPIO0 Remote Enable	Remote GPIO control 1: Enable GPIO control from remote Deserializer. The GPIO pin will be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Deserializer.
			1	RW		GPIO0 Direction	Local GPIO Direction 1: Input 0: Output
			0	RW		GPIO0 Enable	GPIO function enable 1: Enable GPIO operation 0: Enable normal operation

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ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
14	0x0E	GPIO2 and GPIO1 Configurations	7	RW	0x0	GPIO2 Output Value	Local GPIO output value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
			6	RW		GPIO2 Remote Enable	Remote GPIO control 1: Enable GPIO control from remote Deserializer. The GPIO pin will be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Deserializer.
			5	RW		GPIO2 Direction	Local GPIO Direction 1: Input 0: Output
			4	RW		GPIO2 Enable	GPIO function enable 1: Enable GPIO operation 0: Enable normal operation
			3	RW		GPIO1 Output Value	Local GPIO output value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
			2	RW		GPIO1 Remote Enable	Remote GPIO control 1: Enable GPIO control from remote Deserializer. The GPIO pin will be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Deserializer.
			1	RW		GPIO1 Direction	Local GPIO Direction 1: Input 0: Output
			0	RW		GPIO1 Enable	GPIO function enable 1: Enable GPIO operation 0: Enable normal operation
15	0x0F	GPO_REG4 and GPIO3 Configurations	7	RW	0x00	GPO_REG4 Output Value	Local GPO_REG4 output value This value is output on the GPO pin when the GPO function is enabled. (The local GPO direction is Output, and remote GPO control is disabled)
			6:5				***Reserved***
			4	RW		GPO_REG4 Enable	GPO_REG4 function enable 1: Enable GPO operation 0: Enable normal operation
			3	RW		GPIO3 Output Value	Local GPIO output value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
			2	RW		GPIO3 Remote Enable	Remote GPIO control 1: Enable GPIO control from remote Deserializer. The GPIO pin will be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Deserializer.
			1	RW		GPIO3 Direction	Local GPIO Direction 1: Input 0: Output
			0	RW		GPIO3 Enable	GPIO function enable 1: Enable GPIO operation 0: Enable normal operation

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ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
16	0x10	GPO_REG6 and GPO_REG5 Configurations	7	RW	0x00	GPO_REG6 Output Value	Local GPO_REG6 output value This value is output on the GPO pin when the GPO function is enabled. (The local GPO direction is Output, and remote GPO control is disabled)
			6:5				***Reserved***
			4	RW		GPO_REG6 Enable	GPO_REG6 function enable 1: Enable GPO operation 0: Enable normal operation
			3	RW		GPO_REG5 Output Value	Local GPO_REG5 output value This value is output on the GPO pin when the GPO function is enabled, the local GPO direction is Output, and remote GPO control is disabled.
			2:1				***Reserved***
			0	RW		GPO_REG5 Enable	GPO_REG5 function enable 1: Enable GPO operation 0: Enable normal operation
17	0x11	GPO_REG8 and GPO_REG7 Configurations	7	RW	0x00	GPO_REG8 Output Value	Local GPO_REG8 output value This value is output on the GPO pin when the GPO function is enabled. (The local GPO direction is Output, and remote GPO control is disabled)
			6:5				***Reserved***
			4	RW		GPO_REG8 Enable	GPO_REG8 function enable 1: Enable GPO operation 0: Enable normal operation
			3	RW		GPO_REG7 Output Value	Local GPO_REG7 output value This value is output on the GPO pin when the GPO function is enabled, the local GPO direction is Output, and remote GPO control is disabled.
			2:1				***Reserved***
			0	RW		GPO_REG7 Enable	GPO_REG7 function enable 1: Enable GPO operation 0: Enable normal operation

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ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
18	0x12	Data Path Control	7		0x00		***Reserved***
			6	RW		Pass RGB	Setting this bit causes RGB data to be sent independent of DE. It allows operation in systems which may not use DE to frame video data or send other data when DE is de-asserted. Note that setting this bit prevents HDCP operation and blocks packetized audio. This bit does not need to be set in Backwards Compatible mode 1: Pass RGB independent of DE 0: Normal operation (DE gates RGB data transmission - RGB data is transmitted only when DE is active)
			5	RW		DE Polarity	The bit indicates the polarity of the Data Enable (DE) signal. 1: DE is inverted (active low, idle high) 0: DE is positive (active high, idle low)
			4	RW		I2S Repeater Regeneration	I2S Repeater Regeneration 1: Repeater regenerate I2S from I2S pins 0: Repeater pass through I2S from video pins
			3	RW		I2S Channel B Enable Override	I2S Channel B Enable 1: Set I2S Channel B Enable from reg_0x12[0] 0: Set I2S Channel B Enable from MODE_SEL pin
			2	RW		18-bit Video Select	18–bit video select 1: Select 18-bit video mode Note: use of GPIO(s) on unused inputs must be enabled by register. 0: Select 24-bit video mode
			1	RW		I2S Transport Select	I2S Transport Mode Select 1: Enable I2S Data Forward Channel Frame Transport 0: Enable I2S Data Island Transport
			0	RW		I2S Channel B Enable	I2S Channel B Enable 1: Enable I2S Channel B on B1 input 0: I2S Channel B disabled
19	0x13	Mode Status	7:5		0x10		***Reserved***
			4	R		MODE_SEL	MODE_SEL Status 1: MODE_SEL decode circuit is completed 0: MODE_SEL decode circuit is not completed
			3	R		Low Frequency Mode	Low Frequency Mode Status 1: Low frequency (5 - <15 MHz) 0: Normal frequency (15 - 85 MHz)
			2	R		Repeater Mode	Repeater Mode Status 1: Repeater mode *ON* 0: Repeater Mode *OFF*
			1	R		Backward Compatible Mode	Backward Compatible Mode Status 1: Backward compatible *ON* 0: Backward compatible *OFF*
			0	R		I2S Channel B Mode	I2S Channel B Mode Status 1: I2S Channel B *ON*, 18-bit RGB mode with I2S_DB enabled 0: I2S Channel B *OFF*; normal 24-bit RGB mode

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ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
20	0x14	Oscillator Clock Source and BIST Status	7:3		0x00		***Reserved***
			2:1	RW		OSC Clock Source	OSC Clock Source (When LFMODE = 1, Oscillator = 12.5MHz ONLY) 00: External Pixel Clock 01: 33 MHz Oscillator 10: Reserved 11: 25 MHz Oscillator
			0	R		BIST Enable Status	BIST status 1: Enabled 0: Disabled
22	0x16	BCC Watchdog Control	7:1	RW	0xFE	Timer Value	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 ms. This field should not be set to 0
			0	RW		Timer Control	Disable Bidirectional Control Channel Watchdog Timer 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation
23	0x17	I2C Control	7	RW	0x5E	I2C Pass All	I2C Control 1: Enable Forward Control Channel pass-through of all I2C accesses to I2C Slave IDs that do not match the Serializer I2C Slave ID. 0: Enable Forward Control Channel pass-through only of I2C accesses to I2C Slave IDs matching either the remote Deserializer Slave ID or the remote Slave ID.
			6				***Reserved***
			5:4	RW		SDA Hold Time	Internal SDA Hold Time Configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 40 ns
			3:0	RW		I2C Filter Depth	Configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 ns
24	0x18	SCL High Time	7:0	RW	0xA1	SCL HIGH Time	I2C Master SCL High Time This field configures the high pulse width of the SCL output when the Serializer is the Master on the local I2C bus. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL high time with the internal oscillator clock running at 32.5MHz rather than the nominal 25MHz.
25	0x19	SCL Low Time	7:0	RW	0xA5	SCL LOW Time	I2C SCL Low Time This field configures the low pulse width of the SCL output when the Serializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL low time with the internal oscillator clock running at 32.5MHz rather than the nominal 25MHz.

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ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
27	0x1B	BIST BC Error	7:0	R	0x00	BIST Back Channel CRC Error Counter	BIST Mode Back Channel CRC Error Counter This error counter is active only in the BIST mode. It clears itself at the start of the BIST run.
100	0x64	Pattern Generator Control	7:4	RW	0x10	Pattern Generator Select	Fixed Pattern Select This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. The following table shows the color selections in non-inverted followed by inverted color mode 0000: Reserved 0001: White/Black 0010: Black/White 0011: Red/Cyan 0100: Green/Magenta 0101: Blue/Yellow 0110: Horizontally Scaled Black to White/White to Black 0111: Horizontally Scaled Black to Red/Cyan to White 1000: Horizontally Scaled Black to Green/ Magenta to White 1001: Horizontally Scaled Black to Blue/Yellow to White 1010: Vertically Scaled Black to White/White to Black 1011: Vertically Scaled Black to Red/Cyan to White 1100: Vertically Scaled Black to Green/Magenta to White 1101: Vertically Scaled Black to Blue/Yellow to White 1110: Custom color (or its inversion) configured in PGRS, PGGS, PGBS registers 1111: Reserved
			3:1				***Reserved***
			0	RW		Pattern Generator Enable	Pattern Generator Enable 1: Enable Pattern Generator 0: Disable Pattern Generator

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ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
101	0x65	Pattern Generator Configuration	7:5		0x00		***Reserved***
			4	RW		Pattern Generator 18 Bits	18-bit Mode Select 1: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 0: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness.
			3	RW		Pattern Generator External Clock	Select External Clock Source 1: Selects the external pixel clock when using internal timing. 0: Selects the internal divided clock when using internal timing This bit has no effect in external timing mode (PATGEN_TSEL = 0).
			2	RW		Pattern Generator Timing Select	Timing Select Control 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size. Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals.
			1	RW		Pattern Generator Color Invert	Enable Inverted Color Patterns 1: Invert the color output. 0: Do not invert the color output.
			0	RW		Pattern Generator Auto-Scroll Enable	Auto-Scroll Enable: 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. 0: The Pattern Generator retains the current pattern.
102	0x66	Pattern Generator Indirect Address	7:0	RW	0x00	Indirect Address	This 8-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register. See *AN-2198*
103	0x67	Pattern Generator Indirect Data	7:0	RW	0x00	Indirect Data	When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the read back value. See *AN-2198*
128	0x80	RX_BKSV0	7:0	R	0x00	RX BKSV0	BKSV0: Value of byte 0 of the Deserializer KSV
129	0x81	RX_BKSV1	7:0	R	0x00	RX BKSV1	BKSV1: Value of byte 1 of the Deserializer KSV
130	0x82	RX_BKSV2	7:0	R	0x00	RX BKSV2	BKSV2: Value of byte 2 of the Deserializer KSV
131	0x83	RX_BKSV3	7:0	R	0x00	RX BKSV3	BKSV3: Value of byte 3of the Deserializer KSV
132	0x84	RX_BKSV4	7:0	R	0x00	RX BKSV4	BKSV4: Value of byte 4of the Deserializer KSV
144	0x90	TX_KSV0	7:0	R	0x00	TX KSV0	KSV0: Value of byte 0 of the Serializer KSV
145	0x91	TX_KSV1	7:0	R	0x00	TX KSV1	KSV1: Value of byte 1 of the Serializer KSV
146	0x92	TX_KSV2	7:0	R	0x00	TX KSV2	KSV2: Value of byte 2 of the Serializer KSV

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ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
147	0x93	TX_KSV3	7:0	R	0x00	TX KSV3	KSV3: Value of byte 3 of the Serializer KSV
148	0x94	TX_KSV4	7:0	R	0x00	TX KSV4	KSV4: Value of byte 4 of the Serializer KSV
160	0xA0	RX BCAPS	7		0x13		***Reserved***
			6	R		Repeater	Indicates if the attached Receiver supports downstream connections. This bit is valid once the Bksv is ready as indicated by the BKSV_RDY bit in the HDCP
			5	R		KSV FIFO	KSV FIFO Ready Indicates the receiver has built the list of attached KSVs and computed the verification value
			4	R		Fast I2C	Fast I2C: The HDCP Receiver supports fast I2C. Since the I2C is embedded in the serial data, this bit is not relevant
			3:2				***Reserved***
			1	R		Features	HDCP v1.1_Features The HDCP Receiver supports the Enhanced Encryption Status Signaling (EESS), Advance Cipher, and Enhanced Link Verification options.
			0	R		Fast Re-auth	The HDCP Receiver is capable of receiving (unencrypted) video signal during the session re-authentication.
161	0xA1	RX BSTATUS0	7	R	0x00	Max Devices	Maximum Devices Exceeded: Indicates a topology error was detected. Indicates the number of downstream devices has exceeded the depth of the Repeater's KSV FIFO
			6:0	R		Device Count	Total number of attached downstream device. For a Repeater, this will indicate the number of downstream devices, not including the Repeater. For an HDCP Receiver that is not also a Repeater, this field will be 0
162	0xA2	RX BSTATUS1	7:4		0x00		***Reserved***
			3	R		Max Cascade	Maximum Cascade Exceeded: Indicates a topology error was detected. Indicates that more than seven levels of repeaters have been cascaded together
			2:0	R		Cascade Depth	Indicates the number of attached levels of devices for the Repeater
163	0xA3	KSV FIFO	7:0	R	0x00	KSV FIFO	KSV FIFO Each read of the KSV FIFO returns one byte of the KSV FIFO list composed by the downstream Receiver.

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ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
192	0xC0	HDCP DBG	7:4		0x00		***Reserved***
			3	RW		RGB CHKSUM	Enable RGB video line checksum Enables sending of ones-complement checksum for each 8-bit RBG data channel following end of each video data line
			2	RW		Fast LV	Fast Link Verification HDCP periodically verifies that the HDCP Receiver is correctly synchronized. Setting this bit will increase the rate at which synchronization is verified. When set to a 1, Pj is computed every 2 frames and Ri is computed every 16 frames. When set to a 0, Pj is computed every 16 frames and Ri is computed every 128 frames.
			1	RW		TMR Speed Up	Timer Speedup Speed up HDCP authentication timers.
			0	RW		HDCP I2C Fast	HDCP I2C Fast Mode Enable Setting this bit to a 1 will enable the HDCP I2C Master in the HDCP Receiver to operate with Fast mode timing. If set to a 0, the I2C Master will operate with Standard mode timing. This bit is mirrored in the IND_STS register

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ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
194	0xC2	HDCP CFG	7	RW	0x80	ENH LV	Enable Enhanced Link Verification Allows checking of the encryption Pj value on every 16th frame 1: Enhanced Link Verification enabled 0: Enhanced Link Verification disabled
			6	RW		HDCP EESS	Enables Enhanced Encryption Status Signaling (EESS) instead of the Original Encryption Status Signaling (OESS) 1: EESS mode enabled 0: OESS mode enabled
			5	RW		TX RPTR	Transmit Repeater Enable Enables the transmitter to act as a repeater. In this mode, the HDCP Transmitter incorporates the additional authentication steps required of an HDCP Repeater. 1: Transmit Repeater mode enabled 0: Transmit Repeater mode disabled
			4:3	RW		ENC Mode	Encryption Control Mode Determines mode for controlling whether encryption is required for video frames 00: Enc_Authenticated 01: Enc_Reg_Control 10: Enc_Always 11: Enc_InBand_Control (per frame) If the Repeater strap option is set at power-up, Enc_InBand_Control (ENC_MODE == 11) will be se-lected. Otherwise, the default will be Enc_Authenticated mode (ENC_MODE == 00).
			2	RW		Wait	Enable 100ms Wait The HDCP 1.3 specification allows for a 100ms wait to allow the HDCP Receiver to compute the initial encryption values. The FPD-Link III implementation guarantees that the Receiver will complete the computations before the HDCP Transmitter. Thus the timer is unnecessary. To enable the 100ms timer, set this bit to a 1.
			1	RW		RX DET SEL	RX Detect Select Controls assertion of the Receiver Detect Interrupt. If set to 0, the Receiver Detect Interrupt will be asserted on detection of an FPD-Link III Receiver. If set to 1, the Receiver Detect Interrupt will also require a receive lock indication from the receiver.
			0	RW		HDCP AV MUTE	Enable AVMUTE Setting this bit to a 1 will initiate AVMUTE operation. The transmitter will ignore encryption status controls while in this state. If this bit is set to a 0, normal operation resumes. This bit may only be set if the HDCP_EESS bit is also set.

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ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
195	0xC3	HDCP CTL	7	RW	0x00	HDCP RST	HDCP Reset Setting this bit will reset the HDCP transmitter and disable HDCP authentication. This bit is self-clearing.
			6				***Reserved***
			5	RW		KSV List Valid	The controller sets this bit after validating the Repeater's KSV List against the Key revocation list. This allows completion of the Authentication process. This bit is self-clearing
			4	RW		KSV Valid	The controller sets this bit after validating the Receiver's KSV against the Key revocation list. This allows continuation of the Authentication process. This bit will be cleared upon assertion of the KSV_RDY flag in the HDCP_STS register. Setting this bit to a 0 will have no effect
			3	RW		HDCP ENC DIS	HDCP Encrypt Disable Disables HDCP encryption. Setting this bit to a 1 will cause video data to be sent without encryption. Authentication status will be maintained. This bit is self-clearing
			2	RW		HDCP ENC EN	HDCP Encrypt Enable Enables HDCP encryption. When set, if the device is authenticated, encrypted data will be sent. If device is not authenticated, a blue screen will be sent. Encryption should always be enabled when video data requiring content protection is being supplied to the transmitter. When this bit is not set, video data will be sent without encryption. Note that when CFG_ENC_MODE is set to Enc_Always, this bit will be read only with a value of 1
			1	RW		HDCP DIS	HDCP Disable Disables HDCP authentication. Setting this bit to a 1 will disable the HDCP authentication. This bit is self-clearing
			0	RW		HDCP EN	HDCP Enable/Restart Enables HDCP authentication. If HDCP is already enabled, setting this bit to a 1 will restart authentication. Setting this bit to a 0 will have no effect. A register read will return the current HDCP enabled status

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ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
196	0xC4	HDCP STS	7	R	0x00	I2C ERR DET	HDCP I2C Error Detected This bit indicates an error was detected on the embedded communications channel with the HDCP Receiver. Setting of this bit might indicate that a problem exists on the link between the HDCP Transmitter and HDCP Receiver. This bit will be cleared on read
			6	R		RX INT	RX Interrupt Status of the RX Interrupt signal. The signal is received from the attached HDCP Receiver and is the status on the INTB_IN pin of the HDCP Receiver. The signal is active low, a 0 indicates an interrupt condition
			5	R		RX Lock DET	Receiver Lock Detect This bit indicates that the downstream Receiver has indicated Receive Lock to incoming serial data
			4	R		DOWN HPD	Hot Plug Detect This bit indicates the local device or a downstream repeater has reported a Hot Plug event, indicating addition of a new receiver. This bit will be cleared on read
			3	R		RX DET	Receiver Detect This bit indicates that a downstream Receiver has been detected
			2	R		KSV LIST RDY	HDCP Repeater KSV List Ready This bit indicates that the Receiver KSV list has been read and is available in the KSV_FIFO registers. The device will wait for the controller to set the KSV_LIST_VALID bit in the HDCP_CTL register before continuing. This bit will be cleared once the controller sets the KSV_LIST_VALID bit.
			1	R		KSV RDY	HDCP Receiver KSV Ready This bit indicates that the Receiver KSV has been read and is available in the HDCP_ BKSV registers. If the device is not a Repeater, it will wait for the controller to set the KSV_VALID bit in the HDCP_CTL register before continuing. This bit will be cleared once the controller sets the KSV_VALID bit.. The bit will also be cleared if authentication fails.
			0	R		AUTHED	HDCP Authenticated Indicates the HDCP authentication has completed successfully. The controller may now send video data requiring content protection. This bit will be cleared if authentication is lost or if the controller restarts authentication

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ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
198	0xC6	HDCP ICR	7	RW	0x00	IE IND ACC	Interrupt on Indirect Access Complete Enables interrupt on completion of Indirect Register Access
			6	RW		IE RXDET INT	Interrupt on Receiver Detect Enables interrupt on detection of a downstream Receiver. If HDCP_CFG:RX_DET_SEL is set to a 1, the interrupt will wait for Receiver Lock Detect.
			5	RW		IS_RX_INT	Interrupt on Receiver interrupt Enables interrupt on indication from the HDCP Receiver. Allows propagation of interrupts from downstream devices
			4	RW		IE LIST RDY	Interrupt on KSV List Ready Enables interrupt on KSV List Ready
			3	RW		IE KSV RDY	Interrupt on KSV Ready Enables interrupt on KSV Ready
			2	RW		IE AUTH FAIL	Interrupt on Authentication Failure Enables interrupt on authentication failure or loss of authentication
			1	RW		IE AUTH PASS	Interrupt on Authentication Pass Enables interrupt on successful completion of authentication
			0	RW		INT Enable	Global Interrupt Enable Enables interrupt on the interrupt signal to the controller.
199	0xC7	HDCP ISR	7	R	0x00	IS IND ACC	Interrupt on Indirect Access Complete Indirect Register Access has completed
			6	R		INT Detect	Interrupt on Receiver Detect interrupt A downstream receiver has been detected
			5	R		IS RX INT	Interrupt on Receiver interrupt Receiver has indicated an interrupt request from down-stream device
			4	R		IS LIST RDY	Interrupt on KSV List Ready The KSV list is ready for reading by the controller
			3	R		IS KSV RDY	Interrupt on KSV Ready The Receiver KSV is ready for reading by the controller
			2	R		IS AUTH FAIL	Interrupt on Authentication Failure Authentication failure or loss of authentication has occurred
			1	R		IS AUTH PASS	Interrupt on Authentication Pass Authentication has completed successfully
			0	R		INT	Global Interrupt Set if any enabled interrupt is indicated
240	0xF0	HDCP TX ID	7:0	R	0x5F	ID0	First byte ID code, '_'
241	0xF1		7:0	R	0x55	ID1	Second byte of ID code, 'U'
242	0xF2		7:0	R	0x48	ID2	Third byte of ID code. Value will be either 'B' or 'H'. 'H' indicates an HDCP capable device
243	0xF3		7:0	R	0x39	ID3	Forth byte of ID code: '9'
244	0xF4		7:0	R	0x32	ID4	Fifth byte of ID code: '2'
245	0xF5		7:0	R	0x35	ID5	Sixth byte of ID code: '5'

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Applications Information

DISPLAY APPLICATION

The DS90UH925Q, in conjunction with the DS90UH926Q, is intended for interface between a HDCP compliant host (graphics processor) and a Display. It supports a 24-bit color depth (RGB888) and high definition (720p) digital video format. It can receive a three 8-bit RGB stream with a pixel rate up to 85 MHz together with three control bits (VS, HS and DE) and three I2S-bus audio stream with an audio sampling rate up to 192 kHz. The included HDCP 1.3 compliant cipher block allows the authentication of the DS90UH926Q, which decrypts both video and audio contents. The keys are pre-loaded by TI into Non-Volatile Memory (NVM) for maximum security.

TYPICAL APPLICATION CONNECTION

Figure 21 shows a typical application of the DS90UH925Q serializer for an 85 MHz 24-bit Color Display Application. The CML outputs must have an external 0.1 µF AC coupling capacitor on the high speed serial lines. The serializer has an internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, six (6) 4.7µF capacitors (and two (2) additional 1µF capacitors should be used for local device bypassing. Ferrite beads are placed on the two (2) VDDs (V_{DD33} and V_{DDIO}) for effective noise suppression. The interface to the graphics source is with 3.3V LVCMOS levels, thus the V_{DDIO} pin is connected to the 3.3 V rail. A RC delay is placed on the PDB signal to delay the enabling of the device until power is stable.

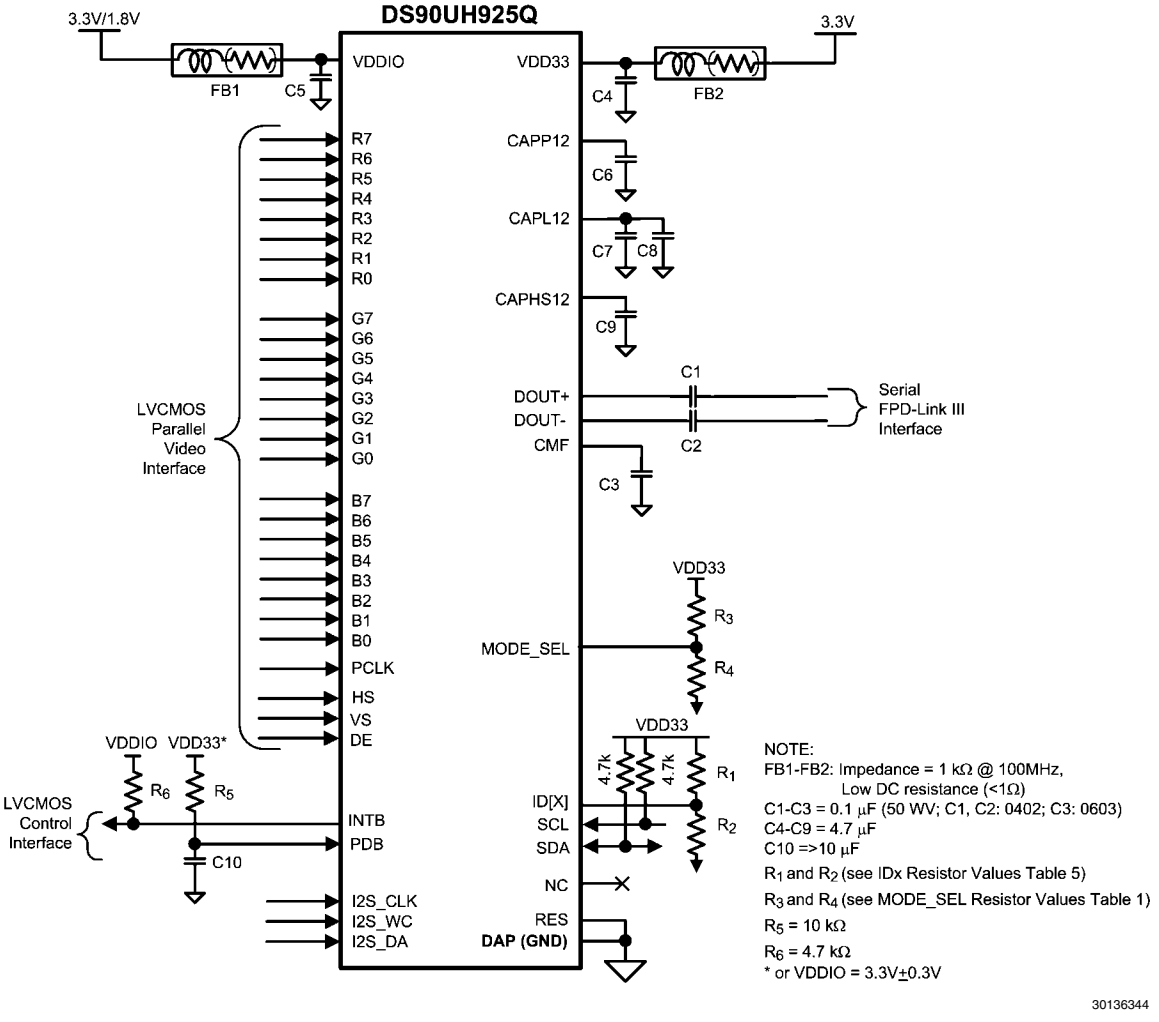


FIGURE 21. Typical Connection Diagram

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POWER UP REQUIREMENTS AND PDB PIN

The VDDs (V_{DD33} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise. A large capacitor on the PDB pin is needed to ensure PDB arrives after all the VDDs have settled to the recommended operating voltage. When PDB pin is pulled to V_{DDIO} = 3.0V to 3.6V or V_{DD33}, it is recommended to use a 10 kΩ pull-up and a >10 uF cap to GND to delay the PDB input signal. All inputs must not be driven until V_{DD33} and V_{DDIO} has reached its steady state value.

PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the FPD-Link III devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the CML lines to prevent coupling from the LVCMOS lines to the CML lines. Closely-coupled differential lines of 100 Ohms are typically recommended for CML interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the LLP style package is provided in TI Application Note: AN-1187.

CML INTERCONNECT GUIDELINES

See AN-1108 and AN-905 for full details.

- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500 Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the TI web site at: **www.ti.com/lvds**

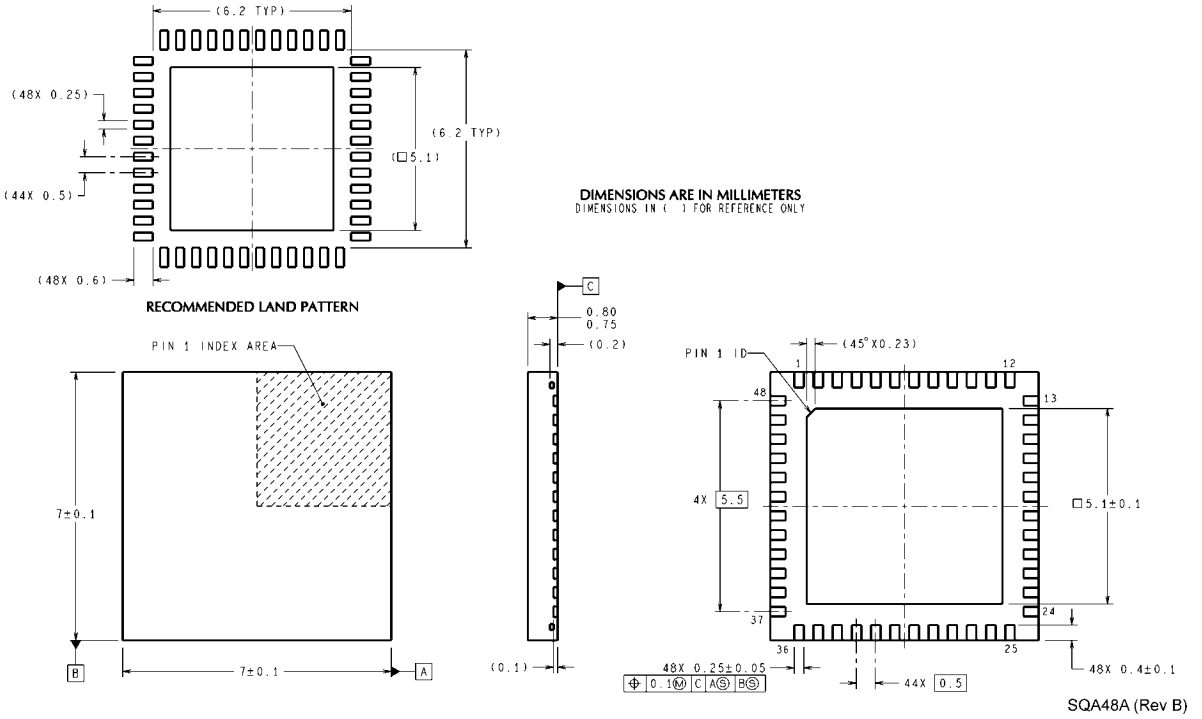
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Revision

- **March 7, 2012**
  - Corrected under “Recommended Operating Conditions” from RxCLKIN Frequency to PCLK Frequency
  - Added under “AC Electrical Characteristics: min. limit t_{IJIT} = 0.4UI at 78MHz
  - Deleted under “DC Electrical Characteristics” PDB VDDIO = 1.71 to 1.89V
  - Deleted under “DC Electrical Characteristics “V_{OS} Min and Max limits”
  - Added “INTERRUPT PIN — FUNCTIONAL DESCRIPTION AND USAGE (INTB)” under Functional Description section
  - Updated "POWER DOWN (PDB)” description under Functional Description from VDDIO to VDDIO = 3.0 to 3.6V or V_{DD33}
  - Updated “FIGURE 21. Typical Connection Diagram”
- **Aug 6, 2012**
  - Converted to hybrid TI format
  - Corrected typo in Pin Descriptions SCL Pin # from 6 to 8
  - Corrected typo in Pin Descriptions SDA Pin # from 7 to 9
  - Corrected typo in TABLE 1: Configuration Select (MODE_SEL) #6 I2S Channel B (18–bit Mode) from L to H
  - Corrected typo in TABLE 5. Serial Control Bus Addresses for IDx #11 Ideal V_{R2}(V) from 2.475 to 1.475
  - Added “Note: BIST is not available in backwards compatible mode.”
  - Corrected typo in table “DC and AC Serial Control Bus Characteristics” from VDDIO to VDD33
  - Added” Note: frequency range = 15 - 65MHz when LFMODE = 0 and frequency range = 5 - <15MHz when LFMODE = 1.” under Functional Description. Reformatted TABLE 1 and added clarification to notes. Added clarification to notes on TABLE 6 Serial Control Bus Registers, address 0x04[3:0] (backwards compatible and LFMODE registers).

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Physical Dimensions inches (millimeters) unless otherwise noted



48–pin LLP Package (7.0 mm X 7.0 mm X 0.8 mm, 0.5 mm pitch)
NS Package Number SQA48A

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Notes

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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