Data Sheet
June 2000

microelectronics group

Lucent Technologies
Bell Labs Innovations

TTSI4K32T
4096-Channel, 32-Highway Time-Slot Interchanger

Features

- Thirty-two full-duplex, serial time-division multiplexed (TDM) highways.
- Full availability, nonblocking 4096-channel time/space switch.
- 2.048 Mbits/s (32 time slots), 4.096 Mbits/s (64 time slots), or 8.192 Mbits/s (128 time slots) data rates, independently programmable per highway.
- 64 kbits/s granularity with optional 32 kbits/s (4-bit) and 16 kbits/s (2-bit) subrate switching, selectable per highway.
- Low-latency mode for voice channels.
- Frame integrity for wideband data applications.
- Concentration highway interface (CHI) compatible with the IOM2, GCI, K2, SLD, *MVIP**, ST-Bus, SC-Bus, and H.100.
- Single highway clock and frame synchronization input.
- Independently programmable bit and byte offsets with 1/4 bit resolution for all highways.
- Capable of broadcasting data to the transmit highways from a variety of sources including host data.
- High-impedance control per time slot.
- Software-compatible family of 1K, 2K, and 4K time-slot interchangers.
- Thirty-two independent high-impedance indicators (output enables) for transmit highways, allowing external drivers.
- Direct access to device registers, connection store, and data store via microprocessor interface.
- *IEEE*† 1149.1 boundary scan (JTAG).
- Test-pattern generation and checking for on-line system testing (PRBS, QRSS, or user-defined byte).
- User-accessible BIST for data and connection stores.
- 3.3 V power supply with 5 V tolerant I/O.
- Low-power, high-density CMOS technology, and TTL compatible switching thresholds.
- 217-pin PBGA package.
- –40 °C to +85 °C operating temperature range.

* *MVIP* is a registered trademark of Natural Microsystems Corporation.

† *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Applications

- Small and medium digital switch matrices.
- Computer telephony integration (CTI).
- Access concentrators.
- PABX.
- Cellular infrastructure.
- ISP modem banks.
- T1/E1 multiplexers.
- Digital cross connects.
- Digital loop carriers.
- Multiport DS1/E1 service cards.
- LAN/WAN gateways.
- TDM highway data rate adaptation.

Description

The TTSI4K32T Time-Slot Interchanger (TSI) switches data between 32 full-duplex, serial, time-division multiplexed highways. The TTSI4K32T can make any connection between 4096 input and output time slots.

Each of the 32 transmit and 32 receive highways can be independently programmed for data rate (2.048 Mbits/s, 4.096 Mbits/s, or 8.192 Mbits/s) and offset. The offset can range from 0 bits to 127 bytes and 7 3/4 bits on a 8.192 Mbits/s highway. The TTSI4K32T can perform rate adaptation between varying speed highways as well.

The TTSI4K32T is configured via a microprocessor interface with a demultiplexed address and data bus. In addition to accessing the registers and connection store, this interface can also be used to read received time slots and specify user data for transmission.

The TTSI4K32T ensures that interchanged time slots retain their frame integrity. Frame integrity is required for applications that switch wideband data (i.e., ISDN H-channels). For voice applications where low delay is important, a low-latency mode can be selected.

Table of Contents

Contents **Page**

Features 1
Applications 1
Description 1
Functional Description 5
Pin Information 7
Typical TSI Application 15
Interchange Fabric 16
Small and Large TSIs 17
Microprocessor Interface 18
  Asynchronous Mode (MM = 0) 18
  Synchronous Mode (MM = 1) 19
Mixed-Highway Data Rates 20
TDM Highway Interface Timing 21
  Virtual and Physical Frames 21
  TDM Highway Alignment at Zero Offset 22
TDM Highway Offsets 22
Reset Sequence 23
Low-Latency and Frame-Integrity Modes 24
  Low Latency 24
  Frame Integrity 25
Test-Pattern Generation 28
Test-Pattern Checking 28
Error Injection 29
Error Checking 29
JTAG Boundary-Scan Specification 30
  Principle of the Boundary Scan 30
  Test Access Port Controller 31
  Instruction Register 33
  Boundary-Scan Register 34
  BYPASS Register 34
  IDCODE Register 34
  3-State Procedures 34
Register Architecture 35
Configuration Register Architecture 37
  Transmit Highway 3-State Options 50
Data Store Memory 51
Connection Store Memory 51
Absolute Maximum Ratings 54
Operating Conditions 54
Handling Precautions 54
Electrical Characteristics 55
Timing Characteristics 55
Outline Diagram 62
  217-Pin PBGA 62
Ordering Information 63
DS99-178PDH Replaces DS98-291TIC to Incorporate the Following Updates 63

List of Figures

Figures **Page**

Figure 1. Block Diagram of the TTSI4K32T 6
Figure 2. 217-Pin PBGA (Bottom View) 7
Figure 3. A Typical TSI Application 15
Figure 4. An 8K Time-Slot Switch Made from 4K TSIs 17
Figure 5. Asynchronous Read 18
Figure 6. Asynchronous Write 18
Figure 7. Synchronous Read 19
Figure 8. Synchronous Write 19
Figure 9. Mixed-Highway Data Rates 20
Figure 10. Virtual and Physical Frames 21
Figure 11. Synchronization to FSYNC 22
Figure 12. Highway Offsets 23
Figure 13. Mixed Low-Latency and Frame-Integrity Modes 27
Figure 14. Block Diagram of the TTSI4K32T's Boundary-Scan Test Logic 30
Figure 15. BS TAP Controller State Diagram 31
Figure 16. Asynchronous Read Cycle Timing Using $\overline{DT}$ Handshake 56
Figure 17. Asynchronous Write Cycle Timing Using $\overline{DT}$ Handshake 56
Figure 18. Asynchronous Read Cycle Timing Using Only $\overline{CS}$ 57
Figure 19. Asynchronous Write Cycle Timing Using Only $\overline{CS}$ 57
Figure 20. Synchronous Read Cycle Timing 58
Figure 21. Synchronous Write Cycle Timing 58
Figure 22. TDM Highway Timing 60
Figure 23. JTAG Interface Timing 61

List of Tables

Tables **Page**

Table 1. Data Rate and Switch Size Examples 5
Table 2. Pin Assignments for a 217-Pin PBGA—Pin Number Order 8
Table 3. Pin Assignments for a 217-Pin PBGA—Signal Name Order 10
Table 4. TTSI4K32T Pin Descriptions 12
Table 5. The TSI Family 17
Table 6. Time-Slot Separation Required for Transmission with Minimum Latency (0 Offsets) 24
Table 7. Offset Difference and Its Effect on Frame for Transmission 26
Table 8. Offset Difference Boundaries 26
Table 9. TAP Controller States in the Data Register Branch 32
Table 10. TAP Controller States in the Instruction Register Branch 32
Table 11. TTSI2K32T's Boundary-Scan Instructions 33
Table 12. TTSI4K32T Register Summary 35
Table 13. General Command Register (0x00) 37
Table 14. Software Reset Register (0x01) 38
Table 15. BIST Command Register (0x02) 38
Table 16. Idle Code 1 Register (0x03) 39
Table 17. Idle Code 2 Register (0x04) 39
Table 18. Idle Code 3 Register (0x05) 39
Table 19. Global Interrupt Mask Register (0x06) 39
Table 20. Interrupt Status Register (0x07) 40
Table 21. Interrupt Mask Register (0x08) 41
Table 22. Test Command Register (0x09) 42
Table 23. Test-Pattern Style Register (0x0A) 43
Table 24. Test-Pattern Checker Highway Register (0x0B) 44
Table 25. Test-Pattern Checker Upper Time-Slot Register (0x0C) 44
Table 26. Test-Pattern Checker Lower Time-Slot Register (0x0D) 44
Table 27. Test-Pattern Checker Data Register (0x0E) 44
Table 28. Test-Pattern Error Injection Register (0x0F) 44
Table 29. Test-Pattern Error Counter (Byte 0) (0x10) 45
Table 30. Test-Pattern Error Counter (Byte 1) (0x11) 45
Table 31. Test-Pattern Generator Data Register (0x12) 45
Table 32. Version Register (0x13) 45
Table 33. Transmit Highway Configuration Register (Byte 0) (0x1000 + 4i) 46
Table 34. Transmit Highway Configuration Register (Byte 1) (0x1001 + 4i) 47
Table 35. Transmit Highway Configuration Register (Byte 2) (0x1002 + 4i) 47
Table 36. Receive Highway Configuration Register (Byte 0) (0x1800 + 4i) 48
Table 37. Receive Highway Configuration Register (Byte 1) (0x1801 + 4i) 49
Table 38. Receive Highway Configuration Register (Byte 2) (0x1802 + 4i) 49
Table 39. Transmit Highway 3-State Options 50
Table 40. Address Scheme for Data Store Memory 51
Table 41. Address Scheme for Connection Store Memory 51
Table 42. Connection Store Memory (Byte 0) 52
Table 43. Connection Store Memory (Byte 1) 52
Table 44. Clock Specifications 55
Table 45. Asynchronous Read and Write Interface Timing Using $\overline{DT}$ Handshake 56
Table 46. Asynchronous Microprocessor Interface Timing Using Only $\overline{CS}$ 57
Table 47. Synchronous Microprocessor Interface Timing 59
Table 48. TDM Highway Timing 60
Table 49. JTAG Interface Timing 61

Functional Description

The TTSI4K32T is a 4096 time-slot switch that can be used in a variety of ways, with some or all of the highways active and running at different data rates. The table below lists a few of the possible combinations of switch size and data rates. By selecting different rates for receive and transmit highways, rate adaptation can be performed also. Each one of the 64 (32 transmit and 32 receive) highways can be independently programmed for data rate (2.048 Mbits/s, 4.096 Mbits/s, or 8.192 Mbits/s) as well as a full range of bit (0—7.75) and byte (0—127) offsets.

Table 1. Data Rate and Switch Size Examples

Number of Receive Highways Used	Receive Highway Data Rates (Mbits/s)	Receive Time Slots per Frame	Total Switch Size	Number of Transmit Highways Used	Transmit Highway Data Rates (Mbits/s)	Transmit Time Slots per Frame
32	8.192	128	4096	32	8.192	128
16	8.192	128	2048	32	4.096	64
32	2.048	32	1024	8	8.192	128
16 and 16	4.096 8.192	64 128	3072	12 and 18	4.096 8.192	64 128

This device uses a single clock (CK) and frame synchronization (FSYNC) signal for all highways. The CK rate can be 2.048 MHz, 4.096 MHz, 8.192 MHz, or 16.384 MHz, and this speed is indicated to the device via the CKSPD [0—2] strap pins. A pulse is expected on the FSYNC pin once every 125 µs.

Each one of the 4096 time slots can be independently programmed in any one of the data modes listed below:

- Low latency
- Frame integrity
- Host data substitution
- Idle code substitution
- Test-pattern substitution (PRBS, QRSS, or a fixed byte)
- High impedance

The low-latency mode causes a receive highway time slot to be transmitted as soon as possible, which is dependent on the relative offset of the input and output time slots. This mode is useful for voice channels where it is important to keep the transmission delay to a minimum.

The frame integrity mode will guarantee that all selected time slots received in a common frame will be transmitted together in a common frame. This mode is useful for wideband data (e.g., ISDN H-channels) where multiple time slots received in a single frame cannot be split across two transmit frames.

The TTSI4K32T is a nonblocking DS0 (64 kbits/s channel) switch where a time slot is 8 bits. Since each Rx and Tx highway data rate can be individually selected, the TTSI4K32T can also be used to switch time slots that are smaller than 8 bits.

- 32 kbits/s channels (4-bit time slots) such as in compressed voice (ADPCM) applications. The TTSI4K32T will be configured to sample the data at twice the data rate for highways carrying traffic at 2.048 Mbits/s or 4.096 Mbits/s.
- 16 kbits/s channels (2-bit time slots) such as in cellular (GSM) applications. The TTSI4K32T will be set to sample the data at four times the data rate on a 2.048 Mbits/s highway carrying such traffic.
- 8 kbits/s channels (1-bit time slots) such as in half-rate GSM applications. This can be done by looping the data through the TSI multiple times, thus oversampling the same data multiple times. However, in this configuration, the total switching capacity of the device will drop and the latency will go up.

The TTSI4K32T is one in a family of 1K, 2K, and 4K TSIs. The high-impedance control per time-slot feature allows four of the 4K devices to be connected to make an 8K time-slot switch.

If external drivers are needed on the transmit highway pins, support for 32 output enables, corresponding to the 32 transmit highways, is provided.

Functional Description (continued)

The device capabilities include several test features for board and device diagnostics.

- Test-pattern checking on input time slots (PRBS, QRSS, or a fixed byte).
- Test-pattern generation on output time slots (PRBS, QRSS, or a fixed byte).
- JTAG on all I/O.
- Software-controlled BIST of data store and connection store memory.
- $\overline{\text{TEST}}$ pin for isolating the TTSI4K32T during board test.

The microprocessor interface supports two modes of operation, synchronous and asynchronous. These modes are selected based on the MM input pin. Both modes provide an 8-bit demultiplexed address and data bus. Fifteen address pins allow direct access to the 32 Kbyte address space. This interface provides direct access to the control registers and data store and connection store memories.

The TTSI4K32T is fabricated using a low-power, high-density, CMOS process that nominally operates at 3.3 V with TTL switching thresholds and 5 V tolerance on the inputs and outputs. A basic block diagram of the architecture is shown in Figure 1.

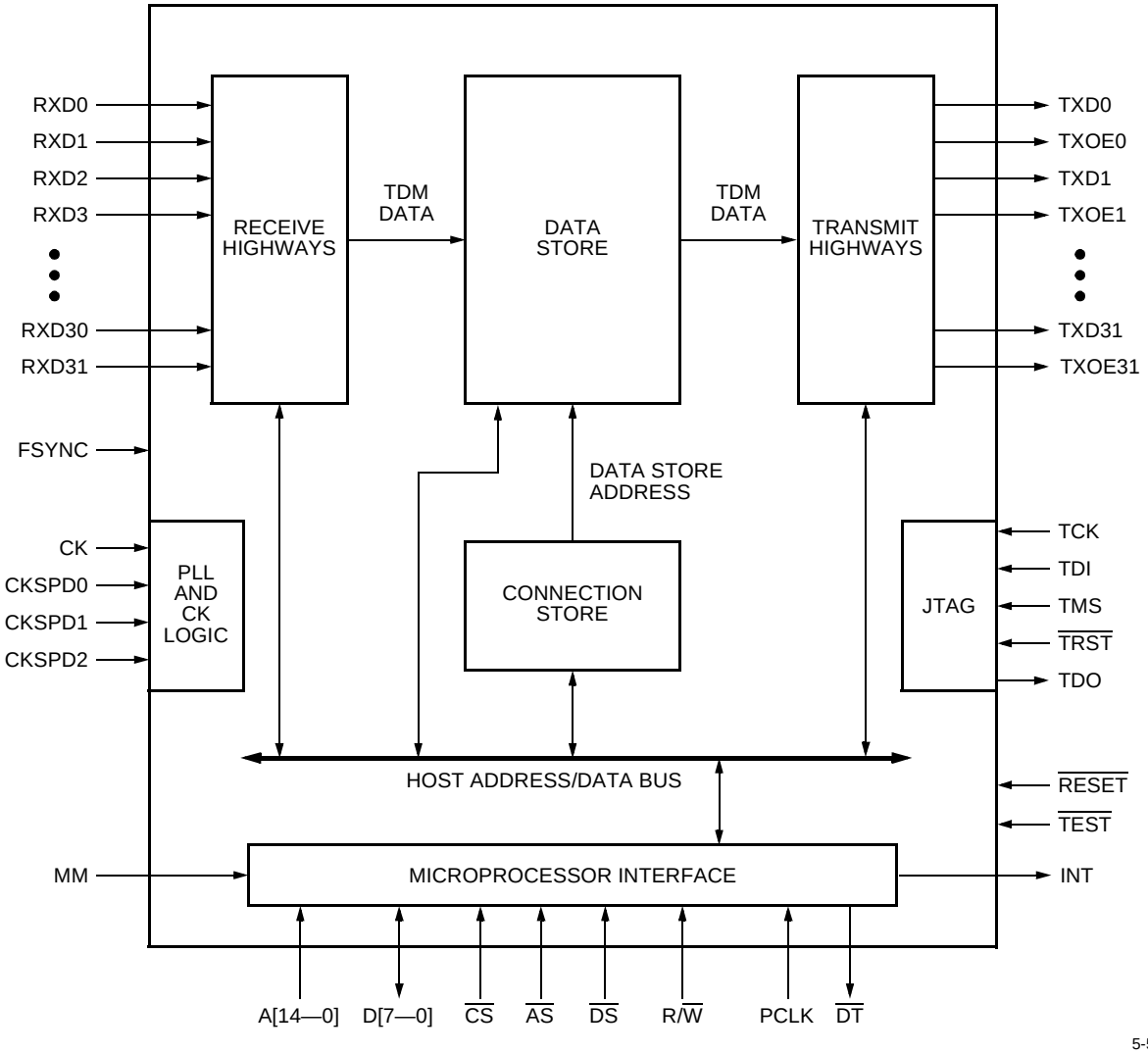
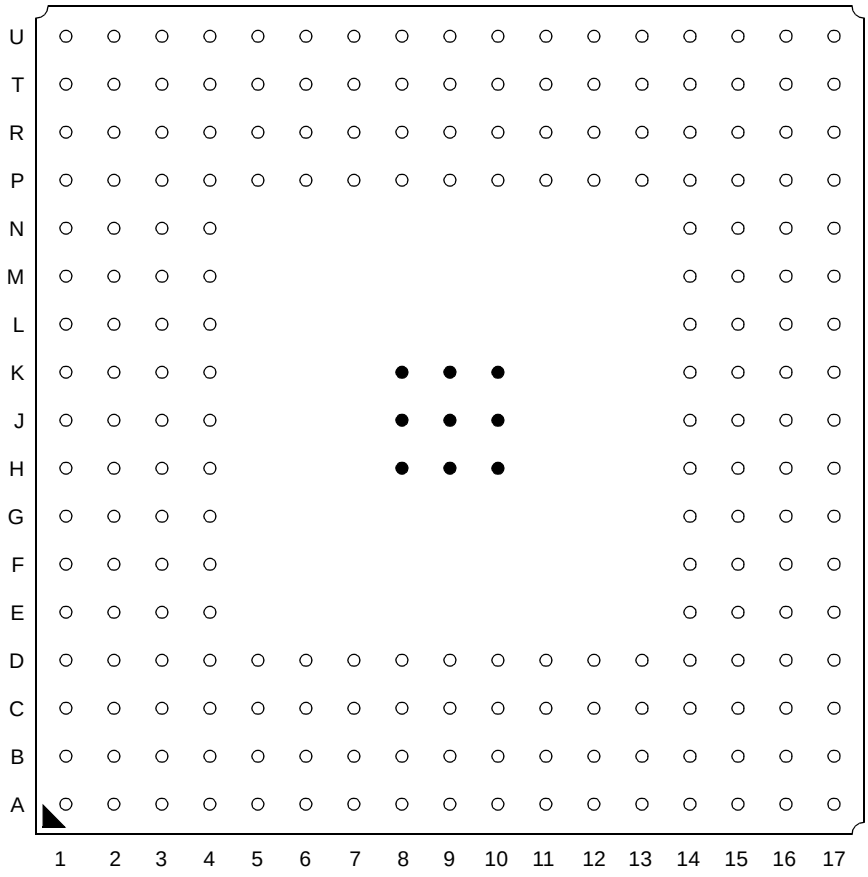


Figure 1. Block Diagram of the TTSI4K32T

Pin Information

The TTSI4K32T is available in a 217-pin PBGA with 1.27 mm (50 mil) pin pitch.



5-6953(F)

○ SIGNAL/PWR/GND

● THERMAL BALLS
(SHOULD BE CONNECTED TO
CIRCUIT BOARD'S GROUND PLAN)

Figure 2. 217-Pin PBGA (Bottom View)

Pin Information (continued)

Table 2. Pin Assignments for a 217-Pin PBGA—Pin Number Order

Pin	Signal Name
A1	NC
A2	NC
A3	NC
A4	TXOE1
A5	TXD18
A6	TXD2
A7	VDD
A8	NC
A9	VDDPLL
A10	CKSPD0
A11	CKSPD2
A12	TXD3
A13	NC
A14	TXOE22
A15	TXD21
A16	NC
A17	VSS
B1	RXD25
B2	VSS
B3	TXOE0
B4	NC
B5	TXD1
B6	TXOE2
B7	NC
B8	VSSPLL
B9	CK
B10	CKSPD1
B11	VDD
B12	NC
B13	TXD4
B14	TXOE21
B15	NC
B16	VSS
B17	$\overline{\text{RESET}}$
C1	VDD
C2	RXD24
C3	VSS
C4	TXD0
C5	TXD15
C6	TXOE18
C7	TXOE19
C8	TXD19
C9	NC
C10	TXOE3
C11	TXD20
C12	TXOE4
C13	TXD22
C14	TXD23
C15	VSS
C16	$\overline{\text{TEST}}$
C17	TCK
D1	RXD6
D2	RXD7
D3	RXD23
D4	VSS
D5	TXOE15
D6	VDD
D7	NC
D8	VDD
D9	VSS
D10	VDD
D11	TXOE20
D12	VDD
D13	TXOE23
D14	VSS
D15	TDI
D16	TMS
D17	$\overline{\text{TRST}}$
E1	RXD12
E2	RXD21
E3	RXD13
E4	RXD14
E14	TDO
E15	VDD
E16	TXOE16
E17	TXOE17
F1	RXD4
F2	VDD
F3	RXD20
F4	RXD22
F14	NC
F15	TXD16
F16	NC
F17	TXD17
G1	RXD3
G2	VDD
G3	RXD5
G4	RXD19
G14	TXD26
G15	TXOE26
G16	TXOE24
G17	TXD24
H1	VDD
H2	RXD2
H3	NC
H4	VDD
H8	VSS
H9	VSS
H10	VSS
H14	VDD
H15	FSYNC
H16	VDD
H17	TXOE5
J1	RXD0
J2	RXD1
J3	A7
J4	VSS
J8	VSS
J9	VSS
J10	VSS
J14	VSS
J15	TXD5
J16	TXD8
J17	TXOE8
K1	RXD11
K2	RXD10
K3	RXD18
K4	VDD
K8	VSS
K9	VSS
K10	VSS
K14	VDD
K15	NC
K16	TXD9
K17	TXOE9
L1	RXD17
L2	VDD
L3	RXD16
L4	RXD9
L14	TXOE6
L15	VDD
L16	NC
L17	TXOE10
M1	RXD8
M2	A8
M3	A10
M4	VDD
M14	TXOE25
M15	VSS
M16	VSS
M17	TXD10
N1	A9
N2	A11
N3	A13
N4	NC
N14	TXOE11
N15	INT
N16	TXOE7
N17	TXD6
P1	A12
P2	A14
P3	RXD26

Pin Information (continued)

Table 2. Pin Assignments for a 217-Pin PBGA—Pin Number Order (continued)

Pin	Signal Name
P4	VSS
P5	VDD
P6	A2
P7	TXD30
P8	VDD
P9	VSS
P10	VDD
P11	TXOE29
P12	D6
P13	NC
P14	VSS
P15	$\overline{CS}$
P16	TXD25
P17	TXD7
R1	MM
R2	RXD27
R3	VSS
R4	RXD31
R5	A3
R6	NC
R7	TXOE31
R8	TXD14
R9	D0
R10	D2
R11	TXD28
R12	VDD
R13	D7
R14	TXD12
R15	VSS
R16	$\overline{AS}$
R17	VDD
T1	RXD28
T2	VSS
T3	RXD30
T4	A1
T5	A5
T6	TXD31
T7	TXOE30
T8	$\overline{DS}$
T9	$\overline{DT}$
T10	VDD
T11	TXD29
T12	TXD27
T13	D4
T14	TXD13
T15	TXOE12
T16	VSS
T17	NC
U1	RXD15
U2	RXD29
U3	A0
U4	A4
U5	A6
U6	VDD
U7	TXOE14
U8	PCLK
U9	NC
U10	D1
U11	D3
U12	TXOE28
U13	TXOE27
U14	D5
U15	TXOE13
U16	TXD11
U17	R/$\overline{W}$

Pin Information (continued)

Table 3. Pin Assignments for a 217-Pin PBGA—Signal Name Order

Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin
A0	U3	NC	A16	RXD17	L1	TXD17	F17
A1	T4	NC	B4	RXD18	K3	TXD18	A5
A2	P6	NC	B7	RXD19	G4	TXD19	C8
A3	R5	NC	B12	RXD20	F3	TXD20	C11
A4	U4	NC	B15	RXD21	E2	TXD21	A15
A5	T5	NC	D7	RXD22	F4	TXD22	C13
A6	U5	NC	F14	RXD23	D3	TXD23	C14
A7	J3	NC	F16	RXD24	C2	TXD24	G17
A8	M2	NC	H3	RXD25	B1	TXD25	P16
A9	N1	NC	K15	RXD26	P3	TXD26	G14
A10	M3	NC	L16	RXD27	R2	TXD27	T12
A11	N2	NC	N4	RXD28	T1	TXD28	R11
A12	P1	NC	P13	RXD29	U2	TXD29	T11
A13	N3	NC	R6	RXD30	T3	TXD30	P7
A14	P2	NC	T17	RXD31	R4	TXD31	T6
$\overline{AS}$	R16	NC	U9	TCK	C17	TXOE0	B3
CK	B9	NC	C9	TDI	D15	TXOE1	A4
CKSPD0	A10	NC	A8	TDO	E14	TXOE2	B6
CKSPD1	B10	PCLK	U8	$\overline{TEST}$	C16	TXOE3	C10
CKSPD2	A11	R/$\overline{W}$	U17	TMS	D16	TXOE4	C12
$\overline{CS}$	P15	$\overline{RESET}$	B17	$\overline{TRST}$	D17	TXOE5	H17
D0	R9	RXD0	J1	TXD0	C4	TXOE6	L14
D1	U10	RXD1	J2	TXD1	B5	TXOE7	N16
D2	R10	RXD2	H2	TXD2	A6	TXOE8	J17
D3	U11	RXD3	G1	TXD3	A12	TXOE9	K17
D4	T13	RXD4	F1	TXD4	B13	TXOE10	L17
D5	U14	RXD5	G3	TXD5	J15	TXOE11	N14
D6	P12	RXD6	D1	TXD6	N17	TXOE12	T15
D7	R13	RXD7	D2	TXD7	P17	TXOE13	U15
$\overline{DS}$	T8	RXD8	M1	TXD8	J16	TXOE14	U7
$\overline{DT}$	T9	RXD9	L4	TXD9	K16	TXOE15	D5
FSYNC	H15	RXD10	K2	TXD10	M17	TXOE16	E16
INT	N15	RXD11	K1	TXD11	U16	TXOE17	E17
MM	R1	RXD12	E1	TXD12	R14	TXOE18	C6
NC	A1	RXD13	E3	TXD13	T14	TXOE19	C7
NC	A2	RXD14	E4	TXD14	R8	TXOE20	D11
NC	A3	RXD15	U1	TXD15	C5	TXOE21	B14
NC	A13	RXD16	L3	TXD16	F15	TXOE22	A14

Pin Information (continued)

Table 3. Pin Assignments for a 217-Pin PBGA—Signal Name Order (continued)

Signal Name	Pin
TXOE23	D13
TXOE24	G16
TXOE25	M14
TXOE26	G15
TXOE27	U13
TXOE28	U12
TXOE29	P11
TXOE30	T7
TXOE31	R7
VDD	A7
VDD	B11
VDD	C1
VDD	D6
VDD	D8
VDD	D10
VDD	D12
VDD	E15
VDD	F2
VDD	H4
VDD	H14
VDD	H16
VDD	K4
VDD	K14
VDD	L2
VDD	L15
VDD	M4
VDD	P5
VDD	P8
VDD	P10
VDD	R12
VDD	R17
VDD	T10
VDD	U6
VDD	G2
VDD	H1
VDDPLL	A9
VSS	B2
VSS	B16

Signal Name	Pin
VSS	C3
VSS	C15
VSS	D4
VSS	D9
VSS	D14
VSS	H8
VSS	H9
VSS	H10
VSS	J4
VSS	J8
VSS	J9
VSS	J10
VSS	J14
VSS	K8
VSS	K9
VSS	K10
VSS	P4
VSS	P9
VSS	P14
VSS	R3
VSS	R15
VSS	T2
VSS	T16
VSS	M15
VSS	M16
VSS	A17
VSSPLL	B8

Pin Information (continued)

Table 4. TTSI4K32T Pin Descriptions

Symbol	Type*	Description	
$\overline{\text{RESET}}$	I	**Reset (Active-Low).** A low on this pin resets the TTSI4K32T. It is asynchronous to any other clock or input signal. All flip-flops will be cleared when $\overline{\text{RESET}}$ is low. All counters, state machines, and configuration registers will be set to the default state following a reset.	
$\overline{\text{TEST}}$	I^u	**Test (Active-Low).** When low, $\overline{\text{TEST}}$ causes the output and bidirectional pins of the TTSI4K32T device to be in a high-impedance state. This pin has an internal pull-up resistor.	
MM	I	**Microprocessor Mode.** When MM = 0, the TTSI4K32T uses an asynchronous type handshake (equal to mode 1 of the Lucent dual T1/E1 terminator devices). When MM = 1, the TTSI4K32T uses a synchronous type handshake which requires a host processor clock (PCLK) input. Both modes use a demultiplexed address and data bus.	
—		**Synchronous Mode** (MM = 1)	**Asynchronous Mode** (MM = 0)
PCLK	I	**Host Processor Clock.** Valid from 0 MHz to 65 MHz.	**Unused.** Must be either tied high or low.
$\overline{\text{AS}}$	I	**Address Valid (Active-Low).** Valid for one PCLK cycle. Indicates the start of a processor access.	**Address Valid (Active-Low).** Indicates a valid address for a processor access. Must be held low for the duration of the access.
$\overline{\text{CS}}$	I	**Chip Select (Active-Low).** This pin is asserted low to enable any transfers through the microprocessor interface. $\overline{\text{CS}}$ should be a decode of all address and cycle type signals defining the memory map location of the TTSI4K32T.	**Chip Select (Active-Low).** This pin is asserted low to enable any transfers through the microprocessor interface. $\overline{\text{CS}}$ should be a decode of all address and cycle type signals defining the memory map location of the TTSI4K32T. In this mode, $\overline{\text{CS}}$ is used to control the tristating of $\overline{\text{DT}}$ at the end of the cycle. The input timing requirement of $\overline{\text{CS}}$ relative to $\overline{\text{AS}}$ is described in the Timing Characteristics section on page 55.
$\overline{\text{DS}}$	I	**Not Used.** Must be tied high.	**Data Valid (Active-Low).** Indicates valid data during processor writes. The TTSI4K32T will start driving D[7—0] when this signal is asserted during processor reads.
$\overline{\text{DT}}$	O	**Data Transfer Acknowledge (Active-Low).** Active for one PCLK cycle. Indicates that data has been written during processor writes. Indicates that read data is valid during processor reads. An external pull-up is required on this output.	**Data Transfer Acknowledge (Active-Low).** Indicates that data has been written during processor writes. Indicates that read data is valid during processor reads. Once driven active, this signal is held active until $\overline{\text{AS}}$, $\overline{\text{DS}}$, or $\overline{\text{CS}}$ is removed. An external pull-up is required on this output.

* I^u indicates internal 100 kΩ pull-up resistor, and I^d indicates 17.5 kΩ pull-down resistor.

Pin Information (continued)

Table 4. TTSI4K32T Pin Descriptions (continued)

Symbol	Type*	Description	
D[7—0]	I/O	**Host Processor Data Bus.** These pins provide an 8-bit, bidirectional data bus. Read data is valid for one PCLK cycle coincident with the assertion of $\overline{DT}$. Write data must be held throughout the access.	**Host Processor Data Bus.** These pins provide an 8-bit, bidirectional data bus. Write data must be valid for the duration of $\overline{DS}$. Read data is valid while $\overline{DT}$ is asserted.
A[14—0]	I	**Host Processor Address Bus.** A14—A0 must remain valid throughout the entire processor access. A0 is the least significant address signal and is used to select byte locations.	
R/$\overline{W}$	I	**Read/$\overline{Write}$.** This signal indicates a read or write cycle. Read cycle is indicated with a logic 1; a write cycle is indicated with a logic 0.	
INT	O	**Interrupt.** This pin will be asserted to indicate that an interrupt condition has occurred. This output will remain active until the interrupt status register has been cleared (read). The polarity of this output is controlled through the INTP bit (bit 3) of the general command register. The default value of this register is 0, which indicates active-high. This output is tristated until INTOE (bit 4) of the general command register is set to 1. The polarity of this output should be selected before the pin is enabled.	
RXD[0—31]	I^u	**Receive Data Highways 0—31.** Serial TDM highways receiving data at rates of 2.048 Mbits/s, 4.096 Mbits/s, or 8.192 Mbits/s.	
FSYNC	I	**Frame Synchronization.** This signal indicates the beginning of a frame every 125 μs (8 kHz). FSYNC can be active-low or active-high, but its polarity is the same for all highways. FSYNC can be sampled on a positive or negative CK edge. Time-slot numbers and bit offsets are assigned relative to the detection of FSYNC. There are no restrictions on the duty cycle of FSYNC as long as the setup and hold timing requirements relative to CK are met.	
CK	I	**Clock.** This input is the clock reference for all the transmit and receive highways. Its frequency can be 2.048 MHz, 4.096 MHz, 8.192 MHz, or 16.384 MHz. The frequency selection for CK must be set equal to or greater than the fastest highway data rate.	
CKSPD[2—0]	I	**Clock Speed Select for CK Pin.** These strap pins indicate the frequency of CK: CKSPD2 / CKSPD1 / CKSPD0 / CK (MHz) 0 / 0 / 0 / 2.048 0 / 0 / 1 / 4.096 0 / 1 / 0 / 8.192 0 / 1 / 1 / 16.384 1 / X / X / Reserved	
TXD[0—31]	O	**Transmit Data Highways 0—31.** Serial TDM highway transmitting data at rates of 2.048 Mbits/s, 4.096 Mbits/s, or 8.192 Mbits/s. During external driver mode, the TXD[0—31] outputs will be continuously driven. The only exception to this is when the $\overline{TEST}$ input is asserted. When not in external driver mode, this highway can be tristated on a per-time-slot basis. See Table 39, Transmit Highway 3-State Options, on page 50 for a detailed description of all methods for 3-stating the transmit highways.	

*I^u indicates internal 100 kΩ pull-up resistor, and I^d indicates 17.5 kΩ pull-down resistor.

Pin Information (continued)

Table 4. TTSI4K32T Pin Descriptions (continued)

Symbol	Type*	Description
TXOE[0—31]	O	**Transmit Output Enables 0—31.** These output pins reflect the active/high-impedance status for the corresponding transmit highways. They are continuously driven to reflect the status of the output enables of the transmit highways, regardless of whether or not external driver mode is enabled via the ED (bit 6) in the general command register. The external driver for transmit highway [i] should be enabled when TXOE[i] is a 1. Also see Table 39, Transmit Highway 3-State Options, on page 50 for other methods of 3-stating the transmit highways.
TDI	I^u	**JTAG Test Data Input.**
TCK	I	**JTAG Test Clock.** Maximum 10 MHz.
TMS	I^u	**JTAG Test Mode Select.**
$\overline{\text{TRST}}$	I^d	**JTAG Test Reset (Active-Low).** To disable the JTAG interface, tie $\overline{\text{TRST}}$ low or leave unconnected.
TDO	O	**Test Data Output.**
V_{DD}	P	**3.3 V Supply.** All V_{DD} leads must be connected to the 3.3 V supply.
V_{SS}	P	**Ground.**
V_{DD}PLL	P	**3.3 V PLL Supply.** V_{SS}PLL and V_{DD}PLL should be decoupled with a high-speed capacitor with a value in the range of 2 μF—5 μF.
V_{SS}PLL	P	**PLL Ground.** V_{SS}PLL and V_{DD}PLL should be decoupled with a high-speed capacitor with a value in the range of 2 μF—5 μF.
NC	—	**No Connect.** This pin must be left unconnected.

*I^u indicates internal 100 kΩ pull-up resistor, and I^d indicates internal 17.5 kΩ pull-down resistor.

Typical TSI Application

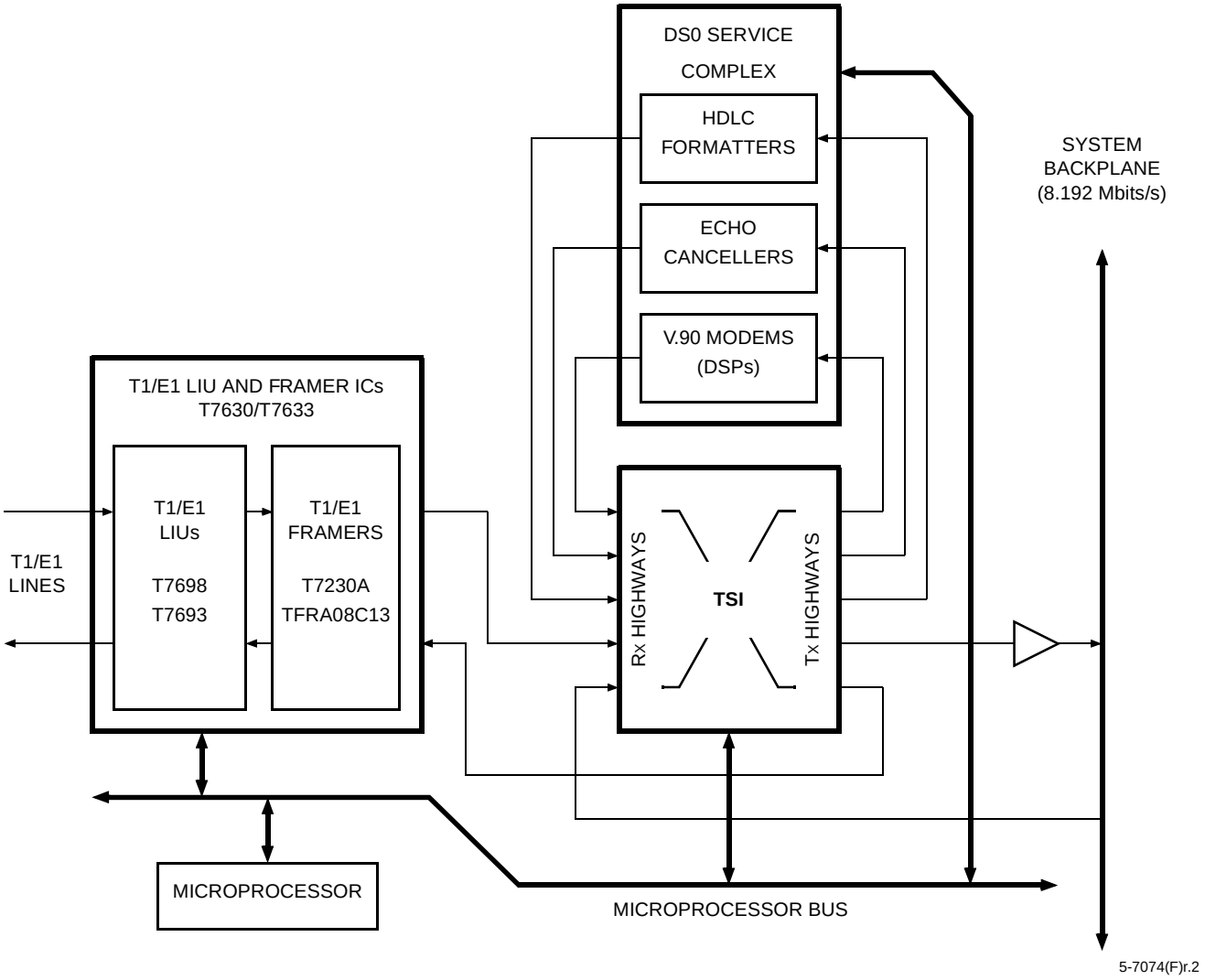


Figure 3. A Typical TSI Application

A typical application that requires a TSI is where TDM highways that are carrying different types of data in 8-bit time slots (64 kbits/s channels) need to be switched and sent to different destinations. For example, TDM highways may contain time slots that are carrying voice, Internet traffic, signaling information, etc.

The TSI could be programmed to select all the time slots, carrying Internet data from different Rx highways to be put on a another Tx highway that is connected to a bank of V.90 modems. Return data from these modems would be sent via another set of Rx highways back to the TSI, which could send the data back out over a Tx highway and to a T1 line via a T1 framer and LIU.

Similarly, time slots containing signaling information which is HDLC formatted can be sent to a bank of HDLC formatters. Voice channels that have echo on them could be selectively sent to echo cancellers. Data that needs to be sent to another card in the system could be put on the system backplane via optional bus drivers.

Interchange Fabric

The time-slot interchanger core has a memory-based architecture. The received time slots are converted from serial to parallel by the receive highways block and stored in an internal dual-ported memory called the data store, see Figure 1, Block Diagram of the TTSI4K32T on page 6. These time slots are then read out of the data store in the order specified by the connection store, converted from parallel to serial by the transmit highways section, and sent out on the transmit highways.

All the time slots (bytes) coming into the device are stored in the data store. Each TDM highway can bring in up to 32 valid time slots at 2.048 Mbits/s, 64 time slots at 4.096 Mbits/s, or 128 time slots on an 8.192 Mbits/s highway, during a 125 µs frame. With 32 Rx highways running at the maximum rate of 8.192 Mbits/s, the maximum capacity of the switch will be utilized. The addresses used to retreive the data from the data store are stored in the connection store. If host substituted data is to be transmitted instead of data that was received on a TDM highway, then it is stored in the connection store.

Any mode that is selected on a time-slot basis is typically made via the connection store. There are 8192 bytes in the connection store, two for each time slot that can be selected for transmission. Each one of the 4096 possible transmit time slots can be individually 3-stated. This is useful when multiple devices need to drive the same TDM highway as a bus or backplane. For extra drive, 32 individual output enables (TXOE pins) are also provided to individually control an external bus or backplane driver, one for each transmit highway. A low latency (send as soon as possible) or frame integrity (keep tagged time slots from the same highway together in the same frame) can also be selected on a time-slot basis. The user also has the option to send one of 13 predefined test patterns, a user-defined byte, or one of three user-defined idle codes, on any time slot of any Tx highway.

Time slots received on any TDM highway can be easily broadcasted on any transmit highway using the connection store. If, for example, the entire connection store is filled with all zeros, this then implies low-latency mode and that the source for all transmitted data is Rx highway 0, time slot 0. Thus, the data received on RXD0 time slot 0 will end up being broadcasted on all outgoing time slots.

Small and Large TSIs

The TTSI4K32T is one in a family of time-slot interchanger (TSI) devices offered by Lucent Technologies Microelectronics Group. This family of devices are all software compatible since they all have similar register maps. The larger devices of course have extra registers to configure the extra highways and also have larger connection and data stores. However, software written for a smaller TSI will run without alterations with a larger device. The TTSI2K32T and TTSI4K32T are also pin compatible, since they are in the same package.

Table 5. The TSI Family

Device	Time-Slot Capacity	Number of Rx/Tx Highways	Package
TTSI1K16T	1024	16/16	144-pin TQFP
TTSI2K32T	2048	32/32	217-pin PBGA
TTSI4K32T	4096	32/32	217-pin PBGA

The capacity of the TTSI1K16T can be fully utilized by receiving and/or transmitting data on all 16 highways at 4.096 Mbits/s or eight highways at 8.192 Mbits/s. Similarly, the TTSI2K32T can be fully utilized by receiving and/or transmitting data on all 32 highways at 4.096 Mbits/s or 16 highways at 8.192 Mbits/s. Other combinations of different data rates on different highways can also be used to fully utilize the TTSI1K16T and TTSI2K32T. The capacity of the TTSI4K32T is fully utilized only when data is being received and/or transmitted on all 32 highways at 8.192 Mbits/s.

The TTSI4K32T can be used to make even larger switches; for example, an 8192 time-slot switch with 64 Rx and 64 Tx highways. The Rx and Tx highways of the 8K switch are labeled LRXD[0—63] and LTXD[0—63], respectively, in the figure below.

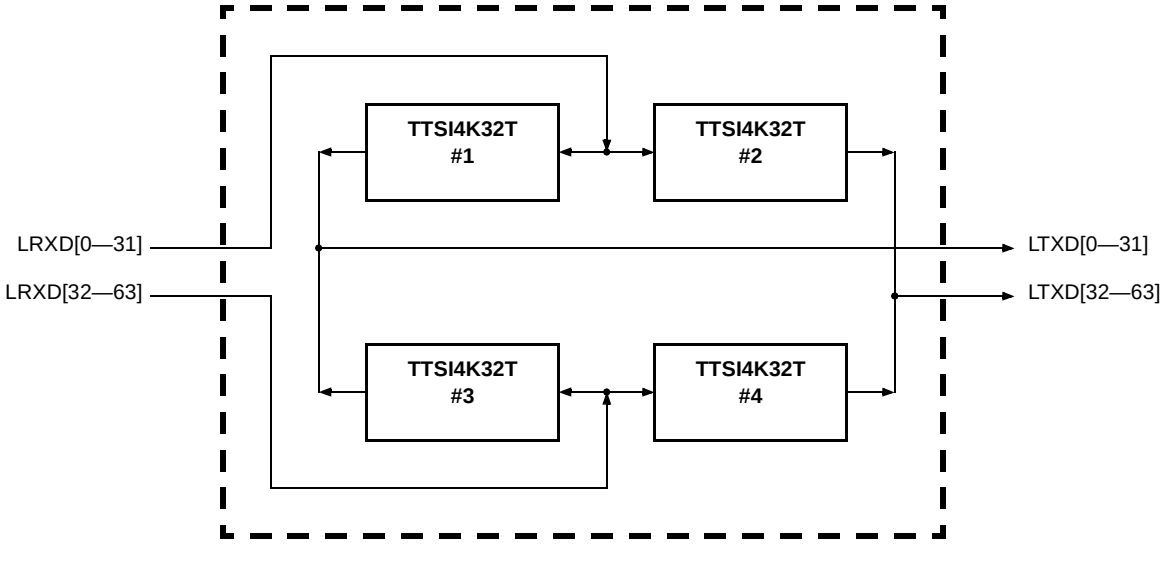


Figure 4. An 8K Time-Slot Switch Made from 4K TSIs

LRXD[0—31] are sent to both TSI #1 and #2. Similarly, LRXD[32—63] are sent to both TSI #3 and #4. The TXD[0—31] of TSI #1 are wire-ORed with the TXD[0—31] of TSI #3, to make LTXD[0—31]. Similarly, the TXD[0—31] of TSI #2 are wire-ORed with the TXD[0—31] of TSI #4, to make LTXD[32—63].

Now, if time slots on highway LRXD0 need to be switched to LTXD63, it can be done via TSI #2. The connection stores of TSI #2 and #4 must be programmed such that they both never drive their TXD31 simultaneously. The 3-state per time-slot feature of the TSI allows this to be accomplished easily.

Microprocessor Interface

The host interface is designed to connect directly to a typical synchronous or asynchronous host bus. The interface to the TTSI4K32T includes a separate clock, PCLK, which is used only in the synchronous interface mode. This device will be a slave on the host bus and will provide the host microprocessor with the capability to read and write the TTSI4K32T address space in a minimal number of clock cycles. There is no posting of writes in the host interface, and all registers and the data and connection stores are directly accessible.

Asynchronous Mode (MM = 0)

The following two timing diagrams show read and write in the asynchronous mode.

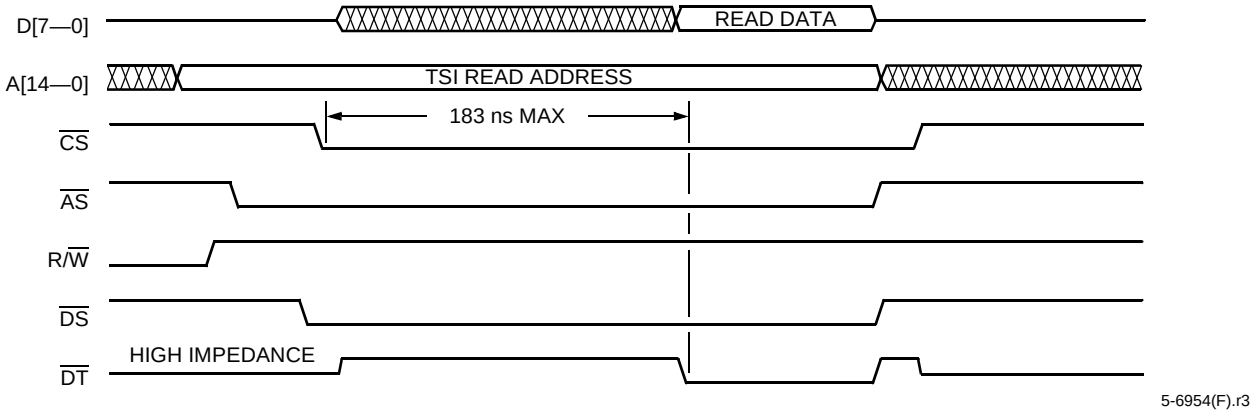


Figure 5. Asynchronous Read

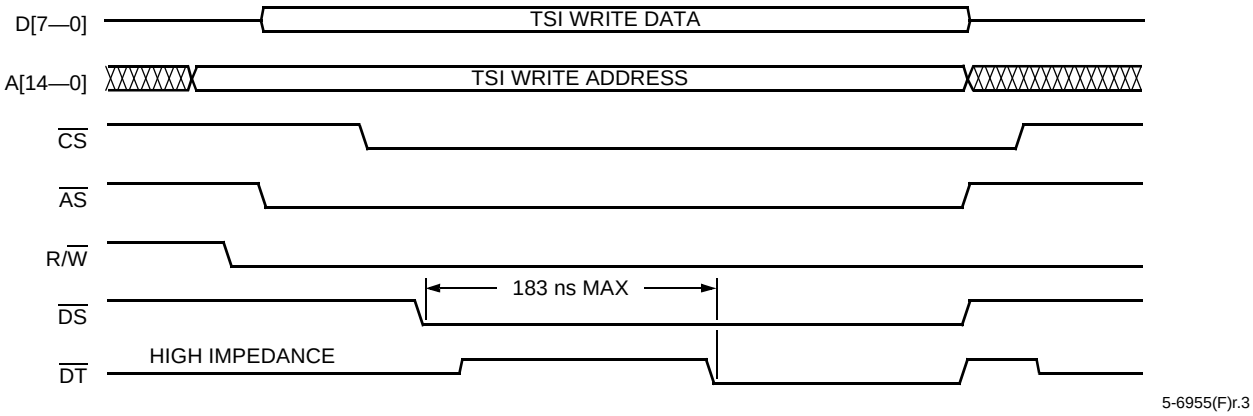


Figure 6. Asynchronous Write

The presence of $\overline{AS}$, $\overline{CS}$, and $\overline{DS}$ being asserted will start the TTSI4K32T internal access. Once data has been retrieved or written, $\overline{DT}$ will be asserted indicating the TTSI4K32T is ready to terminate the access. $\overline{DT}$ will continue to be asserted until $\overline{AS}$, $\overline{CS}$, or $\overline{DS}$ is negated.

The duration of an asynchronous read or write cycle will be a maximum of 183 ns. This duration is measured from when $\overline{AS}$, $\overline{CS}$, and $\overline{DS}$ are all asserted low until $\overline{DT}$ is asserted low by the TTSI4K32T.

Microprocessor Interface (continued)

Synchronous Mode (MM = 1)

The following two timing diagrams show read and write in the synchronous mode.

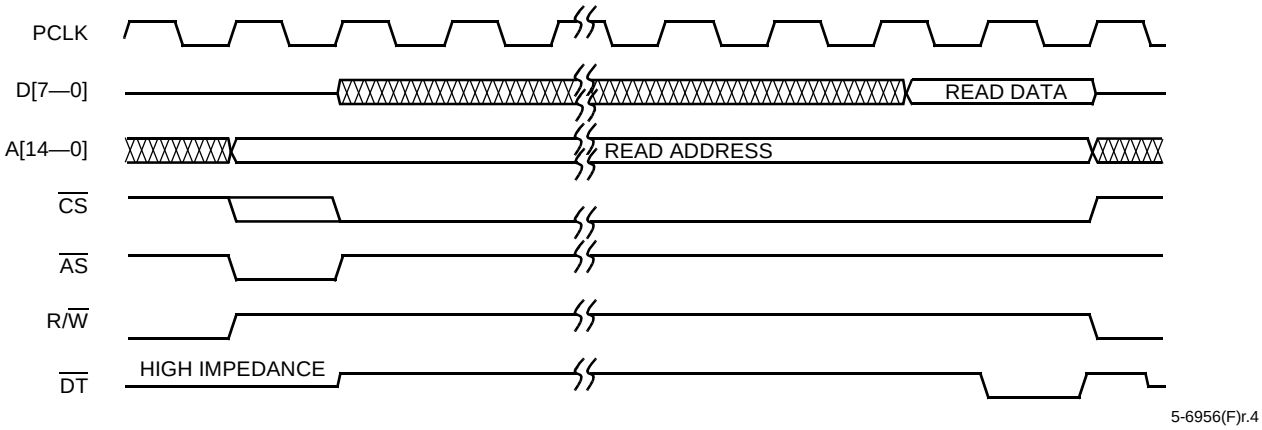


Figure 7. Synchronous Read

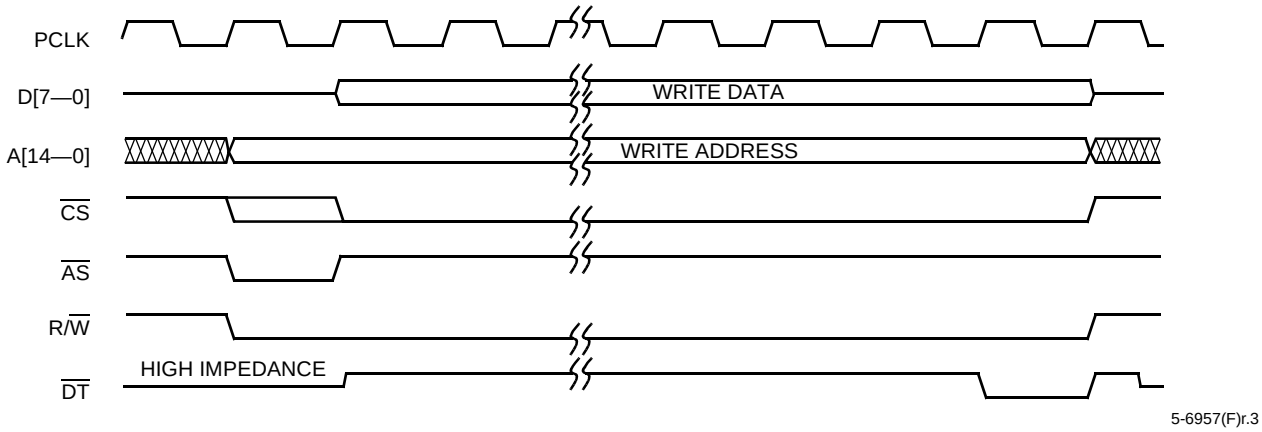


Figure 8. Synchronous Write

The synchronous write or read cycle is started when $\overline{AS}$ is sampled active with the rising edge of PCLK. In order for the TTSI4K32T to respond, $\overline{CS}$ must be active during the first or second cycle of an access depending on the value of CSV (bit 7) of the general command register. Once data has been retrieved or written, $\overline{DT}$ will be asserted for one clock, terminating the access.

The duration of a synchronous read or write cycle is a combination of two periods of time. One period is the duration of the internal cycle, which will be a maximum of 160 ns. The other time period is the initiation, termination, and synchronization of activity on the processor bus, which will be a maximum of six PCLK cycles. The total duration of the cycle, from the assertion of $\overline{AS}$ to the removal of $\overline{DT}$, will be the sum of these two periods of time.

Note: The number of processor clock cycles can be reduced by one PCLK cycle if the $\overline{CS}$ input signal can be delivered soon enough to be sampled with $\overline{AS}$ and CSV (bit 7) of the general command register is set to a 1.

Mixed-Highway Data Rates

Each receive (Rx) highway can be selected to sample at a rate of either 2.048 Mbits/s, 4.096 Mbits/s, or 8.192 Mbits/s. This rate selection is made via the HDR[1—0] field in the receive highways configuration register (byte 2). Similarly, each transmit (Tx) highway can be programmed to clock the data out at 2.048 Mbits/s, 4.096 Mbits/s, or 8.192 Mbits/s via the transmit highway configuration register (byte 2). Thus, 64 independent data rate selections can be made: 32 on the Rx side and 32 on the Tx side. Highways can also be selected to be idle, i.e., neither receiving nor transmitting data.

The data rate on a receive highway does not have to match that on its corresponding transmit highway either, e.g., RXD0 and TXD0 data rates can be different. Data received on a 2.048 Mbits/s highway can be transmitted on a 4.096 Mbits/s or 8.192 Mbits/s highway too. All of this flexibility allows this device to be used to solve a variety of design problems such as data rate adaptation, etc. Many slow-speed highways can also be combined and sent out on a single high-speed highway.

The figure below depicts an example where time slots are being received on different highways at different data rates and are being switched and sent out at a slower, same, or faster data rate. Each rectangle, labeled A—N, represents an 8-bit time slot.

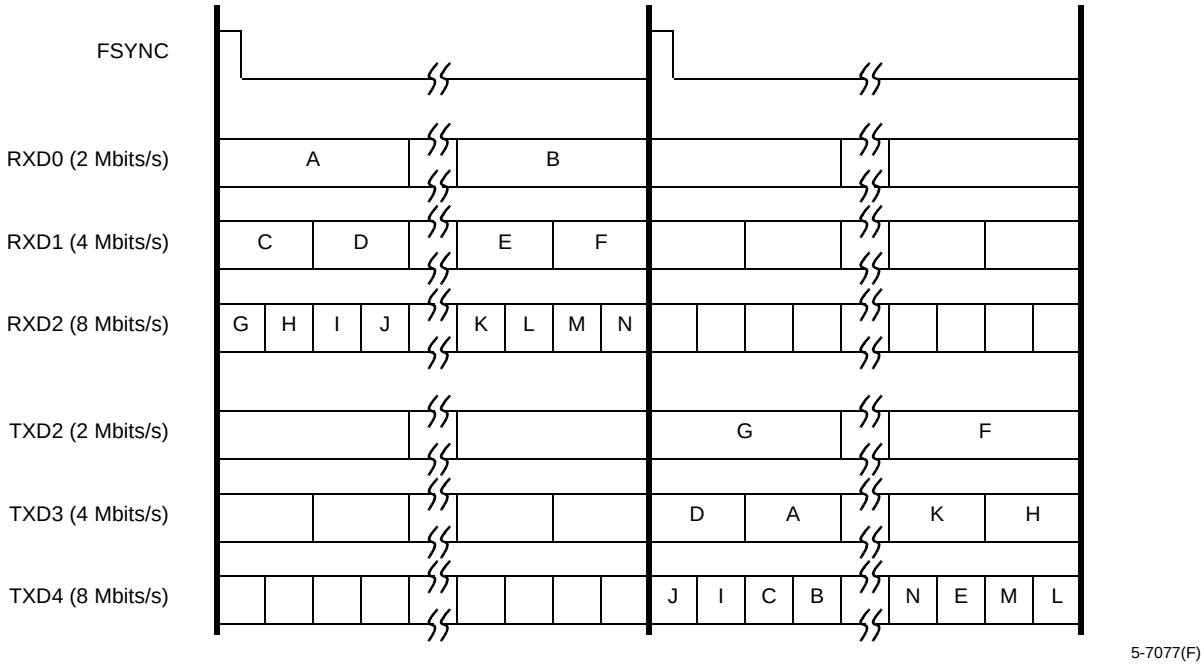


Figure 9. Mixed-Highway Data Rates

TDM Highway Interface Timing

Virtual and Physical Frames

Figure 10 below shows a virtual frame offset from the physical frame. The FSYNC pulse marks the beginning of the physical frame, but the TSI can be programmed to interpret the location of time slot 0 at any point in a frame. Several parameters are available to make up the offset for a virtual frame with various levels of granularity. There is XTSOFF/RTSOFF for transmit/receive time-slot offsets. This offset can be up to 31 time slots for a 2.048 Mbits/s highway, 63 time slots for a 4.096 Mbits/s highway, or 127 time slots for an 8.192 Mbits/s highway. XBITOFF/ RBITOFF allow the setting of up to a 7-bit offset for transmit/receive frames. XFBOFF/RFBOFF allow fractional bit offsets of 0, 1/4, 1/2, or 3/4 bits. All of these offsets mentioned above can be independently programmed for each one of the transmit and receive highways. The maximum offset that can be introduced on an 8.192 Mbits/s highway is 127 time slots, 7 3/4 bits. The maximum offset on a 4.096 Mbits/s highway is 63 time slots and 7 3/4 bits. The maximum offset on a 2.048 Mbits/s highway is 31 time slots, 7 3/4 bits.

The following examples indicate how virtual offsets can be used to simplify system designs. For example, data that is being sent to the TSI on a particular Rx highway may have incurred a several time-slot delay due to processing by HDLC formatters, echo cancellers, communication protocol processors, etc. Rather than adding an external buffer to realign all the highway data to the next FSYNC, an offset to create a virtual frame on that Rx highway can be used instead. On a transmit highway, for example, there may be a device downstream that has a processing latency of N time slots. An offset of (32 – N) time slots can be added beforehand on a 2.048 Mbits/s highway so that after processing, the TDM data is aligned to FSYNC again.

Fractional bit offsets are handy for adjusting the sampling point on a Rx highway. With a 1/4-bit resolution possible, setup and hold time requirements on the Rx TDM highways for the TSI should be easily met. On transmit highways, fractional bit offsets can be used to shift the outgoing highway data slightly, so the destination device's setup and hold times can be met with adequate margins. Note that the time slot, bit, and fractional bit offsets are relative to the highway data rate and imply different durations on different speed highways. For example, a 1/4-bit offset on a 2.048 Mbits/s highway means 122 ns, on a 4.096 Mbits/s highway, it is 61 ns, and on an 8.192 Mbits/s highway, it implies a 30.5 ns offset.

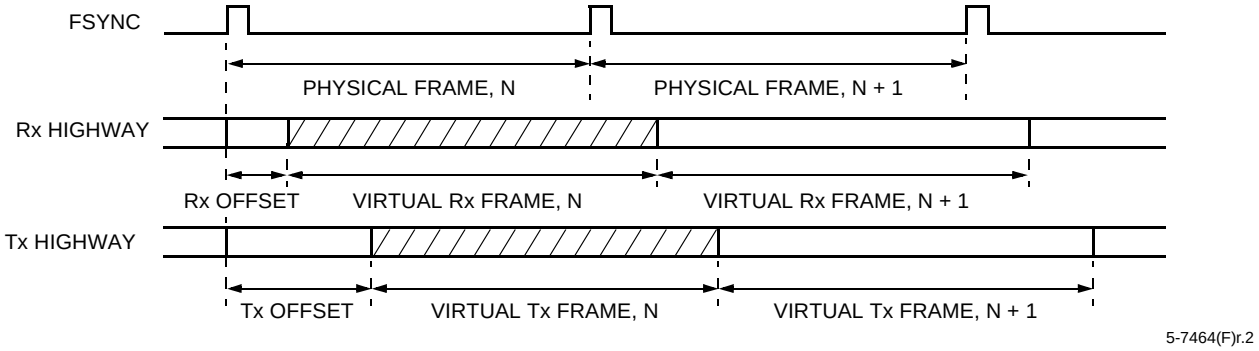


Figure 10. Virtual and Physical Frames

TDM Highway Interface Timing (continued)

TDM Highway Alignment at Zero Offset

The TDM highway interface logic is designed to make interconnection to the TTSI4K32T as simple as possible. Consider the timing diagram shown in Figure 11 below. Assume the following configuration register settings:

- FSYNC is active-high, FSP (bit 2) is set to 1 in the general command register.
- FSYNC is sampled by the rising edge of CK, FSSE (bit 1) is set to 1 in the general command register.
- The Tx and Rx highways are all set for zero bit and time-slot offset.
- The input CK speed is equal to the highway data rate.

One can see that time slot 0 of a frame coincides with the sampling of an active FSYNC.

At that edge:

- Bit 0 of time slot 0 is latched from the Rx highway with the coincident clock.
- Bit 0 of time slot 0 is transmitted starting with the coincident clock.

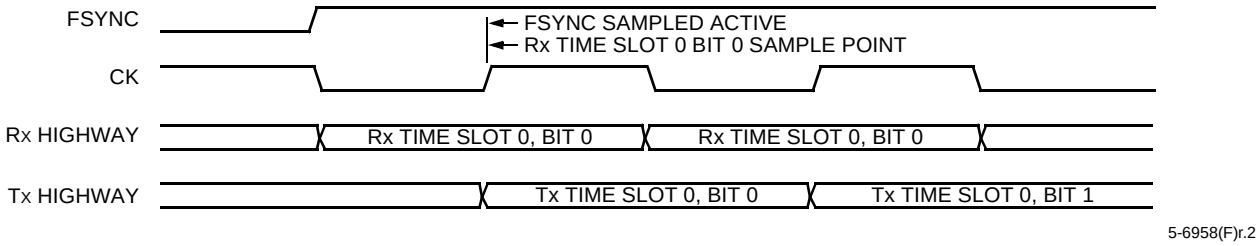


Figure 11. Synchronization to FSYNC

TDM Highway Offsets

An offset may be added to the sampling of Rx time slot 0, bit 0 or the transmission of Tx time slot 0, bit 0. This can be done on any of the receive and/or transmit highways, totally independent from one another. This is done by setting the time-slot offset number, bit offset number, and fractional bit offset number on a per-highway basis using the receive and transmit highway configuration registers. To illustrate this point, consider the timing diagram shown in Figure 12 on page 23. Assume the following configuration register programming:

- The input CK speed is set to 8.192 MHz.
- FSYNC is active-high, FSP (bit 2) is set to 1 in the general command register.
- FSYNC is sampled by the rising edge of CK, FSSE (bit 1) is set to 1 in the general command register.
- The RXD0 highway is set for 3/4-bit offset and a highway data rate of 4.096 Mbits/s.
- The TXD0 highway is set for 1-bit offset and a highway data rate of 2.048 Mbits/s.

One can see that bit 0 of the receive time slot 0 is sampled 1 and 1/2 CK cycles after FSYNC is sampled active. Since CK is set for 8.192 MHz and RXD0 is set for 4.096 Mbits/s, then 1 and 1/2 CK cycles equals 3/4 of a 4.096 Mbits/s bit period.

TDM Highway Offsets (continued)

One can also see that bit 0 of the transmit time slot 0 is driven four CK cycles after FSYNC is sampled active. Since CK is set for 8.192 MHz and TXD0 is set for 2.048 Mbits/s, then four CK cycles equals one 2.048 Mbits/s bit period.

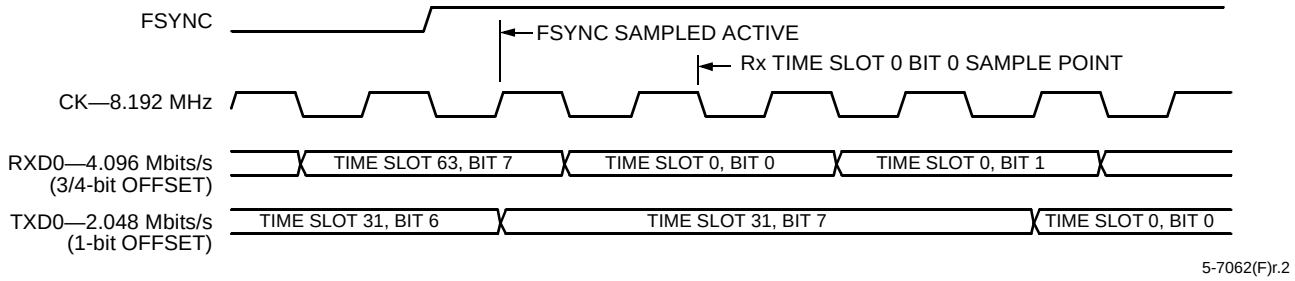


Figure 12. Highway Offsets

Reset Sequence

The reset sequence of the TTSI4K32T is related to the PLL operation. In order for the chip to be properly reset, the PLL must have already established a lock on the CK input signal. That event will occur 250 µs after the CK input is functioning. After the PLL is locked onto the input clock, the TTSI4K32T will be in a reset state within 200 ns. This results in a reset time of 250.2 µs. Subsequent resets will take 200 ns, provided CK is not interrupted.

$\overline{\text{RESET}}$ is an asynchronous signal and requires no setup or hold margins relative to any other input clock or signal.

After a reset, BIST must be run on the TTSI4K32T to bring all the memories in the device to a known state. This is required for correct operation of the chip. See the description below Table 15, BIST Command Register (0x02), on page 38, on how to run BIST.

Low-Latency and Frame-Integrity Modes

Transmit time slots can be selected for low-latency (minimum delay) or for frame-integrity modes using the connection store memory.

Low Latency

Low latency causes a received time slot to be transmitted as soon as possible. This mode is useful for voice channels where minimum delay through the network is desirable. If the transmit (Tx) time slot is very close or before the receive (Rx) time slot, then the data will be transmitted in the next frame. If a particular transmit time slot is physically later in time than the receive time slot by a certain duration (time-slot separation), then the data will be transmitted in the current frame. The latency will be equal to the separation of the two time slots involved. The maximum latency that data can encounter through the TSI in low-latency mode is 134 µs. If this latency is sufficient for a particular application, disregard any of the following details.

The required separation that will cause the time slot to be transmitted in the current frame is as follows: the Tx time-slot position in the physical frame must be greater than or equal to the Rx time-slot position in the physical frame, by a duration of 2 Rx time slots + (4 + i) x 30.5176 ns, where i is the Tx highway number.

When Rx and Tx highway data rates are equal and the Rx and Tx highway offsets are set to zero, the following table shows the result of the above relationship for various Tx highways.

Table 6. Time-Slot Separation Required for Transmission with Minimum Latency (0 Offsets)

Rx Highway Data Rate (Mbits/s)	Tx Highway Data Rate (Mbits/s)	Time-Slot (ts) Separation Required for Transmission in Current Frame on Highway				
		TXD0	TXD4	TXD8	TXD15	TXD31
2.048	2.048	2 ts, 1/4 bit	2 ts, 1/2 bit	2 ts, 3/4 bit	2 ts, 1 1/4 bits	2 ts, 2 1/4 bits
4.096	4.096	2 ts, 1/2 bit	2 ts, 1 bit	2 ts, 1 1/2 bits	2 ts, 2 1/2 bits	2 ts, 4 1/2 bits
8.192	8.192	2 ts, 1 bit	2 ts, 2 bits	2 ts, 3 bits	2 ts, 4 3/4 bits	3 ts, 3/4 bits

For example:

- If data is received in time slot 0 at 2.048 Mbits/s, it could be passed through the device with minimum latency if transmitted on time slot 3 at 2.048 Mbits/s of TXD0.
- If data is received in time slot 1 at 4.096 Mbits/s, it could be passed through the device with minimum latency if transmitted on time slot 4 at 4.096 Mbits/s of TXD8.
- If data is received in time slot 2 at 8.192 Mbits/s, it could be passed through the device with minimum latency if transmitted on time slot 6 at 8.192 Mbits/s of TXD31.

If the Rx highway has an offset, then the relationship can be updated. The Rx_time-slot_position is defined as the Rx_time-slot_number + Rx_highway offset. The new relationship will determine the transmit time-slot position in the physical frame at which the received data can be transmitted with minimum delay. The new relationship is (i = Tx highway number):

$$\text{Tx_time-slot_position} \geq \text{Rx_time-slot_number} + \text{Rx highway offset} + 2\ \text{Rx time slots} + (4 + i) \times 30.5176\ \text{ns}$$

If the Tx highway also has an offset, then the relationship becomes (i = Tx highway number):

$$\text{Tx_time-slot_number} + \text{Tx highway offset} \geq \text{Rx_time-slot_number} + \text{Rx highway offset} + 2\ \text{Rx time slots} + (4 + i) \times 30.5176\ \text{ns}$$

Low-Latency and Frame-Integrity Modes (continued)

Low Latency (continued)

For example, consider any Rx highway running at 4.096 Mbits/s using time slot 5 to receive data, with an Rx highway offset of 3 time slots. It is to be transmitted on TXD6. The right hand side of the relationship evaluates to:

```
    5   time slots @ 4.096 Mbits/s
+   3   time slots @ 4.096 Mbits/s
+   2   time slots @ 4.096 Mbits/s
+ (4 + 6) x 30.5176 ns
  19,836.426 ns
```

The results of the calculation show that the received data can be transmitted with minimum delay using a Tx time slot located 19,836.426 ns (or later) into the physical frame on TXD6. With a zero offset on TXD6, the time-slot number for transmission with minimum delay would be:

Tx time slot 21 @ 8.192 Mbits/s
Tx time slot 11 @ 4.096 Mbits/s
Tx time slot 6 @ 2.048 Mbits/s

Frame Integrity

Frame integrity is applied to multiple transmit time slots in order to force data received in the same frame to be transmitted together in a subsequent frame. This rule causes added delay, but it is useful for wideband data. Such data could be ISDN BRI (2B channels) that take up two time slots on a receive highway. It could also be an ISDN H0 channel (six contiguous time slots) that is being used to carry video.

The maximum latency through the device for any time slot marked for frame integrity mode is 378 µs. If that latency is sufficient for a particular application, disregard any of the following details.

To understand the latency involved with frame-integrity mode, consider the following information. The definition of frame integrity states that integrity is maintained between a particular Rx and Tx highway pair. This pair can be made up of any Rx highway and any Tx highway.

Latency due to frame integrity mode is a function of the highway offsets of the Rx and Tx pair rather than the relative position of the time slots. Latency in this mode will be expressed in terms of physical frames. Whether time slots received in virtual Rx frame N will end up going out in virtual Tx frame N + 1, N + 2, or N + 3 is dependent on the relative highway Rx and Tx highway offsets. For a description of virtual frames, see Figure 10, Virtual and Physical Frames on page 21.

Consider the following example. Assume RXD0 is switched to TXD1 with all Tx time slots marked for frame integrity (FI) on TXD1. If it is desirable to have the lowest possible latency for the data received on RXD0, then TXD1 must have a highway offset which is 3.90625 µs (1 time slot @ 2.048 Mbits/s) greater than the highway offset selected for RXD0. In that case, time slots received in the virtual Rx frame (frame N) will be transmitted in the next virtual Tx frame (frame N + 1).

The greatest latency will be incurred when the RXD0 offset is at least 121.09375 µs (31 time slots @ 2.048 Mbits/s) greater than the offset selected for TXD1. In that case, time slots received in the current virtual Rx frame (frame N) will be transmitted three frames later, i.e., in virtual Tx frame N + 3.

For all other RXD0 and TXD1 offset values, time slots received in the current virtual Rx frame will be transmitted two frames later, i.e., in virtual Tx frame N + 2.

Low-Latency and Frame-Integrity Modes (continued)

Frame Integrity (continued)

The range of Rx and Tx offsets can be independently selected from 0 μs to (125 – Δ)μs via the Rx and Tx highway configuration registers, bytes 0 and 1, where Δ = 1/4 bit. The offset difference (Tx highway offset – Rx highway offset) can therefore take the range from –(125 – Δ)μs to +(125 – Δ)μs. The table below shows the virtual frame for transmission for the various cases of offset difference.

Table 7. Offset Difference and Its Effect on Frame for Transmission

Offset Difference = (Tx Highway Offset – Rx Highway Offset)	Virtual Frame for Transmission
A ≤ offset difference < B*	N + 3
B ≤ offset difference < C*	N + 2
C ≤ offset difference ≤ D*	N + 1

* The values for A, B, C, and D are specified in Table 8 below.

Table 8. Offset Difference Boundaries

Offset Difference Boundary	Boundary Value (μs)	Boundary Value in Terms of Time Slots (ts) and Bits, at Different Data Rates		
		2.048 Mbits/s	4.096 Mbits/s	8.192 Mbits/s
A	–(125 – Δ)	–(31 ts, 7 3/4 bits)	–(63 ts, 7 3/4 bits)	–(127 ts, 7 3/4 bits)
B	–121.09375	–31 ts	–62 ts	–124 ts
C	+3.90625	1 ts	2 ts	4 ts
D	+(125 – Δ)	31 ts, 7 3/4 bits	63 ts, 7 3/4 bits	127 ts, 7 3/4 bits

Table 7 and Table 8 can be used to determine the latency of time slots through the TSI in a frame integrity situation. Keep in mind that the offset difference is the major factor in determining which virtual Tx frame the time slots will go out in. The boundary values given in Table 8 are accurate to within ±1 time slot @ 8.192 Mbits/s (= ±4 bits @ 4.096 Mbits/s = ±2 bits @ 2.048 Mbits/s) and will depend on your particular register settings.

This example can be used to determine the latency of a frame integrity situation. Keep in mind that only the Tx and Rx highway offsets are relevant when determining the number of physical frames that the transmit data will incur. However, there is a small range of offset separation where the data will go out in either virtual Tx frame N + 2 or N + 3, depending on the actual Rx and Tx offsets chosen.

There may be many Rx/Tx highway pairs performing frame integrity simultaneously, but the definition of frame integrity states that integrity is maintained between each Rx and Tx pair and not across multiple receive highways. However, in practice, if a Tx highway contains FI time slots from multiple Rx highways and those Rx highways have the same highway offset, then all of the FI time slots will incur equal delay with frame integrity through the switch.

Low-Latency and Frame-Integrity Modes (continued)

Frame Integrity (continued)

In the example shown below in Figure 13, a receive and transmit highway are both running at 2.048 Mbits/s. There are 32 time slots for each 125 µs frame. The Rx and Tx highway offsets are zero. This makes the offset difference zero. Therefore, time slots selected for FI will be transmitted two frames later.

The TSI is configured to perform the following switching function:

Tx time slot 31 is sourced from Rx time slot 0 in low-latency mode. It goes out in frame N.
Tx time slot 2 is sourced from Rx time slot 2 in low-latency mode. It goes out in frame N + 1.
Tx time slot 30 is source from Rx time slot 1 in frame-integrity mode. It goes out in frame N + 2.
Tx time slot 0 is sourced from Rx time slot 3 in frame-integrity mode. It goes out in frame N + 2.

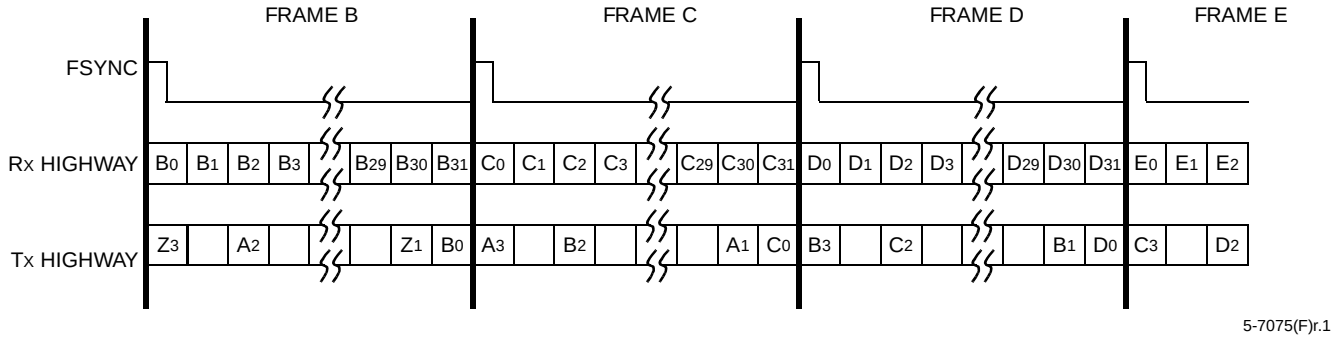


Figure 13. Mixed Low-Latency and Frame-Integrity Modes

Test-Pattern Generation

Test-pattern generation involves selecting outgoing time slots on a particular transmit highway for use in transmitting one of 15 patterns of data. The patterns available are selected using TPS[3—0] (bits 7—4) of the Test-Pattern Style Register (0x0A), Table 23 on page 43. The transmit highway and time slots involved are selected using the connection store.

Using the connection store, time slots can be set for test-pattern mode and the on-chip test-pattern generator will be the source for that transmitted data. The type of test pattern used is determined by the values in the Test-Pattern Style Register (0x0A), Table 23 on page 43. Test-pattern data can be applied to any number of time slots on only one highway at a time. Any highway may be selected to transmit test-pattern data. The only restrictions for selecting the time slots set for test-pattern mode are that the time slots must be from the same highway and they must be contiguous.

The sequence for enabling test-pattern generation is as follows:

1. Set TSDSM[2—0] (bits 7—5) in byte 1 of the connection store locations which correspond to the time slots involved in test-pattern substitution mode. Any range of time slots may be selected for test-pattern substitution mode, starting at any time-slot position. The remaining time slots of that highway will be unaffected.
2. Set TPS[3—0] (bits 7—4) of the Test-Pattern Style Register (0x0A), Table 23 on page 43 to select the test pattern to be sent. If a fixed user-defined byte is selected for transmission via the TPS[3—0] bits, then the Test-Pattern Generator Data Register (0x12), Table 31 on page 45 must also be programmed.
3. Select the data rate of the test-pattern generator via GENHDR[1—0] (bits 5—4) and set STTPG (bit 7) to 1 in the Test Command Register (0x09), Table 22 on page 42 to start transmitting a good test pattern on the selected time slots.

In order for data to be transmitted, highways need to be enabled using XE (bit 2) of the Transmit Highway Configuration Register (Byte 2) (0x1002 + 4i), Table 35 on page 47 and GXE (bit 0) of the General Command Register (0x00), Table 13 on page 37. This can be done before or after the above sequence.

The Tx highway that has been selected for test-pattern generation must be the only highway that has time slots selected for test-pattern substitution mode (i.e., TSDSM[2—0] = 110) in the connection store. No time slots on any other Tx highway may be selected for test-pattern substitution mode. If the Tx highway selected for test-pattern generation is changed, then the previous highway must have all its time slots that were in the TSDSM[2—0] = 110 mode, to be changed to a non-test-pattern substitution mode.

Test-Pattern Checking

Test-pattern checking involves selecting incoming time slots on a particular receive highway for reception of one of 15 test patterns. The patterns available are selected by setting CPS[3—0] (bits 3—0) of the Test-Pattern Style Register (0x0A), Table 23 on page 43. The input highway and time slots involved are selected using the following registers:

- Test-Pattern Checker Highway Register (0x0B), Table 24 on page 44
- Test-Pattern Checker Upper Time-Slot Register (0x0C), Table 25 on page 44
- Test-Pattern Checker Lower Time-Slot Register (0x0D), Table 26 on page 44

Test-pattern data can be checked on any number of time slots on only one highway at a time. Any receive highway may be selected to check for test-pattern data. The only restriction on selecting the time slots set for test-pattern checking is that the time slots must be from the same highway and they must be contiguous.

The sequence for enabling test-pattern checking is as follows:

1. Set Test-Pattern Checker Highway Register (0x0B), Table 24 on page 44 to select a highway for receiving the test data.

Test-Pattern Checking (continued)

2. Set the Test-Pattern Checker Upper Time-Slot Register (0x0C), Table 25 on page 44 and the Test-Pattern Checker Lower Time-Slot Register (0x0D), Table 26 on page 44 to indicate the range of input time slots which will be carrying test data. The range is inclusive of the time slots indicated in both registers. If only one time slot is to be selected, then the upper and lower registers should be set to the same value.
3. Set CPS[3—0] (bits 3—0) of the Test-Pattern Style Register (0x0A), Table 23 on page 43 to select the test pattern to detect. If a fixed, user-defined byte is to be detected, the CTP[7—0] bits in the Test-Pattern Checker Data Register (0x0E), Table 27 on page 44 should also be programmed with the user-defined pattern.
4. Select the data rate of the test-pattern checker via CHKHDR[1—0] (bits 3—2) and set STTPC (bit 6) in the Test Command Register (0x09), Table 22 on page 42 to prompt the checker to attempt to lock onto the selected test-pattern style.

If there is a need to restart the checker (i.e., the test-pattern style has changed), then STTPC (bit 6) of the Test Command Register (0x09), Table 22 on page 42 must first be cleared to 0, and then steps 3 and 4 should be repeated.

There is an interrupt register status bit related to the test-pattern checker. TPD (bit 5) of the Interrupt Status Register (0x07), Table 20 on page 40 is used to determine when, if ever, the pattern is detected. The TPD interrupt status bit will remain 0 until the pattern has been detected. This bit is cleared when read. Once TPD is set, it will not be set again until the checker is instructed to relock on the test pattern by clearing and then setting STTPC (bit 6) in the test command register.

Error Injection

The error injection feature provides the capability to inject errors into the outgoing test-pattern data. The number of errors injected is set using the Test-Pattern Error Injection Register (0x0F), Table 28 on page 44.

If error injection is required, the process should start by setting up the test-pattern generator using steps 1—3 in the Test-Pattern Generation section on page 28. In order to start injecting errors into the outgoing test pattern, write the Test-Pattern Error Injection Register (0x0F), Table 28 on page 44 with the number of errors desired. When all of the errors have been injected into the outgoing data stream, the interrupt status bit BEI (bit 0) will be set in the Interrupt Status Register (0x07), Table 20 on page 40. Errors will be injected at the rate of one per time slot. Test Command Register (0x09), Table 22 on page 42 will be cleared to 0 when BEI is set.

Error Checking

Errors are checked on time slots marked for test-pattern data once the checker has locked onto the test pattern. Every time an error is detected, the ERD (bit 3) interrupt status bit is set and the test-pattern error counter register contents are incremented. There are two registers Test-Pattern Error Counter (Byte 0) (0x10), Table 29 on page 45 and Test-Pattern Error Counter (Byte 1) (0x11), Table 30 on page 45, that are used to track the number of errors detected on incoming test patterns.

The error counter registers are reset after both have been read. In order to ensure that the correct value is read from these registers, byte 0 must be read first followed by byte 1. This action will latch the counter value and allow the counter logic to be reset and then continue recording.

JTAG Boundary-Scan Specification

Principle of the Boundary Scan

The boundary scan (BS) is a test aid for chip, module, and system testing. The key aspects of BS are as follows:

1. Testing the connections between ICs on a particular board.
2. Observation of signals to the IC pins during normal operating functions.
3. Controlling the built-in self-test (BIST) of an IC. TTSI4K32T does not support BS-BIST.

Designed according to the *IEEE* Std. 1149.1-1990 standard, the BS test logic consists of a defined interface: the test access port (TAP). The TAP is made up of four signal pins assigned solely for test purposes. The fifth test pin ensures that the test logic is initialized asynchronously. The BS test logic also comprises a 16-state TAP controller, an instruction register with a decoder, and several test data registers (BS register, BYPASS register, and IDCODE register). The main component is the BS register that links all the chip pins to a shift register by means of special logic cells. The test logic is designed in such a way that it is operated independently of the application logic of the TTSI4K32T (the mode multiplexer of the BS output cells may be shared). Figure 14 illustrates the block diagram of the TTSI4K32T's BS test logic.

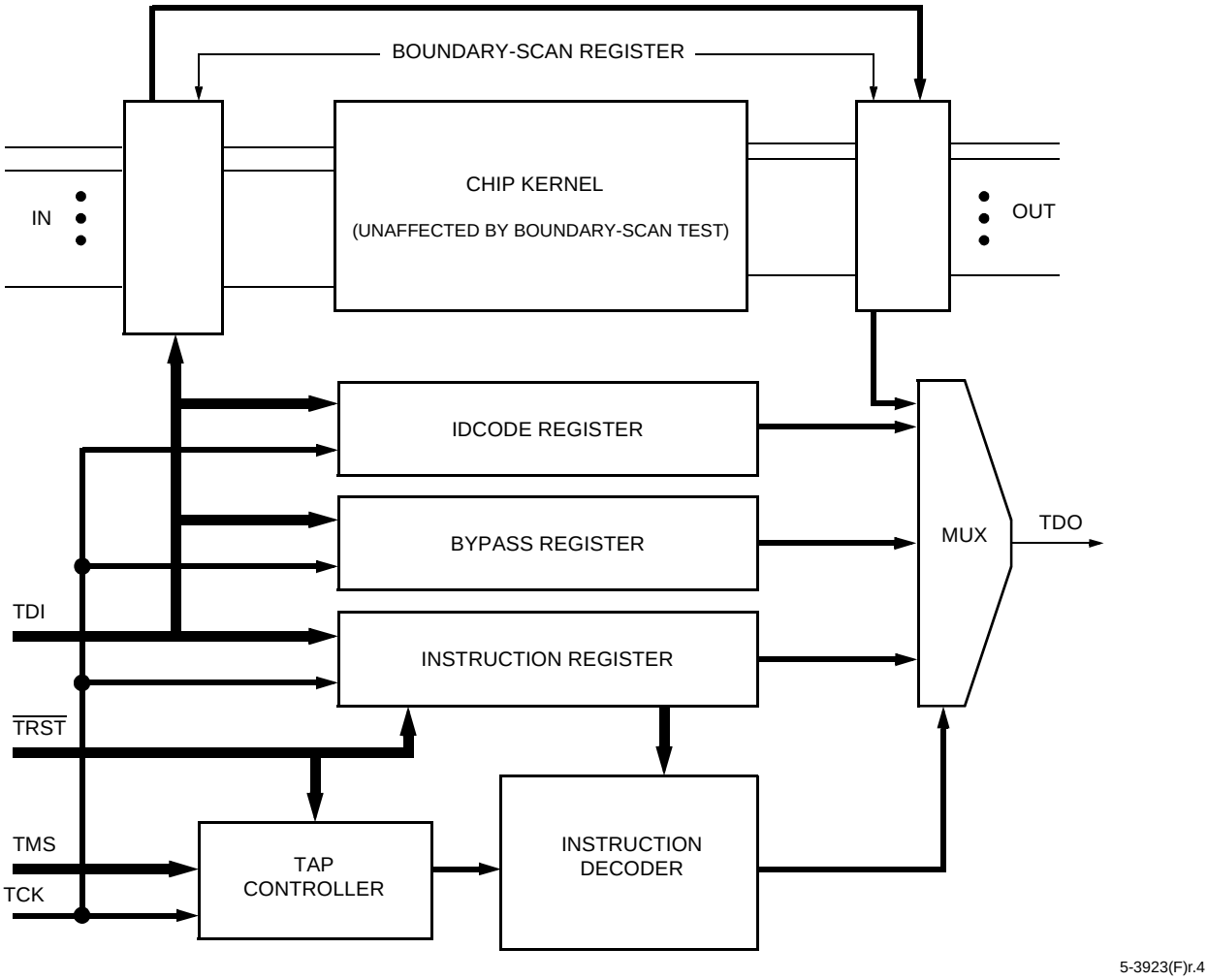


Figure 14. Block Diagram of the TTSI4K32T's Boundary-Scan Test Logic

JTAG Boundary-Scan Specification (continued)

Test Access Port Controller

The test access port controller is a synchronous sequence controller with 16 states. The state changes are preset by the TMS, TCK, and $\overline{\text{TRST}}$ signals and by the previous state. The state changes always take place when the TCK edge rises. Figure 15 shows the TAP controller state diagram.

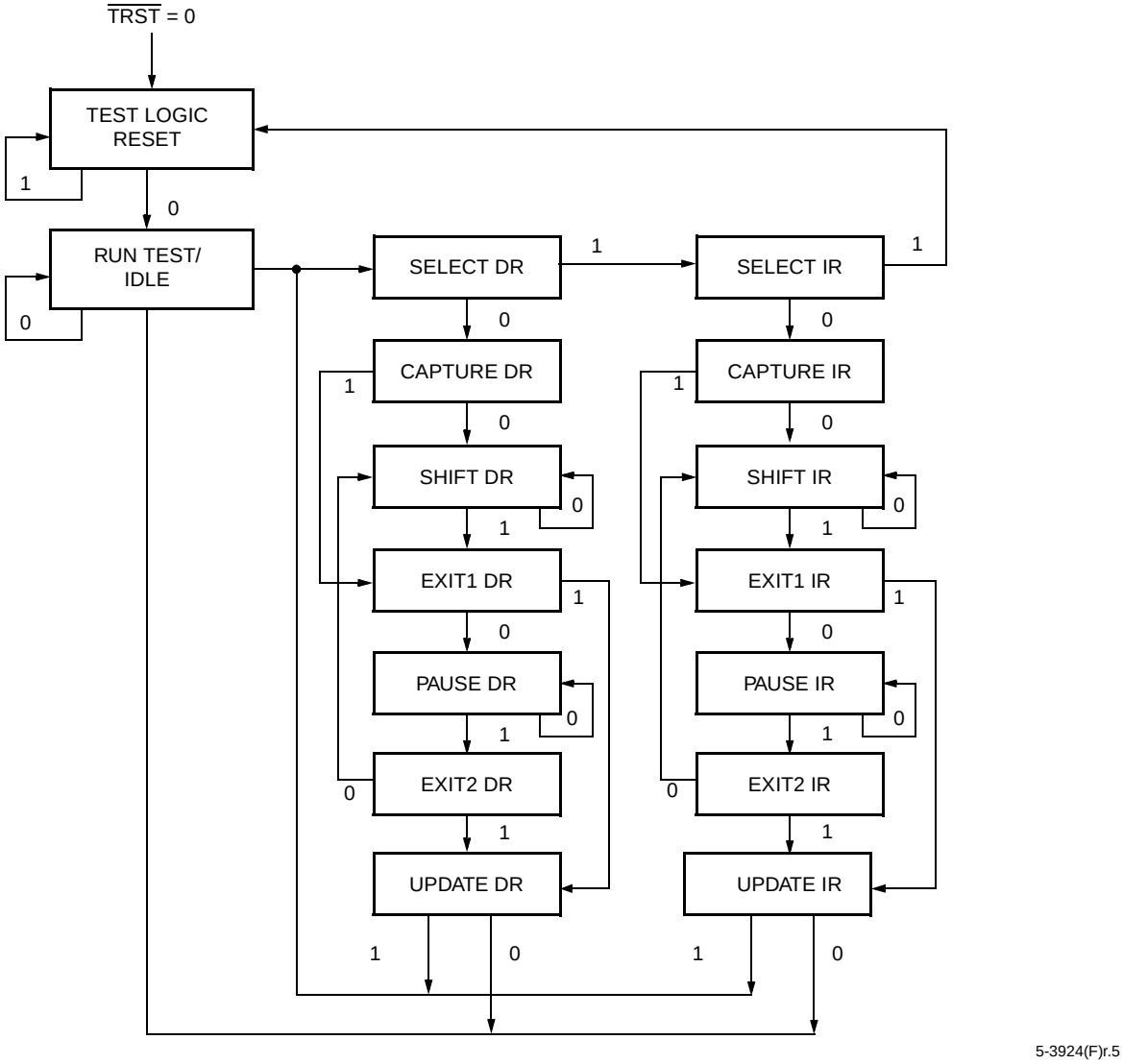


Figure 15. BS TAP Controller State Diagram

The value shown next to each state transition in Figure 15 represents the signal present at TMS at the time of a rising edge at TCK.

The description of the TAP controller states is given in *IEEE* Std. 1149.1-1990 Section 5.1.2 and is reproduced in Table 9 and Table 10.

JTAG Boundary-Scan Specification (continued)

Test Access Port Controller (continued)

Table 9. TAP Controller States in the Data Register Branch

Name	Description
TEST LOGIC RESET	The BS logic is switched in such a way that normal operation of the ASIC is adjusted. The IDCODE instruction is initialized by TEST LOGIC RESET. Irrespective of the initial state, the TAP controller has achieved TEST LOGIC RESET after five control pulses at the latest when TMS = 1. The TAP controller then remains in this state. This state is also achieved when $\overline{TRST}$ = 0.
RUN TEST/IDLE	Using the appropriate instructions, this state can activate circuit parts or initiate a test. All of the registers remain in their present state if other instructions are used.
SELECT DR	This state is used for branching to the test data register control.
CAPTURE DR	The test data is loaded in the test data register parallel to the rising edge of TCK in this state.
SHIFT DR	The test data is clocked by the test data register serially to the rising edge of TCK in the state. The TDO output driver is active.
EXIT (1/2) DR	This temporary state causes a branch to a subsequent state.
PAUSE DR	The input and output of test data can be interrupted in this state.
UPDATE DR	The test data is clocked into the second stage of the test data register parallel to the falling edge of TCK in this state.

Table 10. TAP Controller States in the Instruction Register Branch

Name	Description
SELECT IR	This state is used for branching to the instruction register control.
CAPTURE IR	The instruction code 0001 is loaded in the first stage of the instruction register parallel to the rising edge of TCK in this state.
SHIFT IR	The instructions are clocked into the instruction register serially to the rising edge of TCK in the state. The TDO output driver is active.
EXIT (1/2) IR	This temporary state causes a branch to a subsequent state.
PAUSE IR	The input and output of instructions can be interrupted in this state.
UPDATE IR	The instruction is clocked into the second stage of the instruction register parallel to the falling edge of TCK in this state.

JTAG Boundary-Scan Specification (continued)

Instruction Register

The instruction register (IR) is 4 bits in length. Table 11 shows the BS instructions implemented by the TTSI4K32T.

Table 11. TTSI4K32T's Boundary-Scan Instructions

Instruction	Code	Act. Register TDI→TDO	Mode	Function	Output Defined Via
EXTEST	0000	Boundary Scan	TEST	Test external connections	BS Register
IDCODE	0001	Identification	NORMAL	Read Manuf. Register	Core Logic
HIGHZ	0100	BYPASS	X	3-state	Output—High Impedance
SAMPLE/PRELOAD	0101	Boundary Scan	NORMAL	Sample/load	Core Logic
BYPASS	1111	BYPASS	NORMAL	Min shift path	Core Logic
EVERYTHING ELSE	—	BYPASS	X	—	Output—High Impedance

The instructions not supported in TTSI4K32T are INTEST, RUNBIST, and TOGGLE. A fixed binary 0001 pattern (the 1 into the least significant bit) is loaded into the IR in the CAPTURE IR controller state. The IDCODE instruction (binary 0001) is loaded into the IR during the test-logic-reset controller state and at powerup.

The following is an explanation of the instructions supported by TTSI4K32T and their effect on the devices' pins.

EXTEST:

This instruction enables the path cells, the pins of the ICs, and the connections between ASICs to be tested via the circuit board. The test data can be loaded in the chosen position of the BS register by means of the SAMPLE/PRELOAD instruction. The EXTEST instruction selects the BS register as the test data register. The data at the function inputs is clocked into the BS register on the rising edge of TCK in the CAPTURE DR state. The contents of the BS register can be clocked out via TDO in the SHIFT DR state. The value of the function outputs is solely determined by the contents of the data clocked into the BS register and only changes in the UPDATE DR state on the falling edge of TCK.

IDCODE:

Information regarding the manufacturer's ID for Lucent, the IC number, and the version number can be read out serially by means of the IDCODE instruction. The IDCODE register is selected, and the BS register is set to normal mode in the UPDATE IR state. The IDCODE is loaded at the rising edge of TCK in the CAPTURE DR state. The IDCODE register is read out via TDO in the SHIFT DR state.

HIGHZ:

All 3-statable outputs are forced to a high-impedance state, and all bidirectional ports are forced to an input state by means of the HIGHZ instruction. The impedance of the outputs is set to high in the UPDATE IR state. The function outputs are only determined in accordance with another instruction if a different instruction becomes active in the UPDATE IR state. The BYPASS register is selected as the test data register. The HIGHZ instruction is implemented in a similar manner to that used for the BYPASS instruction.

SAMPLE/PRELOAD:

The SAMPLE/PRELOAD instruction enables all the input and output pins to be sampled during operation (SAMPLE) and the result to be output via the shift chain. This instruction does not impair the internal logic functions. Defined values can be serially loaded in the BS cells via TDI while the data is being output (PRELOAD).

JTAG Boundary-Scan Specification (continued)

Instruction Register (continued)

BYPASS:

This instruction selects the BYPASS register. A minimal shift path exists between TDI and TDO. The BYPASS register is selected after the UPDATE IR. The BS register is in normal mode. A 0 is clocked into the BYPASS register during CAPTURE DR state. Data can be shifted by the BYPASS register during SHIFT DR. The contents of the BS register do not change in the UPDATE DR state. Please note that a 0 that was loaded during CAPTURE DR appears first when the data is being read out.

Boundary-Scan Register

The boundary-scan register is a shift register, whereby one or more BS cells are assigned to every digital TTSI4K32T pin. The TTSI4K32T's boundary-scan register bit-to-pin assignment is defined in the BSDL file, which is available upon request.

BYPASS Register

The BYPASS register is a one-stage shift register that enables the shift chain to be reduced to one stage in the TTSI4K32T.

IDCODE Register

The IDCODE register identifies the TTSI4K32T by means of a parallel, loadable, 32-bit shift register. The code is loaded on the rising edge of TCK in the CAPTURE DR state. The contents of this register is indicated in the BSDL file.

3-State Procedures

The 3-state input participates in the boundary scan. It has a BS cell, but buffer blocking via this input is suppressed for the EXTEST instruction. The 3-state input is regarded as a signal input that is to participate in the connection test during EXTEST. The buffer blocking function should not be active during EXTEST to ensure that the update pattern at the TTSI4K32T outputs does not become corrupted.

Register Architecture

Table 12 is an overview of the register architecture. The table is a summary of the register function and address. Complete detail of each register is given in the following sections.

Table 12. TTSI4K32T Register Summary

Register Name/Function	Register Address (Hex)
Reserved	6000—7FFF
Connection Store Memory	4000—5FFF
Reserved	3000—3FFF
Data Store Memory	2000—2FFF
Reserved	1880—1FFF
Receive Highway 31—Reserved	187F
Receive Highway 31 Configuration Byte 2	187E
Receive Highway 31 Configuration Byte 1	187D
Receive Highway 31 Configuration Byte 0	187C
. . .	. . .
Receive Highway 0—Reserved	1803
Receive Highway 0 Configuration Byte 2	1802
Receive Highway 0 Configuration Byte 1	1801
Receive Highway 0 Configuration Byte 0	1800
Reserved	1080—17FF
Transmit Highway 31—Reserved	107F
Transmit Highway 31 Configuration Byte 2	107E
Transmit Highway 31 Configuration Byte 1	107D
Transmit Highway 31 Configuration Byte 0	107C
. . .	. . .
Transmit Highway 0—Reserved	1003
Transmit Highway 0 Configuration Byte 2	1002
Transmit Highway 0 Configuration Byte 1	1001
Transmit Highway 0 Configuration Byte 0	1000
Reserved	0014—0FFF
Version Register	0013
Test-Pattern Generator Data Register	0012
Test-Pattern Error Counter Byte 1	0011
Test-Pattern Error Counter Byte 0	0010

Register Architecture (continued)

Table 12. TTSI4K32T Register Summary (continued)

Register Name/Function	Register Address (Hex)
Test-Pattern Error Injection Register	000F
Test-Pattern Checker Data Register	000E
Test-Pattern Checker Lower Time-Slot Register	000D
Test-Pattern Checker Upper Time-Slot Register	000C
Test-Pattern Checker Highway Register	000B
Test-Pattern Style Register	000A
Test Command Register	0009
Interrupt Mask Register	0008
Interrupt Status Register	0007
Global Interrupt Mask Register	0006
Idle Code 3 Register	0005
Idle Code 2 Register	0004
Idle Code 1 Register	0003
BIST Command Register	0002
Software Reset Register	0001
General Command Register	0000

Configuration Register Architecture

Note: All registers' bits default to 0 upon reset, unless noted otherwise.

All TDM highway data, which is stored in the TSI, will have the following convention. Bit 7 is first transmitted and first received; bit zero is last transmitted and last received. This convention applies to the data read from the data store, the host data transmitted via the connection store, and any other configuration register which stores highway data, such as the idle code registers and the test-pattern generator data register.

Table 13. General Command Register (0x00)

Bit	Symbol	Name/Description
7	CSV	**Chip Select Valid.** This bit is valid while the TTSI4K32T is in synchronous microprocessor interface mode only. When this bit is programmed to be 1, the chip select input pin is sampled when $\overline{AS}$ is active. When 0, chip select is latched one PCLK after $\overline{AS}$ is active.
6	ED	**External Drivers.** Used to select the use of external drivers on transmit highways. A 0 indicates that no external buffers are being used; therefore, the TXD pins will become 3-stated for time slots that are programmed as such. A 1 indicates that the TXD output highways are connected to external drivers; thus, the TXD pins will always be driven to prevent floating nodes at the inputs of the external drivers. The TXOE[0—31] outputs always reflect the high-impedance status of the corresponding TXD[0—31] highways, regardless of the ED bit setting. The only exception to this is when $\overline{TEST}$ is asserted, which 3-states all outputs. See Table 39, Transmit Highway 3-State Options, on page 50 for other methods of 3-stating the transmit highways.
5	—	**Reserved.** Read as 0.
4	INTOE	**Interrupt Output Enable.** This bit, when set to a 1, enables the INT output signal to be driven based on the status of the internal interrupts and their corresponding individual mask bits. When 0, the output will remain 3-stated.
3	INTP	**Interrupt Polarity.** This bit defines the polarity of INT, as output from the TTSI4K32T. A 1 selects an active-low interrupt output ($\overline{INT}$). A 0 selects an active-high interrupt output (INT), and is the default polarity.
2	FSP	**Frame Sync Polarity.** This bit defines the polarity of FSYNC, as sampled by CK, which designates the beginning of the frame. A 1 selects an active-high frame synchronization (FSYNC). A 0 selects an active-low frame synchronization ($\overline{FSYNC}$).
1	FSSE	**Frame Sync Sample Edge.** This bit selects the clock edge of the CK input that is used to sample the frame synchronization input. A 1 selects the rising edge; and a 0 selects the falling edge of CK.
0	GXE	**Global Transmit Enable.** When 0, all 32 transmit highways are 3-stated. GXE defaults to 0 so that all outputs can be held in a high-impedance state until they have been configured and individually enabled. For other methods of 3-stating transmit highways, see Table 39, Transmit Highway 3-State Options, on page 50.

Configuration Register Architecture (continued)

Table 14. Software Reset Register (0x01)

Bit	Symbol	Name/Description
7—1	—	**Reserved.** Read as 0.
0	SR	**Software Reset.** Writing a 1 to this bit resets the chip. This bit has a function similar to the $\overline{\text{RESET}}$ pin. When set to 1, all registers and control logic will be initialized to their default values except the software reset register. A 0 must be written to this bit in order to clear and release the software reset. The microprocessor interface will not be affected by the software reset, and the write to this bit will terminate normally.

Table 15. BIST Command Register (0x02)

Bit	Symbol	Name/Description
7	RB	**Run BIST.** Writing a 1 to this bit begins the built-in self-test for all internal memory blocks (i.e., the data and connection stores). This bit must be cleared by writing a 0 when BIST is complete. That event is indicated via the BIST complete (BC) bit in the interrupt status register, as well as the BIST done (BD) bit in the BIST command register. Writing a 0 to this bit position will also clear the BD bit. A software reset should be performed after the BIST testing sequence is complete.
6	BD	**BIST Done (Read Only).** This bit indicates when the BIST test is complete. This bit is used for polling to determine the completion of the BIST test. The real-time duration of the TSI BIST test is 2.8 seconds. This bit will remain set to a 1 reflecting the fact that the BIST is complete until the RB bit is written to a 0.
5	BPF	**BIST $\overline{\text{Pass}}$/Fail (Read Only).** This bit indicates the status of the BIST test results. A 0 indicates that no errors were detected.
4—0	—	**Reserved.** Read as 0.

The BIST test sequence is performed as follows:

1. Set RB (bit 7) in the BIST command register to 1 in order to initiate the internal BIST test.
2. Wait for the BIST complete (BC) (bit 1 of the interrupt status register) interrupt to occur via the interrupt status register, if it is not masked via the interrupt mask register MASKBC bit (bit 1). Alternatively, the host can poll the BD bit in the BIST command register which will also indicate the completion of BIST.
3. Once the BIST interrupt occurs or the BD bit is set, the BPF bit in the BIST command register will reflect the BIST pass/fail result. A BPF set to 0 indicates a pass.
4. Set RB (bit 7) in the BIST command register to a 0 in order to end the internal BIST test.
5. Issue a software reset via the SR bit in the software reset register.

During BIST, the TTSI4K32T will corrupt traffic and the contents of the connection store memory. The TTSI4K32T should, therefore, be taken off-line prior to running BIST and reprogrammed afterwards.

Configuration Register Architecture (continued)

Table 16. Idle Code 1 Register (0x03)

Bit	Symbol	Name/Description
7—0	IC1	**Idle Code 1[7—0].** This register is used to identify the data to be sent on any outgoing time slot marked for idle code 1 transmission. Idle code transmission is enabled via the time-slot data select mode bits. See Table 43, Connection Store Memory (Byte 1), on page 52.

Table 17. Idle Code 2 Register (0x04)

Bit	Symbol	Name/Description
7—0	IC2	**Idle Code 2[7—0].** This register is used to identify the data to be sent on any outgoing time slot marked for idle code 2 transmission. Idle code transmission is enabled via the time-slot data select mode bits. See Table 43, Connection Store Memory (Byte 1), on page 52.

Table 18. Idle Code 3 Register (0x05)

Bit	Symbol	Name/Description
7—0	IC3	**Idle Code 3[7—0].** This register is used to identify the data to be sent on any outgoing time slot marked for idle code 3 transmission. Idle code transmission is enabled via the time-slot data select mode bits. See Table 43, Connection Store Memory (Byte 1), on page 52.

Table 19. Global Interrupt Mask Register (0x06)

Bit	Symbol	Name/Description
7—1	—	**Reserved.** Read as 0.
0	GIE	**Global Interrupt Enable.** This bit must be written to a 1 in order for INT to be asserted as a result of the possible interrupt conditions. This is in addition to the mask bits in the interrupt mask register. When 0, the INT output is blocked independent of the programming of the interrupt mask register. When 1, the INT output is enabled and will be asserted based on the interrupt status and mask bits.

Configuration Register Architecture (continued)

Table 20. Interrupt Status Register* (0x07)

Bit	Symbol	Name/Description
7	—	**Reserved.** Read as 0.
6	FSERR	**Frame Sync Error.** When set to 1, this bit indicates that an error related to frame sync has occurred. This error could be a result of a missing FSYNC or a mis-aligned FSYNC.
5	TPD	**Test Pattern Detected.** The TPD bit indicates the state of the test-pattern checker. When TPD = 0, the test-pattern checker **has not** yet located the selected test pattern. When TPD = 1, the test-pattern checker **has** located the selected test pattern. Test-pattern data must be error-free for 32 time slots before it is considered detected. If 32 or more time slots are selected for test-pattern checking, this event could occur within one 125 µs frame. If only two time slots are selected for test-pattern checking, then the test pattern will be detected after 16 frames.
4	—	**Reserved.** Read as 0 or 1.
3	ERD	**Error Detected.** This bit is set to 1 each time an error has been detected in the test pattern once the test pattern has first been detected.
2	—	**Reserved.** Read as 0.
1	BC	**BIST Complete.** When set to 1, this status bit indicates that the BIST sequence is complete.
0	BEI	**Bit Errors Inserted.** When set to 1, this status bit indicates that the request to insert bit errors into the outgoing test pattern is complete.

* Read-only register.

This register is clear on read. Once the status bits are read, they will remain cleared until the next interrupt event occurs. The interrupt mask register in combination with the global interrupt enable GIE (bit 0) in the global interrupt mask register determines when the INT pin gets asserted when an interrupt status bit gets set. In general, the interrupt status register bits will update regardless of the mask bits. The exception to this is the FSERR bit, which will not be set if the corresponding mask bit is set.

Configuration Register Architecture (continued)

Table 21. Interrupt Mask Register (0x08)

Bit	Symbol	Name/Description
7	—	**Reserved.** Read as 0.
6	MASKFS	**Mask Frame Sync Error Interrupt.** Set this bit to a 1 to mask the generation of an interrupt as a result of a frame sync error. Resets to a 1, which prevents the status bit from generating an interrupt. Setting this bit to a 1 also prevents the detection of a frame sync error and, thus, the setting of the FSERR bit in the interrupt status register. This is done to prevent an unintended interrupt at the first FSYNC pulse after the reset sequence.
5	MASKTPD	**Mask Test-Pattern Detection Interrupt.** Set this bit to a 1 to mask the generation of an interrupt as a result of a test-pattern detection. Resets to a 1, which prevents the status bit from generating an interrupt.
4	—	**Reserved.** Read as 1. Always write a 1 to this bit when writing this register.
3	MASKERD	**Mask Error Detected Interrupt.** Set this bit to a 1 to mask the generation of an interrupt as a result of a single bit error detected in the incoming test pattern. Resets to a 1, which prevents the status bit from generating an interrupt.
2	—	**Reserved.** Read as 1. Always write a 1 to this bit when writing this register.
1	MASKBC	**Mask BIST Complete Interrupt.** Set this bit to a 1 to mask the generation of an interrupt as a result of completing the memory BIST. Resets to a 1, which prevents the status bit from generating an interrupt.
0	MASKBEI	**Mask Bit Errors Inserted Interrupt.** Set this bit to a 1 to mask the generation of an interrupt as a result of completing the insertion of all requested bit errors. Resets to a 1, which prevents the status bit from generating an interrupt.

Configuration Register Architecture (continued)

Table 22. Test Command Register (0x09)

Bit	Symbol	Name/Description
7	STTPG	**Start Test-Pattern Generator.** Writing a 1 to this register will cause the generator to start generating a test pattern based on the pattern indicated in the test-pattern style register. Writing a 0 to this register will stop the test-pattern generation and provide the opportunity to change the test-pattern style.
6	STTPC	**Start Test-Pattern Checker.** Writing a 1 to this register will cause the checker to start locking on to a test pattern based on the pattern indicated in the test-pattern style register. Writing a 0 to this register will stop the test-pattern checking and provide the opportunity to change the test-pattern style.
5—4	GENHDR [1—0]	**Test-Pattern Generator Highway Data Rate.** These bits are used to indicate the highway data rate of the transmit highway selected for test-pattern generation. It must match the Tx highway data rate which was set in transmit highway configuration register (byte 2), HDR[1—0] bits. The transmit highway selection for test-pattern generation is done using the connection store. Only one highway at a time can be involved with test-pattern generation. Test-pattern generation and checking does not affect the operation of other time slots or highways. GENHDR1 GENHDR0 0 0 2.048 Mbits/s (default) 0 1 4.096 Mbits/s 1 0 8.192 Mbits/s 1 1 0.000 Mbits/s (idle, not transmitting data)
3—2	CHKHDR [1—0]	**Test-Pattern Checker Highway Data Rate.** These bits are used to indicate the highway data rate of the receive highway selected for test-pattern checking. It must match the Rx highway data rate which was set in receive highway configuration register (byte 2), HDR[1—0] bits. The transmit highway selection for test-pattern generation is done using the test-pattern checker highway register. Only one highway at a time can be involved with test-pattern checking. Test-pattern generation and checking does not affect the operation of other time slots or highways. CHKHDR1 CHKHDR0 0 0 2.048 Mbits/s (default) 0 1 4.096 Mbits/s 1 0 8.192 Mbits/s 1 1 0.000 Mbits/s (idle, not receiving data)
1—0	—	**Reserved.** Read as 0.

Configuration Register Architecture (continued)

Table 23. Test-Pattern Style Register (0x0A)

<table>
<tr><th>Bit</th><th>Symbol</th><th>Name/Description</th></tr>
<tr><td>7—4</td><td>TPS[3—0]</td><td>Generator Test-Pattern Style[3—0]. These 4 bits determine the type of test pattern that will be generated by the on-line maintenance test-pattern generator.

TPS3 TPS2 TPS1 TPS0 Test-Pattern Description
0 0 0 0 MARK (all 1s) (AIS - red alarm)
0 0 0 1 QRSS (2^{20} – 1 with zero suppression) (O.151)
0 0 1 0 31(2^5 – 1) PRBS
0 0 1 1 63(2^6 – 1) PRBS
0 1 0 0 511(2^9 – 1) PRBS (O.153)
0 1 0 1 511(2^9 – 1) PRBS (reversed)
0 1 1 0 2047(2^{11} – 1) PRBS (O.152)
0 1 1 1 2047(2^{11} – 1) PRBS (reversed)
1 0 0 0 2^{15} – 1 PRBS (O.151) (noninverted)
1 0 0 1 2^{20} – 1 PRBS (O.153)
1 0 1 0 2^{20} – 1 PRBS (reversed)
1 0 1 1 2^{23} – 1 PRBS (V.33) (noninverted)
1 1 0 0 1:1 (alternating 1s and 0s).
1 1 0 1 Reserved.
1 1 1 0 Reserved.
1 1 1 1 Fixed. User-defined byte, stored in the test-pattern generator data register will be sent.

PRBS = pseudorandom binary sequence.
QRSS = quasi-random signal source.</td></tr>
<tr><td>3—0</td><td>CPS[3—0]</td><td>Checker Test-Pattern Style[3—0]. These 4 bits determine the type of test pattern that will be detected by the on-line maintenance test-pattern checker.

CPS3 CPS2 CPS1 CPS0 Test-Pattern Description
0 0 0 0 MARK (all 1s) (AIS - red alarm)
0 0 0 1 QRSS (2^{20} – 1 with zero suppression) (O.151)
0 0 1 0 31(2^5 – 1) PRBS
0 0 1 1 63(2^6 – 1) PRBS
0 1 0 0 511(2^9 – 1) PRBS (O.153)
0 1 0 1 511(2^9 – 1) PRBS (reversed)
0 1 1 0 2047(2^{11} – 1) PRBS (O.152)
0 1 1 1 2047(2^{11} – 1) PRBS (reversed)
1 0 0 0 2^{15} – 1 PRBS (O.151) (noninverted)
1 0 0 1 2^{20} – 1 PRBS (O.153)
1 0 1 0 2^{20} – 1 PRBS (reversed)
1 0 1 1 2^{23} – 1 PRBS (V.33) (noninverted)
1 1 0 0 1:1 (alternating 1s and 0s).
1 1 0 1 Reserved.
1 1 1 0 Reserved.
1 1 1 1 Fixed. The checker will compare against the user-defined byte, stored in the test-pattern checker data register.

PRBS = pseudorandom binary sequence.
QRSS = quasi-random signal source.</td></tr>
</table>

Configuration Register Architecture (continued)

Table 24. Test-Pattern Checker Highway Register (0x0B)

Bit	Symbol	Name/Description
7—5	—	**Reserved.**
4—0	CHS[4—0]	**Checker Highway Select[4—0].** These 5 bits determine the receive highway to which the test-pattern checker is connected.

Table 25. Test-Pattern Checker Upper Time-Slot Register (0x0C)

Bit	Symbol	Name/Description
7	—	**Reserved.**
6—0	CKRUP[6—0]	**Checker Upper Time-Slot Select[6—0].** These 7 bits determine the upper time slot in the input highway to which the test-pattern checker is connected. All contiguous time slots that lie between the lower and upper time-slot boundaries inclusive are monitored for the test pattern. The range of time slots that can be monitored is from 1 time slot to the entire span (32, 64, and 128 time slots for a 2.048 Mbits/s, 4.096 Mbits/s, 8.192 Mbits/s highway, respectively). If one time slot is to be monitored, then CKRUP and CKRLOW should be set to the same value.

Table 26. Test-Pattern Checker Lower Time-Slot Register (0x0D)

Bit	Symbol	Name/Description
7	—	**Reserved.**
6—0	CKRLOW [6—0]	**Checker Lower Time-Slot Select[6—0].** These 7 bits determine the lower time slot in the input highway to which the test-pattern checker is connected. All contiguous time slots that lie between the lower and upper time-slot boundaries inclusive are monitored for the test pattern. The range of time slots that can be monitored is from 1 time slot to the entire span (32, 64, and 128 time slots for a 2.048 Mbits/s, 4.096 Mbits/s, 8.192 Mbits/s highway, respectively). If one time slot is to be monitored, then CKRUP and CKRLOW should be set to the same value.

Table 27. Test-Pattern Checker Data Register (0x0E)

Bit	Symbol	Name/Description
7—0	CTP[7—0]	**Checker Test Pattern[7—0].** The data written here will be used for comparison when the fixed mode is programmed into the test-pattern style register.

Table 28. Test-Pattern Error Injection Register (0x0F)

Bit	Symbol	Name/Description
7—0	BEC[7—0]	**Bit Error Count[7—0].** This register is used to indicate the number of single bit errors that are to be injected into the outgoing test pattern (QRSS, PRBS, or fixed user-defined byte). This register can be programmed to inject up to 255 bit errors. The BEI bit in the interrupt status register will indicate when all of the errors have been injected. BEC[7—0] will automatically be reset when BEI is set. In order to send out additional errors, BEC[7—0] should be rewritten. Errors are injected at the rate of one per time slot.

Configuration Register Architecture (continued)

Table 29. Test-Pattern Error Counter (Byte 0) (0x10)*

Bit	Symbol	Name/Description
7—0	EC[7—0]	**Error Counter[7—0].** Least significant bits of 16-bit error counter. See note below for resetting counter.

* Read-only register.

Table 30. Test-Pattern Error Counter (Byte 1) (0x11)*

Bit	Symbol	Name/Description
7—0	EC[15—8]	**Error Counter[15—8].** Most significant bits of 16-bit error counter. See note below for resetting counter.

* Read-only register.

Note: The error counter will be incremented each time a bit error is detected by the pattern checker.

In order to ensure that the correct value is read from these registers, byte 0 must be read first followed by byte 1. This action will latch the error counter value and allow the counter to be reset and continue recording as time proceeds.

Table 31. Test-Pattern Generator Data Register (0x12)

Bit	Symbol	Name/Description
7—0	GTP[7—0]	**Generator Test Pattern[7—0].** The data written here will be sent out repeatedly if the fixed data test-pattern mode is selected in the test-pattern style register.

Table 32. Version Register (0x13)*

Bit	Symbol	Name/Description
7—2	—	**Reserved.**
1—0	VER[1—0]	**Version Number.** Read as 00†.

* Read-only register.
† Reading a 00 from this register indicates version number 1.0.

Configuration Register Architecture (continued)

Table 33. Transmit Highway Configuration Register (Byte 0) (0x1000 + 4i)*

Bit	Symbol	Name/Description
7	—	**Reserved.** Read as 0.
6—4	XBITOFF [2—0]	**Transmit Highway Bit Offset[2—0].** XBITOFF is used to offset the beginning of an outgoing frame by the indicated number of bit times. If no bit offsets are required, these bits should be set to 000. The following list shows the effect of setting these bits. 000 = no bit offset 001 = 1-bit offset 010 = 2-bit offset . . . 111 = 7-bit offset **Note:** Bit periods are relative to the highway data rate set for each highway. XTSOFF, XBITOFF, and XFBOFF are used in conjunction to define the start of the outgoing frame. The values are added together to position the sampling of time slot 0, bit 0 for each highway.
3—2	XFBOFF [1—0]	**Transmit Highway Fractional Bit Offset[1—0].** XFBOFF is used to offset the beginning of an outgoing frame by the indicated number of fractional bit times. If no fractional bit offsets are required, these bits should be set to 00. The following list shows the effect of these bits. 00 = no fractional bit offset 01 = 1/4-bit fractional offset 10 = 1/2-bit fractional offset 11 = 3/4-bit fractional offset **Note:** Bit periods are relative to the highway data rate set for each highway. XTSOFF, XBITOFF, and XFBOFF are used in conjunction to define the start of the outgoing frame. The values are added together to position the sampling of time slot 0, bit 0 for each highway.
1—0	—	**Reserved.** Must be written to 00.

* i = the transmit highway number.

Configuration Register Architecture (continued)

Table 34. Transmit Highway Configuration Register (Byte 1) (0x1001 + 4i)*

Bit	Symbol	Name/Description
7	—	**Reserved.** Read as 0.
6—0	XTSOFF [6—0]	**Transmit Highway Time-Slot Offset[6—0].** XTSOFF is used to offset the beginning of an outgoing frame by the indicated number of time slots (bytes). If no time-slot offsetting is required, these bits should be set to zero. The following table shows the range of offsets for the different highway data rates. Highway Data Rate — Time-Slot Offset Range 2.048 Mbits/s — 0—31 4.096 Mbits/s — 0—63 8.192 Mbits/s — 0—127 **Note:** A time slot is always 8 bits. A bit period is relative to the highway data rate set for each highway. XTSOFF, XBITOFF, and XFBOFF are used in conjunction to define the start of the outgoing frame. The values are added together to position the transmission of time slot 0, bit 0.

* i = the transmit highway number.

Table 35. Transmit Highway Configuration Register (Byte 2) (0x1002 + 4i)*

Bit	Symbol	Name/Description
7—3	—	**Reserved.** Read as 0.
2	XE	**Transmit Highway 3-State Enable**. The associated output highway is high impedance when this bit is 0 (default after reset). When this bit is set to 1, the output driver is enabled. The effect of this bit is dependent on the status of the external drive bit of the general command register. See Table 13, General Command Register (0x00), on page 37 for details. For other methods of 3-stating transmit highways, see Table 39, Transmit Highway 3-State Options, on page 50.
1—0	HDR[1—0]	**Transmit Highway Data Rate[1—0].** HDR1 — HDR0 0 — 0 — 2.048 Mbits/s (default) 0 — 1 — 4.096 Mbits/s 1 — 0 — 8.192 Mbits/s 1 — 1 — 0.000 Mbits/s (idle, not transmitting data)

* i = the transmit highway number.

Note: During CK input interruptions (e.g., clock switching), the transmit highways should be 3-stated by clearing the GXE (bit 0) of the general command register. The highways can be enabled by writing a 1 to the GXE bit once the PLL has regained lock (250 µs later).

Configuration Register Architecture (continued)

Table 36. Receive Highway Configuration Register (Byte 0) (0x1800 + 4i)*

Bit	Symbol	Name/Description
7	—	**Reserved.** Read as 0.
6—4	RBITOFF [2—0]	**Receive Highway Bit Offset[2—0].** RBITOFF is used to offset the beginning of an incoming frame by the indicated number of bit times. If no bit offsets are required, these bits should be set to 000. The following list shows the effect of setting these bits. 000 = no bit offset 001 = 1-bit offset 010 = 2-bit offset . . . 111 = 7-bit offset **Note:** Bit periods are relative to the highway data rate set for each highway. RTSOFF, RBITOFF, and RFBOFF are used in conjunction to define the start of the incoming frame. The values are added together to position the sampling of time slot 0, bit 0 for each highway.
3—2	RFBOFF [1—0]	**Receive Highway Fractional Bit Offset[1—0].** RFBOFF is used to offset the beginning of an incoming frame by the indicated number of fractional bit times. If no fractional bit offsets are required, these bits should be set to 00. The following list shows the effect of these bits. 00 = no fractional bit offset 01 = 1/4-bit fractional offset 10 = 1/2-bit fractional offset 11 = 3/4-bit fractional offset **Note:** Bit periods are relative to the highway data rate set for each highway. RTSOFF, RBITOFF, and RFBOFF are used in conjunction to define the start of the incoming frame. The values are added together to position the sampling of time slot 0, bit 0 for each highway.
1—0	—	**Reserved.** (Read/Write) Must be written to 00.

* i = the receive highway number.

Configuration Register Architecture (continued)

Table 37. Receive Highway Configuration Register (Byte 1) (0x1801 + 4i)*

Bit	Symbol	Name/Description
7	—	**Reserved.** Read as 0.
6—0	RTSOFF [6—0]	**Receive Highway Time-Slot Offset[6—0].** RTSOFF is used to offset the beginning of an incoming frame by the indicated number of time slots (bytes). If no time-slot offsetting is required, these bits should be set to zero. The following table shows the range of offsets for the different highway data rates. Highway Data Rate — Time-Slot Offset Range 2.048 Mbits/s — 0—31 4.096 Mbits/s — 0—63 8.192 Mbits/s — 0—127 **Note:** A time slot is always 8 bits. A bit period is relative to the highway data rate set for each highway. RTSOFF, RBITOFF, and RFBOFF are used in conjunction to define the start of the incoming frame. The values are added together to position the sampling of time slot 0, bit 0.

* i = the receive highway number.

Table 38. Receive Highway Configuration Register (Byte 2) (0x1802 + 4i)*

Bit	Symbol	Name/Description
7—3	—	**Reserved.** Read as 0.
2	LC	**Loopback Control.** This bit is used to control the internal loopback of the TXD highway to the corresponding RXD highway. When set to 1, the TXD highway as input to this RXD highway. The transmit highway involved will be internally looped back to the matching receive highway so that the TXD[i] output is now the input to RXD[i]. When a particular highway is in this mode, the receive highway offset must be 1/2-bit greater than the corresponding transmit highway offset. When LC is cleared to 0, the RXD pin is the source of highway data (default).
1—0	HDR[1—0]	**Receive Highway Data Rate[1—0].** HDR1 — HDR0 0 — 0 — 2.048 Mbits/s (default) 0 — 1 — 4.096 Mbits/s 1 — 0 — 8.192 Mbits/s 1 — 1 — 0.000 Mbits/s (idle, not receiving data)

* i = the receive highway number.

Configuration Register Architecture (continued)

Transmit Highway 3-State Options

There are several ways of 3-stating the transmit highways:

$\overline{\text{TEST}}$ (active-low) is the input pin that 3-states all outputs and bidirectional pins of the device.

GXE (bit 0) (active-high) is the global transmit enable bit in the general command register. It applies to all transmit highways.

XE (bit 2) (active-high) is the transmit highway 3-state enable bit in the transmit highway configuration register (byte 2). There is a separate XE bit for each one of the 32 transmit highways.

ED (bit 6) (active-high) is the external drivers bit in the general command register. This bit applies to all the transmit highways. It affects the 3-stating of the transmit highways. Time slots that are selected to be 3-stated, by setting the TSDSM[2—0] bits to 0x7 in byte 2 of the connection store, will be driven with random data if ED = 1. Otherwise, these time slots will be 3-stated.

Table 39. Transmit Highway 3-State Options

$\overline{\text{TEST}}$ (Input Pin)	GXE (Cfg Bit)	ED (Cfg Bit)	XE for Transmit Highway [i] (Cfg Bit)	TXD[0—31] Pins	TXOE[0—31] Pins
0	X	X	X	All high impedance.	All high impedance.
1	0	0	X	All high impedance.	All 0.
1	0	1	X	All driven with random data.	All 0.
1	1	0	0	TXD[i] = high impedance.	TXOE[i] = 0.
1	1	0	1	TXD[i] = 0, 1, or high impedance according to connection store programming.	TXOE[i] = 0 or 1, representing high-impedance state according to connection store programming.
1	1	1	0	TXD[i] is driven with random data.	TXOE[i] = 0.
1	1	1	1	TXD[i] = 0 or 1 reflecting the correct transmit data. Time slots which are selected for high-impedance mode via the connection store will be driven with random data and not 3-stated.	TXOE[i] = 0 or 1, representing high-impedance state according to connection store programming.

Data Store Memory

Microprocessor access to the incoming highway data is provided by directly reading the data store memory. Each one of the time slots is addressable by constructing the address in the following way. Microprocessor reads to this address space will occur immediately. Microprocessor writes to this address space will not change the contents of the data store. If user data is to be sent out on a particular time slot, the host data substitution mode in the connection store should be used.

Table 40. Address Scheme for Data Store Memory

Data Store Memory Address	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	1	0	Receive Highway Number (0—31)					Receive Time-Slot Address (0—127)						

To illustrate the addressing scheme, consider the following examples:

To read the data received in time slot 7 on RXD6, the following address is used to access the TSI data store memory location.

A[14—0] = 010_00110_0000111 = 0x2307

Note: All TDM highway data which is stored in the TSI will have the following convention. The most significant bit of a byte is first transmitted and first received, the least significant bit is last transmitted and last received. This convention applies to the data read from the data store, the host data transmitted via the connection store, and any other configuration register that stores highway data.

Connection Store Memory

The connection store memory is primarily used to set up the switching matrix and selects the transmit data source for each one of the outgoing time slots. There are two connection store byte locations associated with each one of the outgoing time slots. The address for each of the corresponding connection store memory locations is constructed in the following way.

Table 41. Address Scheme for Connection Store Memory

Connection Store Memory Address	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	0	Transmit Highway Number (0—31)					Transmit Time-Slot Address (0—127)							Byte 0, 1 Select

If any particular transmit highway is not programmed to use the total available bandwidth (8.192 Mbits/s), then the connection store memory locations representing the unused time slots are not used. For example, assume highway 7 is set for a highway data rate of 4.096 Mbits/s. This translates to a total of 64 time slots being transmitted on highway 7. In that case, addresses A[14—0] = 0x4700—0x477F must be set. Addresses A[14—0] = 0x4780—0x47FF are irrelevant for a 4.096 Mbits/s highway and need not be set.

The connection store memory does not have a default state. Therefore, after powerup, the relevant locations in the connection store must be programmed. However, the connection store contents are not affected by a software or hardware reset of the TTSI4K32T.

Connection Store Memory (continued)

Table 42. Connection Store Memory (Byte 0)

Bit	Symbol	Name/Description
7—0	RTSA[6—0]/ HSD[7—0]	**Receive Time-Slot Address[6—0]/Host Substituted Data [7—0].** If low-latency or frame-integrity time-slot data select modes are selected for the particular transmit time slot being configured, then these bits are used to indicate the receive time-slot address from which the transmit time-slot data is sourced. Bit 7 should be set to 0. If the host data substitution mode is selected for the particular transmit time slot being configured, then these 8 bits will represent the data byte to be transmitted. These bits are not valid for time-slot data select modes 3—7.

Table 43. Connection Store Memory (Byte 1)

Bit	Symbol	Name/Description
7—5	TSDSM[2—0]	**Time-Slot Data Select Mode[2—0]** 0 0 0 Low-latency mode. 0 0 1 Frame-integrity mode. 0 1 0 Host data substitution mode. 0 1 1 Idle code 1 substitution mode. 1 0 0 Idle code 2 substitution mode. 1 0 1 Idle code 3 substitution mode. 1 1 0 Test-pattern substitution mode—test pattern is selected via test-pattern style register. 1 1 1 High-impedance mode.
4—0	RXHWY [4—0]	**Receive Highway Number.** Used to select the receive highway from which the outgoing time-slot data is sourced. These bits are only valid for time-slot data select modes 0 and 1.

To illustrate the connection store programming scheme, consider the following example:

To configure the transmission of time slot 7 on TXD6, the following addresses are used to access the relevant TSI connection store memory locations.

A[14—0] = 10_00110_0000111_0 = 0x460E—to access byte 0

A[14—0] = 10_00110_0000111_1 = 0x460F—to access byte 1

Now, if it is desired to send Rx time slot 4 from RXD3 to time slot 7 on TXD6 in frame integrity mode, then the following data should be written to the above addresses.

Data byte 0 = 0_0000100 = 0x04

Data byte 1 = 001_00011 = 0x23

Thus, to map Rx time slot 4 from RXD3 to Tx time slot 7 on TXD6, in frame integrity mode, the following two TSI writes must be performed.

Write location 0x460E with 0x04

Write location 0x460F with 0x23

Connection Store Memory (continued)

TSDSM[5—0] (bits 7—5) of byte 1 of the connection store select the source of data for each of the time slots being transmitted by the TTSI4K32T. The configuration can be divided into three groups.

Group 1 **Low-Latency Mode.** For the time slots marked as low latency, the transmit data will be retrieved from the data store based on the programming of TSA[6—0] (bits 6—0) of byte 0 and RXHWY[4—0] (bits 4—0) of byte 1. Bit 7 of byte 0 is ignored. When each of the individual transmit time slots are retrieved from the data store memory for transmission, the most recent copy of the receive time slot will be fetched resulting in a latency that never exceeds 134 µs. This is the maximum latency for low-latency mode independent of highway configurations (e.g., highway speed, clock speed, offsets, etc.). Refer to the Low-Latency and Frame-Integrity Modes section on page 24 for a detailed description of the latency calculation.

Frame-Integrity Mode. For the time slots marked as frame integrity, the transmit data will be retrieved from the data store based on the programming of TSA[6—0] (bits 6—0) of byte 0 and RXHWY[4—0] (bits 4—0) of byte 1. Bit 7 of byte 0 is ignored. Any number of time slots from any number of transmit highways can be marked for frame integrity. When each of the individual transmit time slots marked for frame integrity are retrieved from the data-store memory for transmission, the internal controller ensures that they are chosen from a receive frame which has already been entirely stored in the data store, thereby ensuring frame integrity.

Refer to the Low-Latency and Frame-Integrity Modes section on page 24 for a detailed description of the actual latency incurred through the device.

Group 2 **Host-Data Substitution Mode.** This mode also provides the means to transmit host-supplied data repeatedly onto any or all of the 4096 transmit time slots; however, the data to be substituted is stored in HSD[7—0] (bits 7—0) of byte 0 for each transmit time slot. RXHWY[4—0] (bits 4—0) of byte 1 are ignored in this mode. Host-data mode can be used to customize the data for each of the 4096 transmit time slots. When a time slot is configured for host-data substitution mode, the data written to byte 0 of the connection store will have the following convention. Bit 7 is first transmitted, and bit 0 is last transmitted.

Idle-Code Substitution Mode. These three idle-code substitution modes provide the means to transmit microprocessor data repeatedly onto any or all of the 4096 transmit time slots. Three idle-code registers (separate from the connection store memory) provide the capability to repeatedly broadcast three different programmed values to any or all time slots set for idle-code substitution mode. When programming idle-code substitution mode, only the TSDSM[2—0] (bits 7—5) of byte 1 for all of the transmit time slots involved needs to be written. Byte 0 and RXHWY[4—0] (bits 4—0) of byte 1 are both ignored.

Test-Pattern Substitution Mode. This mode is also used to substitute alternative transmit data rather than use the receive time slots being stored in the data store. Since the test-pattern selection is done outside of the connection store, only TSDSM[2—0] (bits 7—5) of byte 1 for each of the time slots involved needs to be programmed. Byte 0 and RXHWY[4—0] (bits 4—0) of byte 1 are both ignored. The test-pattern selection and usage rules are described in the Test-Pattern Generation section on page 28.

Group 3 **High-Impedance Mode.** This mode is used to 3-state any of the 4096 transmit time slots on an individual basis. For example, consider the case where an 8.192 Mbits/s highway is shared by four devices, each having one-fourth of the total bandwidth. If the TTSI4K32T were allocated time slots 64—95, then high-impedance mode would be set for time slots 0—63 and 96—127. Time slots 64—95 could be set to any combination of the eight possible modes. When programming the high-impedance mode, only TSDSM[2—0] (bits 7—5) of byte 1 for all of the transmit time slots involved needs to be written. Connection store byte 0 and RXHWY[4—0] (bits 4—0) of byte 1 are both ignored.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability. External leads can be safely soldered or bonded at temperatures up to 300 °C.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	–65	125	°C
Voltage on Any Pin with Respect to Ground	V_{IN}	–0.5	5.8*	V
Power Dissipation	P_D	—	460	mW

* This maximum rating only applies when the device is powered up with V_{DD}.

Operating Conditions

Parameter	Symbol	Min	Max	Unit
Power Supply	V_{DD}	2.97	3.63	V
Low-level Input Voltage	V_{IL}	—	0.8	V
High-level Input Voltage	V_{IH}	2.1	5.8	V
Ambient Operating Temperature Range	T_A	–40	85	°C

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison. The HBM ESD threshold presented here was obtained by using these circuit parameters:

Human-Body Model ESD Threshold	
Device	**Voltage**
TTSI4K32T	>1000 V

Electrical Characteristics

T_A = –40 °C to +85 °C; V_{DD} = 3.3 V ± 10%; V_{SS} = 0 V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current:						
Non-pull-up Pins	I_{IL}	$V_{SS} < V_{IN} < V_{DD}$ ± 10%	—	—	10	µA
Pull-up Pins	I_{IL}	$V_{IN} = V_{SS}$	—	—	60	µA
Non-pull-up I/O Pins	I_{IL}	$V_{SS} < V_{IN} < V_{DD}$ ± 10%	—	—	70	µA
Pull-down Pins	I_{IL}	$V_{IN} = V_{DD}$ ± 10%	—	—	300	µA
Output Voltage:						
Low:	V_{OL}					
DT, D[7—0]		I_{OL} = –10 mA	—	—	0.4	V
TXD[31—0], TXOE[31—0]		I_{OL} = –6 mA	—	—	0.4	V
TDO, INT		I_{OL} = –2 mA	—	—	0.4	V
High:	V_{OH}					
DT, D[7—0]		I_{OH} = 10 mA	2.4	—	—	V
TXD[31—0], TXOE[31—0]		I_{OH} = 6 mA	2.4	—	—	V
TDO, INT		I_{OH} = 2 mA	2.4	—	—	V
Load Capacitance:						
DT, D[7—0], INT	C_L	—	—	—	50	pF
TXD[31—0]	C_L	—	—	—	25	pF
TXOE[31—0]	C_L	—	—	—	20	pF
TDO	C_L	—	—	—	70	pF

Timing Characteristics

T_A = –40 °C to +85 °C; V_{DD} = 3.3 V ± 10%; V_{SS} = 0 V

The following timing characteristics are generated for the TTL input and output levels.

Table 44. Clock Specifications

Pin Name	Frequency	Duty Cycle	Clock Period Stability	Rise Time (max)	Fall Time (max)
PCLK	0 MHz—65 MHz	50% ± 10%	—	—	—
CK	2.048 MHz	50% ± 10%	±64 ns	10 ns	10 ns
	4.096 MHz	50% ± 10%	±32 ns	10 ns	10 ns
	8.192 MHz	50% ± 10%	±16 ns	10 ns	10 ns
	16.384 MHz	50% ± 10%	±8 ns	10 ns	10 ns
TCK	10 MHz	50% ± 10%	—	—	—

Timing Characteristics (continued)

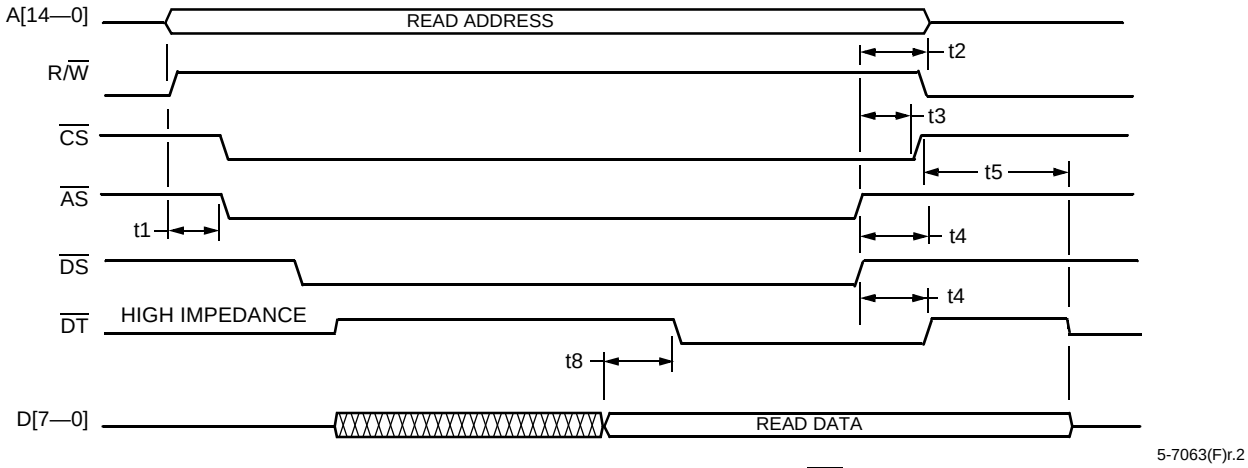


Figure 16. Asynchronous Read Cycle Timing Using $\overline{DT}$ Handshake

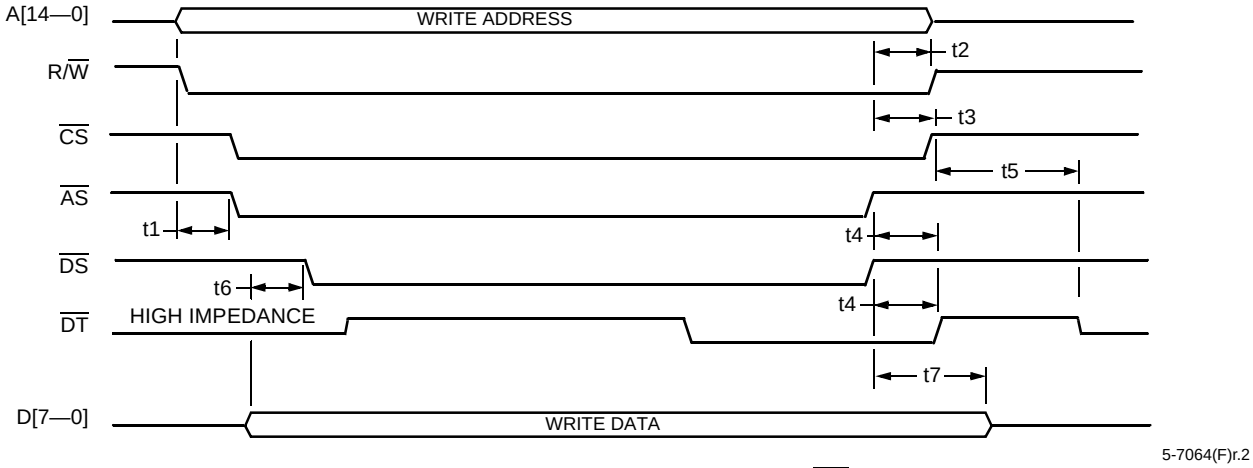


Figure 17. Asynchronous Write Cycle Timing Using $\overline{DT}$ Handshake

Table 45. Asynchronous Read and Write Interface Timing Using $\overline{DT}$ Handshake

Symbol	Description	Min	Max	Unit
t1	A[14—0] or R/$\overline{W}$ Setup to $\overline{AS}$	0	—	ns
t2	A[14—0] or R/$\overline{W}$ Hold from $\overline{AS}$	0	—	ns
t3	$\overline{CS}$ Hold from $\overline{AS}$ or $\overline{DS}$	4*	—	ns
t4	$\overline{DT}$ Output Delay from $\overline{AS}$ or $\overline{DS}$ (C_L = 50 pF)	3*	8*	ns
t5	$\overline{DT}$ or D[7—0] High-impedance from $\overline{CS}$ (C_L = 50 pF)	—	8.5*	ns
t6	D[7—0] Input Setup to $\overline{DS}$ (C_L = 50 pF)	0	—	ns
t7	D[7—0] Input Hold from $\overline{DS}$ (C_L = 50 pF)	0	—	ns
t8	D[7—0] Output Setup Prior to $\overline{DT}$ Output (C_L = 50 pF)	0	—	ns

* $\overline{CS}$ asynchronously controls the output enable of D[7—0] and $\overline{DT}$. The delay from $\overline{CS}$ to the output enable of $\overline{DT}$ is equivalent to the delay from $\overline{AS}$ or $\overline{DS}$ to $\overline{DT}$. Therefore, in order to guarantee that $\overline{DT}$ is driven high before being 3-stated, a $\overline{CS}$ hold time is required (t3). If this timing cannot be met, then there are two options. One, disconnect $\overline{DT}$ and rely on wait-states to terminate the cycle. The read or write cycle will be completed by the device 183 ns after the start of the cycle, which is defined by $\overline{CS}$, $\overline{AS}$, and $\overline{DS}$ all being active. The second option is to use an external pull-up on $\overline{DT}$ to pull $\overline{DT}$ high within the timing requirements of the microprocessor.

Timing Characteristics (continued)

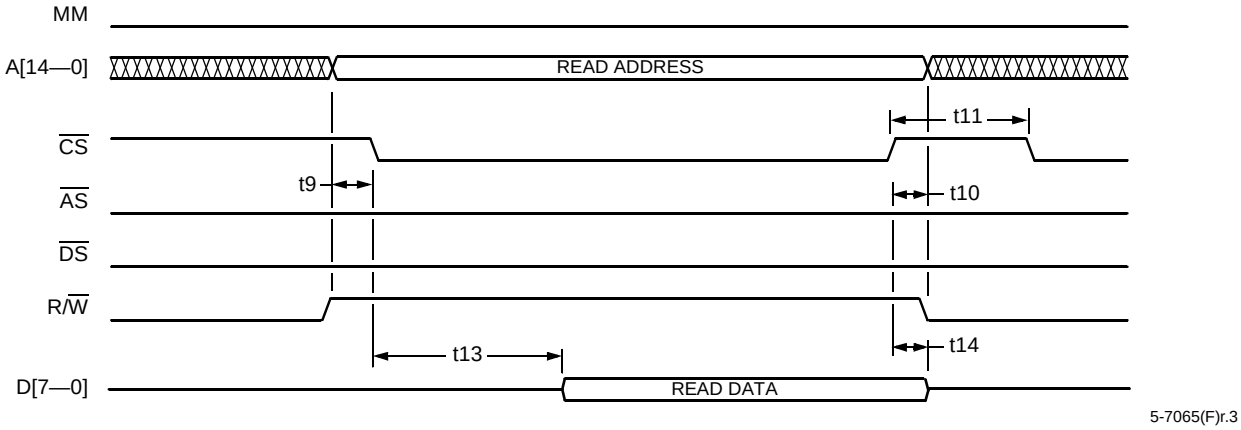


Figure 18. Asynchronous Read Cycle Timing Using Only $\overline{CS}$

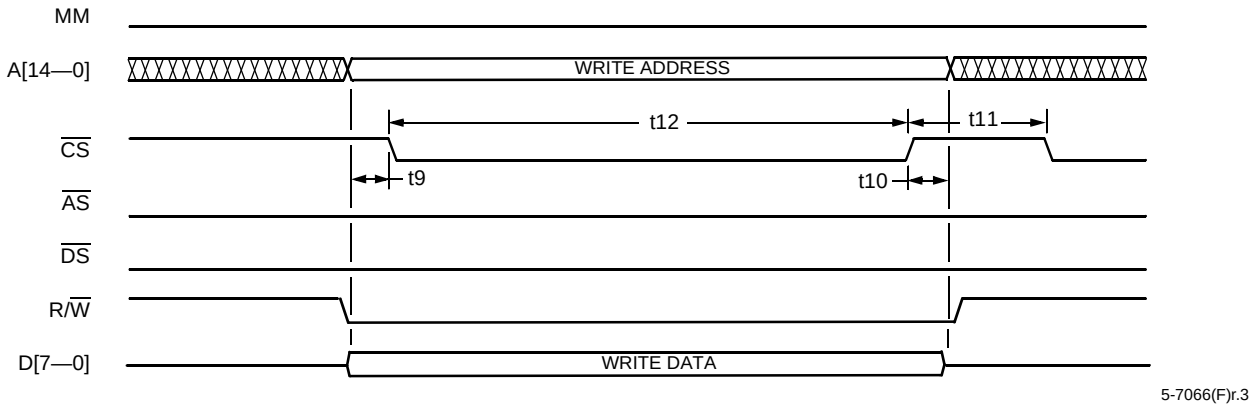


Figure 19. Asynchronous Write Cycle Timing Using Only $\overline{CS}$

Table 46. Asynchronous Microprocessor Interface Timing Using Only $\overline{CS}$

Symbol	Description	Min	Max	Unit
t9	A[14—0], R/$\overline{W}$, D[7—0] Input Setup to $\overline{CS}$	0	—	ns
t10	A[14—0], R/$\overline{W}$, D[7—0] Input Hold from $\overline{CS}$	0	—	ns
t11	Pulse Width of $\overline{CS}$ Inactive	100	—	ns
t12	Pulse Width of $\overline{CS}$ Active	200	—	ns
t13	D[7—0] Output Delay from $\overline{CS}$ (C_L = 50 pF)	—	200	ns
t14	D[7—0] Output Hold from $\overline{CS}$ (C_L = 50 pF)	0	—	ns

Timing Characteristics (continued)

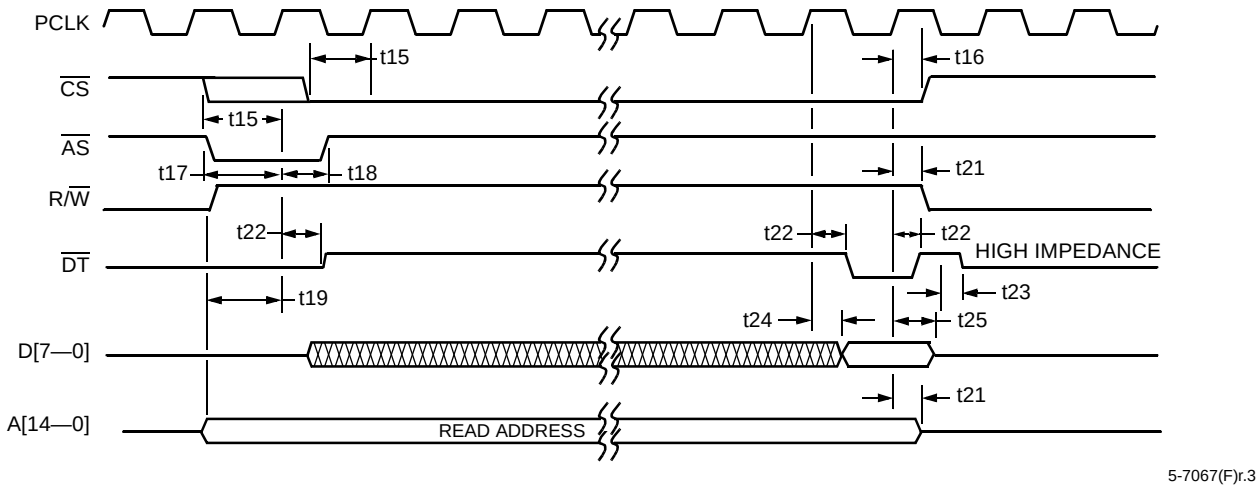


Figure 20. Synchronous Read Cycle Timing

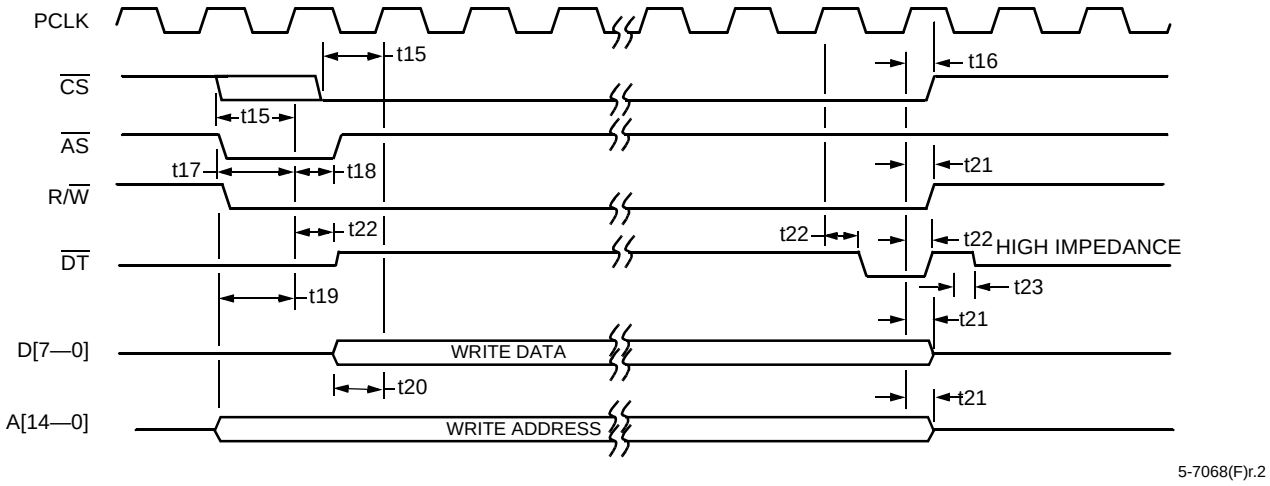


Figure 21. Synchronous Write Cycle Timing

Timing Characteristics (continued)

Table 47. Synchronous Microprocessor Interface Timing

Symbol	Description	Min	Max	Unit
t15	$\overline{CS}$ Setup to Rising PCLK Edge	10*	—	ns
t16	$\overline{CS}$ Hold from Rising PCLK Edge	0	—	ns
t17	$\overline{AS}$ Setup to Rising PCLK Edge	6	—	ns
t18	$\overline{AS}$ Hold from Rising PCLK Edge	0	—	ns
t19	R/$\overline{W}$, A[14—0] Input Setup to Rising PCLK Edge	0	—	ns
t20	D[7—0] Input Setup to Rising PCLK Edge	0†	—	ns
t21	R/$\overline{W}$, A[14—0], D[7—0] Input Hold from Rising PCLK Edge	0	—	ns
t22	$\overline{DT}$ Output Delay from Rising PCLK Edge (C_L = 10 pF to 50 pF)	2.6	10	ns
t23	$\overline{DT}$ High Impedance from Falling PCLK Edge (C_L = 50 pF)	—	7	ns
t24	D[7—0] Output Delay from Rising PCLK Edge (C_L = 50 pF)	—	0‡	ns
t25	D[7—0] Output High Impedance from Rising PCLK Edge (C_L = 10 pF to 50 pF)	4	12	ns

* The $\overline{CS}$ setup timing requirement relative to PCLK can be programmed for either the first or second clock cycle of a microprocessor access using CSV (bit 7) of the general command register.

† The input setup timing requirement assumes a PCLK frequency of at least 25 MHz. For frequencies slower than 25 MHz, the D[7—0] propagation delay must be less than 40 ns from the rising edge of PCLK which samples $\overline{AS}$.

‡ When data is driven by the TSI during a synchronous read cycle, good data is driven prior to $\overline{DT}$ being asserted.

Timing Characteristics (continued)

TDM highway timing is shown below for the following scenario (i = 0, 1, 2 . . . 31; j = 0, 1, 2 . . . 31):

- The input CK speed is set to 8.192 MHz.
- FSYNC is programmed to be active-high and sampled by a rising edge of CK.
- The RXD[i] highway is set for 0-bit offset and a highway data rate of 4.096 Mbits/s.
- The TXD[j] highway is set for 0-bit offset and a highway data rate of 8.192 Mbits/s.

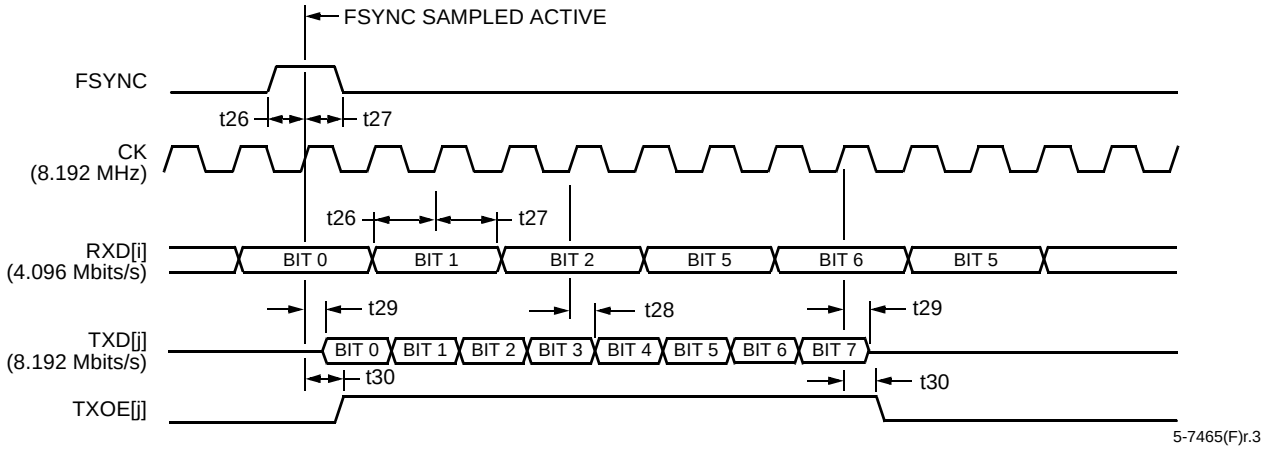


Figure 22. TDM Highway Timing

Table 48. TDM Highway Timing

Symbol	Description	Min	Max	Unit
t26	FSYNC, RXD[0—31] Setup to Active CK Edge	10	—	ns
t27	FSYNC, RXD[0—31] Hold from Active CK Edge	5	—	ns
t28	TXD[0—31] Delay from Active CK Edge (C_L = 25 pF)	5	15	ns
t29	TXD[0—31] High Impedance (C_L = 25 pF)	—	15	ns
t30	TXOE[0—31] Delay from Active CK Edge (C_L = 20 pF)	5	15	ns

The TDM highway timing numbers, t26—t30, also apply for all other cases as well, i.e.,

- CK speed is 2.048 MHz, 4.096 MHz, or 16.384 MHz.
- FSYNC is sampled on the falling edge of CK.
- FSYNC is active-low.
- RXD[i] is sampled on the falling edge of CK.
- RXD[i] data rate is 2.048 Mbits/s or 8.192 Mbits/s.
- TXD[j] is driven on the falling edge of CK.
- TXD[j] data rate is 2.048 Mbits/s or 4.096 Mbits/s.
- TXOE[j] is driven on the falling edge of CK. TXOE[j] is driven on the same edge as TXD[j].

Timing Characteristics (continued)

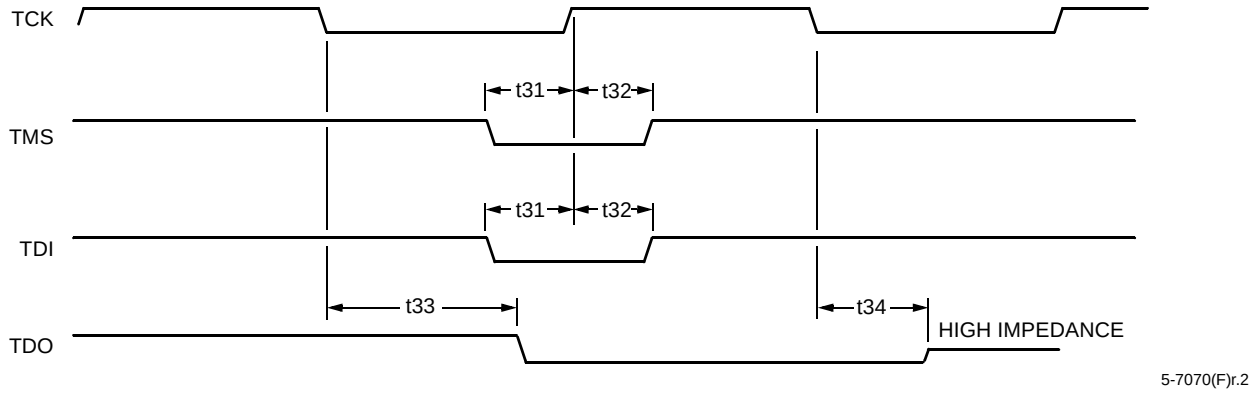


Figure 23. JTAG Interface Timing

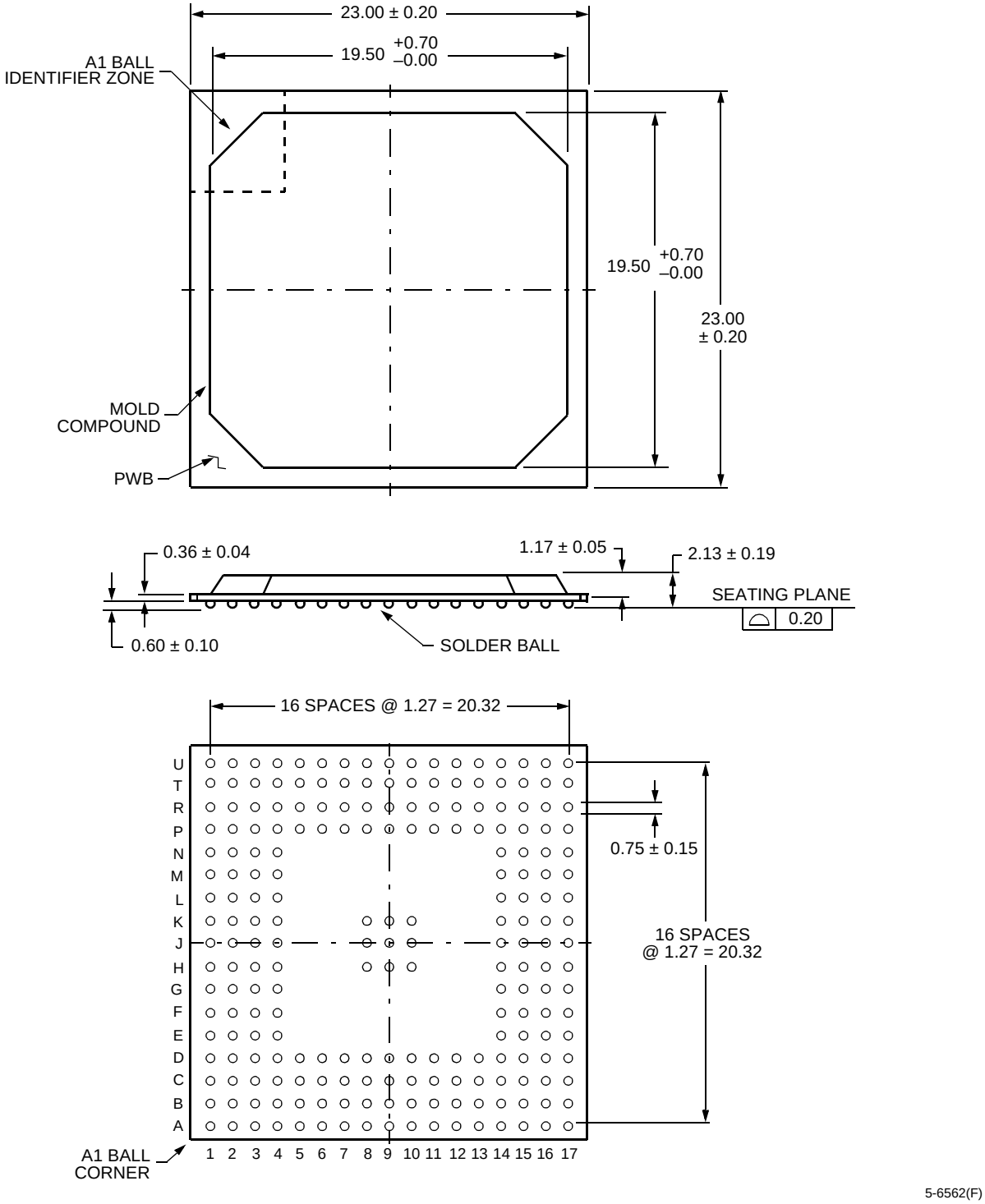
Table 49. JTAG Interface Timing

Symbol	Description	Min	Max	Unit
t31	TDI, TMS Setup to Rising TCK Edge	10	—	ns
t32	TDI, TMS Hold from Rising TCK Edge	—	10	ns
t33	TDO Delay from Falling TCK Edge (C_L = 70 pF)	5	35	ns
t34	TDO High Impedance from Falling TCK Edge (C_L = 70 pF)	—	35	ns

Outline Diagram

217-Pin PBGA

Dimensions are in millimeters.



5-6562(F)

Ordering Information

Device Code	Package	Temperature	Comcode (Ordering Number)
TTSI4K32T3BAL	217-pin PBGA	–40 °C to +85 °C	108246844

DS99-178PDH Replaces DS98-291TIC to Incorporate the Following Updates

1. Page 8, Pin D17, added overline to show active-low ($\overline{\text{TRST}}$).
2. Page 8, removed duplicate E1, E2, E3, E4, E14, E15, E16, and E17 pins.
3. Page 21, updated Figure 10, Virtual and Physical Frames on page 21.
4. Page 23, Reset Sequence section, added paragraph on BIST requirement.
5. Page 24—page 27, Low-Latency and Frame-Integrity Modes section updated.
6. Page 28, Test-Pattern Generation section updated.
7. Page 28 and page 29, Test-Pattern Checking section updated.
8. Page 37, Table 13, General Command Register (0x00), removed last sentence in description of bit 2 and bit 1.
9. Page 37, Table 13, General Command Register (0x00), updated bit 0 symbol from GXEN to GXE.
10. Page 38, Table 14, Software Reset Register (0x01), updated bit 0, software reset description.
11. Page 40, Table 20, Interrupt Status Register (0x07), updated bit 4 and bit 2 to reserved status.
12. Page 41, Table 21, Interrupt Mask Register (0x08), updated bit 4 and bit 2 to reserved status.
13. Page 41, Table 21, Interrupt Mask Register (0x08), bit 3 symbol changed from MASKED to MASKERD.
14. Page 43, Table 23, Test-Pattern Style Register (0x0A), updated test-pattern descriptions.
15. Page 44, Table 25, Test-Pattern Checker Upper Time-Slot Register (0x0C), updated description.
16. Page 44, Table 26, Test-Pattern Checker Lower Time-Slot Register (0x0D), updated description.
17. Page 44, Table 28, Test-Pattern Error Injection Register (0x0F), changed register name from test-pattern error selection register to test-pattern error injection register and added sentence to end of description.
18. Page 46, Table 33, Transmit Highway Configuration Register (Byte 0) (0x1000 + 4i), updated bit 3—bit 2 symbol from XCEOFF to XFBOFF.
19. Page 47, Table 35, Transmit Highway Configuration Register (Byte 2) (0x1002 + 4i), updated bit 2 symbol name from XEN to XE.
20. Page 48, Table 36, Receive Highway Configuration Register (Byte 0) (0x1800 + 4i), updated bit 3—bit 2 symbol from RCEOFF to RFBOFF.
21. Page 50, Transmit Highway 3-State Options section and Table 39, Transmit Highway 3-State Options updated.
22. Page 51, Data Store Memory section updated.
23. Page 52, Table 42, Connection Store Memory (Byte 0), changed TSA symbol to RTSA and updated description.
24. Page 52, Table 43, Connection Store Memory (Byte 1), changed PORTNUM symbol to RXHWY.
25. Page 51—page 53, Connection Store Memory section updated.
26. Page 54, Absolute Maximum Ratings table, power dissipation, P_D, updated from 450 mW to 460 mW.
27. Page 55, Table 44, Clock Specifications, updated clock period stability for CK.
28. Page 60, Timing Characteristics section, updated Figure 22, TDM Highway Timing and text.
29. Page 60, Table 48, TDM Highway Timing, timing parameter t26, minimum changed from 15 ns to 10 ns.

For additional information, contact your Microelectronics Group Account Manager or the following:

INTERNET: **http://www.lucent.com/micro**

E-MAIL: **docmaster@micro.lucent.com**

N. AMERICA: Microelectronics Group, Lucent Technologies Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18109-2386
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)

ASIA PACIFIC: Microelectronics Group, Lucent Technologies Singapore Pte. Ltd., 77 Science Park Drive, #03-18 Cintech III, Singapore 118256
Tel. (65) 778 8833, FAX (65) 777 7495

CHINA: Microelectronics Group, Lucent Technologies (China) Co., Ltd., A-F2, 23/F, Zao Fong Universe Building, 1800 Zhong Shan Xi Road, Shanghai 200233 P. R. China **Tel. (86) 21 6440 0468**, **ext. 325**, FAX (86) 21 6440 0652

JAPAN: Microelectronics Group, Lucent Technologies Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
Tel. (81) 3 5421 1600, FAX (81) 3 5421 1700

EUROPE: Data Requests: MICROELECTRONICS GROUP DATALINE: **Tel. (44) 1189 324 299**, FAX (44) 1189 328 148
Technical Inquiries: GERMANY: **(49) 89 95086 0** (Munich), UNITED KINGDOM: **(44) 1344 865 900** (Ascot),
FRANCE: **(33) 1 40 83 68 00** (Paris), SWEDEN: **(46) 8 594 607 00** (Stockholm), FINLAND: **(358) 9 4354 2800** (Helsinki),
ITALY: **(39) 02 6608131** (Milan), SPAIN: **(34) 1 807 1441** (Madrid)

Lucent Technologies Inc. reserves the right to make changes to the product(s) or information contained herein without notice. No liability is assumed as a result of their use or application. No rights under any patent accompany the sale of any such product(s) or information.

Copyright © 2000 Lucent Technologies Inc.
All Rights Reserved

June 2000
DS00-322PDH (Replaces DS99-178PDH)

microelectronics group

Lucent Technologies
Bell Labs Innovations

