

Oscillator THT, programmable

APQO 14

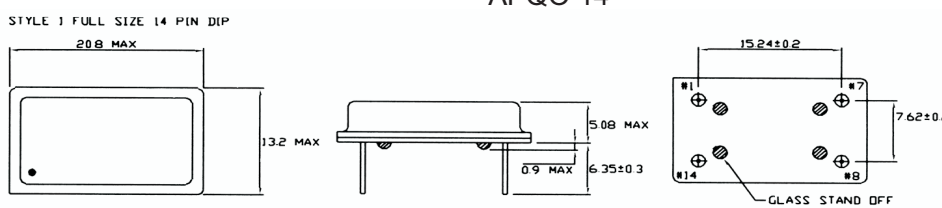
Features:

- Standard DIL 14 package
- Low cost to performance
- 3.0 ~ 5.5 volt available
- Tolerance and stability to $\pm 25\text{ppm}$
- Ultra low jitter <11ps
- Tristate or power down available



Specifications		
	APQO 14	Remarks
Frequency range	1 ~ 133MHz	Please specify
Frequency stability	$\pm 25\text{ppm} \sim \pm 100\text{ppm}$	Please specify
Operating temperature	$0^{\circ}\text{C} \sim +70^{\circ}\text{C} - -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$	Please specify
Storage temperature	$-55^{\circ}\text{C} \sim +125^{\circ}\text{C}$	
Programmable voltage 1 ~ 133 MHz	4.5V ~ 5.5V	
Programmable voltage 1 ~ 100 MHz	3.0V ~ 3.6V	
Aging (ppm / Year), Ta = 25C, Vdd = 5 / 3.3 V	$\pm 5\text{ppm}$	
Programmable output level	CMOS / TTL	

Operating conditions			
Description	Min	Max	Unit
Vdd Supply voltage	3.0	5.5	V
CTTL Max capacitive load on outputs for TTL levels			
4.5 V ~ 5.5 V Vdd 40 MHz		50	pF
4.5 V ~ 5.5 V Vdd > 40 ~ 133 MHz		25	pF
Ccmos Max capacitive load on outputs for CMOS levels			
4.5 V ~ 5.5 V Vdd 66 MHz		50	pF
4.5 V ~ 5.5 V Vdd > 66 ~ 133 MHz		25	pF
3.0 V ~ 3.6 V Vdd 40 MHz		30	pF
3.0 V ~ 3.6 V Vdd > 40 ~ 100 MHz		15	pF

Drawing	
<p style="text-align: center;">APQO 14</p>  <p>PIN FUNCTION</p> <ul style="list-style-type: none"> 1 CONTROL 2 GND 3 OUTPUT 4 Vdd <p style="text-align: right;">Dimensions in mm</p>	

Order key							
O	- 50.000000M	- APQO 14	- 50	- 5.0	- A	/ T	/
Part	Frequency	Type/Package	Tolerance	Voltage	Temperature	Option	Packaging
O=Oscillator	M=MHz	APQO=programmable QO 14=DIL 14	$\pm\text{ppm}$	5.0=5.0Volt 3.3=3.3Volt	A= $0^{\circ}\text{C} \sim +70^{\circ}\text{C}$ B= $-10^{\circ}\text{C} \sim +60^{\circ}\text{C}$ C= $-10^{\circ}\text{C} \sim +70^{\circ}\text{C}$ D= $-20^{\circ}\text{C} \sim +70^{\circ}\text{C}$ E= $-40^{\circ}\text{C} \sim +85^{\circ}\text{C}$	T = Tristate P = Power down	blank = Tube

Oscillator THT, programmable

APQO 14

Electrical characteristics					
Discription	Test conditions	Min	Typ	Max	Unit
Input characteristics (Pin 1)					
V _{IL} , Low-level input voltage	4.5 ~ 5.5 V V _{dd}			0.8	V
TO Tri-state or power-down	3.0 ~ 3.6 V V _{dd}			0.2 V _{dd}	V
V _{IH} , High-level input voltage	4.5 ~ 5.5 V V _{dd}	2.0			V
TO Enable output or no connect	3.0 ~ 3.6 V V _{dd}	0.7 V _{dd}			V
I _{IL} , Input low current	V _{IN} = 0V			10	μA
I _{IH} , Input high current	V _{IN} = V _{dd}			5	μA
Output characteristics					
V _{OL} , Low-level output voltage	4.5 V ~ 5.5 V V _{dd} , 16 mA I _{OL}			0.4	V
	3.0 V ~ 3.6 V V _{dd} , 8 mA I _{OL}			0.4	V
V _{OHTTL} , High-level output voltage TTL	4.5 V ~ 5.5 V V _{dd} , -16 mA I _{OL}	2.4			V
V _{OHC} MOS	4.5 ~ 5.5 V _{dd} , -16 mA I _{OL}	V _{dd} - 0.4			V
High-level CMOS voltage	3.0 V ~ 3.6 V V _{dd} , -8 mA I _{OL}	V _{dd} - 0.4			V
Power supply current (unloaded)	4.5 ~ 5.5 V _{dd} , OUTPUT FREQ 133 MHz			45	mA
	3.0 ~ 3.6 V _{dd} , OUTPUT FREQ 100 MHz			25	mA
Standby current			10	50	μA
Input pull-up resistor (PIN 1)	4.5 ~ 5.5 V _{dd} , V _{IN} = 0V	1.1	3.0	8.0	MΩ
	4.5 ~ 5.5 V _{dd} , V _{IN} = 0.7 V	50	100	200	KΩ
Tri-state leakage current	5.0 V _{dd}		20		μA
Output enable mode	Output is tri-stated				
Power down mode	Output is tri-stated				

Output clock switching characteristics					
Description	Test conditions	Min	Typ	Max	Unit
Duty cycle					
TTL @ 1.4 V	50 MHz, C _L = 50 pF	45		55	%
4.5 ~ 5.5 V _{dd}	50 ~ 66 MHz, C _L = 15 pF	45		55	%
	66 ~ 125 MHz, C _L = 25 pF	40		60	%
	125 ~ 133 MHz, C _L = 15 pF	40		60	%
Duty cycle: CMOS @ V _{dd} / 2					
4.5 ~ 5.5 V _{dd}	66 MHz, C _L 25 pF	45		55	%
3.0 ~ 3.6 V _{dd}	66 ~ 125 MHz, C _L 25 pF	40		60	%
	125 ~ 133 MHz, C _L 15 pF	40		60	%
	40 MHz, C _L 30 pF	45		55	%
	40 ~ 100 MHz, C _L 15 pF	40		60	%
Output clock rise / fall					
	0.8 V ~ 2.0 V, 4.5 ~ 5.5 V _{dd} , C _L = 50			1.8	ns
	0.8 V ~ 2.0 V, 4.5 ~ 5.5 V _{dd} , C _L = 25			1.2	ns
	0.8 V ~ 2.0 V, 4.5 ~ 5.5 V _{dd} , C _L = 15			0.9	ns
	0.2 ~ 0.8 V _{dd} , 4.5 ~ 5.5 V _{dd} , C _L = 50			3.4	ns
	0.2 ~ 0.8 V _{dd} , 3.0 ~ 3.6 V _{dd} , C _L = 30			4.0	ns
	0.2 ~ 0.8 V _{dd} , 3.0 ~ 3.6 V _{dd} , C _L = 15			2.4	ns
Start up time	From power on			2	ms
Power down delay time					
Synchronous	PWR_DWN pin LOW to output Hi-Z		T / 2	T+10	ns
Asynchronous			10	15	ns
Output disable time					
Synchronous	OE pin LOW to output Hi-Z		T / 2	T+10	ns
Asynchronous	T = Frequency oscillator period		10	15	ns
Output enable time				100	ns
Period Jitter: Σ	1 - 133 MHz		8	11	ps
Peak to peak	33.000 MHz		65	99	ps
	> 33.000 MHz		65	80	ps