Low Voltage, 300-MHz - 3 dB Bandwidth, SPDT Analog Switch with Power Down Protection

(2:1 Multiplexer/Demultiplexer Bus Switch)

DESCRIPTION

The DG3157A, DG3157B are high-speed single-pole double-throw, low voltage switch. Using sub-micro CMOS technology, the DG3157A, DG3157B achieves low on-resistance and negligible propagation delay. The DG3157A, DG3157B can handle both analog and digital signals and permits signals with amplitudes of up to V_{CC} to be transmitted in either direction. Select pin of control logic input can be over the V+. When the select pin is low, B_0 is connected to the output A pin. When the select pin is high, B_1 is connected to the output A pin. The path that is open will have a high-impedance state with respect to the output A pin. Break before make is guaranteed. The DG3157A has an internal pull down resistor on the control pin S, while the DG3157B does not.

FEATURES

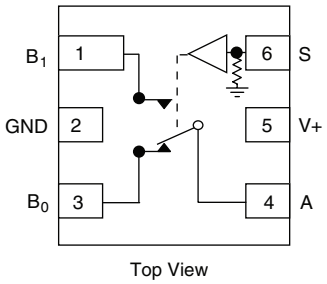
- Ultra small miniQFN6 package of 1 mm x 1.2 mm
- Wide operation voltage range: 1.8 V to 5.5 V
- Useful in both analog and digital signal switching
- 300 MHz - 3 dB bandwidth
- Power down safe design
- Low voltage logic threshold: V_{th}(high) = 1.2 V at V+ = 3.3 V
- Minimal propagation delay
- Break-before-make switching
- Zero bounce in flow-through mode
- > 300 mA latch up current per JESD78
- > 8 kV ESD/HBM
- DG3157A version has internal pull down resistor on control pin S

Pb-free Available

RoHS* COMPLIANT

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

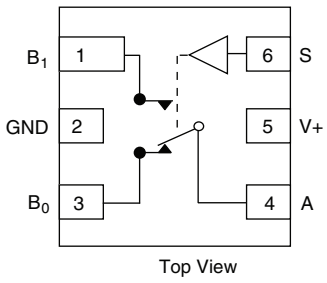
miniQFN-6
DG3157A



Top View

Device Marking: E

miniQFN-6
DG3157B



Top View

Device Marking: D

TRUTH TABLE	
Logic Input (S)	**Function**
0	B_0 Connected to A
1	B_1 Connected to A

ORDERING INFORMATION		
Temp. Range	**Package**	**Part Number**
- 40 °C to 85 °C	miniQFN-6	DG3157ADN-T1-E4
		DG3157BDN-T1-E4

* Pb containing terminations are not RoHS compliant, exemptions may apply.

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Reference V+ to GND		- 0.3 to + 6	V
S, A, B[a]		- 0.3 to (V+ + 0.3)	
Continuous Current (Any terminal)		± 50	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 200	
Storage Temperature	D-Suffix	- 65 to 150	°C
Power Dissipation (Packages)[b]	miniQFN-6[c]	160	mW

Notes:
a. Signals on A, or B or S exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 2.0 mW/°C above 70 °C.

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 3.0 V, V_{SL} = 0.5 V, V_{SH} = 2.0 V[e]		Temp.[a]	Limits - 40 °C to 85 °C Min.[b]	Typ.[c]	Max.[b]	Unit
DC Characteristics								
High Level Input Voltage	V_{SH}	V+ = 1.65 to 1.95 V		Full	1.2			V
		V+ = 2.0 to 2.6 V			1.4			
		V+ = 2.7 to 3.6 V			2.0			
		V+ = 4.5 to 5.5 V			2.4			
Low Level Input Voltage	V_{SL}	V+ = 1.65 to 1.95 V					0.3	
		V+ = 2.0 to 2.6 V					0.4	
		V+ = 2.7 to 3.6 V					0.5	
		V+ = 4.5 to 5.5 V					0.8	
On-Resistance	R_{ON}	V+ = 4.5 V	V_{BN} = 0 V, I_A = 30 mA	Full		4.8	7	Ω
			V_{BN} = 2.4 V, I_A = - 30 mA			5.7	12	
			V_{BN} = 4.5 V, I_A = - 30 mA			10.3	15	
		V+ = 3.0 V	V_{BN} = 0 V, I_A = 24 mA			5.9	9	
			V_{BN} = 3.0 V, I_A = - 24 mA			13.7	20	
		V+ = 2.3 V	V_{BN} = 0 V, I_A = 8 mA			7	12	
			V_{BN} = 2.3 V, I_A = - 8 mA			16.2	30	
		V+ = 1.65 V	V_{BN} = 0 V, I_A = 4 mA			9.2	20	
			V_{BN} = 1.65 V, I_A = - 4 mA			24	50	
On-Resistance Flatness	R_{FLAT}	0 < V_{BN} < V+	V+ = 4.5 V, I_A = - 30 mA	Room		8		
			V+ = 3.0 V, I_A = - 24 mA			13		
			V+ = 2.3 V, I_A = - 8 mA			24		
			V+ = 1.65 V, I_A = - 4 mA			89		
On-Resistance Matching Between Channels	ΔR_{ON}	V+ = 4.5 V, V_{BN} = 3.15 V, I_A = - 30 mA				0.8		
		V+ = 3.0 V, V_{BN} = 2.1 V, I_A = - 24 mA				0.1		
		V+ = 2.3 V, V_{BN} = 1.6 V, I_A = - 8 mA				0.2		
		V+ = 1.65 V, V_{BN} = 1.15 V, I_A = - 4 mA				0.9		
Input Leakage Current	I_S	V+ = 5.5 V, V_A = 5.5 V, V_S = 0.8 V, 2.4 V	DG3157B	Full	- 1.0		1.0	µA
			DG3157A		- 1.0	2.5	7.0	
Off Stage Switch Leakage	$I_{BN(off)}$	V+ = 5.5 V, V_A/V_B = 0 V/5.5 V		Room Full	- 0.1 - 1.0		0.1 1.0	
On State Switch Leakage	$I_{BN(on)}$	V+ = 5.5 V, V_A/V_B = 0 V/5.5 V		Room Full	- 0.1 - 1.0		0.1 1.0	

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 3.0 V, V_{SL} = 0.5 V, V_{SH} = 2.0 V[e]		Temp.[a]	Limits - 40 °C to 85 °C Min.[b]	Typ.[c]	Max.[b]	Unit
Power Supply								
Power Supply Range	V+			Full	1.65		5.5	V
Quiescent Supply Current	I+	V+ = 5.5 V, V_A = V+ or GND		Room Full			1 10	µA
AC Electrical Characteristice								
Prop Delay Time[f]	t_{PHL}/t_{PLH}	V_A = 0 V	V+ = 1.65 to 1.95 V	Full		1.5		ns
			V+ = 2.3 to 2.7 V	Full		0.8		
			V+ = 3.0 to 3.6 V	Full		0.4		
			V+ = 4.5 to 5.5 V	Full		0.3		
Output Enable Time[f]	t_{PZL}/t_{PZH}	V_{LOAD} = 2 x V+ for t_{PZL} V_{LOAD} = 0 V for t_{PZH}	V+ = 1.65 to 1.95 V	Room Full		27	50	
			V+ = 2.3 to 2.7 V	Room Full		15	45	
			V+ = 3.0 to 3.6 V	Room Full		10	30	
			V+ = 4.5 to 5.5 V	Room Full		7	25	
Output Disable Time[f]	t_{PLZ}/t_{PHZ}	V_{LOAD} = 2 x V+ for t_{PLZ} V_{LOAD} = 0 V for t_{PHZ}	V+ = 1.65 to 1.95 V	Room Full		16	45	
			V+ = 2.3 to 2.7 V	Room Full		10	40	
			V+ = 3.0 to 3.6 V	Room Full		8	35	
			V+ = 4.5 to 5.5 V	Room Full		6	21	
Break-Before-Make Time[d]	t_{BBM}	V+ = 1.65 to 1.95 V		Full	0.5	11		
		V+ = 2.3 to 2.7 V		Full	0.5	6		
		V+ = 3.0 to 3.65		Full	0.5	4		
		V+ = 4.5 to 5.5 V		Full	0.5	3		
Charge Injection[d]	Q	C_L = 1 nF, V_{GEN} = 0 V R_{GEN} = 0 Ω	V+ = 5 V	Room		7		pC
			V+ = 3.3 V	Room		5		
Off Isolation[d]	OIRR	R_L = 50 Ω, f = 10 MHz		Room		- 57		dB
Crosstalk[d]	X_{TALK}			Room		- 64		
- 3 dB Bandwidth[d]	BW	R_L = 50 Ω		Room		300		MHz
Total Harmonic Distortion[d]	THD	R_L = 600 Ω, 0.5 Vp-p f = 600 Hz - 20 kHz		Room		0.016		%
Capacitance								
Control Pin Capacitance[d]	C_S	V+ = 0 V		Room		3.7		pF
B Port Off Capacitance[d]	C_{IO-B}	V+ = 5 V		Room		7		
A Port Capacitance When Switch Enable[d]	$C_{IO-A(on)}$			Room		19		

Notes:

a. Room = 25 °C, Full = as determined by the operating suffix.

b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

c. Typical values are for design aid only, not guaranteed nor subject to production testing.

d. Guarantee by design, nor subjected to production test.

e. V_S = input voltage to perform proper function.

f. Guaranteed by design and not production tested. The bus switch propagation delay is a function of the RC time constant contributed by the on-resistance and the specified load capacitance with an ideal voltage source (zero output impedance) driving the switch.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

LOGIC DIAGRAM Positive Logic

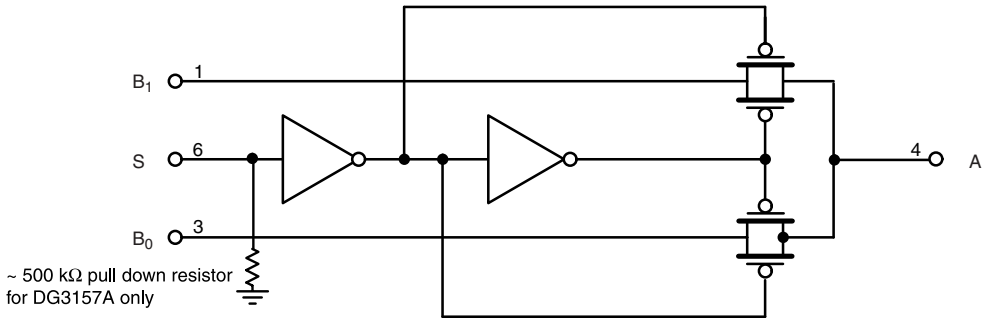
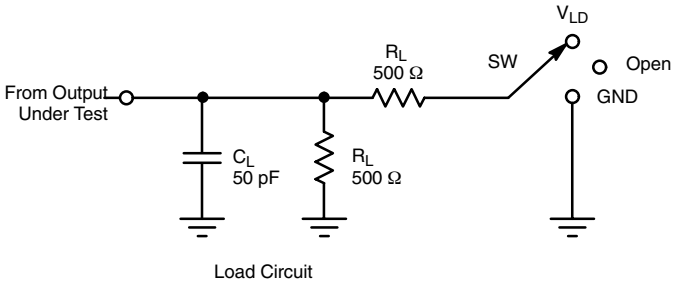


Figure 1.

AC LOADING AND WAVEFORMS



TEST	SW
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LD}
t_{PHZ}/t_{PZH}	GND

Figure 2. AC Test Circuit

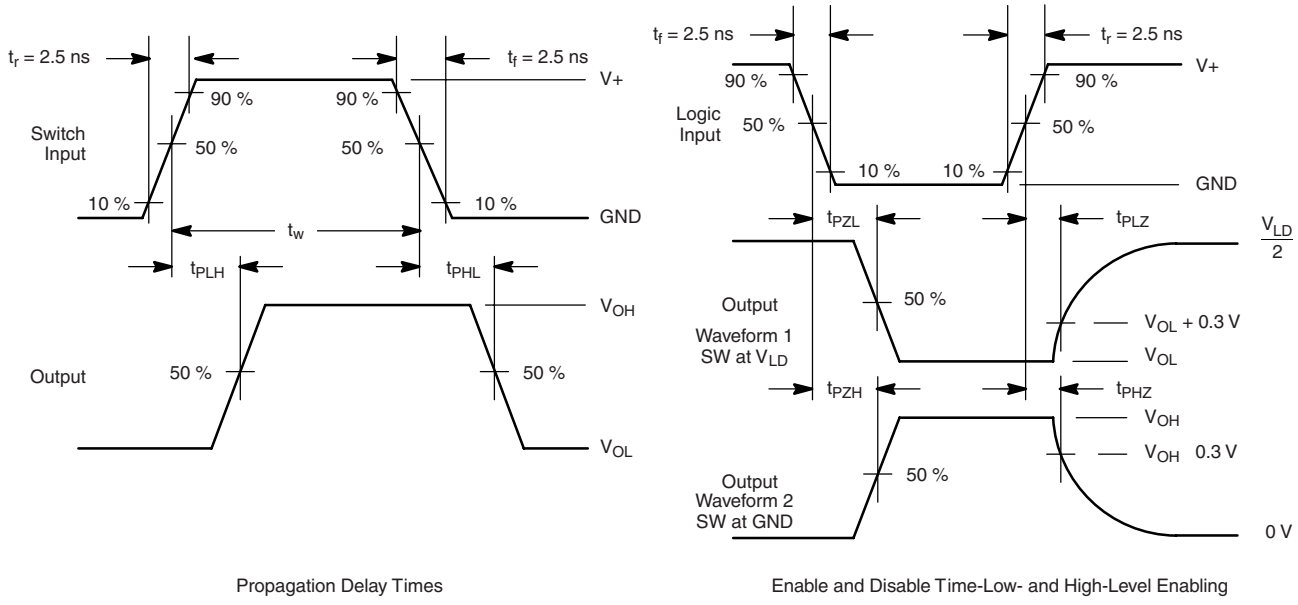
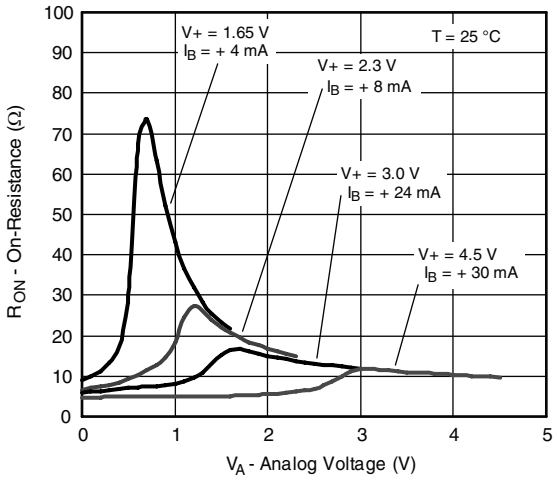


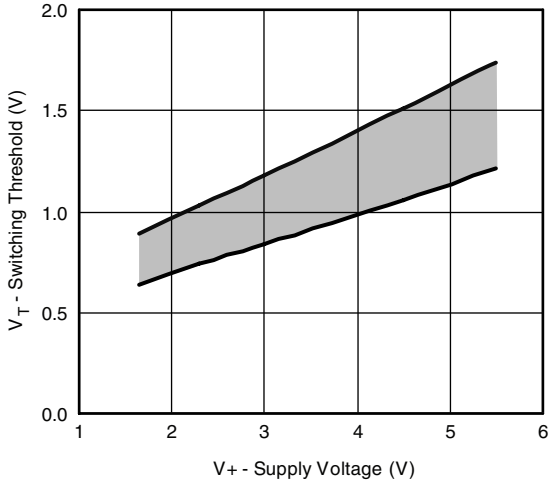
Figure 3. AC Waveforms

Notes:
- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
- Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: Input PRR = 1.0 MHz, t_w = 500 ns.
- The outputs are measured one at a time with one transition per measurement.
- V_{LD} = 2 V+.

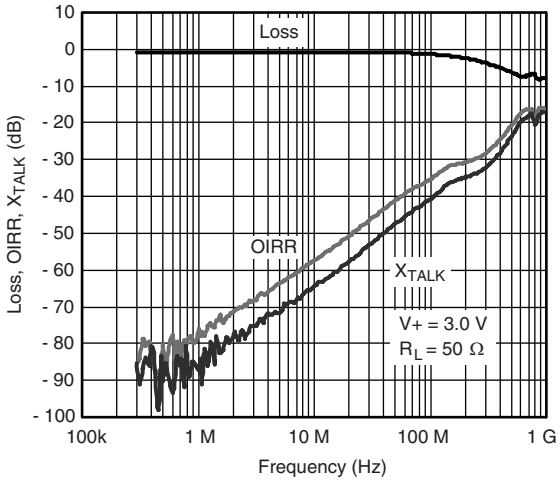
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



R_{ON} vs. V_A and Supply Voltage

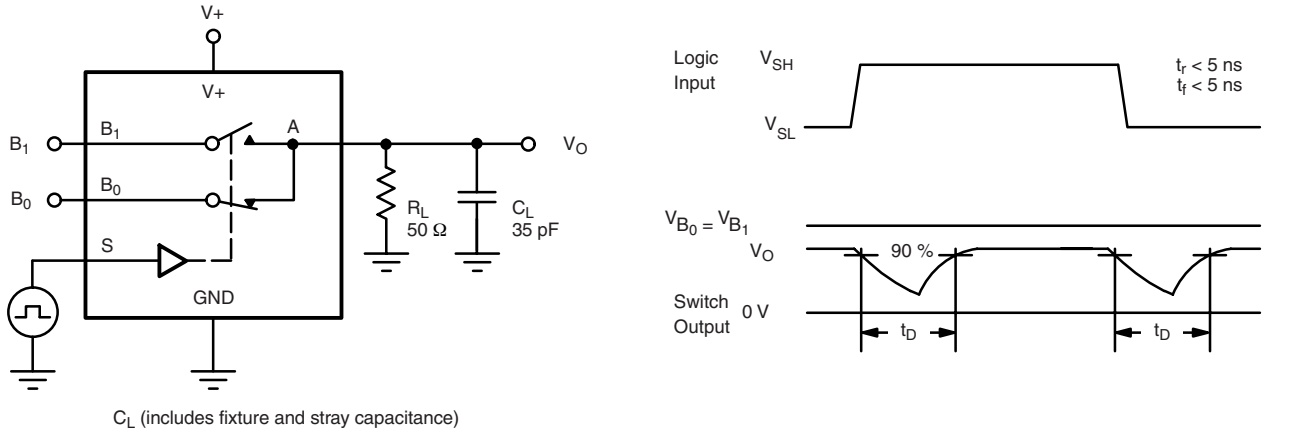


Switching Threshold vs. Supply Voltage



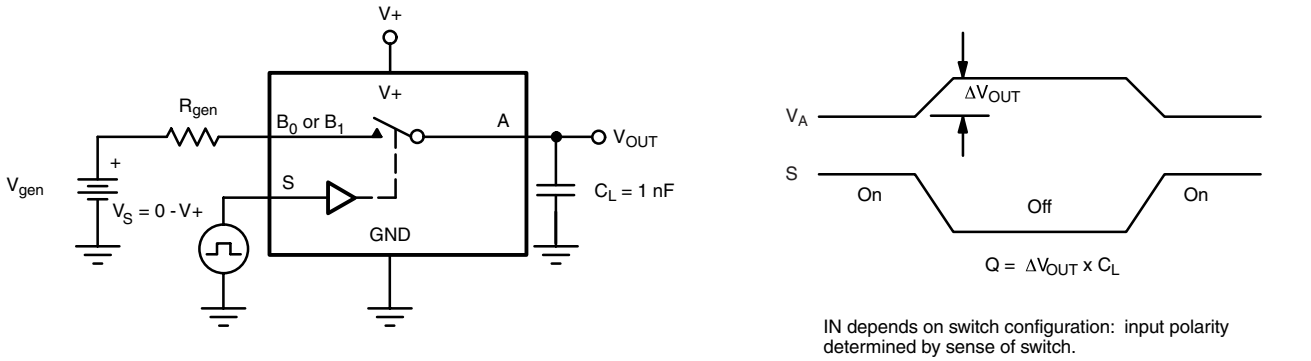
Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

TEST CIRCUITS



CL (includes fixture and stray capacitance)

Figure 4. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Figure 5. Charge Injection

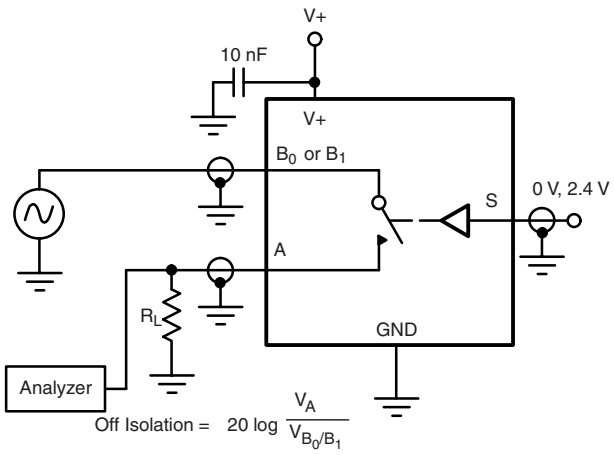


Figure 6. Off-Isolation

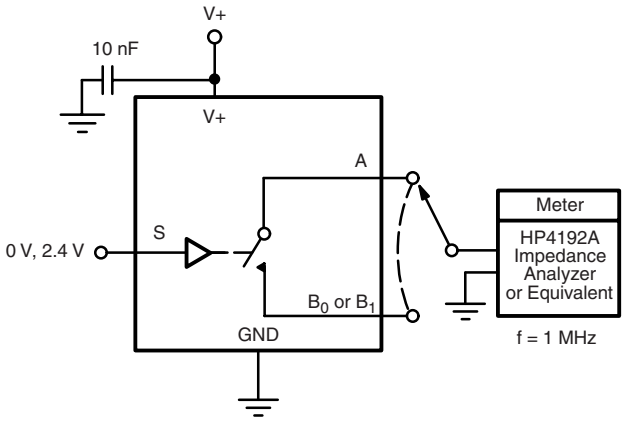


Figure 7. Channel Off/On Capacitance

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