50 MHz CMOS Complete DDS

AD9835

FEATURES
5 V Power Supply
50 MHz Speed
On-Chip COS Look-Up Table
On-Chip 10-Bit DAC
Serial Loading
Power-Down Option
200 mW Power Consumption
16-Lead TSSOP

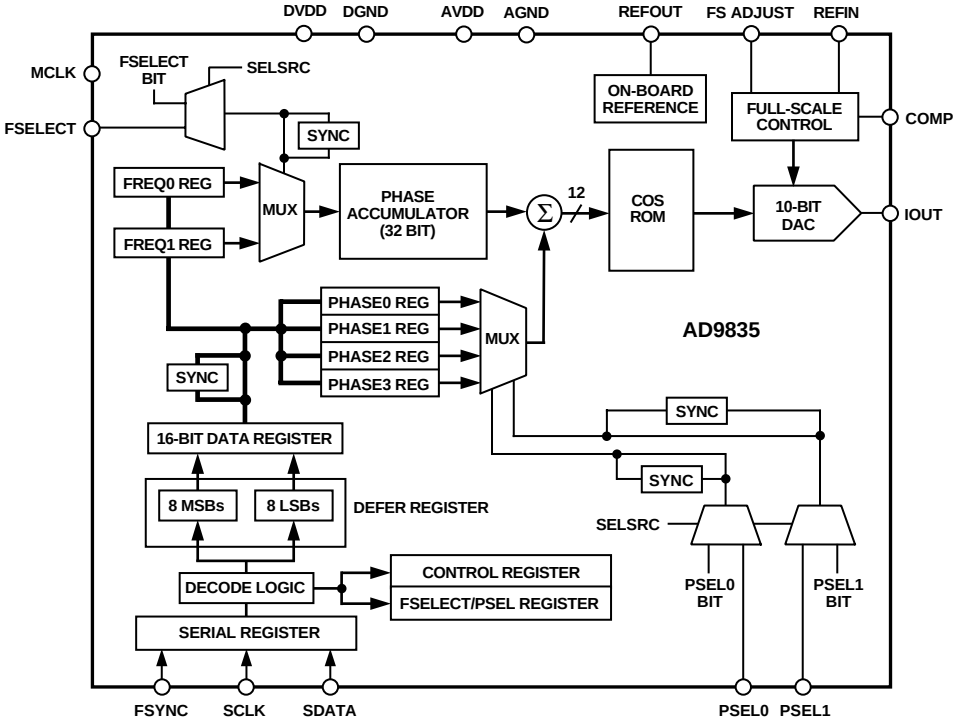
APPLICATIONS
DDS Tuning
Digital Demodulation

GENERAL DESCRIPTION

The AD9835 is a numerically controlled oscillator employing a phase accumulator, a COS Look-Up Table and a 10-bit D/A converter integrated on a single CMOS chip. Modulation capabilities are provided for phase modulation and frequency modulation.

Clock rates up to 50 MHz are supported. Frequency accuracy can be controlled to one part in 4 billion. Modulation is effected by loading registers through the serial interface. A power-down bit allows the user to power down the AD9835 when it is not in use, the power consumption being reduced to 1.75 mW. The part is available in a 16-lead TSSOP package.

FUNCTIONAL BLOCK DIAGRAM



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AD9835–SPECIFICATIONS[1] (V_{DD} = +5 V ± 5%; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX}; REFIN = REFOUT; R_{SET} = 3.9 kΩ; R_{LOAD} = 300 Ω for IOUT, unless otherwise noted)

Parameter	AD9835B	Units	Test Conditions/Comments
SIGNAL DAC SPECIFICATIONS			
Resolution	10	Bits	
Update Rate (f_{MAX})	50	MSPS nom	
IOUT Full Scale	4	mA nom	
	4.75	mA max	
Output Compliance	1.35	V max	
DC Accuracy			
Integral Nonlinearity	±1	LSB typ	
Differential Nonlinearity	±0.5	LSB typ	
DDS SPECIFICATIONS[2]			
Dynamic Specifications			
Signal-to-Noise Ratio	50	dB min	f_{MCLK} = 50 MHz, f_{OUT} = 1 MHz
Total Harmonic Distortion	–52	dBc max	f_{MCLK} = 50 MHz, f_{OUT} = 1 MHz
Spurious Free Dynamic Range (SFDR)[3]			f_{MCLK} = 6.25 MHz, f_{OUT} = 2.11 MHz
Narrow Band (±50 kHz)	–72	dBc min	
Wide Band (±2 MHz)	–50	dBc min	
Clock Feedthrough	–60	dBc typ	
Wake-Up Time	1	ms typ	
Power-Down Option	Yes		
VOLTAGE REFERENCE			
Internal Reference @ +25°C	1.21	V typ	
T_{MIN} to T_{MAX}	1.21 ± 7%	V min/max	
REFIN Input Impedance	10	MΩ typ	
Reference TC	100	ppm/°C typ	
REFOUT Output Impedance	300	Ω typ	
LOGIC INPUTS			
V_{INH}, Input High Voltage	DVDD – 0.9	V min	
V_{INL}, Input Low Voltage	0.9	V max	
I_{INH}, Input Current	10	μA max	
C_{IN}, Input Capacitance	10	pF max	
POWER SUPPLIES			f_{MCLK} = 50 MHz
AVDD	4.75/5.25	V min/V max	
DVDD	4.75/5.25	V min/V max	
I_{AA}	5	mA max	
I_{DD}	2.5 + 0.33/MHz	mA typ	
I_{AA} + I_{DD}[4]	40	mA max	
Low Power Sleep Mode	0.35	mA max	

NOTES
[1]Operating temperature range is as follows: B Version: –40°C to +85°C.
[2]100% production tested.
[3]f_{MCLK} = 6.25 MHz, Frequency Word = 5671C71C HEX, f_{OUT} = 2.11 MHz.
[4]Measured with the digital inputs static and equal to 0 V or DVDD. The AD9835 is tested with a capacitive load of 50 pF. The part can be operated with higher capacitive loads, but the magnitude of the analog output will be attenuated. See Figure 5.

Specifications subject to change without notice.

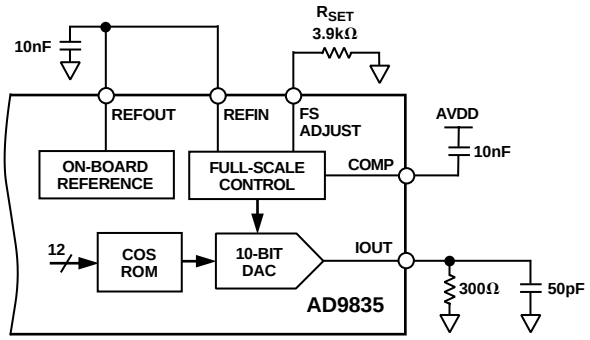


Figure 1. Test Circuit with Which Specifications Are Tested

TIMING CHARACTERISTICS (V_{DD} = +5 V ± 5%; AGND = DGND = 0 V, unless otherwise noted)

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Units	Test Conditions/Comments
t_1	20	ns min	MCLK Period
t_2	8	ns min	MCLK High Duration
t_3	8	ns min	MCLK Low Duration
t_4	50	ns min	SCLK Period
t_5	20	ns min	SCLK High Duration
t_6	20	ns min	SCLK Low Duration
t_7	15	ns min	FSYNC to SCLK Falling Edge Setup Time
t_8	20	ns min	FSYNC to SCLK Hold Time
	SCLK – 5	ns max	
t_9	15	ns min	Data Setup Time
t_{10}	5	ns min	Data Hold Time
t_{11}	8	ns min	FSELECT, PSEL0, PSEL1 Setup Time Before MCLK Rising Edge
t_{11A}[1]	8	ns min	FSELECT, PSEL0, PSEL1 Setup Time After MCLK Rising Edge

NOTES
[1]See Pin Description section.
Guaranteed by design but not production tested.

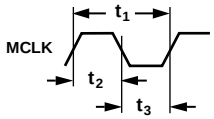


Figure 2. Master Clock

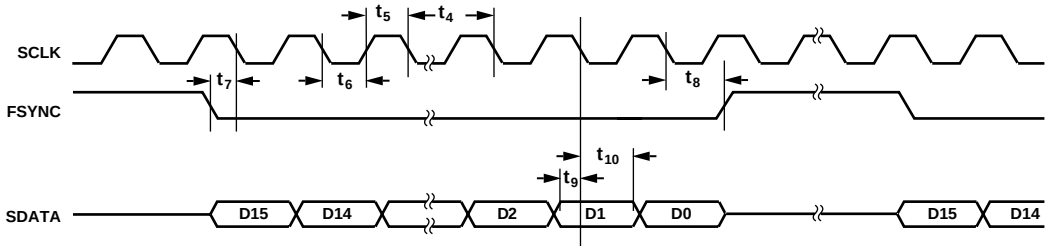


Figure 3. Serial Timing

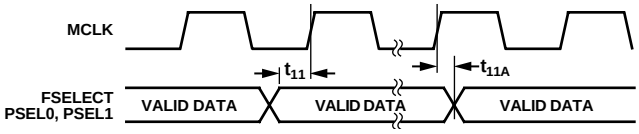


Figure 4. Control Timing

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

AVDD to AGND . . . . . –0.3 V to +7 V
DVDD to DGND . . . . . –0.3 V to +7 V
AVDD to DVDD . . . . . –0.3 V to +0.3 V
AGND to DGND. . . . . –0.3 V to +0.3 V
Digital I/O Voltage to DGND . . . . . –0.3 V to DVDD + 0.3 V
Analog I/O Voltage to AGND . . . . . –0.3 V to AVDD + 0.3 V
Operating Temperature Range
  Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . +150°C
TSSOP θ_{JA} Thermal Impedance . . . . . 158°C/W
Lead Temperature, Soldering
  Vapor Phase (60 sec) . . . . . +215°C
  Infrared (15 sec) . . . . . +220°C
ESD Rating . . . . . > 4500 V

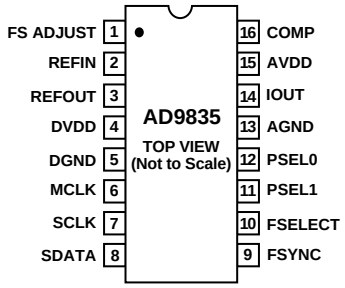
*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9835BRU	–40°C to +85°C	16-Lead TSSOP	RU-16

*RU = Thin Shrink Small Outline Package (TSSOP).

PIN CONFIGURATION



TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale, a point 0.5 LSB below the first code transition (000 . . . 00 to 000 . . . 01) and full scale, a point 0.5 LSB above the last code transition (111 . . . 10 to 111 . . . 11). The error is expressed in LSBs.

Differential Nonlinearity
This is the difference between the measured and ideal 1 LSB change between two adjacent codes in the DAC.

Signal to (Noise + Distortion)
Signal to (Noise + Distortion) is measured signal to noise at the output of the DAC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency ($f_{MCLK}/2$) but excluding the dc component. Signal to (Noise + Distortion) is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical Signal to (Noise + Distortion) ratio for a sine wave input is given by

$$\textit{Signal to (Noise + Distortion)} = (6.02N + 1.76)\ dB$$

where N is the number of bits. Thus, for an ideal 10-bit converter, Signal to (Noise + Distortion) = 61.96 dB.

Total Harmonic Distortion
Total Harmonic Distortion (THD) is the ratio of the rms sum of harmonics to the rms value of the fundamental. For the AD9835, THD is defined as

$$THD = 20 \log \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonic.

Output Compliance
The output compliance refers to the maximum voltage that can be generated at the output of the DAC to meet the specifications. When voltages greater than that specified for the output compliance are generated, the AD9835 may not meet the specifications listed in the data sheet.

Spurious Free Dynamic Range
Along with the frequency of interest, harmonics of the fundamental frequency and images of the MCLK frequency are present at the output of a DDS device. The spurious free dynamic range (SFDR) refers to the largest spur or harmonic present in the band of interest. The wideband SFDR gives the magnitude of the largest harmonic or spur relative to the magnitude of the fundamental frequency in the bandwidth ±2 MHz about the fundamental frequency. The narrow band SFDR gives the attenuation of the largest spur or harmonic in a bandwidth of ±50 kHz about the fundamental frequency.

Clock Feedthrough
There will be feedthrough from the MCLK input to the analog output. Clock feedthrough refers to the magnitude of the MCLK signal relative to the fundamental frequency in the AD9835's output spectrum.

PIN FUNCTION DESCRIPTIONS

Pin #	Mnemonic	Function
ANALOG SIGNAL AND REFERENCE		
1	FS ADJUST	Full-Scale Adjust Control. A resistor (R_{SET}) is connected between this pin and AGND. This determines the magnitude of the full-scale DAC current. The relationship between R_{SET} and the full-scale current is as follows: $IOUT_{FULL\text{-}SCALE} = 12.5 \times V_{REFIN}/R_{SET}$ $V_{REFIN} = 1.21$ *V nominal*, $R_{SET} = 3.9$ kΩ *typical*
2	REFIN	Voltage Reference Input. The AD9835 can be used with either the onboard reference, which is available from pin REFOUT, or an external reference. The reference to be used is connected to the REFIN pin. The AD9835 accepts a reference of 1.21 V nominal.
3	REFOUT	Voltage Reference Output. The AD9835 has an onboard reference of value 1.21 V nominal. The reference is made available on the REFOUT pin. This reference is used as the reference to the DAC by connecting REFOUT to REFIN. REFOUT should be decoupled with a 10 nF capacitor to AGND.
14	IOUT	Current Output. This is a high impedance current source. A load resistor should be connected between IOUT and AGND.
16	COMP	Compensation pin. This is a compensation pin for the internal reference amplifier. A 10 nF decoupling ceramic capacitor should be connected between COMP and AVDD.
POWER SUPPLY		
4	DVDD	Positive Power Supply for the Digital Section. A 0.1 μF decoupling capacitor should be connected between DVDD and DGND. DVDD can have a value of +5 V ± 5%.
5	DGND	Digital Ground.
13	AGND	Analog Ground.
15	AVDD	Positive Power Supply for the Analog Section. A 0.1 μF decoupling capacitor should be connected between AVDD and AGND. AVDD can have a value of +5 V ± 5%.
DIGITAL INTERFACE AND CONTROL		
6	MCLK	Digital Clock Input. DDS output frequencies are expressed as a binary fraction of the frequency of MCLK. The output frequency accuracy and phase noise are determined by this clock.
7	SCLK	Serial Clock, Logic Input. Data is clocked into the AD9835 on each falling SCLK edge.
8	SDATA	Serial Data In, Logic Input. The 16-bit serial data word is applied to this input.
9	FSYNC	Data Synchronization Signal, Logic Input. When this input is taken low, the internal logic is informed that a new word is being loaded into the device.
10	FSELECT	Frequency Select Input. FSELECT controls which frequency register, FREQ0 or FREQ1, is used in the phase accumulator. The frequency register to be used can be selected using the pin FSELECT or the bit FSELECT. FSELECT is sampled on the rising MCLK edge. FSELECT needs to be in steady state when an MCLK rising edge occurs. If FSELECT changes value when a rising edge occurs, there is an uncertainty of one MCLK cycle as to when control is transferred to the other frequency register. To avoid any uncertainty, a change on FSELECT should not coincide with an MCLK rising edge. When the bit is being used to select the frequency register, the pin FSELECT should be tied to DGND.
11, 12	PSEL0, PSEL1	Phase Select Input. The AD9835 has four phase registers. These registers can be used to alter the value being input to the COS ROM. The contents of the phase register are added to the phase accumulator output, the inputs PSEL0 and PSEL1 selecting the phase register to be used. Alternatively, the phase register to be used can be selected using bits PSEL0 and PSEL1. Like the FSELECT input, PSEL0 and PSEL1 are sampled on the rising MCLK edge. Therefore, these inputs need to be in steady state when an MCLK rising edge occurs or there is an uncertainty of one MCLK cycle as to when control is transferred to the selected phase register. When the phase registers are being controlled by the bits PSEL0 and PSEL1, the pins should be tied to DGND.

Table I. Control Registers

Register	Size	Description
FREQ0 REG	32 Bits	Frequency Register 0. This defines the output frequency, when FSELECT = 0, as a fraction of the MCLK frequency.
FREQ1 REG	32 Bits	Frequency Register 1. This defines the output frequency, when FSELECT = 1, as a fraction of the MCLK frequency.
PHASE0 REG	12 Bits	Phase Offset Register 0. When PSEL0 = PSEL1 = 0, the contents of this register are added to the output of the phase accumulator.
PHASE1 REG	12 Bits	Phase Offset Register 1. When PSEL0 = 1 and PSEL1 = 0, the contents of this register are added to the output of the phase accumulator.
PHASE2 REG	12 Bits	Phase Offset Register 2. When PSEL0 = 0 and PSEL1 = 1, the contents of this register are added to the output of the phase accumulator.
PHASE3 REG	12 Bits	Phase Offset Register 3. When PSEL0 = PSEL1 = 1, the contents of this register are added to the output of the phase accumulator.

Table II. Addressing the Registers

A3	A2	A1	A0	Destination Register
0	0	0	0	FREG0 REG 8 L LSBs
0	0	0	1	FREG0 REG 8 H LSBs
0	0	1	0	FREG0 REG 8 L MSBs
0	0	1	1	FREG0 REG 8 H MSBs
0	1	0	0	FREG1 REG 8 L LSBs
0	1	0	1	FREG1 REG 8 H LSBs
0	1	1	0	FREG1 REG 8 L MSBs
0	1	1	1	FREG1 REG 8 H MSBs
1	0	0	0	PHASE0 REG 8 LSBs
1	0	0	1	PHASE0 REG 8 MSBs
1	0	1	0	PHASE1 REG 8 LSBs
1	0	1	1	PHASE1 REG 8 MSBs
1	1	0	0	PHASE2 REG 8 LSBs
1	1	0	1	PHASE2 REG 8 MSBs
1	1	1	0	PHASE3 REG 8 LSBs
1	1	1	1	PHASE3 REG 8 MSBs

Table III. 32-Bit Frequency Word

16 MSBs		16 LSBs	
8 H MSBs	8 L MSBs	8 H LSBs	8 L LSBs

Table IV. 12-Bit Frequency Word

4 MSBs (The 4 MSBs of the 8-Bit Word Loaded = 0)	8 LSBs

Table V. Commands

C3	C2	C1	C0	Command
0	0	0	0	Write 16 Phase bits (Present 8 Bits + 8 Bits in Defer Register) to Selected PHASE REG.
0	0	0	1	Write 8 Phase bits to Defer Register.
0	0	1	0	Write 16 Frequency bits (Present 8 Bits + 8 Bits in Defer Register) to Selected FREQ REG.
0	0	1	1	Write 8 Frequency bits to Defer Register.
0	1	0	0	Bits D9 (PSEL0) and D10 (PSEL1) are used to Select the PHASE REG when SELSRC = 1. When SELSRC = 0, the PHASE REG is selected using the pins PSEL0 and PSEL1 Respectively.
0	1	0	1	Bit D11 is used to select the FREQ REG when SELSRC = 1. When SELSRC = 0, the FREQ REG is selected using the pin FSELECT.
0	1	1	0	This command is used to control the PSEL0, PSEL1 and FSELECT bits using only one write. Bits D9 and D10 are used to select the PHASE REG and Bit 11 is used to select the FREQ REG when SELSRC = 1. When SELSRC = 0, the PHASE REG is selected using the pins PSEL0 and PSEL1 and the FREQ REG is selected using the pin FSELECT.
0	1	1	1	Reserved. Configures the AD9835 for Test Purposes.

Table VI. Controlling the AD9835

D15	D14	Command
1	0	Selects source of Control for the PHASE and FREQ Registers and Enables Synchronization. Bit D13 is the SYNC Bit. When this bit is High, reading of the FSELECT, PSEL0 and PSEL1 bits/pins and the loading of the Destination Register with data is synchronized with the rising edge of MCLK. The latency is increased by 2 MCLK cycles when SYNC = 1. When SYNC = 0, the loading of the data and the sampling of FSELECT/PSEL0/PSEL1 occurs asynchronously. Bit D12 is the Select Source Bit (SELSRC). When this bit Equals 1, the PHASE/FREQ REG is Selected using the bits FSELECT, PSEL0 and PSEL1. When SELSRC = 0, the PHASE/FREQ REG is Selected using the pins FSELECT, PSEL0 and PSEL1.
1	1	Sleep, Reset and Clear. D13 is the SLEEP bit. When this bit equals 1, the AD9835 is powered down, internal clocks are disabled and the DAC's current sources and REFOUT are turned off. When SLEEP = 0, the AD9835 is powered up. When RESET (D12) = 1, the phase accumulator is set to zero phase which corresponds to an analog output of full scale. When CLR (D11) = 1, SYNC and SELSRC are set to zero. CLR automatically resets to zero.

Table VII. Writing to the AD9835 Data Registers

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
C3	C2	C1	C0	A3	A2	A1	A0	MSB							LSB

Table VIII. Setting SYNC and SELSRC

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	SYNC	SELSRC	X	X	X	X	X	X	X	X	X	X	X	X

Table IX. Power-Down, Resetting and Clearing the AD9835

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	SLEEP	RESET	CLR	X	X	X	X	X	X	X	X	X	X	X

Typical Performance Characteristics

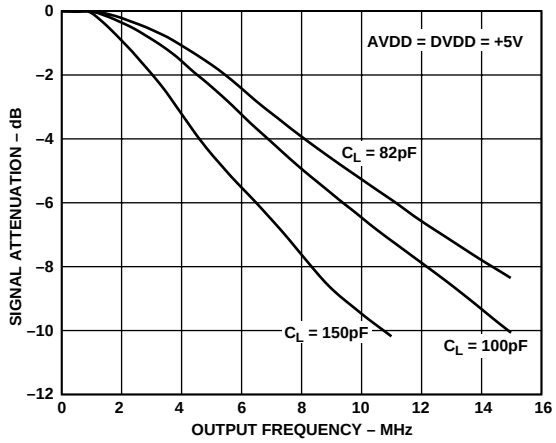


Figure 5. Signal Attenuation vs. Output Frequency for Various Capacitive Load (R_L = 300 Ω)

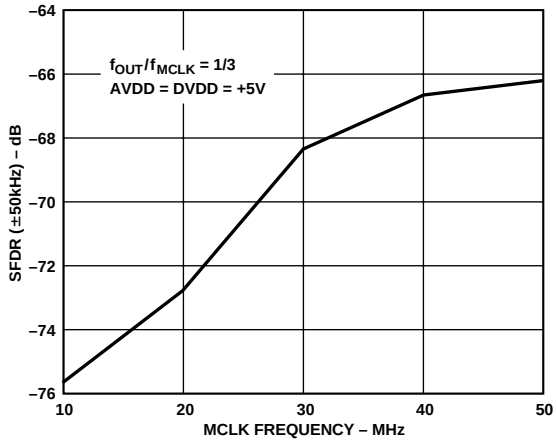


Figure 7. Narrow Band SFDR vs. MCLK Frequency

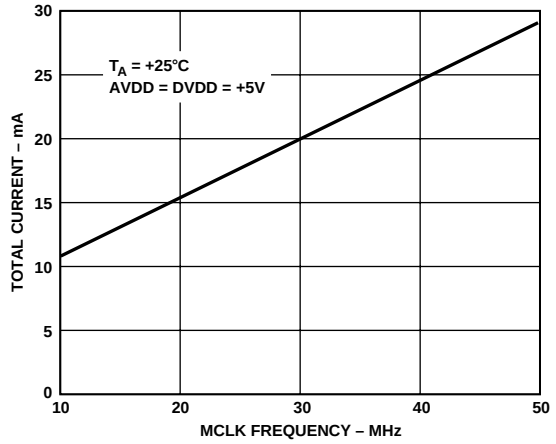


Figure 6. Typical Current Consumption vs. MCLK Frequency

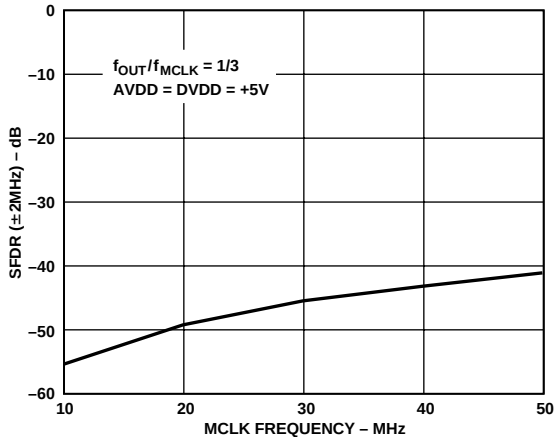


Figure 8. Wide Band SFDR vs. MCLK Frequency

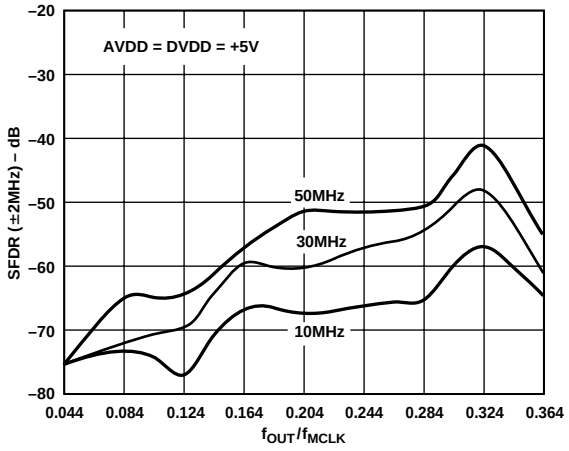


Figure 9. Wide Band SFDR vs. f_{OUT}/f_{MCLK} for Various MCLK Frequencies

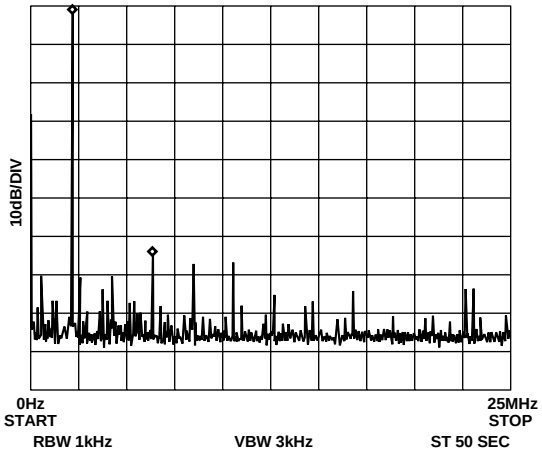


Figure 12. f_{MCLK} = 50 MHz, f_{OUT} = 2.1 MHz. Frequency Word = ACO8312

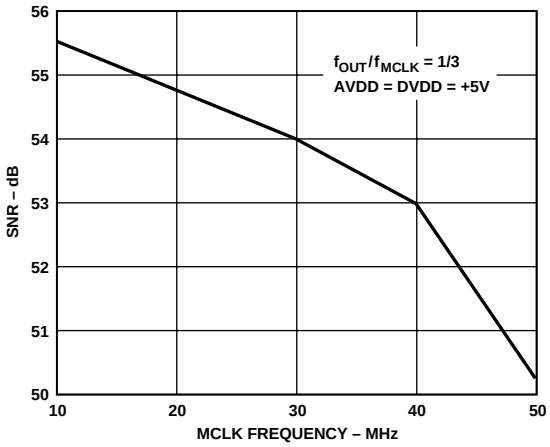


Figure 10. SNR vs. MCLK Frequency

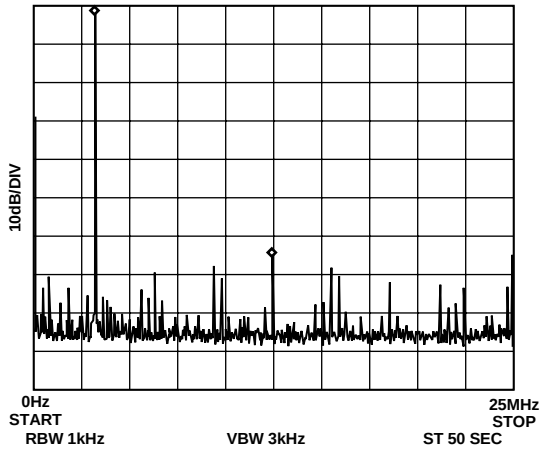


Figure 13. f_{MCLK} = 50 MHz, f_{OUT} = 3.1 MHz. Frequency Word = FDF3B64

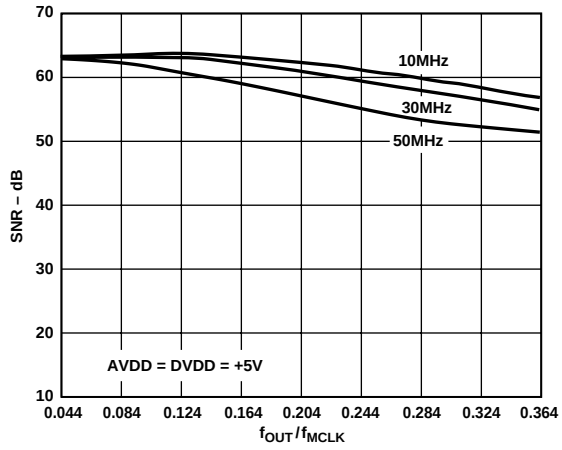


Figure 11. SNR vs. f_{OUT}/f_{MCLK} for Various MCLK Frequencies

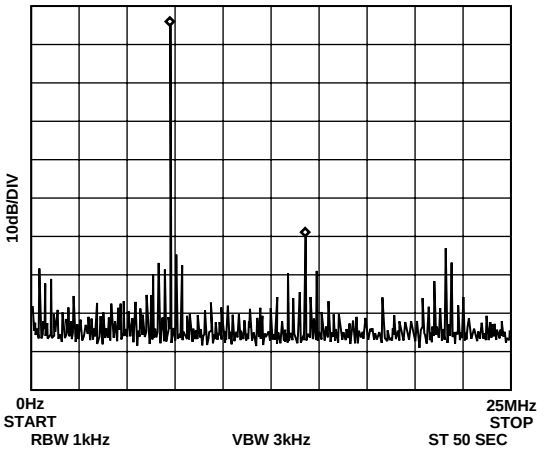


Figure 14. f_{MCLK} = 50 MHz, f_{OUT} = 7.1 MHz. Frequency Word = 245AICAC

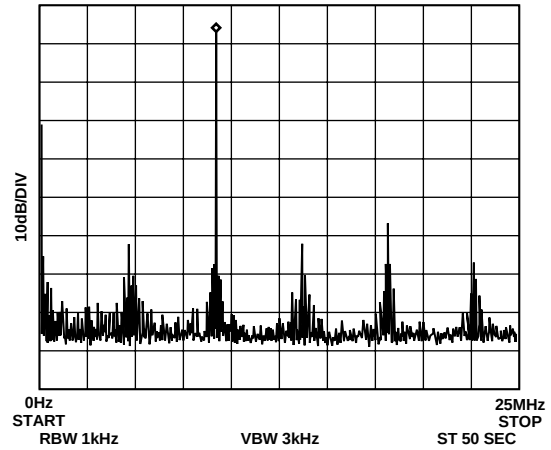


Figure 15. f_{MCLK} = 50 MHz, f_{OUT} = 9.1 MHz. Frequency Word = 2E978D50

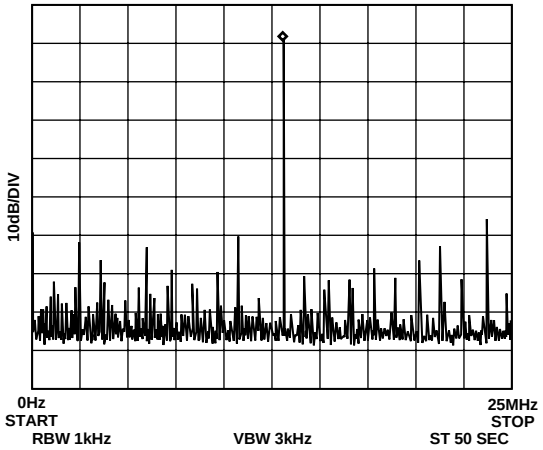


Figure 17. f_{MCLK} = 50 MHz, f_{OUT} = 13.1 MHz. Frequency Word = 43126E98

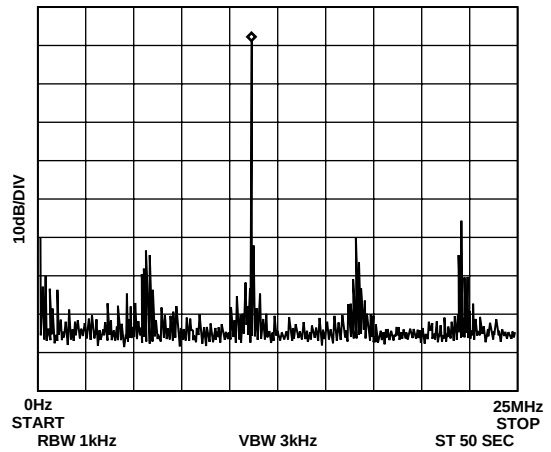


Figure 16. f_{MCLK} = 50 MHz, f_{OUT} = 11.1 MHz. Frequency Word = 38D4FDF4

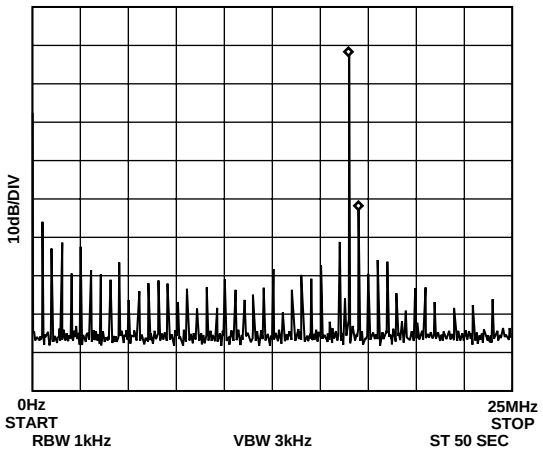


Figure 18. f_{MCLK} = 50 MHz, f_{OUT} = 16.5 MHz. Frequency Word = 547AE148

CIRCUIT DESCRIPTION

The AD9835 provides an exciting new level of integration for the RF/Communications system designer. The AD9835 combines the Numerical Controlled Oscillator (NCO), COS Look-Up Table, Frequency and Phase Modulators, and a Digital-to-Analog Converter on a single integrated circuit.

The internal circuitry of the AD9835 consists of three main sections. These are:

Numerical Controlled Oscillator (NCO) + Phase Modulator
COS Look-Up Table
Digital-to-Analog Converter

The AD9835 is a fully integrated Direct Digital Synthesis (DDS) chip. The chip requires one reference clock, one low precision resistor and eight decoupling capacitors to provide digitally created sine waves up to 25 MHz. In addition to the generation of this RF signal, the chip is fully capable of a broad range of simple and complex modulation schemes. These modulation schemes are fully implemented in the digital domain allowing accurate and simple realization of complex modulation algorithms using DSP techniques.

THEORY OF OPERATION

Cos waves are typically thought of in terms of their magnitude form a(t) = cos (ωt). However, these are nonlinear and not easy to generate except through piece-wise construction. On the other hand, the angular information is linear in nature. That is, the phase angle rotates through a fixed angle for each unit of time. The angular rate depends on the frequency of the signal by the traditional rate of ω = 2 πf.

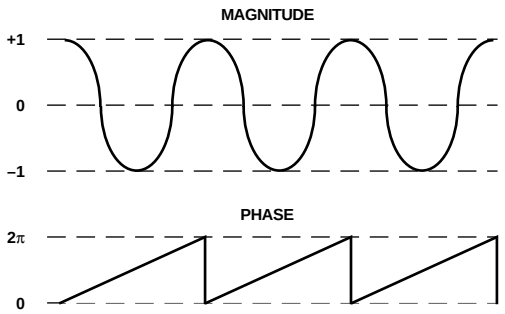


Figure 19. Cos Wave

Knowing that the phase of a cos wave is linear and given a reference interval (clock period), the phase rotation for that period can be determined.

$$\Delta Phase = \omega\delta t$$

Solving for ω

$$\omega = \Delta Phase/\delta t = 2\ \pi f$$

Solving for *f* and substituting the reference clock frequency for the reference period ($1/f_{MCLK} = \delta t$)

$$f = \Delta Phase \times f_{MCLK}/2\ \pi$$

The AD9835 builds the output based on this simple equation. A simple DDS chip can implement this equation with three major subcircuits.

Numerical Controlled Oscillator and Phase Modulator

This consists of two frequency select registers, a phase accumulator and four phase offset registers. The main component of the NCO is a 32-bit phase accumulator which assembles the phase component of the output signal. Continuous time signals have a phase range of 0 π to 2 π. Outside this range of numbers, the sinusoid functions repeat themselves in a periodic manner. The digital implementation is no different. The accumulator simply scales the range of phase numbers into a multibit digital word. The phase accumulator in the AD9835 is implemented with 32 bits. Therefore, in the AD9835, $2\ \pi = 2^{32}$. Likewise, the Δ*Phase* term is scaled into this range of numbers $0 < \Delta Phase < 2^{32} - 1$. Making these substitutions into the equation above

$$f = \Delta Phase \times f_{MCLK}/2^{32}$$

where $0 < \Delta Phase < 2^{32}$

The input to the phase accumulator (i.e., the phase step) can be selected either from the FREQ0 Register or FREQ1 Register and this is controlled by the FSELECT pin or the FSELECT bit. NCOs inherently generate continuous phase signals, thus avoiding any output discontinuity when switching between frequencies.

Following the NCO, a phase offset can be added to perform phase modulation using the 12-bit PHASE Registers. The contents of this register are added to the most significant bits of the NCO. The AD9835 has four PHASE registers, the resolution of these registers being 2 π/4096.

COS Look-Up Table (LUT)

To make the output useful, the signal must be converted from phase information into a sinusoidal value. Since phase information maps directly into amplitude, a ROM LUT converts the phase information into amplitude. To do this, the digital phase information is used to address a COS ROM LUT. Although the NCO contains a 32-bit phase accumulator, the output of the NCO is truncated to 12 bits. Using the full resolution of the phase accumulator is impractical and unnecessary as this would require a look-up table of 2^{32} entries.

It is necessary only to have sufficient phase resolution in the LUTs such that the dc error of the output waveform is dominated by the quantization error in the DAC. This requires the look-up table to have two more bits of phase resolution than the 10-bit DAC.

Digital-to-Analog Converter

The AD9835 includes a high impedance current source 10-bit DAC, capable of driving a wide range of loads at different speeds. Full-scale output current can be adjusted, for optimum power and external load requirements, through the use of a single external resistor (R_{SET}).

The DAC is configured for single-ended operation. The load resistor can be any value required, as long as the full-scale voltage developed across it does not exceed the voltage compliance range. Since full-scale current is controlled by R_{SET}, adjustments to R_{SET} can balance changes made to the load resistor. However, if the DAC full-scale output current is significantly less than 4 mA, the DAC's linearity may degrade.

DSP and MPU Interfacing

The AD9835 has a serial interface, with 16 bits being loaded during each write cycle. SCLK, SDATA and FSYNC are used to load the word into the AD9835. When FSYNC is taken low, the AD9835 is informed that a word is being written to the device. The first bit is read into the device on the next SCLK falling edge with the remaining bits being read into the device on the subsequent SCLK falling edges. FSYNC frames the 16 bits; therefore, when 16 SCLK falling edges have occurred,

FSYNC should be taken high again. The SCLK can be continuous or, alternatively, the SCLK can idle high or low between write operations.

When writing to a frequency/phase register, the first four bits identify whether a frequency or phase register is being written to, the next four bits contain the address of the destination register while the 8 LSBs contain the data. Table II lists the addresses for the phase/frequency registers while Table III lists the commands.

Within the AD9835, 16-bit transfers are used when loading the destination frequency/phase register. There are two modes for loading a register—direct data transfer and a deferred data transfer. With a deferred data transfer, the 8-bit word is loaded into the defer register (8 LSBs or 8 MSBs). However, this data is not loaded into the 16-bit data register so the destination register is not updated. With a direct data transfer, the 8-bit word is loaded into the appropriate defer register (8 LSBs or 8 MSBs). Immediately following the loading of the defer register, the contents of the complete defer register are loaded into the 16-bit data register and the destination register is loaded on the next MCLK rising edge. When a destination register is addressed, a deferred transfer is needed first, followed by a direct transfer. When all 16 bits of the defer register contain relevant data, the destination register can then be updated using 8-bit loading rather than 16-bit loading, i.e., direct data transfers can be used. For example, after a new 16-bit word has been loaded to a destination register, the defer register will also contain this word. If the next write instruction is to the same destination register, the user can use direct data transfers immediately.

When writing to a phase register, the 4 MSBs of the 16-bit word loaded into the data register should be zero (the phase registers are 12 bits wide).

To alter the entire contents of a frequency register, four write operations are needed. However, the 16 MSBs of a frequency word are contained in a separate register to the 16 LSBs. Therefore, the 16 MSBs of the frequency word can be altered independent of the 16 LSBs.

The phase and frequency registers to be used are selected using the pins FSELECT, PSEL0 and PSEL1 or the corresponding bits can be used. Bit SELSRC determines whether the bits or the pins are used. When SELSRC = 0, the pins are used while the bits are used when SELSRC = 1. When CLR is taken high, SELSRC is set to 0 so that the pins are the default source.

Data transfers from the serial (defer) register to the 16-bit data register, and the FSELECT and PSEL registers, occur following the 16th falling SCLK edge. Transfer of the data from the 16-bit data register to the destination register or from the FSELECT/PSEL register to the respective multiplexer occurs on the next MCLK rising edge. Since the SCLK and the MCLK are asynchronous, an MCLK rising edge may occur while the data bits are in transitional state, which will cause a brief spurious DAC output if the register being written to is generating the DAC output. To avoid such spurious outputs, the AD9835 contains synchronizing circuitry. When the SYNC bit is set to 1, the synchronizer is enabled and data transfers from the serial register (defer register) to the 16-bit data register and the FSELECT/PSEL registers occur following a two-stage pipeline delay which is triggered on the MCLK falling edge. The pipeline delay ensures that the data is valid when the transfer occurs. Similarly, selection of the frequency/phase registers using the FSELECT/PSEL pins is synchronized with the MCLK rising edge when SYNC = 1. When SYNC = 0, the synchronizer is bypassed.

Selecting the frequency/phase registers using the pins is synchronized with MCLK internally also when SYNC = 1 to ensure that these inputs are valid at the MCLK rising edge. If times t_{11} and t_{11A} are met, the inputs will be at steady state at the MCLK rising edge. However, if times t_{11} and t_{11A} are violated, the internal synchronizing circuitry will delay the instant at which the pins are sampled, ensuring that the inputs are valid at the sampling instant.

A latency is associated with each operation. When inputs FSELECT/PSEL change value, there will be a pipeline delay before control is transferred to the selected register—there will be a pipeline delay before the analog output is controlled by the selected register. When times t_{11} and t_{11A} are met, PSEL0, PSEL1 and FSELECT have latencies of six MCLK cycles when SYNC = 0. When SYNC = 1, the latency is increased to 8 MCLK cycles. When times t_{11} and t_{11A} are not met, the latency can increase by one MCLK cycle. Similarly, there is a latency associated with each write operation. If a selected frequency/phase register is loaded with a new word, there is a delay of 6 to 7 MCLK cycles before the analog output will change (there is an uncertainty of one MCLK cycle regarding the MCLK rising edge at which the data is loaded into the destination register). When SYNC = 1, the latency will be 8 or 9 MCLK cycles.

The flowchart in Figure 20 shows the operating routine for the AD9835. When the AD9835 is powered up, the part should be reset. This will reset the phase accumulator to zero so that the analog output is at full scale. To avoid spurious DAC outputs while the AD9835 is being initialized, the RESET bit should be set to 1 until the part is ready to begin generating an output. Taking CLR high will set SYNC and SELSRC to 0 so that the FSELECT/PSEL pins are used to select the frequency/phase registers and the synchronization circuitry is bypassed. A write operation is needed to the SYNC/SELSRC register to enable the synchronization circuitry or to change control to the FSELECT/PSEL bits. RESET does not reset the phase and frequency registers. These registers will contain invalid data and should therefore be set to a known value by the user. The RESET bit is then set to 0 to begin generating an output. A signal will appear at the DAC output 6 MCLK cycles after RESET is set to 0.

The analog output is $f_{MCLK}/2^{32} \times$ FREG where FREG is the value loaded into the selected frequency register. This signal will be phase shifted by the amount specified in the selected phase register ($2\pi/4096 \times$ PHASEREG where PHASEREG is the value contained in the selected phase register).

Control of the frequency/phase registers can be interchanged from the pins to the bits.

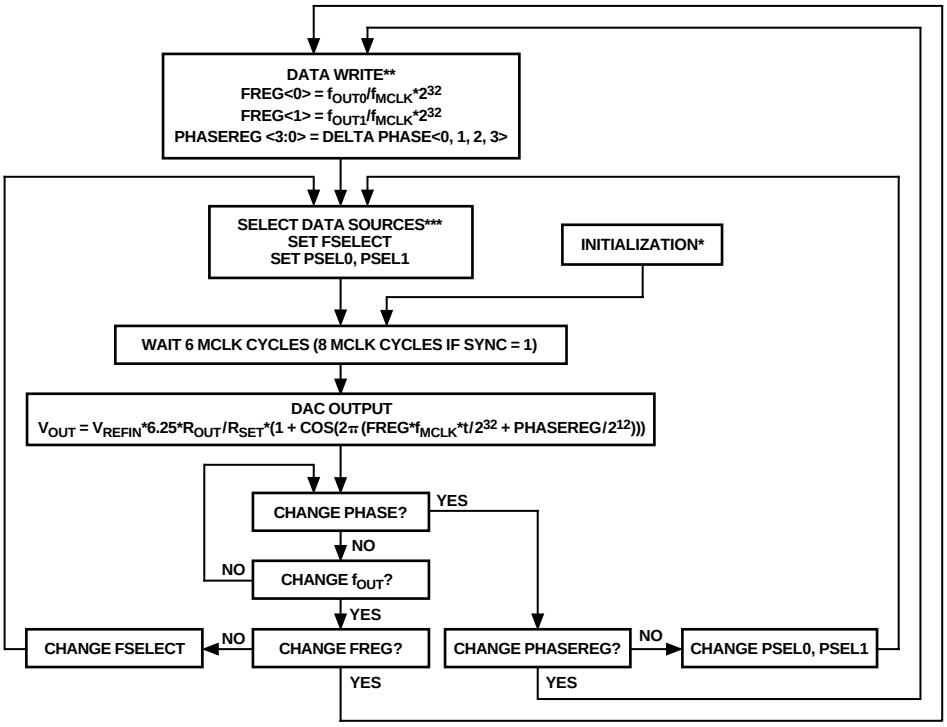


Figure 20. Flowchart for AD9835 Initialization and Operation

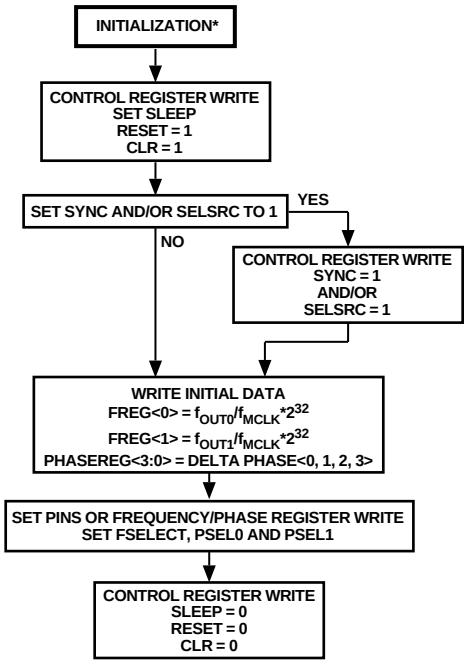


Figure 21. Initialization

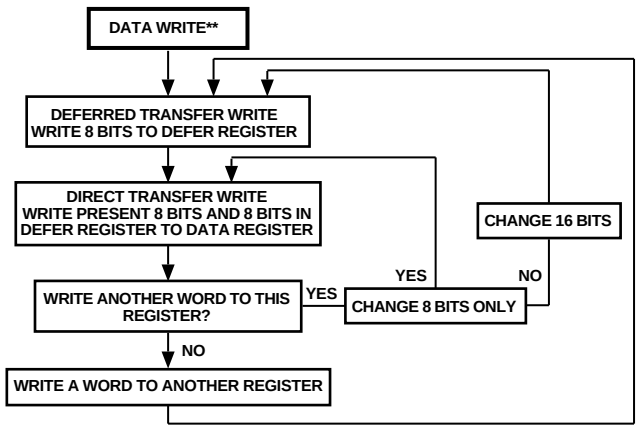


Figure 22. Data Writes

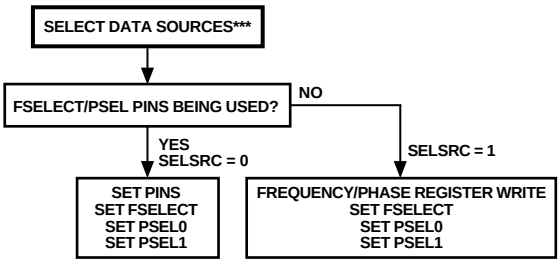


Figure 23. Selecting Data Sources

APPLICATIONS

The AD9835 contains functions that make it suitable for modulation applications. The part can be used to perform simple modulation such as FSK. More complex modulation schemes such as GMSK and QPSK can also be implemented using the AD9835. In an FSK application, the two frequency registers of the AD9835 are loaded with different values; one frequency will represent the space frequency while the other will represent the mark frequency. The digital data stream is fed to the FSELECT pin, which will cause the AD9835 to modulate the carrier frequency between the two values.

The AD9835 has four phase registers; this enables the part to perform PSK. With phase shift keying, the carrier frequency is phase shifted, the phase being altered by an amount that is related to the bit stream being input to the modulator. The presence of four shift registers eases the interaction needed between the DSP and the AD9835.

The AD9835 is also suitable for signal generator applications. With its low current consumption, the part is suitable for applications in which it can be used as a local oscillator.

Grounding and Layout

The printed circuit board that houses the AD9835 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes which can be separated easily. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should only be joined in one place. If the AD9835 is the only device requiring an AGND to DGND connection, then the ground planes should be connected at the AGND and DGND pins of the AD9835. If the AD9835 is in a system where multiple devices require AGND to DGND connections, the connection should be made at one point only, a star ground point that should be established as close as possible to the AD9835.

Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD9835 to avoid noise coupling. The power supply lines to the AD9835 should use as large a track as is possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other sections of the board. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the other side.

Good decoupling is important. The analog and digital supplies to the AD9835 are independent and separately pinned out to minimize coupling between analog and digital sections of the device. All analog and digital supplies should be decoupled to AGND and DGND respectively with 0.1 μF ceramic capacitors in parallel with 10 μF tantalum capacitors. To achieve the best from the decoupling capacitors, they should be placed as close as possible to the device, ideally right up against the device. In systems where a common supply is used to drive both the AVDD and DVDD of the AD9835, it is recommended that the system's AVDD supply be used. This supply should have the recommended analog supply decoupling between the AVDD pins of the AD9835 and AGND and the recommended digital supply decoupling capacitors between the DVDD pins and DGND.

Interfacing the AD9835 to Microprocessors

The AD9835 has a standard serial interface that allows the part to interface directly with several microprocessors. The device uses an external serial clock to write the data/control information into the device. The serial clock can have a frequency of 20 MHz maximum. The serial clock can be continuous or it can idle high or low between write operations. When data/control information is being written to the AD9835, FSYNC is taken low and held low while the 16 bits of data are being written into the AD9835. The FSYNC signal frames the 16 bits of information being loaded into the AD9835.

AD9835-to-ADSP-21xx Interface

Figure 24 shows the serial interface between the AD9835 and the ADSP-21xx. The ADSP-21xx should be set up to operate in the SPORT Transmit Alternate Framing Mode (TFSW = 1). The ADSP-21xx is programmed through the SPORT control register and should be configured as follows: Internal clock operation (ISCLK = 1), Active low framing (INVTFS = 1), 16-bit word length (SLEN = 15), Internal frame sync signal (ITFS = 1), Generate a frame sync for each write operation (TFSR = 1). Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. The data is clocked out on each rising edge of the serial clock and clocked into the AD9835 on the SCLK falling edge.

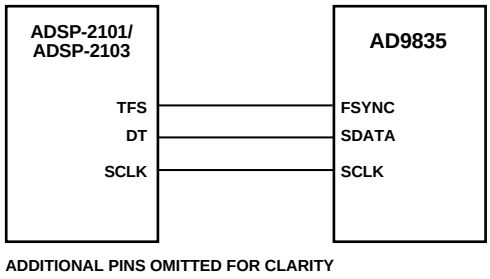


Figure 24. ADSP-2101/ADSP-2103-to-AD9835 Interface

AD9835-to-68HC11/68L11 Interface

Figure 25 shows the serial interface between the AD9835 and the 68HC11/68L11 microcontroller. The microcontroller is configured as the master by setting bit MSTR in the SPCR to 1 and, this provides a serial clock on SCK while the MOSI output drives the serial data line SDATA. Since the microcontroller does not have a dedicated frame sync pin, the FSYNC signal is derived from a port line (PC7). The setup conditions for correct operation of the interface are as follows: the SCK idles high between write operations (CPOL = 0), data is valid on the SCK falling edge (CPHA = 1). When data is being transmitted to the AD9835, the FSYNC line is taken low (PC7). Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight

falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. In order to load data into the AD9835, PC7 is held low after the first eight bits are transferred and a second serial write operation is performed to the AD9835. Only after the second eight bits have been transferred should FSYNC be taken high again.

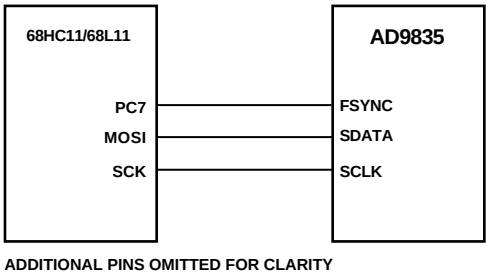


Figure 25. 68HC11/68L11-to-AD9835 Interface

AD9835-to-80C51/80L51 Interface

Figure 26 shows the serial interface between the AD9835 and the 80C51/80L51 microcontroller. The microcontroller is operated in Mode 0 so that TXD of the 80C51/80L51 drives SCLK of the AD9835 while RXD drives the serial data line SDATA. The FSYNC signal is again derived from a bit programmable pin on the port (P3.3 being used in the diagram). When data is to be transmitted to the AD9835, P3.3 is taken low. The 80C51/80L51 transmits data in 8-bit bytes thus, only eight falling SCLK edges occur in each cycle. To load the remaining eight bits to the AD9835, P3.3 is held low after the first eight bits have been transmitted and a second write operation is initiated to transmit the second byte of data. P3.3 is taken high following the completion of the second write operation. SCLK should idle high between the two write operations. The 80C51/80L51 outputs the serial data in a format which has the LSB first. The AD9835 accepts the MSB first (the 4 MSBs being the control information, the next 4 bits being the address while the 8 LSBs contain the data when writing to a destination register). Therefore, the transmit routine of the 80C51/80L51 must take this into account and rearrange the bits so that the MSB is output first.

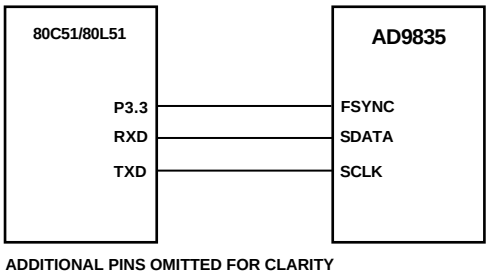


Figure 26. 80C51/80L51 to AD9835 Interface

AD9835-to-DSP56002 Interface

Figure 27 shows the interface between the AD9835 and the DSP56002. The DSP56002 is configured for normal mode asynchronous operation with a Gated internal clock (SYN = 0, GCK = 1, SCKD = 1). The frame sync pin is generated internally (SC2 = 1), the transfers are 16 bits wide (WL1 = 1, WL0 = 0) and the frame sync signal will frame the 16 bits (FSL = 0). The frame sync signal is available on pin SC2 but, it needs to be inverted before being applied to the AD9835. The interface to the DSP56000/DSP56001 is similar to that of the DSP56002.

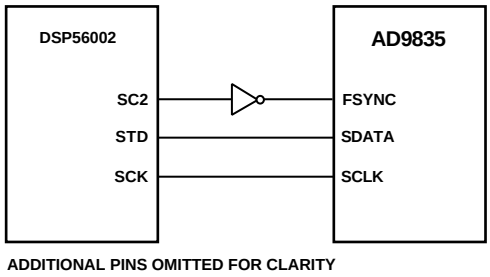


Figure 27. AD9835-to-DSP56002 Interface

AD9835 Evaluation Board

The AD9835 Evaluation Board allows designers to evaluate the high performance AD9835 DDS Modulator with a minimum of effort.

To prove that this device will meet the user's waveform synthesis requirements, the user only requires a 5 V power supply, an IBM-compatible PC and a spectrum analyzer along with the evaluation board. The evaluation setup is shown below.

The DDS Evaluation kit includes a populated, tested AD9835 printed circuit board along with the software that controls the AD9835 in a Windows® environment.

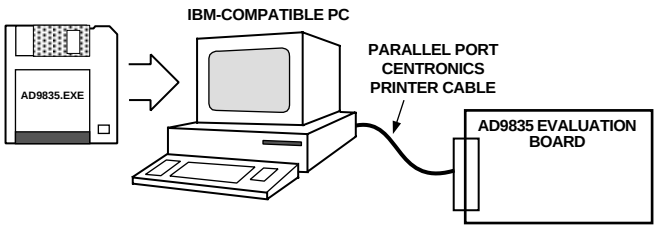


Figure 28. AD9835 Evaluation Board Setup

Using the AD9835 Evaluation Board

The AD9835 Evaluation kit is a test system designed to simplify the evaluation of the AD9835. Provisions to control the AD9835 from the printer port of an IBM-compatible PC are included along with the necessary software. An application note is also available with the evaluation board which gives information on operating the evaluation board.

Prototyping Area

An area is available on the evaluation board where the user can add additional circuits to the evaluation test set. Users may want to build custom analog filters for the output or add buffers and operational amplifiers to be used in the final application.

XO vs. External Clock

The AD9835 can operate with master clocks up to 50 MHz. A 50 MHz oscillator is included on the evaluation board. However, this oscillator can be removed and an external CMOS clock connected to the part, if required.

Power Supply

Power to the AD9835 Evaluation Board must be provided externally through the pin connections. The power leads should be twisted to reduce ground loops.

Windows is a registered trademark of Microsoft Corporation.

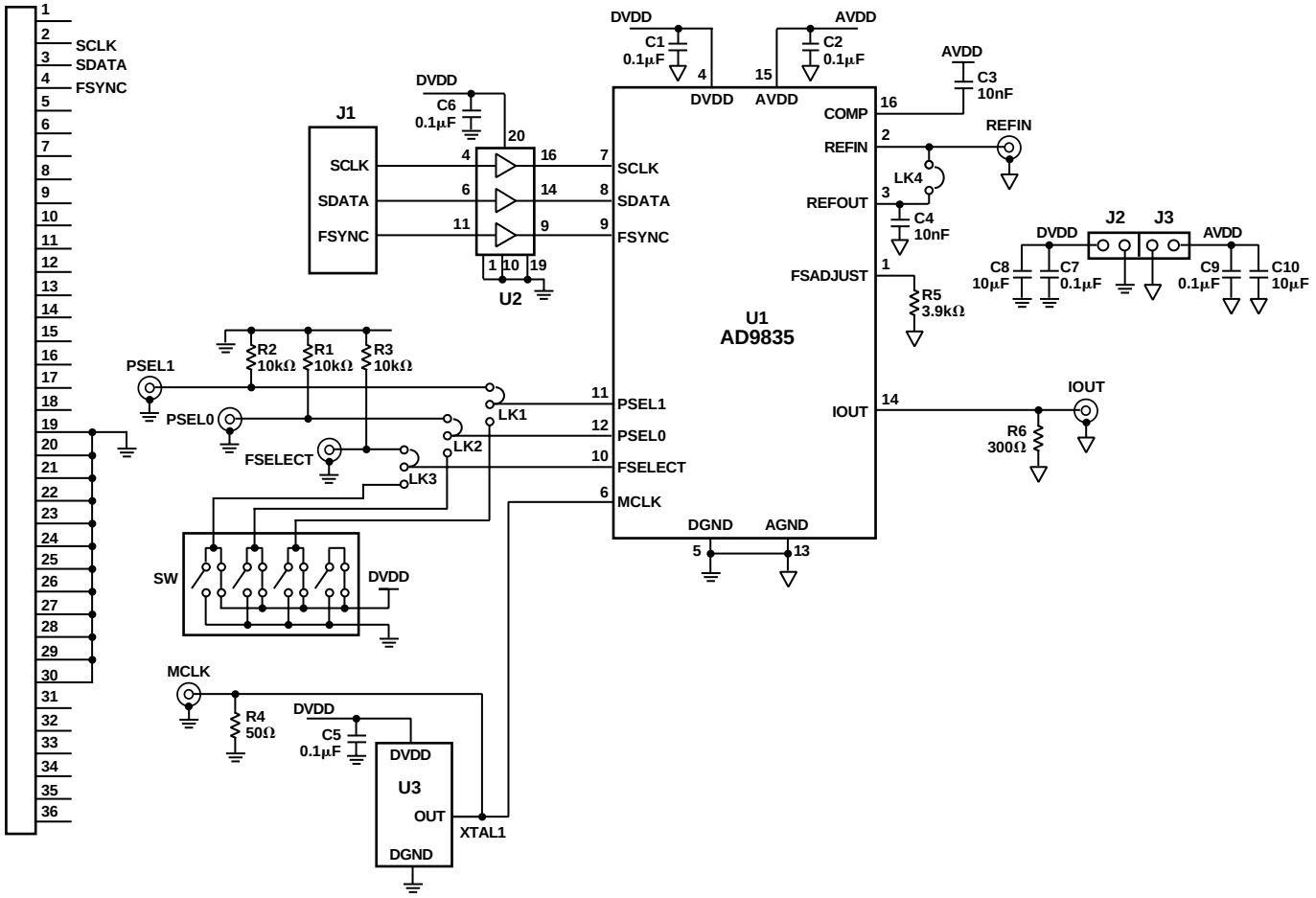


Figure 29. Evaluation Board Layout

Integrated Circuits

XTAL1	OSC XTAL 50 MHz
U1	AD9835 (16-Lead TSSOP)
U2	74HCT244 Buffer

Capacitors

C1, C2	0.1 µF Ceramic Chip Capacitor
C3, C4	10 nF Ceramic Capacitor
C5, C6, C7, C9	0.1 µF Ceramic Capacitor
C8, C10	10 µF Tantalum Capacitor

Resistors

R1–R3	10 kΩ Resistor
R4	50 Ω Resistor
R5	3.9 kΩ Resistor
R6	300 Ω Resistor

Links

LK1–LK3	Three Pin Link
LK4	Two Pin Link

Switch

SW	End Stackable Switch (SDC Double Throw)

Sockets

MCLK, PSEL0, PSEL1, FSELECT, IOUT, REFIN	Subminiature BNC Connector

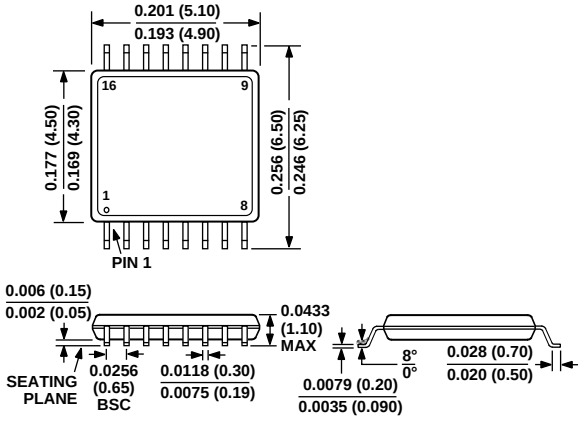
Connectors

J1	36-Pin Edge Connector
J2, J3	PCB Mounting Terminal Block

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead Thin Shrink Small Outline Package (TSSOP)
(RU-16)



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