National Semiconductor

Comlinear CLC423
94MHz, Single Supply Voltage Feedback Op Amp

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General Description

The Comlinear CLC423 is a wideband voltage-feedback operational amplifier that is uniquely designed to provide high performance from a single power supply. The CLC423 provides near rail-to-rail operation and the common-mode input range includes the negative rail. The CLC423 offers plenty of headroom for single-supply applications as evidenced by its 4.3V_{pp} output voltage from a single 5V supply.

Fabricated with a high-speed complementary bipolar process, the CLC423 delivers a wide 94MHz unity-gain bandwidth, 7.5ns rise/fall time and 150V/µs slew rate. For single supply applications such as video distribution or desktop multimedia, the CLC423 offers low 0.35%, 0.55° differential gain and phase errors.

The CLC423 provides high signal fidelity with -74/-94dBc 2nd/3rd harmonics (1V_{pp}, 1MHz, R_L=150Ω). Combining this high fidelity performance with CLC423's quick 46ns settling time to 0.1% makes it an excellent choice for ADC buffering.

With its traditional voltage-feedback architecture and high-speed performance, the CLC423 is the perfect choice for composite signal conditioning circuit functions such as active filters, integrators, differentiators, simple gain blocks and buffering.

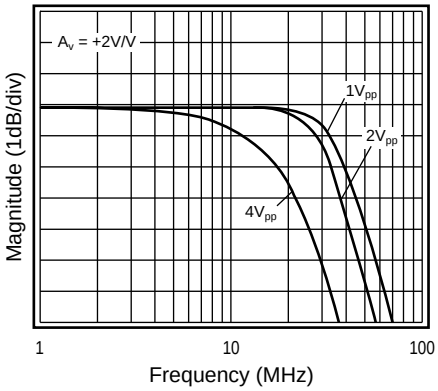
Features

- Single +5V supply
- Input includes V_{EE}
- 94MHz unity-gain bandwidth
- -74/-94dBc HD2/HD3
- 60mA output current
- 7.5ns rise/fall time (1V_{pp})
- 46ns settling time to 0.1%

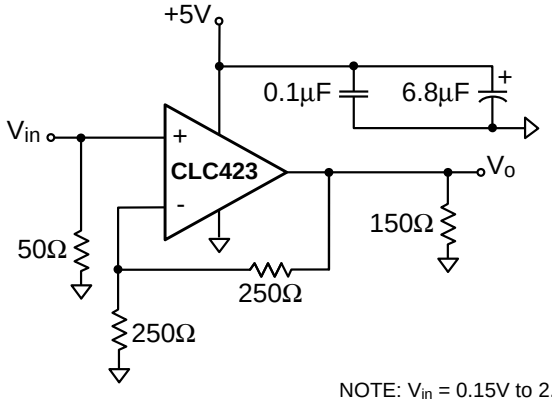
Applications

- Video ADC driver
- Desktop multimedia
- Single supply cable driver
- Instrumentation
- Video cards
- Wireless IF amplifiers
- Telecommunications

Frequency Response vs. V_{out}

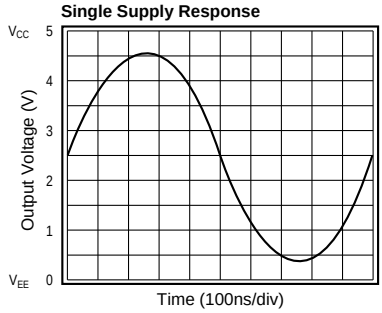


Typical Application
Single +5V Supply operation

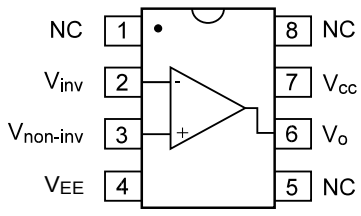


NOTE: V_{in} = 0.15V to 2.3V

Single Supply Response



Pinout
DIP & SOIC



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Electrical Characteristics (V_s = +5V[1], V_{cm} = +2.5V, A_V = +2, R_f = 250Ω, R_L = 150Ω to GND; unless specified)

PARAMETERS	CONDITIONS	TYP	MIN/MAX RATINGS			UNITS	NOTES
	CLC423AJ	25°	25°	0° to +70°	-40° to +85°		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	V_o < 1.0V_{pp}	48	32	28	27	MHz	B
-3dB bandwidth	V_o < 3.0V_{pp}	26	16	14	11	MHz	
-3dB bandwidth A_V = +1V/V	V_o < 1.0V_{pp}	94				MHz	
rolloff	<10MHz	0.1	0.5	0.7	0.8	dB	B
peaking	DC to 200MHz	0	0.5	0.7	0.8	dB	B
linear phase deviation	<15MHz	0.3	0.6	0.8	0.9	deg	
differential gain	NTSC, R_L=150Ω	0.35	0.7	–	–	%	2
differential phase	NTSC, R_L=150Ω	0.55	2	–	–	deg	2
TIME DOMAIN RESPONSE							
rise and fall time	1V step	7.5	13	14	16	ns	
settling time to 0.1%	1V step	46	70	–	–	ns	
overshoot	1V step	5	13	–	–	%	
slew rate A_V = +2	2V step	150	90	83	65	V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	1V_{pp}, 1MHz	74	–	–	–	-dBc	
	1V_{pp}, 5MHz	62	55	52	52	-dBc	B
3rd harmonic distortion	1V_{pp}, 1MHz	94	–	–	–	-dBc	
	1V_{pp}, 5MHz	75	65	63	62	-dBc	B
equivalent input noise							
voltage	>1MHz	10	12.5	13.6	14	nV/√Hz	
current	>1MHz	4	5	5.5	5.7	pA/√Hz	
STATIC DC PERFORMANCE							
input offset voltage		2	7	8	10	mV	A
average drift		4	–	22	35	µV/°C	
input bias current		17	30	36	45	µA	A
average drift		80	–	145	175	nA/°C	
input offset current		0.2	5	6	7.5	µA	
average drift		10	–	22	27	nA/°C	
power supply rejection ratio	DC	82	65	64	60	dB	B
common-mode rejection ratio	DC	82	55	53	50	dB	
supply current	no load	7	8.5	8.5	8.5	mA	A
MISCELLANEOUS PERFORMANCE							
input capacitance		1	2	2	2	pF	
input resistance		700	500	450	360	kΩ	
output impedance	@DC	0.07	0.15	0.24	0.7	Ω	
input voltage range, high		3.7	3.45	3.25	3.15	V	
input voltage range, low		0	0	0	0	V	
output voltage range, high	R_L = 150Ω	4.5	4.35	4.3	4.2	V	
output voltage range, low	R_L = 150Ω	0.35	0.5	0.5	0.55	V	
output voltage range, high	no load	4.8	4.6	4.55	4.45	V	
output voltage range, low	no load	0.45	0.65	0.7	0.75	V	
output current	source	60	50	40	34	mA	
output current	sink	36	20	16	10	mA	
supply voltage, maximum			7	7	7	V	1
supply voltage, minimum			4	4	4	V	1

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

supply voltage (V_s)	+7V
I_{out} is short circuit protected to ground	
common-mode input voltage	V_{EE} to V_{CC}
maximum junction temperature	+175°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+260°C
differential input voltage	±2V
EDS tolerance (Note 3)	4000V

Notes

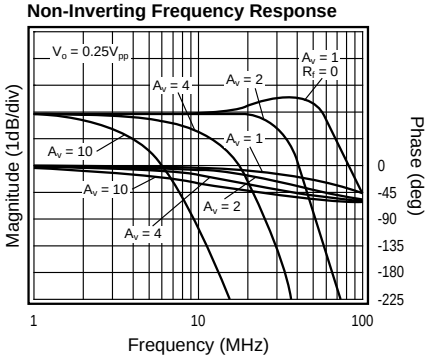
A) J-level: spec is 100% tested at 25°C, sample tested at 85°C.
B) J-level: spec is sample tested at 25°C.
1) $V_s = V_{CC} – V_{EE}$.
2) Tested with R_L tied to +2.5V.
3) Human body model, 1.5kΩ in series with 100pF.

Reliability Information

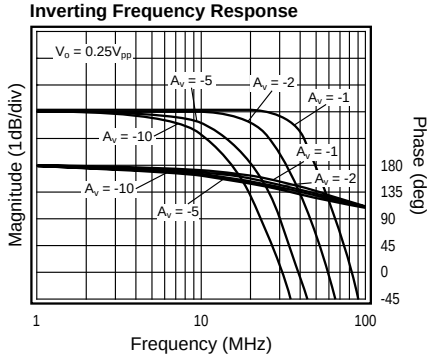
transistor count	62
MTBF	823Mhr

Typical Performance Characteristics (V_s = +5V[1], V_{cm} = +2.5V, A_V = +2, R_f = 250Ω, R_L = 150Ω to GND; unless specified)

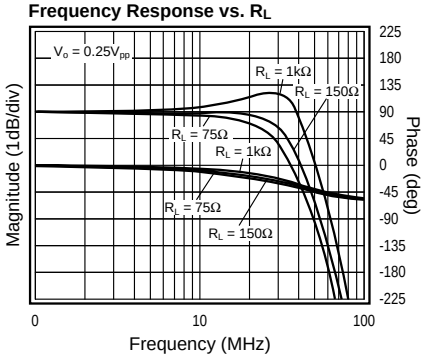
Non-Inverting Frequency Response



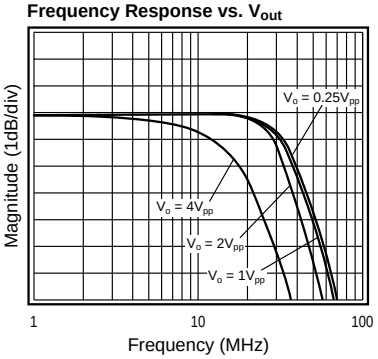
Inverting Frequency Response



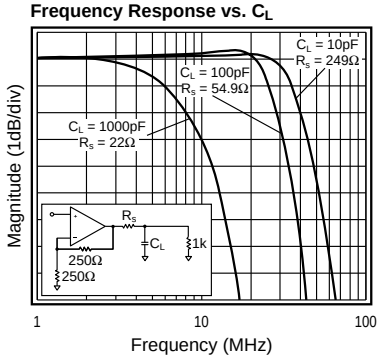
Frequency Response vs. R_L



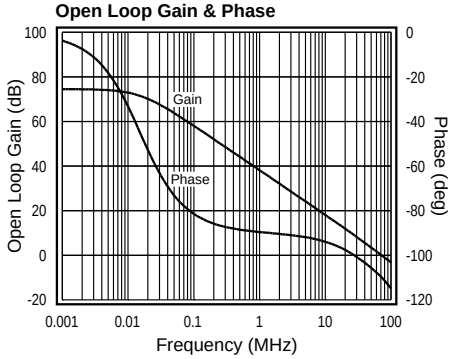
Frequency Response vs. V_{out}



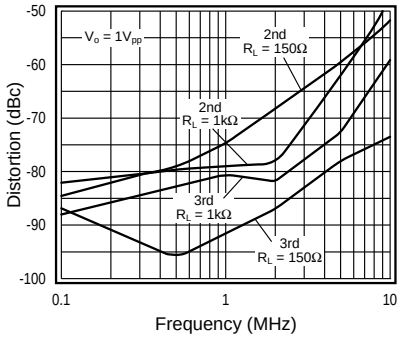
Frequency Response vs. C_L



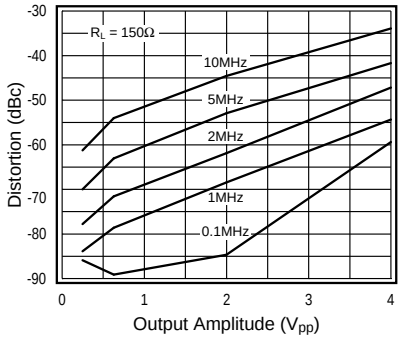
Open Loop Gain & Phase



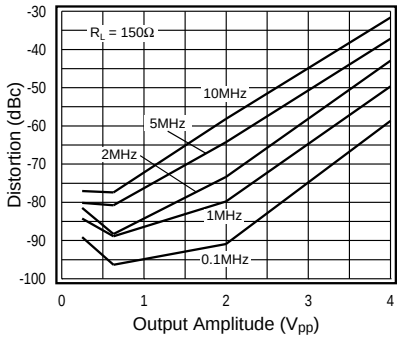
Harmonic Distortion vs. Frequency



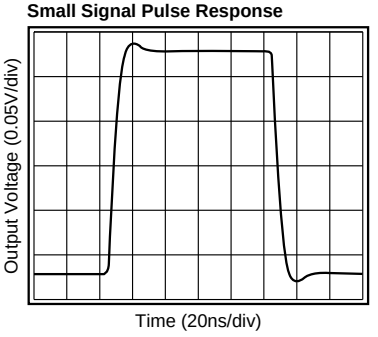
2nd Harmonic Distortion vs. V_{out}



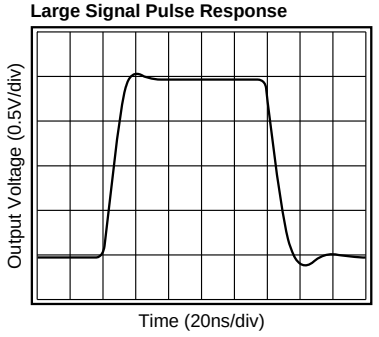
3rd Harmonic Distortion vs. V_{out}



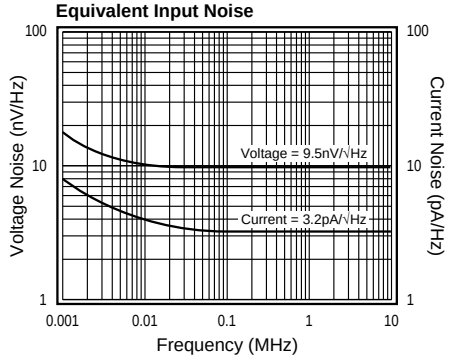
Small Signal Pulse Response



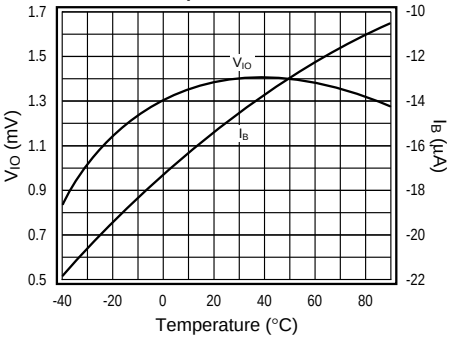
Large Signal Pulse Response



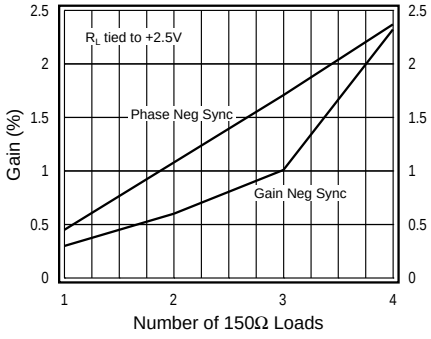
Equivalent Input Noise



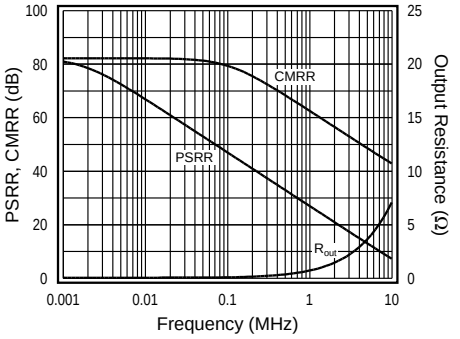
I_B, V_{IO}, vs. Temperature



Differential Gain and Phase (3.58MHz)



PSRR, CMRR & Linear R_{out} vs. Frequency



CLC423 OPERATIONS

Description

The CLC423 is a voltage feedback amplifier designed for single supply operation. The CLC423 is a single version of the CLC427 with the following features:

- Operates from a single +5V supply
- Maintains near rail-to-rail performance
- Includes the negative rail (0V) in the Common Mode Input Range (CMIR)
- Offers low -74/-94dBc 2nd and 3rd harmonic distortion
- Provides BW > 20MHz and 1MHz distortion < -50dBc at $V_o = 4V_{pp}$

Single Supply Operation (V_{CC} = +5V, V_{EE} = GND)

The CLC423 is designed to operate from 0 and 5V supplies. The specifications given in the ***Electrical Characteristics*** table are measured with a common mode voltage (V_{cm}) of 2.5V. V_{cm} is the voltage around which the inputs are applied and the output voltages are specified.

Operating from a single +5V supply, the CMIR of the CLC423 is typically 0V to +3.7V. The typical output range with $R_L = 150\Omega$ is +0.35V to +4.5V.

For DC coupled single supply operation, it is recommended that input signal levels remain above ground. For input signals that drop below ground, AC coupling and level shifting the signal are possible remedies. For input signals that remain above ground, no adjustments need to be made. The non-inverting and inverting configurations for both input conditions are illustrated in the following 2 sections.

DC Coupled Single Supply Operation

Figures 1 and 2 show the recommended non-inverting and inverting configurations for purely positive input signals.

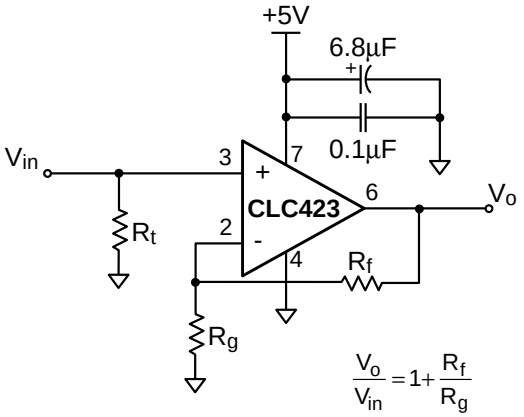


Figure 1: Non-inverting Configuration

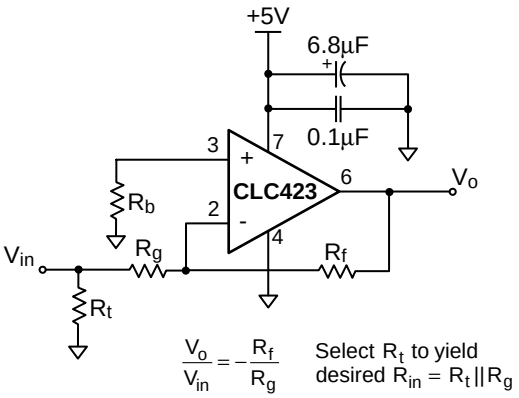


Figure 2: Inverting Configuration

AC Coupled Single Supply Operation

Figures 3 and 4 show possible non-inverting and inverting configurations for input signals that go below ground. The input is AC coupled to prevent the need for level shifting the input signal at the source. The resistive voltage divider biases the non-inverting input to $V_{CC} \div 2 = 2.5V$.

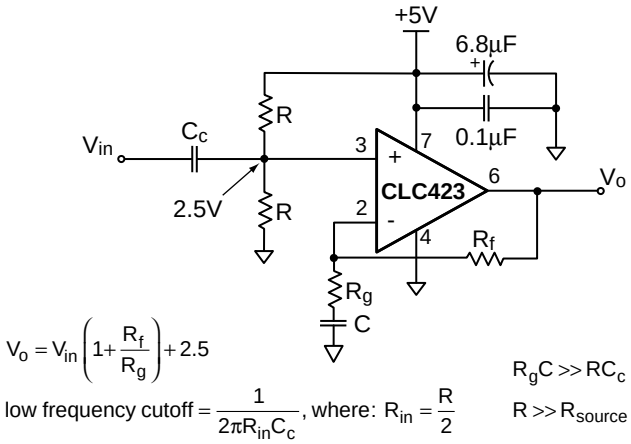


Figure 3: AC Coupled Non-inverting Configuration

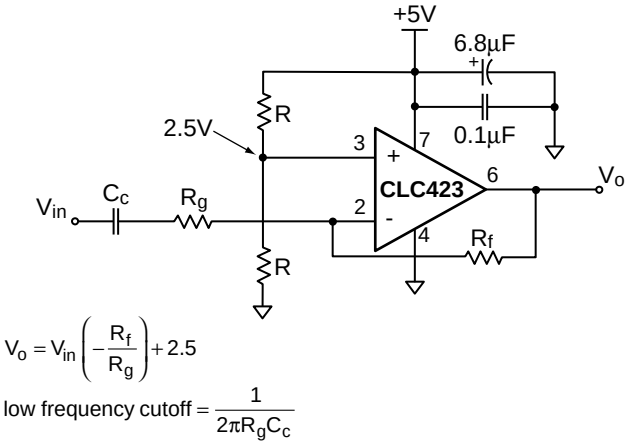


Figure 4: AC Coupled Inverting Configuration

Load Termination

Since the CLC423 design has been optimized for Single Supply Operation, it is more capable of sourcing rather than sinking current. For optimum performance, the load should be tied to V_{EE}. When the load is tied to V_{EE}, the output always sources current.

Output Overdrive Recovery

When the output range of an amplifier is exceeded, time is required for the amplifier to recover from this over driven condition. Figure 5 illustrates the overload recovery of the CLC423 when the output is overdriven. An input was applied in an attempt to drive the output to twice the supply rails ($2 \cdot (V_{CC} - V_{EE}) = 10V$), but the output limits. An inverting gain topolgy was used, see Figure 2. As indicated, the CLC423 recovers within 25ns on the rising edge and within 10ns on the falling edge.

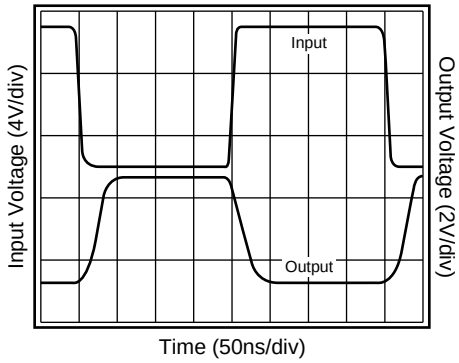


Figure 5: Overdrive Recovery

Driving Cables and Capacitive Loads

When driving cables, double termination is used to prevent reflections. For capacitive load applications, a small series resistor at the output of the CLC423 will improve stability and settling performance. The ***Frequency Response vs. C_L*** plot, in the typical performance section, gives the recommended series resistance value for optimum flatness at various capacitive loads.

Transmission Line Matching

One method for matching the characteristic impedance (Z_o) of a transmission line or cable is to place the appropriate resistor at the input or output of the amplifier. Figure 6 shows typical inverting and non-inverting circuit configurations for matching transmission lines.

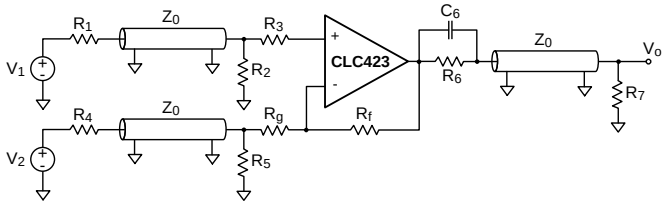


Figure 6: Transmission Line Matching

Non-inverting gain applications:

- Connect R_g directly to ground.
- Make R_1, R_2, R_6, and R_7 equal to Z_o.
- Use R_3 to isolate the amplifier from reactive loading caused by the transmission line, or by parasitics.

Inverting gain applications:

- Connect R_3 directly to ground.
- Make the resistors R_4, R_6, and R_7 equal to Z_o.
- Make R_5 II $R_g = Z_o$.

The input and output matching resistors attenuate the signal by a factor of 2, therefore additional gain is needed. Use C_6 to match the output transmission line over a greater frequency range. C_6 compensates for the increase of the amplifier's output impedance with frequency.

Power Dissipation

Follow these steps to determine the power consumption of the CLC423:

1. Calculate the quiescent (no-load) power:
   $P_{amp} = I_{CC} (V_{CC} - V_{EE})$
2. Calculate the RMS power at the output stage:
   $P_o = (V_{CC} - V_{load}) (I_{load})$, where V_{load} and I_{load} are the RMS voltage and current across the external load.
3. Calculate the total RMS power:
   $P_t = P_{amp} + P_o$

The maximum power that the DIP and SOIC packages can dissipate at a given temperature is illustrated in Figure 7. The power derating curve for any package can be derived by utilizing the following equation:

$$\frac{(175° - T_{amb})}{\theta_{JA}}$$

where:

T_{amb} = Ambient temperature (°C)

θja = Thermal resistance, from junction to ambient, for a given package (°C/W)

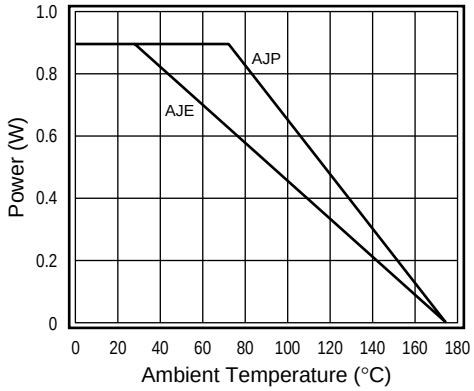


Figure 7: Power Derating Curves

Layout Considerations
A proper printed circuit layout is essential for achieving high frequency performance. Comlinear provides evaluation boards for the CLC423 (730013 - DIP, 730027-SOIC) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization.

General layout and supply bypassing play major roles in high frequency performance. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF tantalum and 0.1µF ceramic capacitors on both supplies.
- Place the 6.8µF capacitors within 0.75 inches of the power pins.
- Place the 0.1µF capacitors less than 0.1 inches from the power pins.
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.
- Use flush-mount printed circuit board pins for prototyping, never use high profile DIP sockets.

Evaluation Board Information
A data sheet is available for the CLC730013 and CLC730027 evaluation boards. This 8-pin op amp evaluation board data sheet provides:

- Evaluation board schematics
- Evaluation board layouts for both DIP and SOIC boards
- General information about the boards

The data sheet also contains tables of recommended components to evaluate several of Comlinear's high speed amplifiers. This table for the CLC423 is illustrated below. Refer to the evaluation board data sheet for schematics and further information.

Components Needed to Evaluate the CLC423 on the Evaluation Board:

- R_f, R_g - Use this product data sheet to select values
- R_{in}, R_{out} - Typically 50Ω (Refer to the ***Basic Operation*** section of the evaluation board data sheet for details)
- R_t - Optional resistor for inverting gain configurations (Select R_t to yield desired input impedance = R_g || R_t)
- C_1, C_2 - 0.1µF ceramic capacitors
- C_3, C_4 - 6.8µF tantalum capacitors

Components not used:

- C_5, C_6, C_7, C_8
- R_1 thru R_8

The evaluation boards are designed to accommodate dual supplies. The boards can be modified to provide single supply operation. For best performance; 1) do not connect the unused supply, 2) provide a wide jumper across C_2. Use a jumper that is equal in width to the trace connecting pin 4 to C_2. This will minimize any additional inductance caused by the jumper.

SPICE Models
SPICE models provide a means to evaluate amplifier designs. Free SPICE models are available for Comlinear's monolithic amplifiers that:

- Support Berkeley SPICE 2G and its many derivatives
- Reproduce typical DC, AC, Transient, and Noise performance
- Support room temperature simulations

The ***readme*** file that accompanies the diskette lists released models, and provides a list of modeled parameters. The application note OA-18, Simulation SPICE Models for Comlinear's Op Amps, contains schematics and a reproduction of the readme file.

Applications Circuits

Typical Application Circuit
The typical application shown on the front page illustrates the near rail-to-rail performance of the CLC423.

Single Supply Cable Driver
Figure 8 illustrates the CLC423 in a typical single supply cable driving application. The CLC423 is set for a gain of +2V/V to compensate for the divide-by-two voltage drop at V_o.

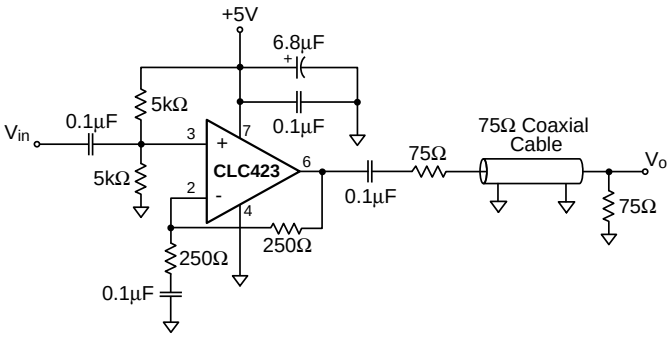
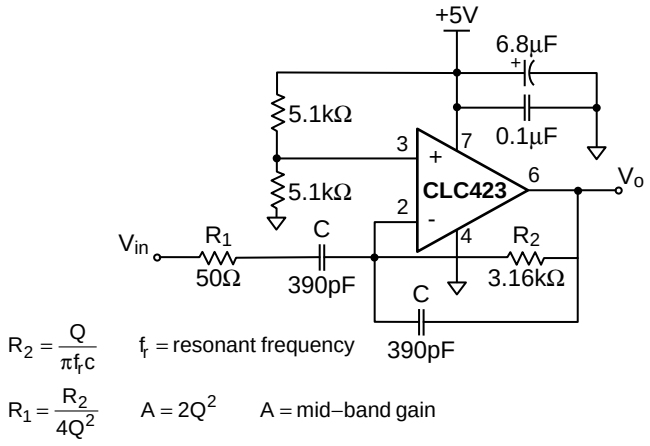


Figure 8: Single Supply Cable Driver

Multiple Feedback Bandpass Filter
Figure 9 illustrates a bandpass filter and design equations. The circuit operates from a single supply of +5V. The voltage divider biases the non-inverting input to 2.5V. The input is AC coupled to prevent the need for level shifting the input signal at the source. Use the design equations to determine R_1 and R_2 based on the desired Q and center frequency.

This example illustrates a bandpass filter with Q = 4 and center frequency f_c = 1MHz. Figure 10 indicates the filter response.



$R_2 = \frac{Q}{\pi f_r c}$ f_r = resonant frequency

$R_1 = \frac{R_2}{4Q^2}$ $A = 2Q^2$ A = mid−band gain

Figure 9: Bandpass Filter Topology

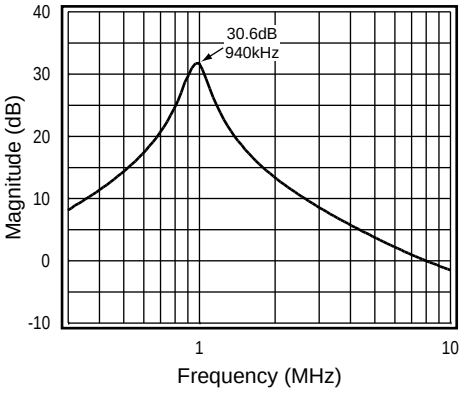


Figure 10: Bandpass Response

Ordering Information

Model	Temperature Range	Description
CLC423AJP	-40°C to +85°C	8-pin PDIP
CLC423AJE	-40°C to +85°C	8-pin SOIC

Package Thermal Resistance

Package	θ_{JC}	θ_{JA}
Plastic (AJP)	100°C/W	15°C/W
Surface Mount (AJE)	145°C/W	165°C/W

Customer Design Applications Support

National Semiconductor is committed to design excellence. For sales, literature and technical support, call the National Semiconductor Customer Response Group at **1-800-272-9959** or fax **1-800-737-7018**.

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1. Life support devices or systems are devices or systems which, a) are intended for surgical implant into the body, or b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
E-mail: europe.support.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Francais Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block
Ocean Centre, 5 Canton Road
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

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