DATA SHEET

TDA9183
Integrated NTSC comb filter

Objective specification
Supersedes data of 2000 Nov 22
File under Integrated Circuits, IC02

2000 Nov 30

Philips
Semiconductors

PHILIPS

Integrated NTSC comb filter TDA9183

FEATURES

- One-chip NTSC adaptive comb filter
- Cross luminance reduction
- Cross colour reduction
- No chroma trap, therefore sharper vertical luminance transients
- Analog discrete-time signal processing, therefore no quantization noise
- Anti-aliasing and reconstruction filters are included
- Input switch selects between two Y/CVBS inputs
- Output switch selects between combed CVBS and an external Y/C source
- f_{SC} as well as $2 \times f_{SC}$ colour subcarrier signal may be applied
- Alignment free
- Few external components
- Low power.

GENERAL DESCRIPTION

The TDA9183 is a an adaptive NTSC comb filter with two internal delay lines, filters, clock control and input clamps. The NTSC M video standard is supported.

Two CVBS input signals can be selected by means of an input switch.

The selected CVBS input signal is filtered to obtain a combed luminance output signal and a combed chrominance output signal. Switched capacitor circuit techniques are used, requiring an internal clock, locked on to the colour subcarrier frequency.

The colour subcarrier frequency as well as twice the colour subcarrier frequency may be applied to the IC.

In addition to the comb filter the circuit contains an output switch so that a selection can be made between the combed CVBS signal and an external Y/C signal.

The IC is available in a DIP16 and SO16 package. The supply voltage is 5 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
I_{CCA}	analog supply current	–	25	–	mA
V_{DDD}	digital supply voltage	4.5	5.0	5.5	V
I_{DDD}	digital supply current	–	10	–	mA
$V_{i(Y/CVBS)(p-p)}$	luminance or CVBS input signal voltage (peak-to-peak value)	0.7	1.0	1.4	V
$V_{i(CIN)(p-p)}$	chrominance input signal voltage (peak-to-peak value)	–	0.7	1.0	V
$V_{i(FSC)(p-p)}$	colour subcarrier input signal voltage (peak-to-peak value)	100	200	400	mV
$V_{o(Y/CVBS)(p-p)}$	luminance or CVBS output signal voltage (peak-to-peak value)	0.6	1.0	1.54	V
$V_{o(CIN)(p-p)}$	chrominance output signal voltage (peak-to-peak value)	–	0.7	1.1	V

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9183P	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-4
TDA9183T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

BLOCK DIAGRAM

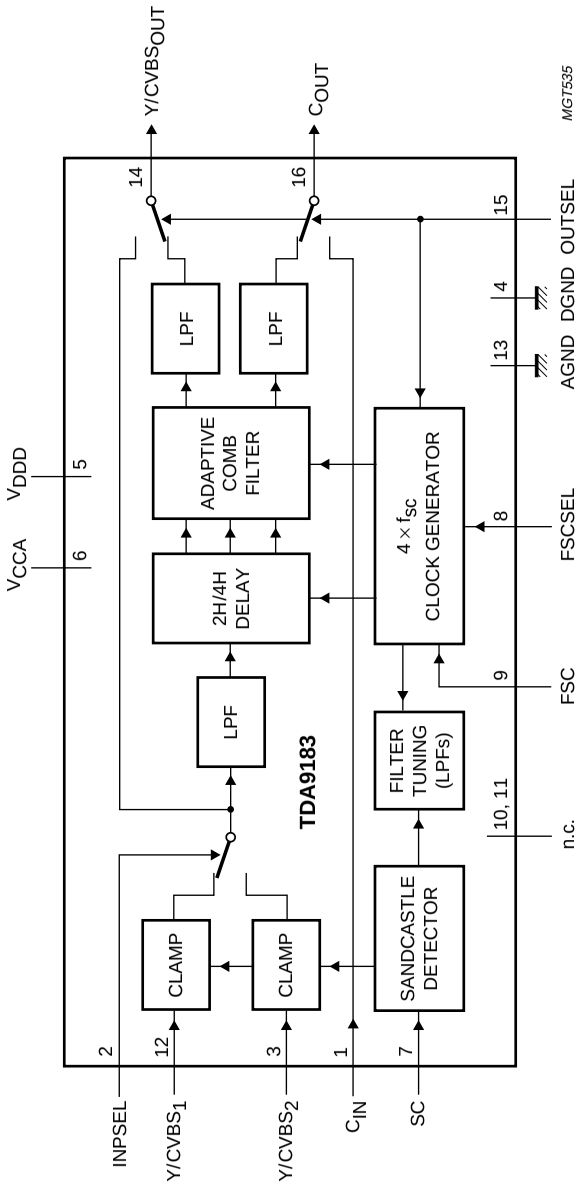


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
C_{IN}	1	chrominance signal input
INPSEL	2	input switch select input
$Y/CVBS_2$	3	luminance or CVBS signal 2 input
DGND	4	digital ground
V_{DDD}	5	digital supply voltage
V_{CCA}	6	analog supply voltage
SC	7	sandcastle signal input
FSCSEL	8	colour subcarrier select input
FSC	9	colour subcarrier signal input
n.c.	10	not connected
n.c.	11	not connected
$Y/CVBS_1$	12	luminance or CVBS signal 1 input
AGND	13	analog ground (signal reference)
$Y/CVBS_{OUT}$	14	luminance or CVBS signal output
OUTSEL	15	output switch select input
C_{OUT}	16	chrominance signal output

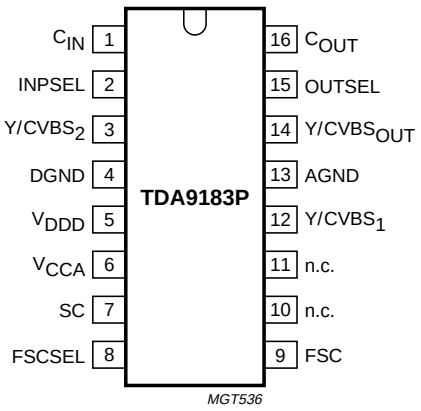


Fig.2 Pin configuration (DIP16).

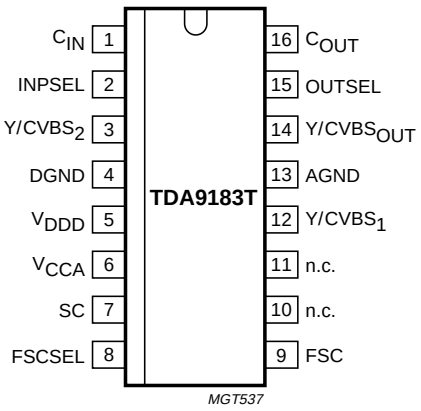


Fig.3 Pin configuration (SO16).

FUNCTIONAL DESCRIPTION

Input configuration

The $Y/CVBS_1$ and $Y/CVBS_2$ input signals are clamped by means of an internally generated clamp pulse which is derived from the sandcastle input signal (pin SC). If no sandcastle signal is available, a clamp pulse signal may be applied to pin SC. External clamp capacitors are needed.

The buffered and clamped $Y/CVBS_1$ and $Y/CVBS_2$ signals are then applied to the input switch. The input switch select signal (INPSEL) determines whether $Y/CVBS_1$ or $Y/CVBS_2$ is passed through to the anti-alias low-pass filter. This 3rd-order low-pass filter is optimized for best performance with respect to step response and clock suppression. The filtered signal is sampled at a clock frequency of four times the colour subcarrier frequency (f_{SC}).

A colour subcarrier frequency signal is applied to pin FSC. The colour subcarrier select input signal (FSCSEL) indicates whether the colour subcarrier frequency (f_{SC}) or twice the colour subcarrier frequency ($2 \times f_{SC}$) is being applied at the FSC input. An external coupling capacitor is needed for the colour subcarrier input signal.

Comb filter

The sampled CVBS signal is applied to two delay lines. One delay line delays the signal over 1H (1H = one line-time).

The direct and delayed signals are applied to an adaptive comb filter. The adaptive comb filter performs band-pass filtering around the colour subcarrier frequency and compares the contents of adjacent lines. In this way the combing of signals with different information is prevented and artifacts such as hanging dots are avoided.

Both the combed chrominance and the combed luminance signal are passed through a reconstruction low-pass filter to obtain continuous-time signals. These low-pass filters are 3rd-order, optimized for best performance with respect to step response and clock suppression. The reconstructed signals are applied to the output switches.

Output configuration

The luminance output switch selects between the reconstructed combed luminance signal and one of the buffered and clamped input signals $Y/CVBS_1$ or $Y/CVBS_2$. The chrominance output switch selects between the reconstructed combed chrominance signal and the chrominance input signal (C_{IN}). An external coupling capacitor is needed for C_{IN}. The selected signals are applied to the outputs $Y/CVBS_{OUT}$ and C_{OUT} respectively via a buffer stage. The output switch signal (OUTSEL) determines whether the output switches select the internal combed signals or the external Y/C signals.

Clock generation and filter tuning

The clock generator is driven by a Phase-Locked Loop (PLL) circuit which generates a reference frequency of four times the colour subcarrier frequency. This PLL circuit is phase-locked to the colour subcarrier input signal (FSC). Several internal clock signals are derived from the $4 \times f_{SC}$ reference.

The filter tuning ensures the automatic alignment of the anti-alias and the reconstruction low-pass filters. A $4 \times f_{SC}$ clock signal is used as a reference for the alignment. The tuning takes place each line during the line blanking and is initiated by means of an internally generated signal which is derived from the sandcastle input signal.

If the output switches select external Y/C signals the oscillator of the PLL circuit is stopped regardless of the FSC input and no internal clock signals are generated. The filter tuning is also stopped.

Mode definitions

Table 1 General mode definitions; note 1

PIN OUTSEL	MODE
LOW	COMB
HIGH	YC

Note

1. If the OUTSEL pin is left open-circuit, the pin is pulled LOW by means of an internal pull-down resistor to analog ground (AGND). Thus the COMB mode can also be selected by not connecting the OUTSEL pin.

Table 2 $Y/CVBS_{OUT}$ output signal definitions

MODE	$Y/CVBS_{OUT}$ OUTPUT SIGNAL
COMB	comb filtered luminance signal
YC	$Y/CVBS_1$ or $Y/CVBS_2$ signal

Table 3 C_{OUT} output signal definitions

MODE	C_{OUT} OUTPUT SIGNAL
COMB	comb filtered chrominance signal
YC	C_{IN} signal

Table 4 Input switch mode definitions; note 1

PIN INPSEL	INPUT SWITCH MODE
LOW	$Y/CVBS_1$ input selected
HIGH	$Y/CVBS_2$ input selected

Note

1. If the INPSEL pin is left open-circuit, the pin is pulled LOW by means of an internal pull-down resistor to analog ground (AGND). Thus the $Y/CVBS_1$ input can also be selected by not connecting the INPSEL pin.

Table 5 FSC mode definitions; note 1

PIN FSCSEL	FSC INPUT SIGNAL FREQUENCY
LOW	f_{SC}
HIGH	$2 \times f_{SC}$

Note

1. If the FSCSEL pin is left open-circuit, the pin is pulled LOW by means of an internal pull-down resistor to analog ground (AGND). Thus the f_{SC} mode can also be selected by not connecting the FSCSEL pin.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage		–	5.5	V
V_{CCA}	analog supply voltage		–	5.5	V
$V_{i(prot)(th)}$	input voltage protection threshold		–0.3	V_{DD} + 0.3	V
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	ambient temperature		–25	+70	°C
T_{sol}	soldering temperature	for 5 s	–	260	°C
T_j	junction temperature		–	150	°C
V_{es}	electrostatic handling voltage	HBM; all pins, except pins 5 and 6; notes 1, 2 and 3	–3000	+3000	V
		MM; all pins, except pins 5 and 6; notes 1, 4 and 5	–300	+300	V

Notes

1. All pins are protected against ESD by means of internal clamping diodes.
2. Human Body Model (HBM): R = 1.5 kΩ; C = 100 pF.
3. Pins 5 (V_{DDD}) and 6 (V_{CCA}): HBM: $-1500\ V < V_{es} < +1500\ V$.
4. Machine Model (MM): R = 0 Ω; C = 200 pF.
5. Pins 5 (V_{DDD}) and 6 (V_{CCA}): MM: $-150\ V < V_{es} < +150\ V$.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	TDA9183P		75	K/W
	TDA9183T		95	K/W

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611E"*.

Latch-up

At an ambient temperature of 70 °C all pins meet the following specification:

- $I_{trigger} \geq 100$ mA or $V_{trigger} \geq 1.5V_{DD(max)}$
- $I_{trigger} \leq -100$ mA or $V_{trigger} \leq -0.5V_{DD(max)}$.

CHARACTERISTICS

V_{CCA} = V_{DDD} = 5 V; T_{amb} = 25 °C; input signal Y/$CVBS_1$ = 1 V (p-p); input signal Y/$CVBS_2$ = 1 V (p-p); input signal C_{IN} = 0.7 V (p-p); input signal FSC = 200 mV (p-p) sine wave at f_{SC}; input signal SC = 5 V (p-p) sandcastle signal; test signal: 100% white 75% amplitude FCC colour bar; source impedance for Y/$CVBS_1$ and Y/CVBS = 75 Ω; coupled with 10 nF; source impedance for C_{IN} and FSC = 75 Ω; coupled with 100 nF; load impedance for CVBS/Y_{OUT} and C_{OUT} = 15 pF to analog ground (pin AGND); all voltages are related to analog ground (pin AGND); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current		–	25	–	mA
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDD}	digital supply current		–	10	–	mA
P	power dissipation		–	175	–	mW
Luminance or CVBS input 1 and 2; pins Y/$CVBS_1$ and Y/$CVBS_2$						
$V_{i(Y/CVBS)(p-p)}$	luminance or CVBS input voltage (peak-to-peak value)	including sync	0.7	1.0	1.4	V
$t_{clamp(Y/CVBS)}$	clamp time constant		–	20	–	lines
$I_{i(Y/CVBS)}$	input current	during clamping	–10	0	+10	μA
		during active video	–10	0	+10	nA
Chrominance input; pin C_{IN}						
$V_{i(CIN)(p-p)}$	chrominance input voltage (peak-to-peak value)		–	0.7	1.0	V
$R_{i(CIN)}$	input resistance		30	–	–	kΩ
Colour subcarrier input; pin FSC						
$V_{i(FSC)(p-p)}$	subcarrier input voltage (peak-to-peak value)		100	200	400	mV
D	duty cycle	square wave	40	50	60	%
$R_{i(FSC)}$	input resistance		30	–	–	kΩ
Sandcastle input; pin SC						
$V_{i(SC)}$	sandcastle input voltage	no clamping	–	–	3.3	V
		clamping	3.7	–	–	V
t_W	pulse width	clamping; note 1	2.6	–	–	μs
$t_{W(rep)}$	input pulse rising edge position	with respect to the end of line blanking; note 1	–	–	–2.6	μs
$R_{i(SC)}$	input resistance		1	–	–	MΩ
$C_{i(SC)}$	input capacitance		–	–	2	pF
Input switch select input; pin INPSEL						
V_{IL}	LOW-level input voltage	Y/$CVBS_1$ selected	–	–	0.5	V
V_{IH}	HIGH-level input voltage	Y/$CVBS_2$ selected	2.0	–	–	V
$R_{i(INPSEL)}$	input resistance		100	–	–	kΩ
$C_{i(INPSEL)}$	input capacitance		–	–	2	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output switch select input; pin OUTSEL						
V_{IL}	LOW-level input voltage	COMB mode	–	–	0.5	V
V_{IH}	HIGH-level input voltage	YC mode	2.0	–	–	V
$R_{i(OUTSEL)}$	input resistance		100	–	–	kΩ
$C_{i(OUTSEL)}$	input capacitance		–	–	2	pF
Colour subcarrier select input; pin FSCSEL						
V_{IL}	LOW-level input voltage	f_{SC} at FSC input; note 2	–	–	0.5	V
V_{IH}	HIGH-level input voltage	$2 \times f_{SC}$ at FSC input	2.0	–	–	V
$R_{i(FSCSEL)}$	input resistance		100	–	–	kΩ
$C_{i(FSCSEL)}$	input capacitance		–	–	2	pF
Luminance output; pin $Y/CVBS_{OUT}$						
$V_{o(Y/CVBSOUT)(p-p)}$	luminance output signal (peak-to-peak value)	including sync	0.6	1.0	1.54	V
$E_{G(Y)}$	luminance gain error		–1	0	+1	dB
$B_{-3dB(Y)}$	–3 dB luminance bandwidth	COMB mode	5	–	–	MHz
		YC mode	10	–	–	MHz
$t_{d(proc)(Y)}$	luminance processing delay	COMB mode; note 3	–	800	–	ns
		YC mode	–	15	–	ns
V_{clamp}	voltage level during clamping		–	1.5	–	V
E_{bl}	black level error	during blanking; note 4	–10	0	+10	mV
S/N	luminance signal-to-noise ratio (1 V/V_{rms} noise)	unweighted; 200 kHz to 5 MHz	56	–	–	dB
α_{ct}	crosstalk between different inputs	0 to 5 MHz	–	–	–50	dB
$f_{clk(res)(Y)}$	residues of clock frequencies in the luminance signal (V_{rms}/1 V)	COMB mode; note 2				
		$f = 4 \times f_{SC}$	–	–	–30	dB
		$f = 2 \times f_{SC}$	–	–	–30	dB
		$f = 1.33 \times f_{SC}$	–	–	–30	dB
		$f = f_{SC}$	–	–	–40	dB
$FSC_{res(YC)}$	FSC residue in YC mode (V_{rms}/1 V)	$f = f_{SC}$; f_{SC} at FSC input; note 2	–	–	–60	dB
		$f = 2 \times f_{SC}$; $2 \times f_{SC}$ at FSC input	–	–	–60	dB
α_{ct}	crosstalk suppression at vertical transient black ←→ multi-burst (1 V/V (p-p))	vertical transition active video ←→ vertical blanking; note 5 and Fig.5	26	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$SUP_{comb(Y)}$	suppression (comb depth) with respect to luminance band-pass nearest to f_{SC}	COMB mode; note 2 and Fig.6				
		$f = f_{SC}$	30	–	–	dB
		$f = \frac{227.5 - 59}{227.5} \times f_{SC}$	–	10	–	dB
		$f = \frac{227.5 + 59}{227.5} \times f_{SC}$	–	10	–	dB
R_o	output resistance		–	–	500	Ω
Z_L	load impedance		–	–	15	pF
Chrominance output; pin C_{OUT}						
$V_{o(COUT)(p-p)}$	chrominance output signal (peak-to-peak value)		–	0.7	1.1	V
$E_{G(chrom)}$	chrominance gain error		–1	0	+1	dB
$B_{-3dB(chrom)}$	–3 dB chrominance bandwidth	COMB mode; around f_{SC}; note 2	1.5	–	–	MHz
		YC mode; base-band	10	–	–	MHz
$\Delta t_{(proc)(Y)}$	difference with luminance processing delay		–	0	20	ns
V_{DC}	DC voltage level		–	1.5	–	V
S/N_{chrom}	chrominance signal-to-noise ratio (0.7 V/V_{rms} noise)	unweighted; $f_{SC} \pm 0.3f_{SC}$; note 2	56	–	–	dB
α_{ct}	crosstalk between different inputs	0 to 5 MHz	–	–	–50	dB
$f_{clk(res)(chrom)}$	residues of clock frequencies in the chrominance signal (V_{rms}/0.7 V)	COMB mode; note 2				
		$f = 4 \times f_{SC}$	–	–	–30	dB
		$f = 2 \times f_{SC}$	–	–	–30	dB
		$f = 1.33 \times f_{SC}$	–	–	–40	dB
		$f = f_{SC}$	–	–	–50	dB
$FSC_{res(YC)}$	FSC residue in YC mode (V_{rms}/0.7 V)	$f = f_{SC}$; f_{SC} at FSC input	–	–	–60	dB
		$f = 2 \times f_{SC}$; $2 \times f_{SC}$ at FSC input; note 2	–	–	–60	dB
α_{ct}	crosstalk suppression at vertical transient no-colour ←→ colour [0.7 V/V (p-p)]	vertical transition active video ←→ vertical blanking; note 6 and Fig.5	26	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$SUP_{comb(chrom)}$	suppression (comb depth) with respect to chrominance band pass at $f = f_{SC}$	COMB mode; note 2 and Fig.7				
		$f = \frac{227}{227.5} \times f_{SC}$	30	–	–	dB
		$f = \frac{227 - 59}{227.5} \times f_{SC}$	30	–	–	dB
		$f = \frac{227 + 59}{227.5} \times f_{SC}$	30	–	–	dB
R_o	output resistance		–	–	500	Ω
Z_L	load impedance		–	–	15	pF

Notes

1. The pulse should fall inside the line-blanking interval, after the rising edge of the synchronizing pulse.
2. f_{SC} = colour subcarrier frequency; f_{SC} = 3.579545 MHz for the NTSC M system.
3. With respect to 227.5 colour subcarrier periods (equals 63.556 μs) due to 1H delay in the comb filter.
4. With respect to the voltage level during clamping.
5. Test signal for NTSC M: 100% amplitude FCC multi-burst (see Fig.4).
6. Test signal for NTSC M: 100% white 75% amplitude FCC colour bar.

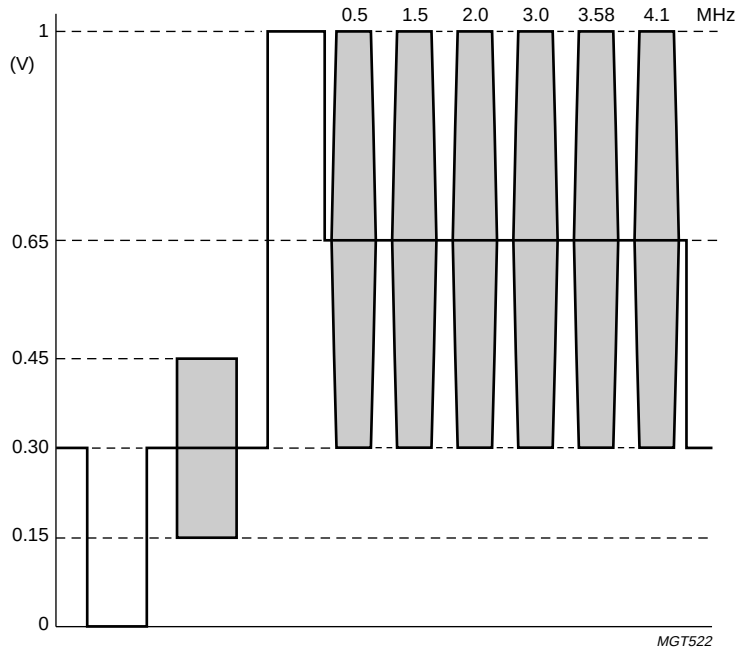


Fig.4 100% amplitude FCC multi-burst.

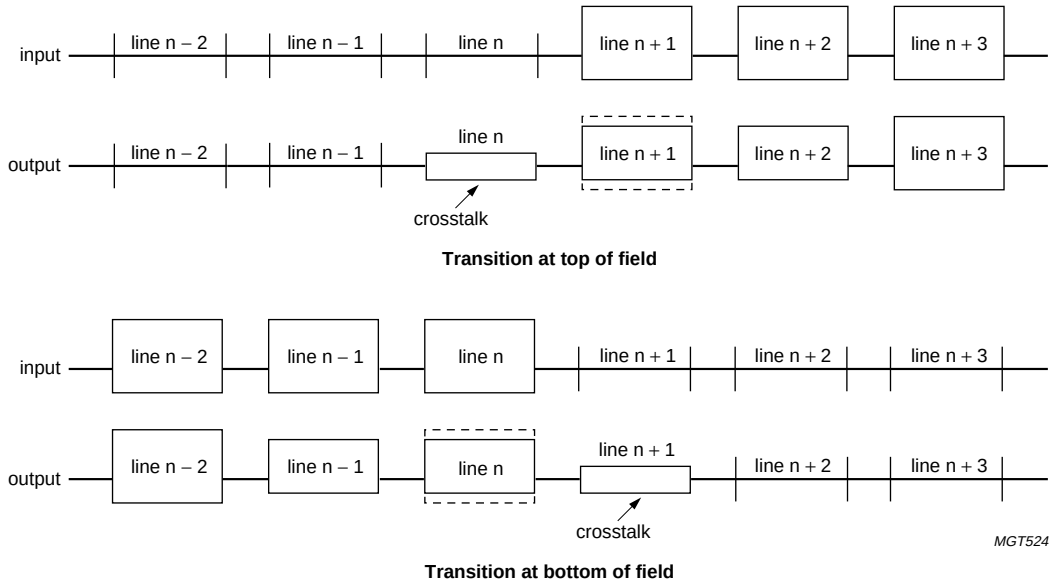


Fig.5 Vertical transitions active video ←→ vertical blanking from line to line (NTSC system).

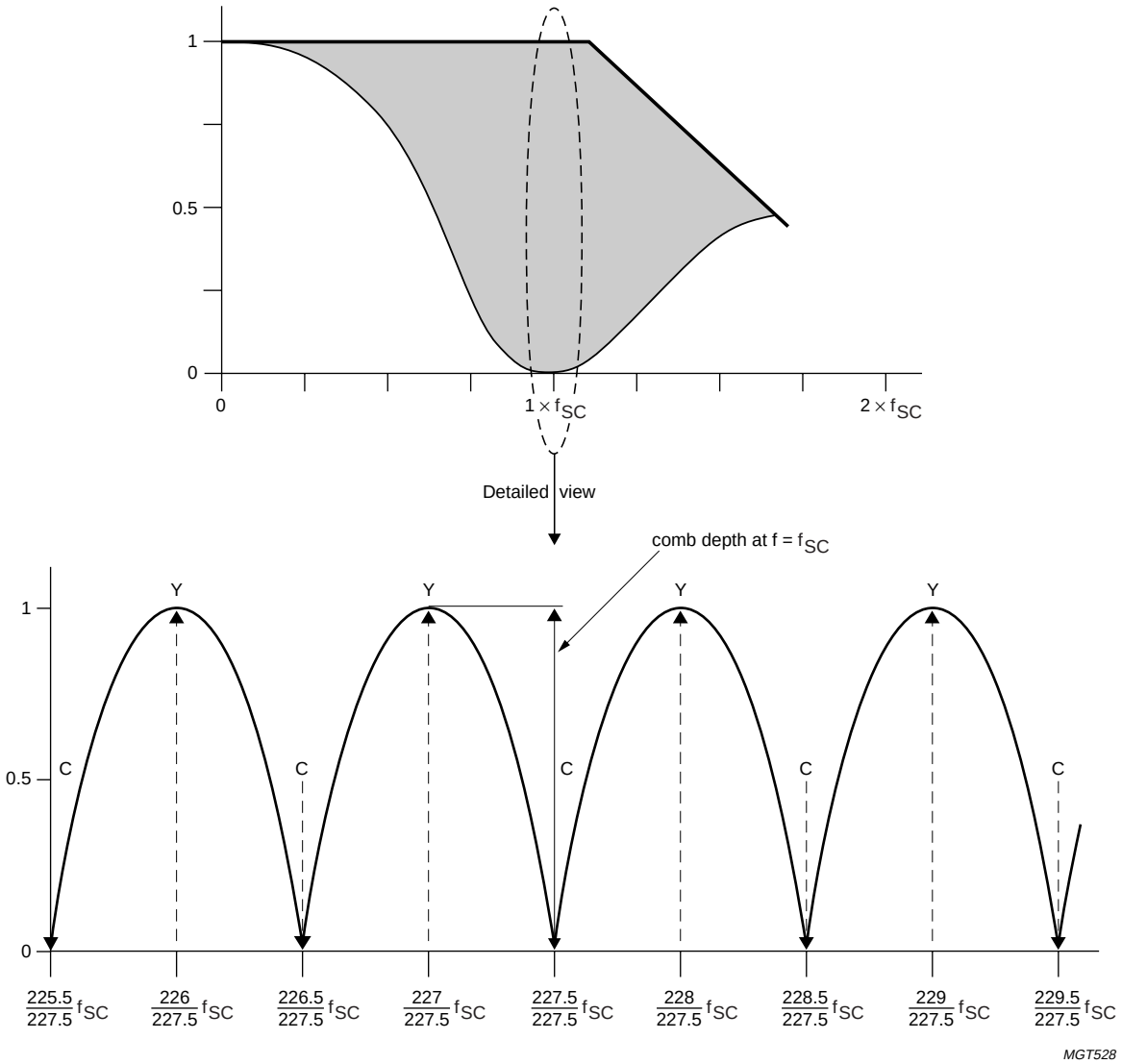


Fig.6 Luminance transfer characteristic (NTSC M system).

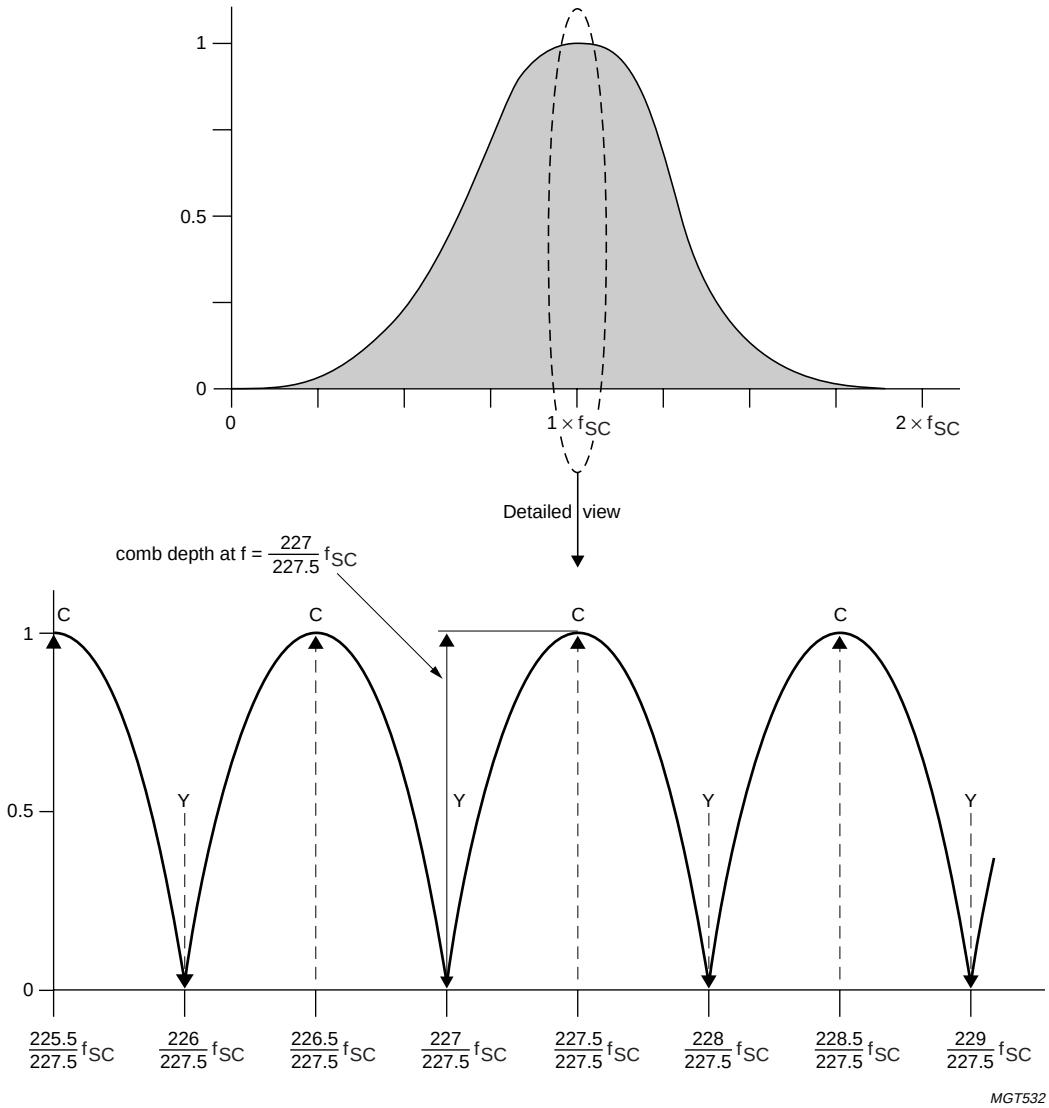


Fig.7 Chrominance transfer characteristic (NTSC M system).

APPLICATION INFORMATION

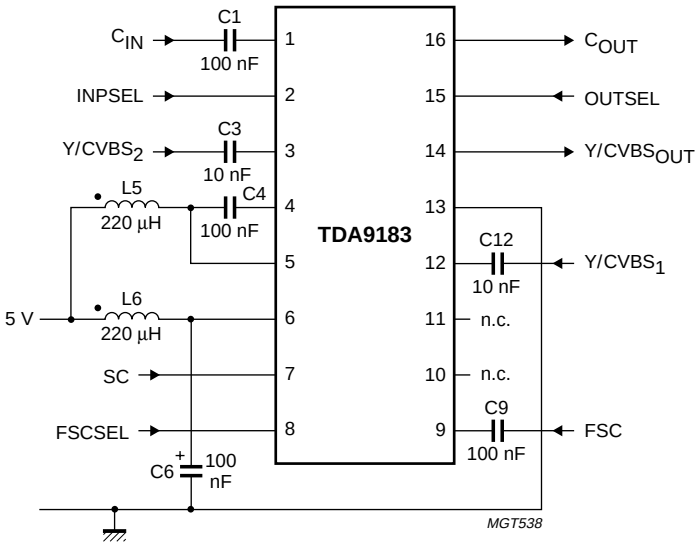
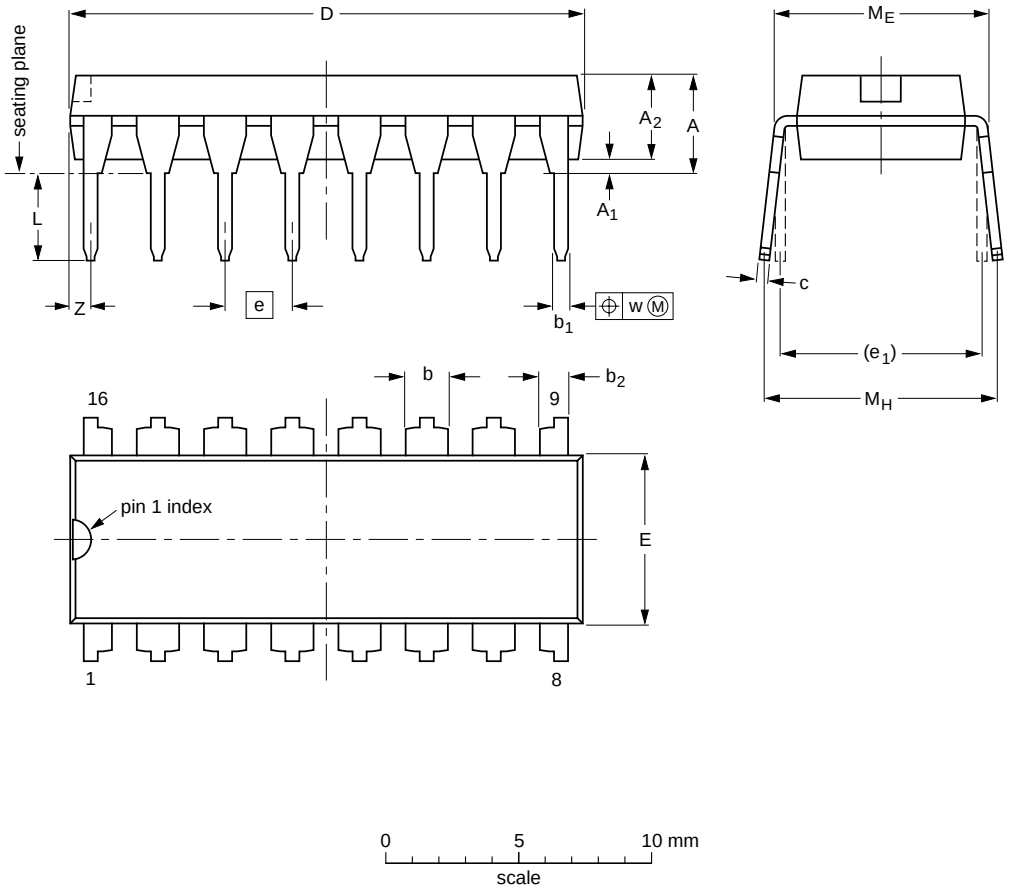


Fig.8 Application diagram.

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

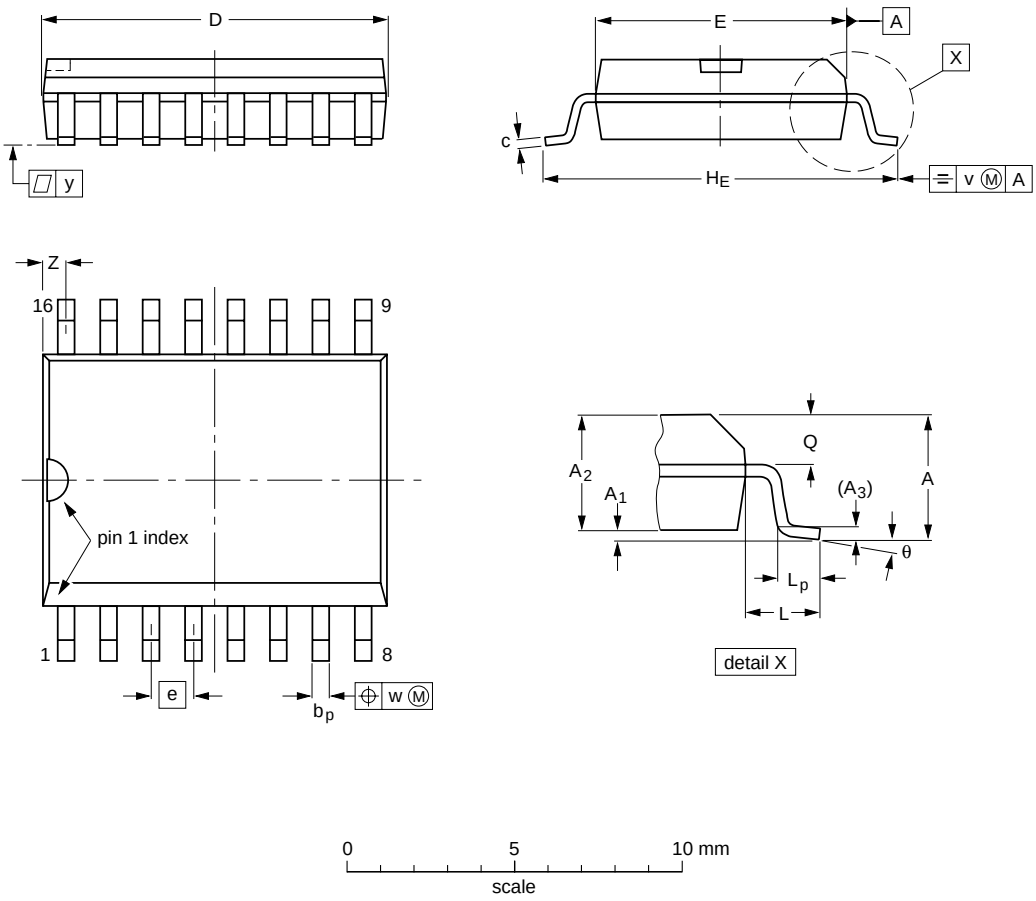
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013				~~97-05-22~~ 99-12-27

SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW[1]	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable[2]	–	suitable
Surface mount	BGA, LFBGA, SQFP, TFBGA	not suitable	suitable	–
	HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable[3]	suitable	–
	PLCC[4], SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended[4][5]	suitable	–
	SSOP, TSSOP, VSO	not recommended[6]	suitable	–

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
3. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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