PM6344

EQUAD

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1 FEATURES

- Integrates four full-featured E1 framers and transmitters in a single device for terminating duplex E1 signals.
- Software and functionally compatible with the PM6341 E1XC Single E1 Transceiver.
- Pin compatible with the PM4344 Quad T1 Framer device.
- Provides an 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power CMOS technology
- Available in a 128 pin PQFP package.

Each one of four receiver sections:

- Recovers clock and data using a digital phase locked loop for high jitter tolerance. A direct clock input is provided to allow clock recovery to be by-passed.
- Accepts dual rail or single rail digital PCM inputs.
- Supports HDB3 or AMI line code.
- Accepts gapped data streams to support higher rate demultiplexing.
- Frames to a G.704 2048 kbit/s signal within 1 ms.
- Frames to the signaling multiframe alignment when enabled.
- Frames to the CRC multiframe alignment when enabled.
- Provides loss of signal detection, and indicates loss of frame alignment (OOF), loss of signaling multiframe alignment and loss of CRC multiframe alignment.
- Supports line and path performance monitoring according to ITU-T recommendations. Accumulators are provided for counting:
- CRC-4 errors to 1000 per second;

Far end block errors to 1000 per second;

Frame sync errors to 127 per second; and

Line code violations to 8191 per second.

- Indicates the reception of remote alarm and remote multiframe alarm.
- Indicates the reception of alarm indication signal (AIS) and time slot 16 AIS.
- Declares RED and AIS alarms using Q.516 recommended integration periods.
- Provides an HDLC/LAPD interface for terminating a data link. Supports polled, interrupt-driven, or DMA servicing of the HDLC interface.
- Optionally extracts the data link from timeslot 16 (64 kbit/s), which may be used to receive common channel signaling, or from any combination of the national bits in timeslot 0 of non-frame alignment signal frames (4 kbit/s - 20 kbit/s).
- Supports fractional E1 channel extraction.
- Provides a two-frame elastic store buffer for jitter and wander attenuation that performs controlled slips and indicates slip occurrence and direction.
- Provides channel associated signaling extraction, with optional data inversion, programmable idle code substitution, and up to 3 multiframes of signaling debounce on a per-timeslot basis.
- Provides trunk conditioning which forces programmable trouble code substitution and signaling conditioning on all timeslots or on selected timeslots.
- Optionally provides dual rail digital PCM output signals to allow BPV transparency. Also supports unframed mode.
- Supports transfer of PCM and signaling data to 2.048 Mbit/s or 16.384Mbit/s backplane buses.
- Can be configured to attenuate jitter on the receive side by placing the digital jitter attenuator in the receive path.

Each one of four transmitter sections:

- Formats data to create a G.704 2048 kbit/s signal. Optionally inserts signaling multiframe alignment signal. Optionally inserts CRC multiframe structure including optional transmission of far end block errors.
- Optionally accepts dual rail digital PCM inputs to allow BPV transparency. Also supports unframed mode and framing bit, CRC, or data link by-pass.
- Supports transfer of PCM and signaling data from 2.048 Mbit/s or 16.384Mbit/s backplane buses.
- Provides channel associated signaling insertion, programmable idle code substitution, digital milliwatt code substitution, and data inversion on a per timeslot basis.
- Provides trunk conditioning which forces programmable trouble code substitution and signaling conditioning on all timeslots or on selected timeslots.
- Supports transmission of the alarm indication signal (AIS), timeslot 16 AIS, remote alarm signal or remote multiframe alarm signal.
- Provides an HDLC/LAPD interface for generating a data link. Supports polled, interrupt-driven, or DMA servicing of the HDLC interface.
- Optionally inserts the data link into timeslot 16 (64 kbit/s), which may be used to transmit common channel signaling, or into any combination of the national bits in timeslot 0 of non-frame alignment signal frames (4 kbit/s - 20 kbit/s).
- Supports fractional E1 channel insertion.
- Provides a digital phase locked loop for generation of a low jitter transmit clock.
- Provides a FIFO buffer for jitter attenuation and rate conversion in the transmitter. FIFO full or empty indication allows for bit-stuffing in higher rate multiplexing applications.
- Supports HDB3 or AMI line code.
- Provides dual rail or single rail digital PCM output signals.

2 APPLICATIONS

- E1 Channel Service Units (CSU) and Data Service Units (DSU)
- E1 Channel Banks and Multiplexers
- Digital Private Branch Exchanges (PBX)
- Digital Access and Cross-Connect Systems (DACS) and Electronic DSX Cross-Connect Systems (EDSX)
- E1 Frame Relay Interfaces
- E1 ATM Interfaces
- ISDN Primary Rate Interfaces (PRI)
- SDH Byte Synchronous TU12 Mappers
- Test Equipment

3 REFERENCES

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2. ITU-T Recommendation G.706, - "Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704", Vol. III, Fascicle III.4 , 1988.

3. ITU-T Recommendation G.706, - "Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704", 1991

4. ITU-T Recommendation G.711, - "Pulse Code Modulation (PCM) of Voice Frequencies", Volume III, Fascicle III.3, 1988.

5. ITU-T Recommendation G.732, - "Characteristics of Primary PCM Multiplex Equipment Operating at 2048 kbit/s", Vol. III, Fascicle III.4, 1988.

6. ITU-T Recommendation G.735, - "Characteristics of Primary PCM Multiplex Equipment Operating at 2048 kbit/s and Offering Synchronous Digital Access at 384 kbit/s and/or 64 kbit/s", Vol. III, Fascicle III.4, 1988.

7. ITU-T Recommendation G.821, - "Error Performance of an International Digital Connection Forming Part of an Integrated Services Digital Network", Vol. III, Fascicle III.5, 1988.

8. ITU-T Recommendation G.823, - "The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048 kbit/s Hierarchy", Vol. III, Fascicle III.5, 1988.

9. ITU-T Recommendation O.151, - "Error Performance Measuring Equipment For Digital Systems at the Primary Bit Rate and Above", Vol. IV, Fascicle IV.4, 1988.

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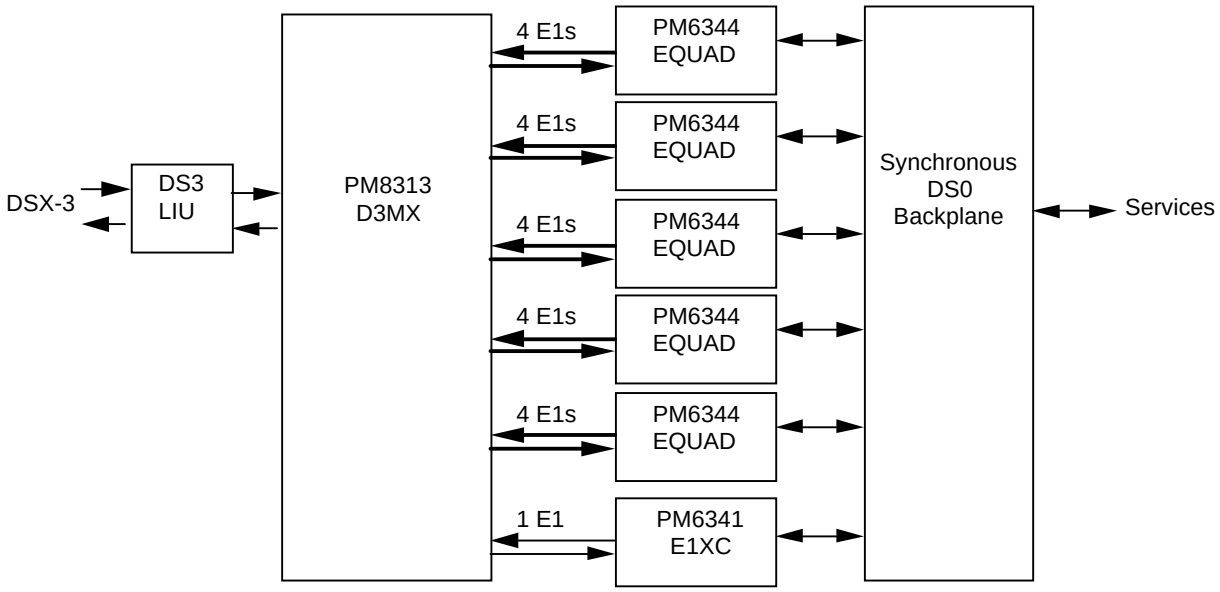
11. ITU-T Recommendation Q.506, - "Operations and maintenance functions", Vol. VI, Fascicle VI.5, 1984.

12. ITU-T Recommendation Q.516, - "Operations and maintenance functions", Vol. VI, Fascicle VI.5, 1984.

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4 APPLICATION EXAMPLES

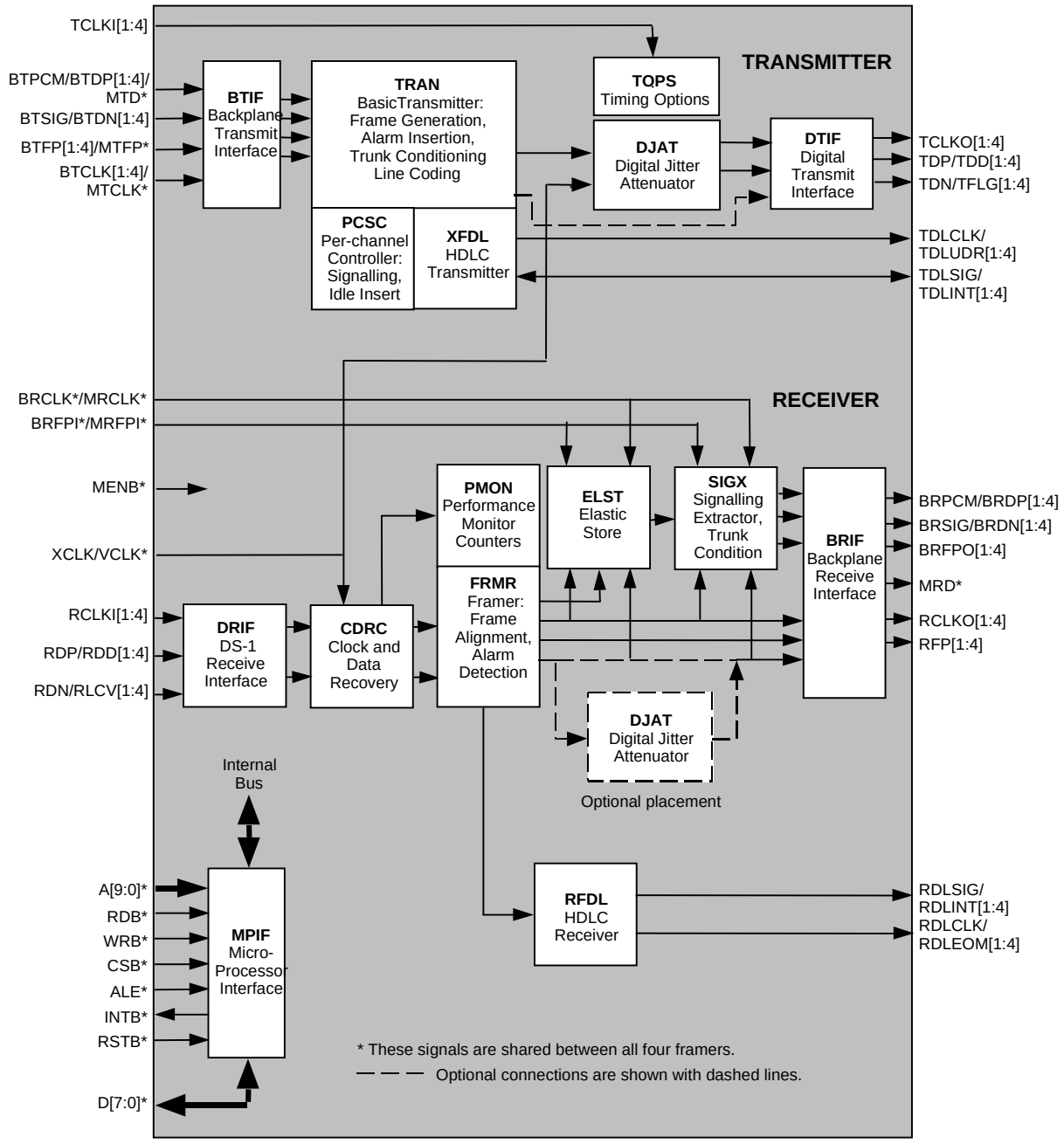
Figure 1 - Example 1. DS-3 Terminal Multiplexer/Channel Bank



Example 1 shows a DS-3 Terminal Multiplexer/Channel Bank using 5 EQUAD devices, PMC-Sierra's PM8313 D3MX M13 Multiplexer, the PM6341 E1XC E1 Transceiver, and Silicon System's SSI 78P236 DS-3 Line Interface Unit.

21 E1 signals can be multiplexed into a DSX-3 formatted signal. Five EQUAD devices and a single E1XC device are used to terminate these 21 signals. The DS-0 backplane data is transmitted and received using a 2.048 MHz system clock.

5 BLOCK DIAGRAM



Description

The PM6344 Quadruple E1 Framer (EQUAD) is a feature-rich device suitable for use in many E1 systems with a minimum of external circuitry. Each of the framers and transmitters is independently software configurable, allowing feature selection without changes to external wiring.

On the receive side, the EQUAD recovers clock and data and can be configured to frame to a basic G.704 2048 kbit/s signal or also frame to the signaling multiframe alignment signal and the CRC multiframe alignment signal.

The EQUAD also supports detection of various alarm conditions such as loss of signal, loss of frame, loss of signaling multiframe, loss of CRC multiframe, and reception of remote alarm signal, remote multiframe alarm signal, alarm indication signal, and timeslot 16 alarm indication signal. The EQUAD detects and indicates the presence of remote alarm and AIS patterns and also integrates red and AIS alarms as per industry specifications.

Performance monitoring with accumulation of CRC-4 errors, far end block errors, framing bit errors, and line code violation is provided. The EQUAD also detects and terminates HDLC messages on a data link. The data link may be extracted from timeslot 16 and used for common channel signaling or may be extracted from the national bits.

An elastic store for slip buffering and adaptation to backplane timing is provided, as is a signaling extractor that supports signaling debounce, signaling freezing, idle code substitution, digital milliwatt tone substitution, data inversion, and signaling bit fixing on a per-channel basis. Receive side data and signaling trunk conditioning is also provided.

On the transmit side, the EQUAD generates framing for a basic G.704 2048 kbit/s signal, or framing can be optionally disabled. The signaling multiframe alignment structure may be optionally inserted and the CRC multiframe structure may be optionally inserted.

Channel associated signaling insertion, idle code substitution, digital milliwatt tone substitution, and data inversion on a per-timeslot basis is also supported. Transmit side data and signaling trunk conditioning is provided.

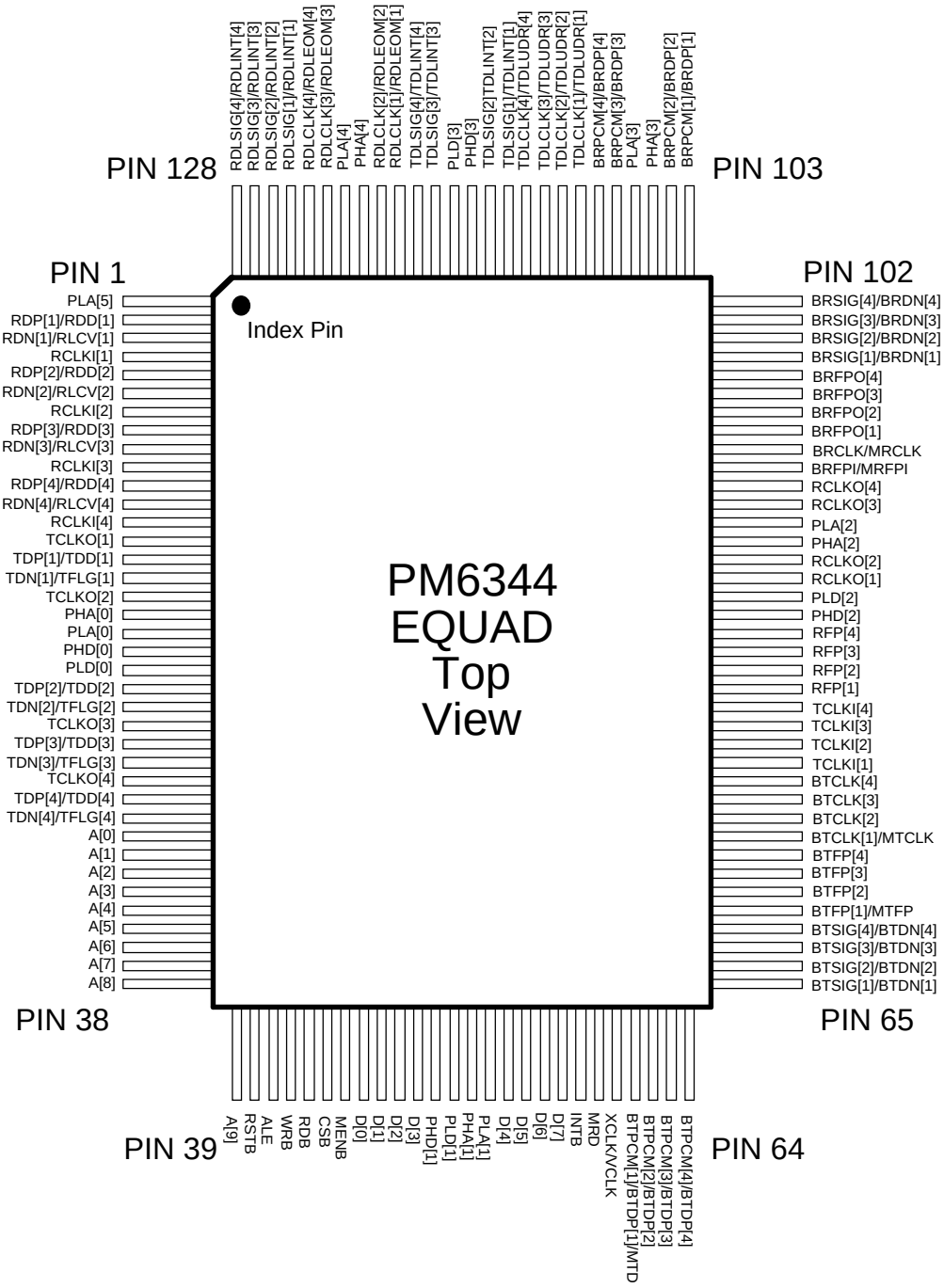
HDLC messages on a data link can be transmitted. The data link may be inserted into timeslot 16 and used for common channel signaling or may be inserted into the national bits. The EQUAD can generate a low jitter transmit clock and provides a FIFO for transmit jitter attenuation. When not used for jitter

attenuation, the full or empty status of this FIFO is made available to facilitate higher order multiplexing applications by controlling bit-stuffing logic.

The EQUAD provides a parallel microprocessor interface for controlling the operation of the EQUAD device. Serial PCM interfaces allow 2.048 Mbit/s backplanes to be directly supported. Tolerance of gapped clocks allows other backplane rates to be supported with a minimum of external logic. Optional bit interleaved multiplexing of the individual serial streams supports 16.384 Mbit/s backplanes.

6 PIN DIAGRAM

The EQUAD is packaged in a 128-pin plastic QFP package having a body size of 14 mm by 20 mm and a pin pitch of 0.5 mm.



7 PIN DESCRIPTION

Pin Name	Type	Pin No.	Function
MENB	Input	45	Multiplex Enable (MENB). When this input is asserted low, the four sets of PCM and signaling streams are combined into a single bit interleaved 16.384 Mbit/s serial stream. In the transmit direction, all data is expected on MTD with alignment indicated by MTFP. MTD and MTFP are sampled on the rising edge of MTCLK. In the receive direction, data is presented on MRD aligned with MRFPI. MRFPI is sampled on the rising edge of MRCLK and MRD is updated on the falling edge of MRCLK. When this input is deasserted high, each PCM and signaling stream has its own dedicated pin. MENB has an integral pull-up.
RDP[1] RDP[2] RDP[3] RDP[4] / RDD[1] RDD[2] RDD[3] RDD[4]	Input	2 5 8 11	Receive Positive Line Pulse (RDP[4:1]). These inputs are available when the EQUAD is configured to receive dual-rail formatted data. The RDP[4:1] inputs may be enabled for either RZ or NRZ waveforms. When enabled for NRZ, this input may be enabled to be sampled on the rising or falling edge of the corresponding RCLKI[4:1]. When enabled for RZ, the clocks are recovered from the corresponding RDP[4:1] and RDN[4:1] inputs. Receive Digital E1 Signal (RDD[4:1]). When the EQUAD is configured to receive single-rail data, these inputs may be enabled to be sampled on the rising or falling edge of the corresponding RCLKI[4:1].

Pin Name	Type	Pin No.	Function
RDN[1] RDN[2] RDN[3] RDN[4] / RLCV[1] RLCV[2] RLCV[3] RLCV[4]	Input	3 6 9 12	Receive Digital Negative Line Pulse (RDN[4:1]). These inputs are available when the EQUAD is configured to receive dual-rail formatted data. The RDN[4:1] inputs may be enabled for either RZ or NRZ waveforms. When enabled for NRZ, these inputs may be enabled to be sampled on the rising or falling edge of the corresponding RCLKI[4:1]. When enabled for RZ, the clocks are recovered from the corresponding RDP[4:1] and RDN[4:1] inputs. Receive Line Code Violation Indication (RLCV[4:1]). When the EQUAD is configured to receive single-rail data, this input may be enabled to be sampled on the rising or falling edge of the corresponding RCLKI[4:1].
RCLKI[1] RCLKI[2] RCLKI[3] RCLKI[4]	Input	4 7 10 13	Receive Line Clock Inputs (RCLKI[4:1]). Each input is an externally recovered 2.048 MHz line clock that may be enabled to sample the RDP[x] and RDN[x] inputs on its rising or falling edge when the input format is enabled for dual-rail NRZ; or to sample the RDD[x] and RLCV[x] inputs on its rising or falling edge when the input format is enabled for single-rail.
RCLKO[1] RCLKO[2] RCLKO[3] RCLKO[4]	Output	87 88 91 92	Recovered PCM Clock Output (RCLKO[4:1]). Each output signal is the recovered 2.048 MHz clock, synchronized to the XCLK signal. Each RCLKO[x] signal is recovered from the RDP[x] and RDN[x] inputs (if the input format is dual-rail RZ) or from the RCLKI[x] input (if the input format is NRZ). When the ELST is by-passed or the RCLKOSEL register bit is set, BRPCM[x] and BRSIG[x] are updated on the falling edge of the associated RCLKO[x]. As an option, the digital attenuator's smooth 2.048 MHz clock may be presented on RCLKO[x]. See the Operations Section for details on this application.

Pin Name	Type	Pin No.	Function
RFP[1] RFP[2] RFP[3] RFP[4]	Output	81 82 83 84	Receive Frame Pulse (RFP[4:1]). The RFP[x] outputs are intended as a timing references. When the EQUAD is configured for receive frame pulse output, RFP[x] pulses high for 1 RCLKO cycle during bit 1 of each 256-bit frame, indicating the frame alignment of the receive stream. When configured for receive signaling multiframe output, RFP[x] pulses high for 1 RCLKO[x] cycle during bit 1 of frame 1 of the 16 frame signaling multiframe, indicating the signaling multiframe alignment of the receive stream. (Even when signaling multiframing is disabled, the RFP[x] output continues to indicate the position of bit 1 of every 16th frame.) When configured for receive CRC multiframe output, RFP[x] pulses high for 1 RCLKO[x] cycle during bit 1 of frame 1 of every 16 frame CRC multiframe, indicating the CRC multiframe alignment of the receive stream. (Even when CRC multiframing is disabled, the RFP[x] output continues to indicate the position of bit 1 of the FAS frame every 16th frame.) When configured for composite multiframe output, RFP[x] goes high on the falling RCLKO[x] edge marking the beginning of bit 1 of frame 1 of every 16 frame signaling multiframe, indicating the signaling multiframe alignment of the receive stream, and returns low on the falling RCLKO[x] edge marking the ending of bit 1 of frame 1 of every 16 frame CRC multiframe, indicating the CRC multiframe alignment of the receive stream. This mode allows both multiframe alignments to be decoded externally from the single RFP[x] signal. Note that if the signaling and CRC multiframe alignments are coincident, RFP[x] will pulse high for 1 RCLKO[x] cycle every 16 frames. Each RFP[x] is updated on the falling edge of the associated RCLKO[x]. RFP[x] should not be used when register bit RCLKOSEL is set to a logic 1.

Pin Name	Type	Pin No.	Function
RDLSIG[1] RDLSIG[2] RDLSIG[3] RDLSIG[4]/	Output	125 126 127 128	Receive Data Link Signal (RDLSIG[4:1]). The RDLSIG[4:1] signals are available on these outputs when the associated internal HDLC receiver (RFDL) is disabled from use, or, optionally, when fractional E1 is extracted. RDLSIG contains the data link stream extracted from the selected data link bits. The EQUAD may be configured to utilize timeslot 16 as a data link or utilize any combination of the national bits as a data link. Each RDLSIG[x] is updated on the falling edge of the associated RDLCLK[x].
RDLINT[1] RDLINT[2] RDLINT[3] RDLINT[4]			Receive Data Link Interrupt (RDLINT[4:1]). The RDLINT[4:1] signals are available on these outputs when the associated RFDL is enabled. Each RDLINT[x] goes high when an event occurs which changes the status of the associated HDLC receiver.
RDLCLK[1] RDLCLK[2] RDLCLK[3] RDLCLK[4]/	Output	119 120 123 124	Receive Data Link Clock (RDLCLK[4:1]). The RDLCLK[4:1] signals are available on these outputs when the associated internal HDLC receiver (RFDL) is disabled from use, or, optionally, when fractional E1 is extracted. The rising edge of RDLCLK[x] can be used to sample the data-link data or the fractional E1 data on the associated RDLSIG[x] when the internal HDLC receiver is disabled or when fractional E1 is enabled respectively.
RDLEOM[1] RDLEOM[2] RDLEOM[3] RDLEOM[4]			Receive Data Link End of Message (RDLEOM[4:1]). The RDLEOM[4:1] signals are available on these outputs when the associated RFDL is enabled. Each RDLEOM[x] goes high when the last byte of a received sequence is read from the associated RFDL FIFO buffer, or when the FIFO buffer is overrun.

Pin Name	Type	Pin No.	Function
BRPCM[1] BRPCM[2] BRPCM[3] BRPCM[4]/	Output	103 104 107 108	Backplane Receive PCM (BRPCM[4:1]). The BRPCM[4:1] signals are available on these outputs when the backplane is configured for single-rail output. Each BRPCM[x] signal contains the recovered data stream passed through the ELST block, and the SIGX block. When the ELST is not by-passed or the RCLKOSEL register bit is not set, the BRPCM[x] stream is aligned to the backplane timing and is updated on the falling edge of the associated BRCLK. When the ELST is by-passed or the RCLKOSEL register bit is set, BRPCM[x] is aligned to the receive line timing and is updated on the falling edge of the associated RCLKO[x].
BRDP[1] BRDP[2] BRDP[3] BRDP[4]			Backplane Receive Positive Line Pulse (BRDP[4:1]). The BRDP[4:1] signals are available on these outputs when the backplane is configured for dual-rail output. Each BRDP[x] NRZ output represents the RZ receive digital positive pulse signal extracted from the input bipolar signal. BRDP[x] is updated on the falling edge of the associated RCLKO[x].
MRD	Output	59	Multiplexed Receive Data (MRD). When the multiplex enable (MENB) input is asserted low, the four sets of PCM and signaling streams are bit interleaved into a single 16.384 Mbit/s serial stream presented on MRD aligned with MRFPI. MRFPI is sampled on the rising edge of MRCLK and MRD is updated on the falling edge of MRCLK. When MENB input is deasserted high, each PCM and signaling stream has its own dedicated pin and MRD is unused.

Pin Name	Type	Pin No.	Function
BRSIG[1] BRSIG[2] BRSIG[3] BRSIG[4]	Output	99 100 101 102	Backplane Receive Signaling (BRSIG[4:1]). The BRSIG[4:1] signals are available on these outputs when the backplane is configured for single-rail output. Each BRSIG[x] contains the extracted signaling bits for each channel in the frame, repeated for the entire superframe. Each channel's signaling bits are valid in bit locations 5,6,7,8 of the channel and are channel-aligned with the BRPCM[x] data stream. When the ELST is not by-passed or the RCLKOSEL register bit is not set, the BRSIG[x] stream is aligned to the backplane timing and is updated on the falling edge of BRCLK. When the ELST is by-passed or the RCLKOSEL register bit is set, BRSIG[x] is aligned to the receive line timing and is updated on the falling edge of the associated RCLKO[x].
BRDN[1] BRDN[2] BRDN[3] BRDN[4]			Backplane Receive Negative Line Pulse (BRDN[4:1]). The BRDN[4:1] signals are available on these outputs when the backplane is configured for dual-rail output. Each BRDN[x] NRZ output represents the RZ receive digital negative pulse signal extracted from the input bipolar signal. BRDN[x] is updated on the falling edge of the associated RCLKO[x].

Pin Name	Type	Pin No.	Function
BRFPO[1] BRFPO[2] BRFPO[3] BRFPO[4]	Output	95 96 97 98	Backplane Frame Pulse Output (BRFPO[4:1]). When the EQUAD is configured for backplane receive frame pulse output, each BRFPO[x] pulses high for 1 BRCLK cycle (or 1 RCLKO[x] cycle if ELST is by-passed or the RCLKOSEL register bit is set) during bit 1 of each 256-bit frame, indicating the frame alignment of the BRPCM[x] data stream. When configured for backplane receive signaling multiframe output, BRFPO[x] pulses high for 1 BRCLK cycle (or 1 RCLKO[x] cycle if ELST is by-passed) during bit 1 of frame 1 of the 16 frame signaling multiframe, indicating the signaling multiframe alignment of the BRPCM[x] data stream. (Even when signaling multiframing is disabled, the BRFPO[x] output continues to indicate every 16th frame.) When configured for backplane receive CRC multiframe output, BRFPO[x] pulses high for 1 BRCLK cycle (or 1 RCLKO[x] cycle if ELST is by-passed) during bit 1 of frame 1 of every 16 frame CRC multiframe, indicating the CRC multiframe alignment of the BRPCM[x] data stream. (Even when CRC multiframing is disabled, the BRFPO[x] output continues to indicate the position of bit 1 of the FAS frame every 16th frame.) When configured for backplane receive composite multiframe output, BRFPO[x] goes high on the falling BRCLK edge (or RCLKO[x] edge if ELST is by-passed) marking the beginning of bit 1 of frame 1 of every 16 frame signaling multiframe, indicating the signaling multiframe alignment of the BRPCM[x] data stream, and returns low on the falling BRCLK edge (or RCLKO[x] edge if ELST is by-passed) marking the end of bit 1 of frame 1 of every 16 frame CRC multiframe, indicating the CRC multiframe alignment of the BRPCM[x] data stream. In this mode both multiframe alignments can be decoded externally from the single BRFPO[x] signal. If the signaling and CRC multiframe alignments are coincident, BRFPO[x] will pulse high for 1 clock cycle. When configured for backplane receive overhead output, BRFPO[x] is high for timeslot 0 and timeslot 16 of each 256-bit frame, indicating the overhead bit positions of the BRPCM[x] data stream. BRFPO[x] is updated on the falling edge of the BRCLK or RCLKO[x].

Pin Name	Type	Pin No.	Function
BRCLK	Input	94	Backplane Receive Clock (BRCLK). When the multiplex enable (MENB) input is deasserted high, BRCLK is a 2.048MHz clock with optional gapping for adaptation to non-uniform backplane data streams. BRCLK is common to all four framers. The EQUAD may be configured to ignore the BRCLK input and use the RCLKO[x] signal in its place when the ELST is bypassed or the RCLKOSEL register bit is set.
MRCLK			Multiplex Receive Clock (MRCLK). When the multiplex enable (MENB) input is asserted low, MRCLK is a 16.384 MHz clock. MRFPI is sampled on the rising edge of MRCLK and MRD is updated on the rising edge of MRCLK. The multiplexed bus can not be used if the ELST is bypassed or the RCLKOSEL register bit is set.
BRFPI	Input	93	Backplane Frame Pulse Input (BRFPI). When the multiplex enable (MENB) input is deasserted high, this input is used to frame align the received data to the system backplane. BRFPI is common to all four framers. If frame alignment only is required, a pulse at least 1 BRCLK cycle wide must be provided on each BRFPI every 256 bit periods.
MRFPI			Multiplexed Frame Pulse Input (MRFPI). When the multiplex enable (MENB) input is asserted low, this input aligns all four sets of PCM and signaling streams to allow bit interleaved multiplexing. If frame alignment only is required, a pulse no more than 1 MRCLK cycle wide must be provided on each MRFPI every 2048 bit periods.

Pin Name	Type	Pin No.	Function
BTPCM[1] BTPCM[2] BTPCM[3] BTPCM[4]/	Input	61 62 63 64	Backplane Transmit PCM (BTPCM[4:1]). The non-return to zero, digital data streams to be transmitted are input on these pins when the backplane is configured for non-multiplexed single-rail input. The BTPCM[x] signal is sampled on the rising edge of the associated BTCLK[x].
BTDP[1] BTDP[2] BTDP[3] BTDP[4]			Backplane Transmit Positive Line Pulse (BTDP[4:1]). The positive pulse of the dual-rail signals to be transmitted is input on these pins when the backplane is configured for non-multiplexed dual-rail input. In dual-rail input mode, the BTDP[x] input by-passes the transmitter and is fed directly into the DJAT. BTDP[x] is sampled on the rising edge of the associated BTCLK[x].
MTD			Multiplexed Transmit Data (MTD). MTD shares a pin with BTPCM[1]. BTPCM[4:2] are unused when the multiplex enable (MENB) input is asserted low. When the multiplex enable (MENB) input is asserted low, the four sets of PCM and signaling streams are expected in a single bit interleaved 16.384 Mbit/s serial stream. Frame alignment is indicated by MTFP. MTD is sampled on the rising edge of MTCLK.
BTSIG[1] BTSIG[2] BTSIG[3] BTSIG[4]	Input	65 66 67 68	Backplane Transmit Signaling (BTSIG[4:1]). The BTSIG[4:1] input signals contain the signaling bits for each channel in the transmit data frame, repeated for the entire superframe. Each signal is input on the BTSIG[x] pin when the backplane is configured for non-multiplexed single-rail input. Each channel's signaling bits are in bit locations 5,6,7,8 of the channel and are channel-aligned with the BTPCM[x] data stream. BTSIG[x] is sampled on the rising edge of the associated BTCLK[x]. If frame alignment is not required, BTFP[x] may be tied to power or ground.
BTDN[1] BTDN[2] BTDN[3] BTDN[4]			Backplane Transmit Negative Line Pulse (BTDN[4:1]). The negative pulse of the dual-rail signal to be transmitted is input on these pins when the backplane is configured for non-multiplexed dual-rail input. In dual-rail input mode, the BTDN[x] input by-passes the transmitter and is fed directly into the DJAT. BTDN[x] is sampled on the rising edge of the associated BTCLK[x]. These inputs are unused when the multiplex enable (MENB) input is asserted low.

Pin Name	Type	Pin No.	Function
BTFP[1] BTFP[2] BTFP[3] BTFP[4]	Input	69 70 71 72	Backplane Transmit Frame Pulse (BTFP[4:1]). These inputs are used to frame align the transmitters to the system backplane. If basic frame alignment only is required, a pulse at least 1 BTCLK[x] cycle wide must be provided on BTFP[x] at multiples of 256 bit periods. If multiframe alignment is required, transmit multiframe alignment must be enabled, and BTFP[x] must be brought high to mark bit 1 of frame 1 of every 16 frame signaling multiframe and brought low following bit 1 of frame 1 of every 16 frame CRC multiframe. This mode allows both multiframe alignments to be independently controlled using the single BTFP[x] signal. Note that if the signaling and CRC multiframe alignments are coincident, BTFP[x] must pulse high for 1 BTCLK[x] cycle every 16 frames. If register bit BTFPREF is set to logic 1, BTFP[x] becomes the reference frame pulse for the associated interface. If frame alignment is not required, BTFP[x] may be tied to logic high or low.
MTFP			Multiplexed Transmit Frame Pulse (MTFP). MTFP shares a pin with BTFP[1]. BTFP[4:2] are unused when the multiplex enable (MENB) input is asserted low. When the multiplex enable (MENB) input is asserted low, MTFP indicates the frame alignment of the bit interleaved PCM and signaling streams in the same way as BTFP[x]. If basic frame alignment only is required, a pulse 1 MTCLK cycle wide must be provided on MTFP at multiples of 2048 clock periods. If multiframe alignment is required, transmit multiframe alignment must be enabled, and MTFP must be brought high to mark bit 1 of frame 1 of the first multiplexed PCM stream (destined for transmitter number one) of every 16 frame signaling multiframe and brought low following bit 1 of frame 1 of the first multiplexed PCM stream of every 16 frame CRC multiframe. This mode allows both multiframe alignments to be independently controlled using the single MTFP signal. All four interfaces will have the same frame alignment. Note that if the signaling and CRC multiframe alignments are coincident, MTFP must pulse high for 1 MTCLK cycle every 16 frames (32768 clock cycles). MTFP is sampled on the rising edge of MTCLK.

Pin Name	Type	Pin No.	Function
BTCLK[1] BTCLK[2] BTCLK[3] BTCLK[4]	Input	73 74 75 76	Backplane Transmit Clock (BTCLK[4:1]). BTCLK[4:1] are the 2.048MHz transmit clocks with optional gapping for adaptation from non-uniform backplane data streams. The EQUAD may be configured to ignore the BTCLK[x] input and use the associated RCLKO[x] signal in its place.
MTCLK			Multiplexed Transmit Clock (MTCLK). MTCLK shares a pin with BTCLK[1]. BTCLK[4:2] are unused when the multiplex enable (MENB) input is asserted low. When the multiplex enable (MENB) input is asserted low, this clock is 16.384 MHz. MTFP and MTD are sampled on the rising edge of MTCLK.
TDLSIG[1] TDLSIG[2] TDLSIG[3] TDLSIG[4]/	I/O	113 114 117 118	Transmit Data Link Signal (TDLSIG[4:1]). The TDLSIG[4:1] signals are input on this pin when the associated internal HDLC transmitter (XFDL) is disabled from use, or if fractional E1 insertion is selected. TDLSIG[x] is the source for the data stream to be inserted into the selected data link bits. The EQUAD may be configured to utilize timeslot 16 as a data link or utilize any combination of the national bits as a data link. If fractional E1 insertion is enabled, TDLSIG[x] is the data source for the E1 channels enabled by the Channel Select registers. TDLSIG[x] is sampled on the rising edge of the associated TDLCLK[x]. The TDLSIG[x] pins have integral pull-ups.
TDLINT[1] TDLINT[2] TDLINT[3] TDLINT[4]			Transmit Data Link Interrupt (TDLINT[4:1]). The TDLINT[4:1] signals are output on these pins when the associated XFDL is enabled. Each TDLINT[x] goes high when the last data byte written to the XFDL has been set up for transmission and processor intervention is required to either write control information to end the message, or to provide more data.

Pin Name	Type	Pin No.	Function
TDLCLK[1] TDLCLK[2] TDLCLK[3] TDLCLK[4]/	Output	109 110 111 112	Transmit Data Link Clock (TDLCLK[4:1]). The TDLCLK[4:1] signals are available on this output when the associated internal HDLC transmitter (XFDL) is disabled from use, or if fractional E1 insertion is selected. The rising edge of TDLCLK[x] is used to sample the data-link or fractional E1 data stream contained on the associated TDLSIG[x] input. When the EQUAD is not configured to transmit a data link and fractional E1 is disabled, the TDLCLK[x] output is held low.
TDLUDR[1] TDLUDR[2] TDLUDR[3] TDLUDR[4]			Transmit Data Link Underrun (TDLUDR[4:1]). The TDLUDR[4:1] signals are available on this output when the associated XFDL is enabled. TDLUDR[x] goes high when the processor has failed to service the TDLINT[x] interrupt before the transmit buffer is emptied.
TCLKO[1] TCLKO[2] TCLKO[3] TCLKO[4]	Output	14 17 24 27	Transmit Clock Output (TCLKO[4:1]). The TDP[4:1], TDN[4:1], and TDD[4:1] outputs may be enabled to be updated on the rising or falling edge of the TCLKO[4:1] outputs. TCLKO[x] is a 2.048 MHz clock that is adequately jitter and wander free in absolute terms to permit an acceptable E1 signal to be generated. Depending on the configuration of the EQUAD, TCLKO[x] may be derived from TCLKI[x], RCLKO[x], or BTCLK[x], with or without jitter attenuation.
TDP[1] TDP[2] TDP[3] TDP[4] /	Output	15 22 25 28	Transmit Digital Positive Line Pulse (TDP[4:1]). These signals are available on the output when the EQUAD is configured to transmit dual-rail data. The TDP[x] signal can be formatted for either RZ or NRZ waveforms, and can be enabled to be updated on the rising or falling edge of the associated TCLKO[x].
TDD[1] TDD[2] TDD[3] TDD[4]			Transmit Digital Data (TDD[4:1]). These signals are available on the output when configured to transmit single-rail data. The TDD[x] signal may be enabled to be updated on the rising or falling edge of the associated TCLKO[x].

Pin Name	Type	Pin No.	Function
TDN[1] TDN[2] TDN[3] TDN[4] / TFLG[1] TFLG[2] TFLG[3] TFLG[4]	Output	16 23 26 29	Transmit Digital Negative Line Pulse (TDN[4:1]). These signals are available on the output when the EQUAD is configured to transmit dual-rail data. The TDN[x] signal can be formatted for either RZ or NRZ waveforms, and can be enabled to be updated on the rising or falling edge of the associated TCLKO[x]. Transmit FIFO Flag (TFLG[4:1]). These signals are available when configured to transmit single-rail data. The TFLG[x] output indicates when the transmit rate conversion FIFO in DJAT is nearing an empty or a full condition. Either indication may be selected. This output may be enabled to be updated on the rising or falling edge of the associated TCLKO[x].
TCLKI[1] TCLKI[2] TCLKI[3] TCLKI[4]	Input	77 78 79 80	Transmit Clock Input (TCLKI[x]). This input signal is used to generate the TCLKO[x] clock signal. Depending upon the configuration of the EQUAD, TCLKO[x] may be derived directly from TCLKI[x] by dividing TCLKI[x] by 8, or TCLKO[x] may be derived from TCLKI[x] after jitter attenuation. If TCLKI[x] is jitter-free when divided down to 8 kHz, then it is possible to derive TCLKO[x] from TCLKI[x] when TCLKI[x] is a multiple of 8 kHz (i.e. Nx8 kHz, for N equals 1 to 256). The EQUAD may be configured to ignore the TCLKI[x] input and utilize BTCLK[x] or RCLKO[x] instead. RCLKO[x] is also substituted for TCLKI[x] if line loopback is enabled.
XCLK/ VCLK	Input	60	Crystal Clock Input (XCLK). This signal provides timing for many portions of the EQUAD. Depending on the configuration of the EQUAD, XCLK is nominally a 49.152 MHz or 16.384 MHz 50% duty cycle clock. When transmit clock generation or jitter attenuation is not required, XCLK may be driven with a 16.384 MHz clock. When transmit clock generation or jitter attenuation is required, XCLK must be driven with a 49.152 MHz clock. Vector Clock (VCLK). The VCLK signal is used during EQUAD production test to verify internal functionality.
INTB	Output	58	Active low open-drain Interrupt signal (INTB). This signal goes low when an unmasked interrupt event is detected on any of the internal interrupt sources, including the internal HDLC transceiver. Note that INTB will remain low until all active, unmasked interrupt sources are acknowledged at their source.

Pin Name	Type	Pin No.	Function
CSB	Input	44	Active low chip select (CSB). This signal must be low to enable EQUAD register accesses. This signal must be toggled high to clear the PMCTST register bit (register 00BH or 20BH) and to ensure the EQUAD will operate in normal mode.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	46 47 48 49 54 55 56 57	Bi-directional data bus (D[7:0]). This bus is used during EQUAD read and write accesses.
RDB	Input	43	Active low read enable (RDB). This signal is pulsed low to enable a EQUAD register read access. The EQUAD drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are both low.
WRB	Input	42	Active low write strobe (WRB). This signal is pulsed low to enable a EQUAD register write access. The D[7:0] bus contents are clocked into the addressed normal mode register on the rising edge of WRB while CSB is low.
ALE	Input	41	Address latch enable (ALE). This signal latches the address bus contents, A[9:0], when low, allowing the EQUAD to be interfaced to a multiplexed address/data bus. When ALE is high, the address latches are transparent. ALE has an integral pull-up.
RSTB	Input	40	Active low reset (RSTB). This signal is set low to asynchronously reset the EQUAD. RSTB is a Schmitt-trigger input with integral pull-up.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8] A[9]	Input	30 31 32 33 34 35 36 37 38 39	Address bus (A[9:0]). This bus selects specific registers during EQUAD register accesses.

Pin Name	Type	Pin No.	Function
PHA[0] PHA[1] PHA[2] PHA[3] PHA[4]	Power	18 52 89 105 121	AC power pins (PHA[4:0]). These pins must be connected to a common, well decoupled +5V DC supply together with the DC power pins PHD[3:0] .
PHD[0] PHD[1] PHD[2] PHD[3]	Power	20 50 85 115	DC power pins (PHD[3:0]). These pins must be connected to a common, well decoupled +5V DC supply together with the AC power pins PHA[4:0].
PLA[0] PLA[1] PLA[2] PLA[3] PLA[4] PLA[5]	Ground	19 53 90 106 122 1	AC ground pins (PLA[5:0]). These pins must be connected to a common ground together with the DC ground pins PLD[3:0].
PLD[0] PLD[1] PLD[2] PLD[3]	Ground	21 51 86 116	DC ground pins (PLD[3:0]). These pins must be connected to a common ground together with the AC ground pins PLA[5:0].

Notes on Pin Description:

1. The PLA[5:0] and PLD[3:0] ground pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the device. The PHA[4:0] and PHD[3:0] power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the device. These power supply connections must all be utilized and must all connect to a common +5 V or ground rail, as appropriate.

2. Inputs MENB, RSTB and ALE have integral pull-up resistors.

3. All outputs have 2 mA drive capability except for MRD and the D[7:0] bidirectionals which have 4 mA drive capability.

4. All inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels.

5. The TDLSIG/TDLINT[4:1] pins have integral pull-up resistors and default to being inputs after a reset.

6. When an internal RFDL is enabled, the RDLINT[x] output goes high:

   1) when the number of bytes specified in the RFDL Interrupt Status/Control Register have been received on the data link,

   2) immediately on detection of RFDL FIFO buffer overrun,

   3) immediately on detection of end of message,

   4) immediately on detection of an abort condition, or,

   5) immediately on detection of the transition from receiving all ones to flags.

   The interrupt is cleared at the start of the next RFDL Data Register read that results in an empty FIFO buffer. This is independent of the FIFO buffer fill level for which the interrupt is programmed. If there is still data remaining in the buffer, RDLINT[x] will remain high. An interrupt due to a RFDL FIFO buffer overrun condition is not cleared on a RFDL Data Register read but on a RFDL Status Register read. The RDLINT[x] output can always be forced low by disabling the RFDL (setting the EN bit in the RFDL Configuration Register to logic 0), or by forcing the RFDL to terminate reception (setting the TR bit in the RFDL Configuration Register to logic 1).

   The RDLINT[x] output may be forced low by disabling the interrupts with the RFDL Interrupt Status/Control Register. However, the internal interrupt latch is not cleared, and the state of this latch can still be read through the RFDL Interrupt Status/Control Register.

7. The RDLEOM[x] output goes high:

   1) immediately on detection of RFDL FIFO buffer overrun,

   2) when the data byte written into the RFDL FIFO buffer due to an end of message condition is read,

   3) when the data byte written into the RFDL FIFO buffer due to an abort condition is read, or,

   4) when the data byte written into the RFDL FIFO buffer due to the transition from receiving all ones to flags is read.

   RDLEOM[x] is set low by reading the associated RFDL Status Register or by disabling the RFDL.

8. The TDLUDR[x] output goes high when the processor is unable to service the TDLINT[x] request for more data before a specific time-out period. This period is dependent upon the frequency of TDLCLK[x]:

   1) for a TDLCLK[x] frequency of 4 kHz, the time-out is 1.0 ms;

   2) for a TDLCLK[x] frequency of 20 kHz, the time-out is 0.2 ms;

   3) for a TDLCLK[x] frequency of 64 kHz, the time-out is 62.5 µs.

8 FUNCTIONAL DESCRIPTION

8.1 Digital Receive Interface (DRIF)

The Digital E1 Receive Interface provides control over the various input options available on the multifunctional digital receive pins RDP/RDD[x] and RDN/RLCV[x]. When configured for dual-rail input, the multifunctional pins become the RDP[x] and RDN[x] inputs. These inputs can be enabled to receive either return-to-zero (RZ) or non-return-to-zero (NRZ) signals; the NRZ input signals can be sampled on either the rising or falling edge of RCLKI[x]. When the interface is configured for single-rail input, the multifunctional pins become the RDD[x] and RLCV[x] inputs, which can be sampled on either the rising or falling RCLKI[x] edge.

8.2 Clock and Data Recovery (CDRC)

The Clock and Data Recovery function is provided by a Data and Clock Recovery (CDRC) block that provides clock and PCM data recovery, HDB3 decoding, bipolar violation detection, and loss of signal detection. The CDRC block recovers the clock from the incoming RZ data pulses using a digital phase-locked-loop and recovers the NRZ data. Loss of signal is indicated after exceeding a programmed threshold of 10, 15, 31, 63 or 175 consecutive bit periods of the absence of pulses on both the positive and negative line pulse inputs and is cleared after the occurrence of a single line pulse. An alternate loss of signal indication is provided which is cleared only after 255 bit periods during which no sequence of four consecutive zeros has been received. If enabled, a microprocessor interrupt is generated when a loss of signal is detected and when the signal returns.

The HDB3 decoding is summarized as follows: If a bipolar violation (BPV) preceded by two zeros is received, the violation and the preceding three bit periods are decoded as four zeros. If AMI line code is selected, no substitution is made.

If HDB3 line code is selected, a line code violation is declared if any bipolar violation is of the same polarity as the previous BPV or if the BPV is not preceded by two spaces (the second criteria is maskable). If AMI line code is selected, all bipolar violations are counted as line code violations.

The input jitter tolerance for E1 interfaces complies with ITU-T Recommendation G.823. The tolerance is measured with a 2^{15}-1 sequence. The E1 jitter tolerance is with ALGSEL set to 1 and to 0 is shown in Figure 2 and Figure 3.

Figure 2 - CDRC jitter tolerance with ALGSEL = 1

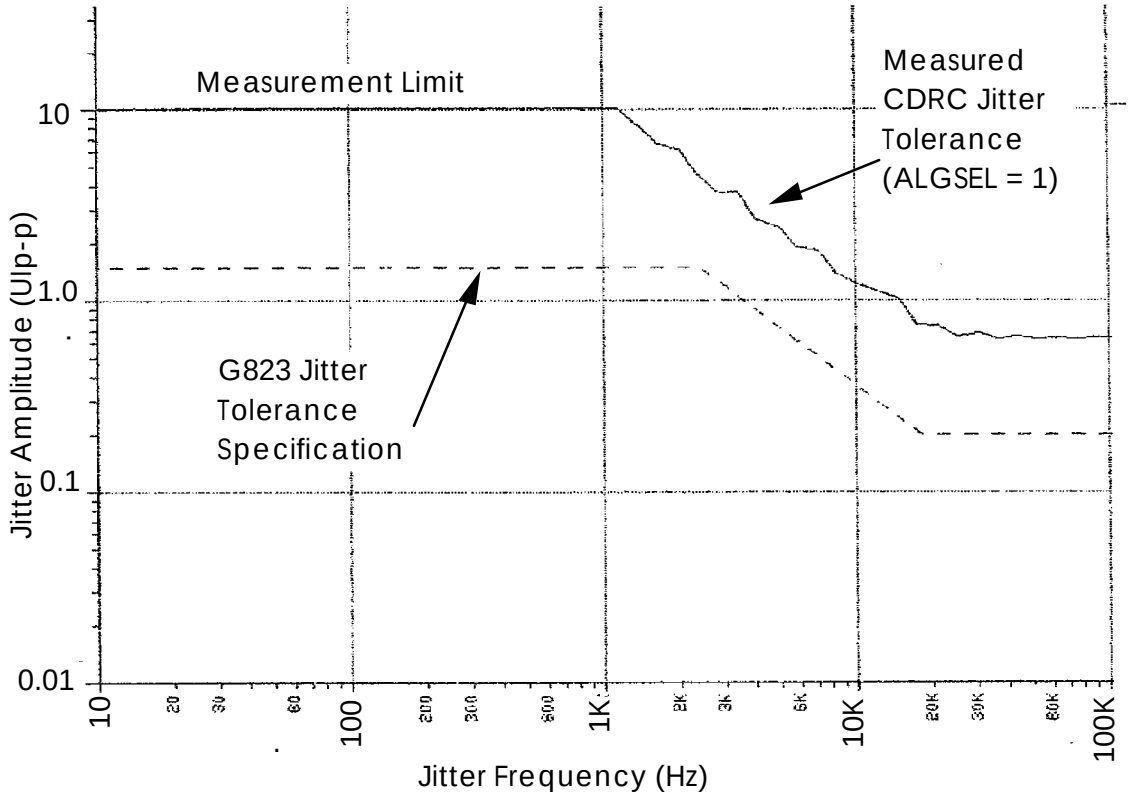
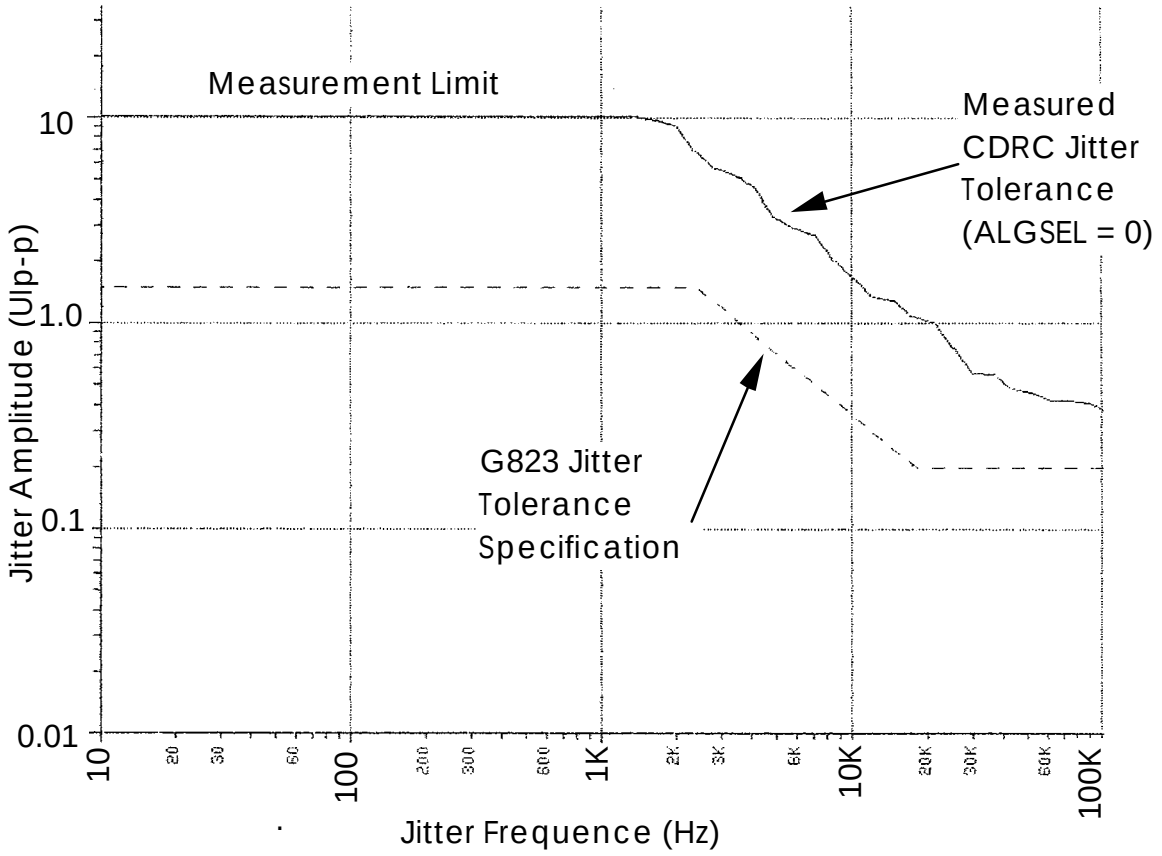


Figure 3 - CDRC jitter tolerance with ALGSEL = 0



8.3 Framer (FRMR)

The Framer (FRMR) block searches for frame alignment, CRC multiframe alignment, and channel associated signaling (CAS) multiframe alignment in the incoming recovered PCM stream.

Once the FRMR has found basic (or FAS) frame alignment, the incoming PCM data is continuously monitored for FAS/NFAS framing bit errors. Framing bit errors are accumulated in the framing bit error counter contained in the PMON block. Once the FRMR has found CAS multiframe alignment, the PCM data is continuously monitored for CAS multiframe alignment pattern errors. Once the

FRMR has found CRC multiframe alignment, the PCM data is continuously monitored for CRC multiframe alignment pattern errors, and CRC-4 errors. The FRMR also detects and indicates loss of frame, loss of CAS multiframe, and loss of CRC multiframe, based on user-selectable criteria. The reframe operation can be initiated by software (via the FRMR Frame Alignment Options Register), by excessive CRC errors, or when CRC multiframe alignment is not found within 8 ms. The FRMR also identifies the position of the frame, the CAS multiframe, and the CRC multiframe.

The FRMR extracts timeslot 16 for optional use as a data link and also extracts the contents of the International bits (from both the FAS frames and the NFAS frames), the National bits, and the Extra bits (from timeslot 16 of frame 0 of the CAS multiframe), and stores them in the FRMR International/National Bits Register, and the FRMR Extra Bits Register respectively.

The FRMR identifies the raw bit values for the remote (or distant frame) alarm (bit 3 in timeslot 0 of NFAS frames) and the remote signaling multiframe (or distant multiframe) alarm (bit 6 of timeslot 16 of frame 0 of the CAS multiframe) via the FRMR International/National Bits Register, and the FRMR Extra Bits Register respectively. Access is also provided to the "debounced" remote alarm and remote signaling multiframe alarm bits which are set when the corresponding signals have been a logic 1 for 2 or 3 consecutive occurrences, as per Recommendation O.162. Detection of AIS and timeslot 16 AIS are provided; AIS is also integrated and an AIS Alarm is indicated if the AIS condition has persisted for at least 100 ms. The out of frame (OOF=1) condition is also integrated, indicating a red Alarm if the OOF condition has persisted for at least 100 ms.

An interrupt may be generated to signal a change in the state of any status bits (OOF, OOSMF, OOCMF, AIS, or RED), and to signal when any event (RRA, RRMA, AISD, T16AISD, COFA, FER, SMFER, CMFER, CRCE, or FEBE) has occurred.

Frame Find

The Frame Find Block searches for frame alignment using one of two user-selectable algorithms, as defined in Recommendation G.706. Optionally, a two frame check sequence can be added to either algorithm to provide protection against false frame alignment in the presence of random mimic patterns.

The first algorithm finds frame alignment by using the following sequence:

1. Search for the presence of the correct 7-bit FAS;

2. Check that the FAS is absent in the following frame by verifying that bit 2 of the assumed timeslot 0 byte is a logic 1;

3. Check that the correct 7-bit FAS is present in the assumed timeslot 0 byte of the next frame.

If either of the conditions in steps 2 or 3 are not met, a new search for frame alignment is initiated in the bit immediately following the errored timeslot 0 byte location.

The second algorithm is similar to the first, but adds a one frame "hold-off" in step 2 to begin a new search in the bit immediately following the second 7-bit FAS that is checked. This "hold-off" is performed only after the condition in step 2 fails, providing a more robust algorithm which allows the framer to operate correctly in the presence of fixed timeslot data imitating the FAS pattern.

A check sequence can be added to either algorithm to verify correct frame alignment in the presence of random imitative FASs. Note that this check sequence should be enabled when monitoring an unframed 2^{15} -1 pseudo random sequence to avoid framing to the single mimic framing pattern contained in the sequence. The check consists of verifying correct frame alignment for an additional two frames, as follows:

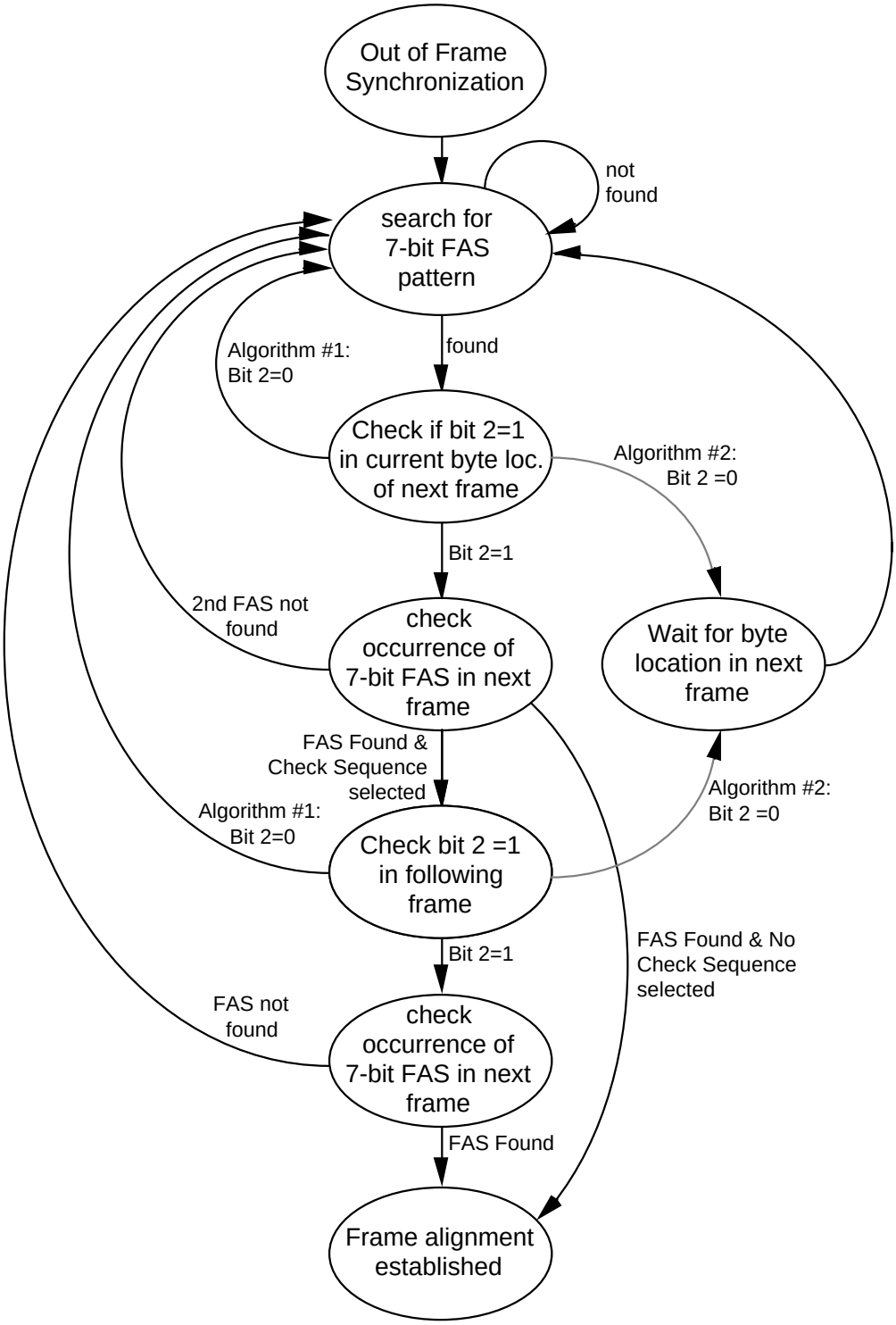
1. Once frame alignment (in frame "n") is determined, check that the FAS is absent in the following frame (frame "n+1") by verifying that bit 2 of timeslot 0 is a logic 1;

2. Then, check that the correct 7-bit FAS is present in timeslot 0 of the next frame (frame "n+2").

If either of the two conditions in the check sequence are not met, a new search for frame alignment is initiated in the bit immediately following the errored byte location when using the first algorithm, and is initiated in the bit immediately following the byte location in frame "n+2" when using the second algorithm.

These algorithms are illustrated in Figure 4.

Figure 4 - Basic Framing Algorithm Flowchart



These algorithms provide robust framing operation even in the presence of random bit errors: framing with algorithm #1 or #2 provides a 99.98% probability of finding frame alignment within 1 ms in the presence of 10^{-3} bit error rate and no mimic patterns.

Once frame alignment is found, the block sets the OOF indication low, indicates a change of frame alignment (if it occurred), and monitors the frame alignment signal, indicating errors occurring in the 7-bit FAS pattern and in bit 2 of NFAS frames, and indicating the debounced value of the Remote Alarm bit (bit 3 of NFAS frames). Using debounce, the Remote Alarm bit has <0.00001% probability of being falsely indicated in the presence of a 10^{-3} bit error rate. The block declares loss of frame alignment if 3 or 4 consecutive FASs have been received in error or, additionally, if bit 2 of NFAS frames has been in error for 3 consecutive occasions. In the presence of a random 10^{-3} bit error rate the frame loss criteria provides a mean time to falsely lose frame alignment of >12 minutes.

The Frame Find Block can be forced to initiate a frame search at any time when any of the following conditions are met:

- the software re-frame bit (REFR) in the Frame Alignment Options Register changes from logic 0 to logic 1;
- the CRC Frame Find Block is unable to find CRC multiframe alignment; or
- the CRC Frame Find Block accumulates excessive CRC evaluation errors (≥ 915 CRC errors in 1 second) and is enabled to force a re-frame.

CRC Frame Find

Once the basic frame alignment has been found, the CRC Frame Find Block searches for CRC multiframe alignment by observing whether the International bits (bit 1 of timeslot 0) of NFAS frames follow the CRC multiframe alignment pattern. Multiframe alignment is declared if at least two valid CRC multiframe alignment signals are observed within 8 ms, with the time separating two alignment signals being a multiple of 2 ms.

Once CRC multiframe alignment is found, the block sets the OOCMF indication low, and monitors the multiframe alignment signal, indicating errors occurring in the 6-bit pattern, and indicating the value of the FEBE bits (bit 1 of frames 13 and 15 of the multiframe).The block declares loss of CRC multiframe alignment if four consecutive CRC multiframe alignment signals have been received in error, or if frame alignment has been lost.

The CRC Frame Find Block will force the Frame Find Block to initiate a basic frame search when CRC multiframe alignment has not been found for 8 ms.

CRC Check and AIS Detection

The CRC Check and AIS Detect Block computes the 4-bit CRC checksum for each incoming sub-multiframe and compares this 4-bit result to the received CRC remainder bits in the subsequent sub-multiframe. The block also accumulates CRC errors over 1 second intervals, monitoring for excessive CRC errors and optionally, forcing the Frame Find Block to initiate a frame search when • 915 CRC errors occur in 1 second. The number of CRC errors accumulated during the previous second is available by reading the FRMR CRC Error Counter Registers.

The block also detects the occurrence of an unframed all-ones receive data stream, indicating the AIS by setting the AISD indication when less than 3 zero bits are received in 2 frames (512 consecutive bits); the AISD indication is reset when 3 or more zeros in the E1 stream are observed, or when frame alignment is found.

Signaling Frame Find

Once the basic frame alignment has been found, the Signaling Frame Find Block searches for CAS multiframe alignment using one of two user-selectable algorithms, one of which is compatible with Recommendation G.732. Once frame alignment has been found, the first algorithm monitors timeslot 16 of each frame; it declares CAS multiframe alignment when 15 consecutive frames with bits 1-4 of timeslot 16 not containing the alignment pattern are observed to precede a frame with timeslot 16 containing the correct alignment pattern. The second algorithm, compatible with G.732, also monitors timeslot 16 of each frame, and declares CAS multiframe alignment when non-zero bits 1-4 of timeslot 16 are observed to precede a timeslot 16 containing the correct alignment pattern.

Once CAS multiframe alignment has been found, the block sets the OOSMF indication to logic 0, and monitors the CAS multiframe alignment signal, indicating errors occurring in the 4-bit pattern, and indicating the debounced value of the remote signaling multiframe alarm bit (bit 6 of timeslot 16 of frame 0 of the multiframe). Using debounce, the remote signaling multiframe alarm bit has < 0.00001% probability of being falsely indicated in the presence of a 10^{-3} bit error rate. This block also indicates the reception of timeslot 16 AIS when timeslot 16 has been all-ones for two consecutive frames while out of CAS multiframe. The block declares loss of CAS multiframe alignment if two

consecutive CAS multiframe alignment signals have been received in error, or additionally, if all the bits in timeslot 16 are logic 0 for 1 or 2 (selectable) CAS multiframes. Loss of CAS multiframe alignment is also declared if frame alignment has been lost.

Alarm Integration

The Alarm Integrator Block monitors the OOF and the AIS indications, verifying that each condition has persisted for 104 ms (±6 ms) before indicating the alarm condition. The alarm is removed when the condition has been absent for 104 ms (±6 ms).

The AIS alarm algorithm accumulates the occurrences of AISD (AIS detection). AISD is defined as an unframed pattern with less than 3 zeros in two consecutive frame times (512 bits). The Alarm Integrator Block counts the occurrences of AISD over a 4 ms interval and indicates a valid AIS presence when 13 or more AISD indications (of a possible 16) have been received. Each interval with a valid AIS presence indication increments an interval counter which declares AIS Alarm when 25 valid intervals have been accumulated. An interval with no valid AIS presence indication decrements the interval counter; the AIS Alarm declaration is removed when the counter reaches 0. This algorithm provides a 99.8% probability of declaring an AIS Alarm within 104 ms in the presence of a 10^{-3} mean bit error rate.

The TS16 AIS alarm algorithm accumulates the occurrences of TS16AISD (TS16 AIS detection). TS16AISD is defined as two consecutive all ones time slot 16 bytes while out of signaling multiframe. Each interval with a valid TS16 AIS presence indication increments an interval counter which declares TS16 AIS Alarm when 22 valid intervals have been accumulated. An interval with no valid TS16 AIS presence indication decrements the interval counter; the TS16 AIS Alarm declaration is removed when the counter reaches 0. This algorithm provides a 99.1% probability of declaring an TS16 AIS Alarm within 3.1 ms after loss of signaling multiframe detection in the presence of a 10^{-3} mean bit error rate.

The red alarm algorithm monitors occurrences of OOF over a 4 ms interval, indicating a valid OOF interval when one or more OOF indications occurred during the interval, and indicating a valid in frame (INF) interval when no OOF indication occurred for the entire interval. Each interval with a valid OOF indication increments an interval counter which declares RED Alarm when 25 valid intervals have been accumulated. An interval with valid INF indication decrements the interval counter; the RED Alarm declaration is removed when the

counter reaches 0. This algorithm biases OOF occurrences, leading to declaration of red alarm when intermittent loss of frame alignment occurs.

8.4 Performance Monitor Counters (PMON)

The Performance Monitor Counters function is provided by the Performance Monitor (PMON) block that accumulates CRC error events, frame synchronization bit error events, line code violation events, and far end block error events with saturating counters over consecutive intervals as defined by the period of the supplied transfer clock signal (typically 1 second). When the transfer clock signal is applied, the PMON block transfers the counter values into holding registers and resets the counters to begin accumulating events for the interval. The counters are reset in such a manner that error events occurring during the reset are not missed. If enabled, an interrupt is generated whenever counter data is transferred into the holding registers. If the holding registers are not read between successive transfer clocks, an OVERRUN register bit is asserted.

Generation of the transfer clock within the EQUAD chip is performed by writing to any counter register location (X4AH to X4FH) or by writing to the EQUAD Revision/Chip ID/Global PMON Update register (00CH). The holding register addresses are contiguous to facilitate polling operations.

8.5 HDLC Receiver (RFDL)

The HDLC Receiver function is provided by the RFDL block. The RFDL is a microprocessor peripheral used to receive LAPD/HDLC frames on either Time Slot 16 or the National Use bits of Time Slot 0.

The RFDL detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives frame data, and calculates the CRC Q.921 frame check sequence (FCS).

Received data is placed into a 4-level FIFO buffer. The Status Register contains bits which indicate overrun, end of message, flag detected, and buffered data available.

On end of message, the Status Register also indicates the FCS status and the number of valid bits in the final data byte. Interrupts are generated when one, two or three bytes (programmable via the RFDL configuration register) are stored in the FIFO buffer. Interrupts are also generated when the terminating flag sequence, abort sequence, or FIFO buffer overrun are detected.

When the internal HDLC receiver is disabled, the serial data extracted by the FRMR block is output on the RDLSIG[x] pin and is updated on the falling clock edge of the RDLCLK[x] pin.

8.6 Elastic Store (ELST)

The Elastic Store function is provided by the ELST block.

The Elastic Store (ELST) block synchronizes incoming PCM frames to the local backplane clock, BRCLK. The frame data is buffered in a two frame circular data buffer. Input data is written to the buffer using a write pointer and output data is read from the buffer using a read pointer.

When the backplane timing is derived from the receive line data (i.e. the RCLKO[x[output is used), the elastic store can be bypassed to eliminate the 2 frame delay. In this configuration the elastic store can be used to measure frequency differences between the recovered line clock and another 2.048 MHz clock applied to the BRCLK input. A typical example might be to measure the difference in frequency between two received E1 streams (i.e. East-West frequency difference) by monitoring the number of SLIP occurrences of one direction with respect to the other.

When the elastic store is being used, if the average frequency of the incoming data is greater than the average frequency of the backplane clock, the write pointer will catch up to the read pointer and the buffer will be filled. Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary. The following frame of PCM data will be deleted.

If the average frequency of the incoming data is less than the average frequency of the backplane clock, the read pointer will catch up to the write pointer and the buffer will be empty. Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary. The last frame which was read will be repeated.

A slip operation is always performed on a frame boundary.

To allow for the extraction of signaling information in the PCM data timeslots, multiframe identification is also passed through the ELST.

8.7 Signaling Extractor (SIGX)

The Signaling Extraction function is provided by the Signaling Extractor (SIGX) block. The block provides channel associated signaling (CAS) extraction from an E1 signaling multiframe. Signaling data is extracted from timeslot 16 of each

frame within a signaling multiframe and buffered. The SIGX selectively debounces the bits, and serializes the results onto the 2048 kbit/s serial stream BRSIG[x] output. Buffered signaling data is aligned with its associated voice timeslot in the E1 frame.

The SIGX provides user control over signaling freezing with a 95% confidence level of freezing with valid signaling data for a 50% ones density out-of-frame condition. The SIGX also provides control over timeslot data inversion, trunk conditioning, and signaling debounce on a per-timeslot basis directly, via the Microprocessor Interface (MPIF).

8.8 Backplane Receive Interface (BRIF)

The Backplane Receive Interface allows data to be presented to a backplane in either a 2.048 Mbit/s or a 16.384 Mbit/s serial stream and allows BPV transparency by outputting dual-rail data at 2.048 Mbit/s.

The block generates the output data stream on the BRPCM[x] pin containing 32 timeslot bytes of data. The BRSIG[x] output pin contains 30 bytes of signaling nibble data located in the least significant nibble of each byte. The framing alignment indication on the BRFPO[x] pin can be configured to indicate the first bit of each 256-bit frame, the first bit of the first frame of the CRC multiframe, the first bit of the first frame of the signaling multiframe or all overhead bits.

When configured for a multiplexed backplane, the four sets of PCM and signaling streams are bit interleaved into a 16.384 Mbit/s serial stream. The MRFPI pin must go to logic "1" for one MRCLK cycle to indicate the alignment of the first PCM bit of the frame or multiframe from receiver number one.

8.9 Transmitter (TRAN)

The Transmitter function is provided by the TRAN block.

The TRAN generates a 2048 kbit/s data stream according to ITU-T recommendations, providing individual enables for frame generation, CRC multiframe generation, and channel associated signaling (CAS) multiframe generation.

In concert with Transmit Per-Channel Serial Controller (TPSC), the TRAN block provides per-timeslot control of idle code substitution, data inversion, digital milliwatt substitution, selection of the signaling source and CAS data. All timeslots can be forced into a trunk conditioning state (idle code substitution and

signaling substitution) by use of the master trunk conditioning bit in the Configuration Register.

Common Channel Signaling (CCS) is supported in time slot 16 either through the internal HDLC Transmitter (XFDL) or through a serial data input and clock output. Support is provided for the transmission of AIS and TS16 AIS, and the transmission of remote alarm and remote multiframe alarm signals.

PCM output signals may be selected to conform to HDB3 or AMI line coding.

8.10 Transmit Per-Channel Serial Controller (PCSC)

The Transmit Per-channel Serial Controller allows data and signaling trunk conditioning or idle code to be applied on the transmit E1 stream on a per-timeslot basis. It also allows per-timeslot control of data inversion and application of digital milliwatt.

The Transmit Per-channel Serial Controller function is provided by a Per-Channel Serial Controller (PCSC) block. The TPSC interfaces directly to the TRAN block and provides serial streams for signaling control, idle code data and PCM data control.

The registers are accessible from the µP interface in an indirect address mode. The BUSY indication signal can be polled from an internal status register to check for completion of the current operation.

8.11 HDLC Transmitter (XFDL)

The HDLC Transmitter function is provided by the XFDL block. The XFDL is designed to provide a serial data link for the TRAN E1 Transmitter block. The XFDL is used under microprocessor or DMA control to transmit HDLC data frames in Time Slot 16 or in the Time Slot 0 National Use bits when the EQUAD is enabled to use the internal HDLC transmitter. The XFDL performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, idle, and abort sequence insertion. Data to be transmitted is provided on an interrupt-driven basis by writing to a double-buffered transmit data register. Upon completion of the frames, a CRC Q.921 frame check sequence is transmitted, followed by idle flag sequences. If the transmit data register underflows, an abort sequence is automatically transmitted.

When enabled for use (via the EN bit in the XFDL Configuration register), the XFDL continuously transmits the flag character (01111110). Data bytes to be transmitted are written into the Transmit Data Register. After the parallel-to-serial

conversion of each data byte, an interrupt is generated to signal the controller to write the next byte into the Transmit Data Register. After the last data frame byte is transmitted, the CRC word (if CRC insertion has been enabled), or a flag (if CRC insertion has not been enabled) is transmitted. The XFDL then returns to the transmission of flag characters.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort characters.

Abort characters can be continuously transmitted at any time by setting a control bit. During transmission, an underrun situation can occur if data is not written to the Transmit Data Register before the previous byte has been depleted. In this case, an abort sequence is transmitted, and the controlling processor is notified via the TDLUDR signal. Optionally, the interrupt and underrun signals can be independently enabled to also generate an interrupt on the INTB output, providing a means to notify the controlling processor of changes in the XFDL operating status.

When the internal HDLC transmitter is disabled, the serial data to be transmitted on data link can be input on the TDLSIG pin timed to the clock rate output on the TDLCLK pin.

8.12 Digital Jitter Attenuator (DJAT)

The Digital Jitter Attenuation function is provided by the Digital Jitter Attenuator (DJAT) block. The DJAT block receives jittered E1 data in NRZ format from TRAN on two separate inputs, which allows bipolar violations to pass through the block uncorrected. The incoming data streams are stored in a FIFO timed to the transmit clock (either BTCLK[x] or RCLKO[x]). The respective input data emerges from the FIFO timed to the jitter attenuated clock (TCLKO[x]) referenced to either TCLKI[x], BTCLK[x], or RCLKO[x].

The jitter attenuator generates the jitter-free 2.048 MHz TCLKO[x] output transmit clock by adaptively dividing the 49.152 MHz XCLK signal according to the phase difference between the generated TCLKO[x] and input data clock to DJAT (either BTCLK[x] or RCLKO[x]). Fluctuations in the phase of the input data clock are attenuated by the phase-locked loop within DJAT so that the frequency of TCLKO[x] is equal to the average frequency of the input data clock. Phase fluctuations with a jitter frequency above 8.8 Hz are attenuated by 6 dB per octave of jitter frequency. Wandering phase fluctuations with frequencies below 8.8 Hz are tracked by the generated TCLKO[x]. To provide a smooth flow of data out of DJAT, TCLKO[x] is used to read data out of the FIFO.

If the FIFO read pointer (timed to TCLKO[x]) comes within one bit of the write pointer (timed to the input data clock, BTCLK[x] or RCLKO[x]), DJAT will track the jitter of the input clock. This permits the phase jitter to pass through unattenuated, inhibiting the loss of data.

Jitter Characteristics

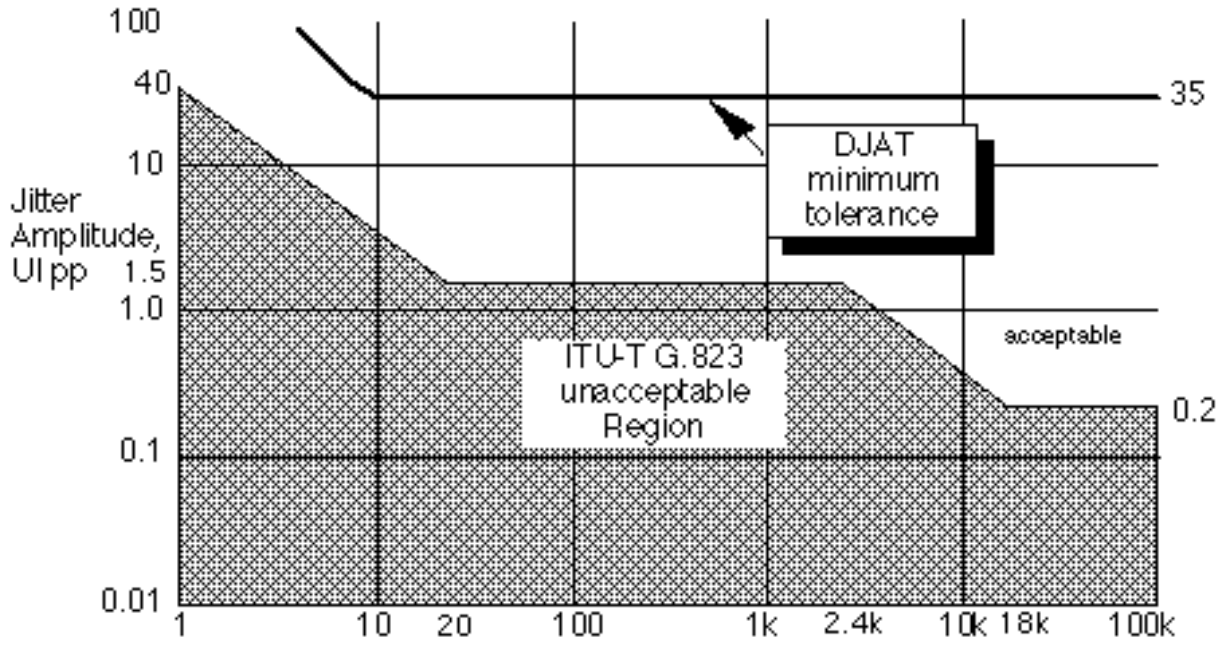
The DJAT Block provides excellent jitter tolerance and jitter attenuation while generating minimal residual jitter. It can accommodate up to 35 UIpp of input jitter at jitter frequencies above 9 Hz. For jitter frequencies below 9 Hz, more correctly called wander, the tolerance increases 20 dB per decade. In most applications the DJAT Block will limit jitter tolerance at lower jitter frequencies only. For high frequency jitter, above 10 kHz for example, other factors such as the clock and data recovery circuitry may limit jitter tolerance and must be considered. For low frequency wander, below 10 Hz for example, other factors such as slip buffer hysteresis may limit wander tolerance and must be considered. The DJAT Block meets the low frequency jitter tolerance requirements of ITU-T Recommendation G.823.

DJAT exhibits negligible jitter gain for jitter frequencies below 8.8 Hz, and attenuates jitter at frequencies above 8.8 Hz by 20 dB per decade. In most applications the DJAT Block will determine jitter attenuation for higher jitter frequencies only. Wander, below 10 Hz for example, will essentially be passed unattenuated through DJAT. Jitter, above 10 Hz for example, will be attenuated as specified, however, outgoing jitter may be dominated by the generated residual jitter of in cases where incoming jitter is insignificant. This generated residual jitter is directly related to the use of 24X (49.152 MHz) digital phase locked loop for transmit clock generation. DJAT meets the jitter attenuation requirements of the ITU-T Recommendations G.737, G.738, G.739 and G.742.

Jitter Tolerance

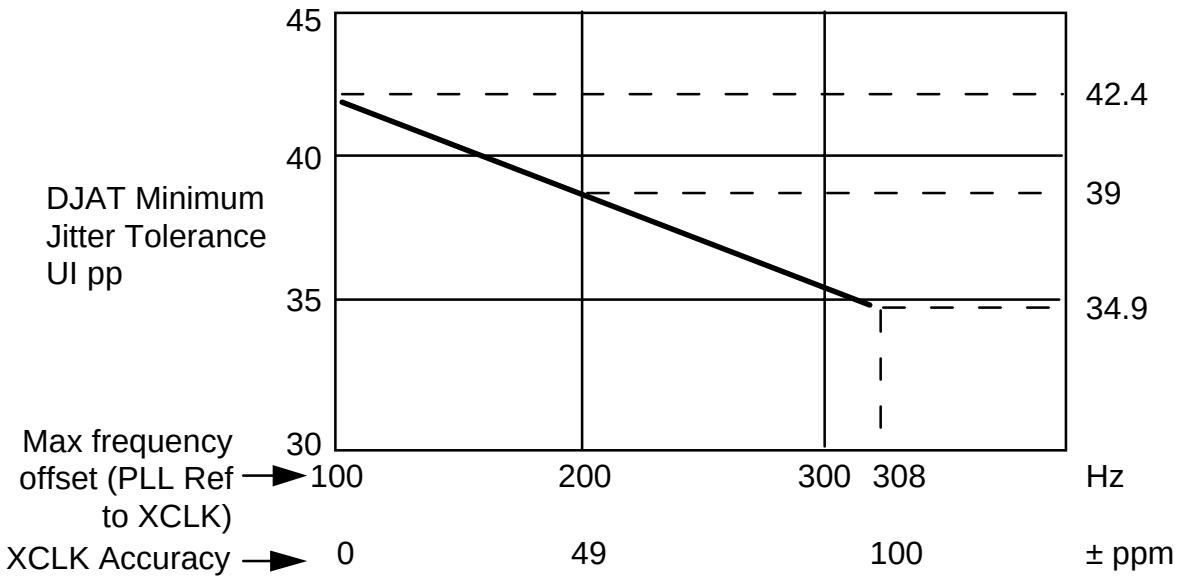
Jitter tolerance is the maximum input phase jitter at a given jitter frequency that a device can accept without exceeding its linear operating range, or corrupting data. For DJAT, the input jitter tolerance is 35 Unit Intervals peak-to-peak (UIpp) with a worst case frequency offset of 308 Hz. It is 48 UIpp with no frequency offset. The frequency offset is the difference between the frequency of XCLK divided by 24 and that of the input data clock.

Figure 5 - DJAT Jitter Tolerance



The accuracy of the XCLK frequency and that of the DJAT PLL reference input clock used to generate the jitter-free TCLKO[x] have an effect on the minimum jitter tolerance. Given that the DJAT PLL reference clock accuracy can be ±103 Hz from 2.048 MHz, and that the XCLK input accuracy can be ±100 ppm from 49.152 MHz, the minimum jitter tolerance for various differences between the frequency of PLL reference clock and XCLK/24 are shown in Figure 6.

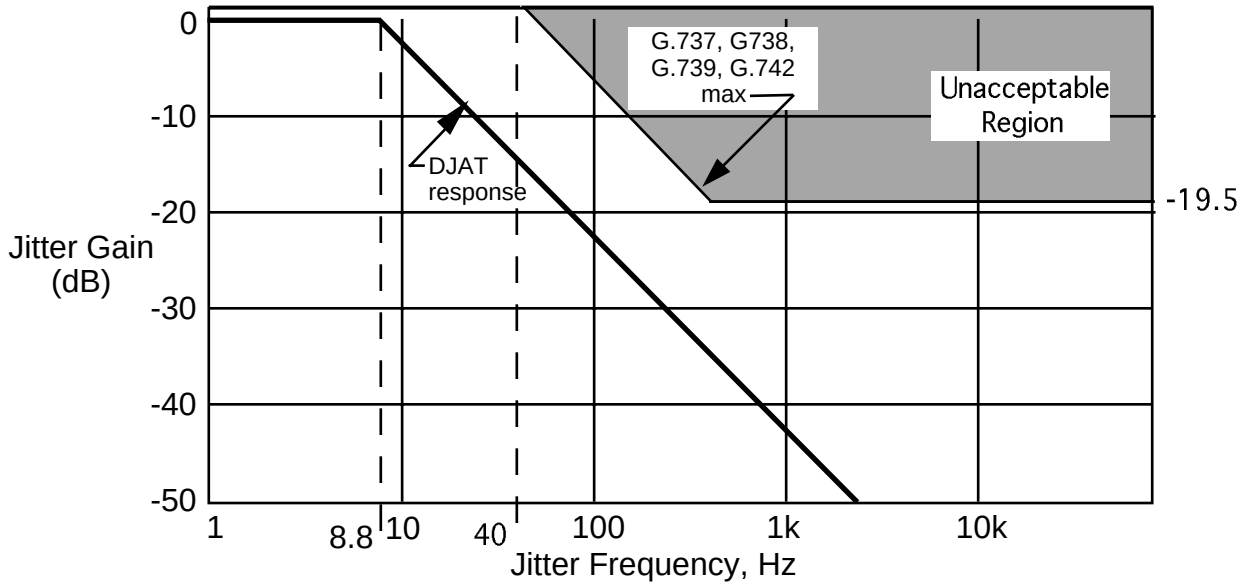
Figure 6 - DJAT Minimum Jitter Tolerance vs. XCLK Accuracy



Jitter Transfer

The output jitter for jitter frequencies from 0 to 8.8 Hz is no more than 0.1 dB greater than the input jitter, excluding the residual jitter. Jitter frequencies above 8.8 Hz are attenuated at a level of 6 dB per octave, as shown in Figure 7.

Figure 7 - DJAT Jitter Transfer



Frequency Range

In the non-attenuating mode, that is, when the FIFO is within one UI of overrunning or under running, the tracking range is 1.963 to 2.133 MHz. The guaranteed linear operating range for the jittered input clock is 2.048 MHz ± 1278 Hz with worst case jitter (42 UIpp) and maximum XCLK frequency offset (± 100 ppm). The nominal range is 2.048 MHz ± 103 Hz with no jitter or XCLK frequency offset.

8.13 Timing Options (TOPS)

The Timing Options block provides a means of selecting the source of the internal input clock to the DJAT block, the reference signal for the digital PLL, and the clock source used to derive the output TCLKO[x] signal.

8.14 Digital E1 Transmit Interface (DTIF)

The Digital E1 Transmit Interface provides control over the various output options available on the multifunctional digital transmit pins TDP/TDD[x] and TDN/TFLG[x]. When configured for dual-rail output, the multifunctional pins become the TDP[x] and TDN[x] outputs. These outputs can be formatted as either return-to-zero (RZ) or non-return-to-zero (NRZ) signals and can be

updated on either the rising or falling edge of TCLKO[x]. When the interface is configured for single-rail output, the multifunctional pins become the TDD[x] and TFLG[x] outputs, which can be enabled to be updated on either the rising or falling TCLKO[x] edge. Further, the TFLG[x] output can be enabled to indicate FIFO empty or FIFO full status.

The DTIF block also provides Alarm Indication Signaling (AIS) generation capability by generating alternating mark signals on the TDP/TDN[x] outputs, or all-ones on the TDD[x] output, when the TAISEN bit is set in the Transmit E1 Interface Configuration register. This is useful when the internal loopback modes are used.

8.15 Backplane Transmit Interface (BTIF)

The Backplane Transmit Interface allows data to be taken from a backplane in either a 2.048 Mbit/s or 16.384 Mbit/s serial stream and allows BPV transparency by accepting dual-rail data input at 2.048 Mbit/s.

When configured to receive a 2.048 Mbit/s data rate stream, the block expects the input data stream on the BTPCM[x] pin to contain 32 timeslots. The BTSIG[x] input pin must contain 30 bytes of signaling nibble data located in the least significant nibble of each byte. The framing alignment indication on the BTFP[x] pin indicates the framing bit position of the 256-bit frame (or, optionally, the framing bit position of the first frame of the signaling multiframe frame, and the CRC multiframe).

When configured to interface to a 16.384 Mbit/s serial stream, the four sets of PCM and signaling streams are expected to be bit interleaved. The MTFP pin marks the framing bit position of the first multiplexed PCM stream (destined for transmitter number one) or, optionally, the framing bit position of the first frame of the signaling multiframe frame, and the CRC multiframe. MTFP operates in a similar fashion to BTFP[x], but is only valid at positions coincident with the first multiplexed PCM stream. All four multiplexed interfaces will have the same frame, signaling multiframe, and CRC multiframe alignment. See the Functional Timing section for more details.

8.16 Microprocessor Interface (MPIF)

The Microprocessor Interface allows the EQUAD to be configured, controlled and monitored via internal registers.

9 REGISTER DESCRIPTION

Table 1 - Normal Mode Register Memory Map

Address				Register
#1	# 2	# 3	# 4	
000H	080H	100H	180H	Receive Options
001H	081H	101H	181H	Receive Backplane Options
002H	082H	102H	182H	Datalink Options
003H	083H	103H	183H	Receive Interface Configuration
004H	084H	104H	184H	Transmit Interface Configuration
005H	085H	105H	185H	Transmit Backplane Options
006H	086H	106H	186H	Transmit Framing and Bypass Options
007H	087H	107H	187H	Transmit Timing Options
008H	088H	108H	188H	Master Interrupt Source
009H	089H	109H	189H	Receive TS0 Data Link Enables
00AH	08AH	10AH	18AH	Master Diagnostics
00BH				EQUAD Master Test
00CH				EQUAD Revision/Chip ID/Global PMON Update
	08BH	10BH	18BH	Reserved
	08CH	10CH	18CH	Reserved
00DH	08DH	10DH	18DH	Framer Reset
00EH	08EH	10EH	18EH	Phase Status Word (LSB)
00FH	08FH	10FH	18FH	Phase Status Word (MSB)
010H	090H	110H	190H	CDRC Configuration
011H	091H	111H	191H	CDRC Interrupt Enable
012H	092H	112H	192H	CDRC Interrupt Status
013H	093H	113H	193H	Alternate Loss of Signal

Address				Register
#1	# 2	# 3	# 4	
014H	094H	114H	194H	Channel Select (1 to 8)
015H	095H	115H	195H	Channel Select (9 to 16)
016H	096H	116H	196H	Channel Select (17 to 24)
017H	097H	117H	197H	Channel Select (25 to 32)
018H	098H	118H	198H	DJAT Interrupt Status
019H	099H	119H	199H	DJAT Reference Clock Divisor (N1) Control
01AH	09AH	11AH	19AH	DJAT Output Clock Divisor (N2) Control
01BH	09BH	11BH	19BH	DJAT Configuration
01CH	09CH	11CH	19CH	ELST Configuration
01DH	09DH	11DH	19DH	ELST Interrupt Enable/Status
01EH	09EH	11EH	19EH	ELST Idle Code
01FH	09FH	11FH	19FH	ELST Reserved
020H	0A0H	120H	1A0H	FRMR Framing Alignment Options
021H	0A1H	121H	1A1H	FRMR FRMR Maintenance Mode Options
022H	0A2H	122H	1A2H	FRMR Framing Status Interrupt Enable
023H	0A3H	123H	1A3H	FRMR Maintenance/Alarm Status Interrupt Enable
024H	0A4H	124H	1A4H	FRMR Framing Status Interrupt Indication
025H	0A5H	125H	1A5H	FRMR Maintenance/Alarm Status Interrupt Indication
026H	0A6H	126H	1A6H	FRMR Framing Status
027H	0A7H	127H	1A7H	FRMR Maintenance/Alarm Status
028H	0A8H	128H	1A8H	FRMR International/National Bits
029H	0A9H	129H	1A9H	FRMR Extra Bits
02AH	0AAH	12AH	1AAH	FRMR CRC Error Count - LSB

Address				Register
#1	# 2	# 3	# 4	
02BH	0ABH	12BH	1ABH	FRMR CRC Error Count - MSB
02CH	0ACH	12CH	1ACH	TS16 AIS Alarm Status
02DH	0ADH	12DH	1ADH	Reserved
02EH	0AEH	12EH	1AEH	Reserved
02FH	0AFH	12FH	1AFH	Reserved
030H	0B0H	130H	1B0H	TPSC Configuration
031H	0B1H	131H	1B1H	TPSC µP Access Status
032H	0B2H	132H	1B2H	TPSC Timeslot Indirect Address/Control
033H	0B3H	133H	1B3H	TPSC Timeslot Indirect Data Buffer
034H	0B4H	134H	1B4H	XFDL Configuration
035H	0B5H	135H	1B5H	XFDL Interrupt Status
036H	0B6H	136H	1B6H	XFDL Transmit Data
037H	0B7H	137H	1B7H	XFDL Reserved
038H	0B8H	138H	1B8H	RFDL Configuration
039H	0B9H	139H	1B9H	RFDL Interrupt Control/Status
03AH	0BAH	13AH	1BAH	RFDL Status
03BH	0BBH	13BH	1BBH	RFDL Receive Data
03CH	0BCH	13CH	1BCH	Interrupt ID (reg 03CH only)/Clock Monitor
03DH	0BDH	13DH	1BDH	Backplane Parity Configuration and Status
03EH	0BEH	13EH	1BEH	Reserved
03FH	0BFH	13FH	1BFH	Reserved
040H	0C0H	140H	1C0H	SIGX Configuration
041H	0C1H	141H	1C1H	SIGX µP Access Status
042H	0C2H	142H	1C2H	SIGX Timeslot Indirect Address/Control
043H	0C3H	143H	1C3H	SIGX Timeslot Indirect Data Buffer

Address				Register
#1	# 2	# 3	# 4	
044H	0C4H	144H	1C4H	TRAN Configuration
045H	0C5H	145H	1C5H	TRAN Transmit Alarm/Diagnostic Control
046H	0C6H	146H	1C6H	TRAN International/National Control
047H	0C7H	147H	1C7H	TRAN Extra Bits Control
048H	0C8H	148H	1C8H	PMON Control/Status
049H	0C9H	149H	1C9H	PMON FER Count
04AH	0CAH	14AH	1CAH	PMON FEBE Count (LSB)
04BH	0CBH	14BH	1CBH	PMON FEBE Count (MSB)
04CH	0CCH	14CH	1CCH	PMON CRC Count (LSB)
04DH	0CDH	14DH	1CDH	PMON CRC Count (MSB)
04EH	0CEH	14EH	1CEH	PMON LCV Count (LSB)
04FH	0CFH	14FH	1CFH	PMON LCV Count (MSB)
050H-07FH	0D0H-0FFH	150H-17FH	1D0H-1FFH	Reserved
200H-3FFH				Reserved for Test

10 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the EQUAD. Normal mode registers (as opposed to test mode registers) are selected when A[9] is low.

Notes on Normal Mode Register Bits:

1. Although the register bit descriptions for the four framers have been combined, each framer is completely independent of the others.

2. Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.

3. All configuration bits that can be written into can also be read back. This allows the processor controlling the EQUAD to determine the programming state of the chip.

4. Writeable normal mode register bits are cleared to zero upon reset unless otherwise noted.

5. Writing into read-only normal mode register bit locations does not affect EQUAD operation unless otherwise noted.

Register 000H, 080H, 100H, 180H: Receive Options

Bit	Type	Function	Default
Bit 7	R/W	WORDERR	0
Bit 6	R/W	CNTNFAS	0
Bit 5	R/W	ELSTBYP	0
Bit 4	R/W	TRSLIP	0
Bit 3		Unused	X
Bit 2	R/W	SRSMFP	0
Bit 1	R/W	SRCMFP	0
Bit 0	R/W	TRKEN	0

This register allows software to configure the receive functions.

WORDERR:

The WORDERR bit determines how frame alignment signal (FAS) errors are reported. When WORDERR is logic 1, one or more errors in the seven bit FAS word results in a single framing error count. When WORDERR is logic 0, each error in a FAS word results in a single framing error count.

CNTNFAS:

When the CNTNFAS bit is a logic 1, a zero in bit 2 of time slot 0 of non-frame alignment signal (NFAS) frames results in an increment of the framing error count. If WORDERR is also a logic 1, the word is defined as the eight bits comprising the FAS pattern and bit 2 of time slot 0 of the next NFAS frame. When the CNTNFAS bit is a logic 0, only errors in the FAS affect the framing error count.

ELSTBYP:

The ELSTBYP bit allows the Elastic Store (ELST) block to be bypassed, eliminating the one frame delay incurred through the ELST. When set to logic 1, the received data and clock inputs to ELST are internally routed directly to the ELST outputs.

TRSLIP:

The TRSLIP bit allows the ELST block to be used to measure, through SLIP indications, the frequency difference between the recovered receive line clock

and the transmit clock driving the TRAN block when the ELST is bypassed. When TRSLIP is set to logic 1, the transmit clock input to TRAN is internally substituted for the BRCLK input to the system side of the ELST. When TRSLIP is set to logic 0, the BRCLK input is routed to the system side of the ELST. The TRSLIP bit should only be set if ELSTBYP is set to logic 1.

SRSMFP, SRCMFP:

The SRSMFP and SRCMFP bits select the output signal seen on the output RFP[x]. RFP[x] can be used to show the frame alignment when fractional E1 extraction is being used (RFRACE1 is set to logic 1 in the DataLink Options register and the CH[32:1] bits are set appropriately in the Channel Select registers). The following table summarizes the four configurations:

SRSMFP	SRCMFP	Result
0	0	Receive frame pulse output: RFP[x] pulses high for 1 RCLKO[x] cycle during bit 1 of each 256-bit frame, indicating the frame alignment of the RDLSIG[x] fractional E1 data stream.
0	1	Receive CRC multiframe output: RFP[x] pulses high for 1 RCLKO[x] cycle during bit 1 of frame 1 of every 16 frame CRC multiframe, indicating the CRC multiframe alignment of the RDLSIG[x] fractional E1 data stream. (Even when CRC multiframing is disabled, the RFP[x] output continues to indicate the position of bit 1 of the FAS frame every 16th frame.)
1	0	Receive signaling multiframe output: RFP[x] pulses high for 1 RCLKO[x] cycle during bit 1 of frame 1 of the 16 frame signaling multiframe, indicating the signaling multiframe alignment of the RDLSIG[x] fractional E1 data stream. (Even when signaling multiframing is disabled, the RFP[x] output continues to indicate the position of bit 1 of every 16th frame.)

SRSMFP	SRCMFP	Result
1	1	Receive composite multiframe output: RFP[x] goes high on the falling RCLKO[x] edge marking the beginning of bit 1 of frame 1 of every 16 frame signaling multiframe, indicating the signaling multiframe alignment of the RDLSIG[x] fractional E1 data stream, and returns low on the falling RCLKO[x] edge marking the end of bit 1 of frame 1 of every 16 frame CRC multiframe, indicating the CRC multiframe alignment of the RDLSIG[x] fractional E1 data stream. This mode allows both multiframe alignments to be decoded externally from the single RFP[x] signal. Note that if the signaling and CRC multiframe alignments are coincident, RFP[x] will pulse high for 1 RCLKO[x] cycle every 16 frames.

TRKEN:

The TRKEN bit enables receive trunk conditioning upon an out-of-frame-condition. If TRKEN is logic 1, the contents of the ELST Idle Code register are inserted into all time slots (including TS0 and TS16) of BRPCM if the framer is out-of-basic frame (i.e. the OOF status bit is logic 1). The TRKEN bit only has effect if the BRX2RAIL and ELSTBYP bits are both logic 0. If TRKEN is a logic 0, receive trunk conditioning can still be performed on a per-timeslot basis via the SIGX Per-Timeslot Trunk Conditioning Data Registers

Upon reset of the EQUAD, these bits are cleared to zero.

Register 001H, 081H, 101H, 181H: Receive Backplane Options

Bit	Type	Function	Default
Bit 7	R/W	RCLKOSEL	0
Bit 6		Unused	X
Bit 5	R/W	RXDMAGAT	0
Bit 4	R/W	ROHM	0
Bit 3	R/W	BRX2RAIL	0
Bit 2	R/W	BRXSMFP	0
Bit 1	R/W	BRXCMFP	0
Bit 0	R/W	OOSMFAIS	0

This register allows software to configure the Receive backplane interface format.

RCLKOSEL:

The RCLKOSEL bit selects the source of the RCLKO[x] output and the internal elastic store output clock. If RCLKOSEL is a logic zero, RCLKO[x] is the recovered clock derived from RDP[x] and RDN[x] or RCLKI[x] and the internal elastic store output clock is BRCLK. If RCLKOSEL is a logic one, RCLKO[x] and the internal elastic store output clock originate from the smooth 2.048 MHz clock generated by the DJAT phase locked loop. If the recovered clock is selected as the PLL reference, the configuration implements jitter attenuation in the receive direction. See the Operations Section for details on this application. TRSLIP must be set to logic 0.

RXDMAGAT:

The RXDMAGAT bit selects the gating of the RDLINT[x] output with the RDLEOM[x] output when the internal HDLC receiver is used with DMA. When RXDMAGAT is set to logic 1, the RDLINT[x] DMA output is gated with the RDLEOM[x] output so that RDLINT[x] is forced to logic 0 when RDLEOM[x] is logic 1. When RXDMAGAT is set to logic 0, the RDLINT[x] and RDLEOM[x] outputs operate independently.

BRX2RAIL:

The BRX2RAIL bit selects whether the backplane receive data signal on the multifunction outputs BRPCM/BRDP[x] and BRSIG/BRDN[x] are in either dual

rail or single rail format. When BRX2RAIL is set to logic 1, the multifunction pins become the BRDP[x] and BRDN[x] dual rail outputs, which contain the received positive and negative line pulses timed to the 2.048MHz receive line rate, RCLKO[x]. When BRX2RAIL is set to logic 0, the multifunction pins become the BRPCM[x] and BRSIG[x] digital outputs.
OOSMFAIS:

This bit controls the receive backplane signaling trunk conditioning in an out of signaling multiframe condition. If OOSMFAIS is set to a logic 0, an OOSMF indication from the FRMR does not affect the BRSIG[x] outputs. When OOSMFAIS is a logic 1, an OOSMF indication from the FRMR will cause the BRSIG[x] outputs to be set to all 1's.

ROHM, BRXSMFP, BRXCMFP:

The ROHM, BRXSMFP and BRXCMFP bits select the output signal seen on the backplane output BRFPO[x]. The following table summarizes the configurations:

ROHM	BRXSMFP	BRXCMFP	Result
0	0	0	Backplane receive frame pulse output: BRFPO[x] pulses high for 1 BRCLK cycle (or 1 RCLKO[x] cycle if ELST is by-passed) during bit 1 of each 256-bit frame, indicating the frame alignment of the BRPCM[x] data stream.
0	0	1	Backplane receive CRC multiframe output: BRFPO[x] pulses high for 1 BRCLK cycle (or 1 RCLKO[x] cycle if ELST is by-passed or RCLKOSEL is set to logic 1) during bit 1 of frame 1 of every 16 frame CRC multiframe, indicating the CRC multiframe alignment of the BRPCM[x] data stream. (Even when CRC multiframing is disabled, the BRFPO[x] output continues to indicate the position of bit 1 of the FAS frame every 16th frame).

ROHM	BRXSMFP	BRXCMFP	Result
0	1	0	Backplane receive signaling multiframe output: BRFPO[x] pulses high for 1 BRCLK cycle (or 1 RCLKO[x] cycle if ELST is by-passed or RCLKOSEL is set to logic 1) during bit 1 of frame 1 of the 16 frame signaling multiframe, indicating the signaling multiframe alignment of the BRPCM[x] data stream. (Even when signaling multiframing is disabled, the BRFPO[x] output continues to indicate the position of bit 1 of every 16th frame.)
0	1	1	Backplane receive composite multiframe output: BRFPO[x] goes high on the falling BRCLK edge (or RCLKO[x] edge if ELST is by-passed or RCLKOSEL is set to logic 1) marking the beginning of bit 1 of frame 1 of every 16 frame signaling multiframe, indicating the signaling multiframe alignment of the BRPCM[x] data stream, and returns low on the falling BRCLK edge (or RCLKO[x] edge if ELST is by-passed or RCLKOSEL is set to logic 1) marking the end of bit 1 of frame 1 of every 16 frame CRC multiframe, indicating the CRC multiframe alignment of the BRPCM[x] data stream. This mode allows both multiframe alignments to be decoded externally from the single BRFPO[x] signal. Note that if the signaling and CRC multiframe alignments are coincident, BRFPO[x] will pulse high for 1 BRCLK cycle (or RCLKO[x] cycle if ELST is by-passed or RCLKOSEL is set to logic 1) every 16 frames.
1	X	X	Backplane receive overhead output: BRFPO[x] is high for timeslot 0 and timeslot 16 of each 256-bit frame, indicating the overhead of the BRPCM[x] data stream.

Upon reset of the EQUAD, these bits are cleared to zero.

Register 002H, 082H, 102H, 182H: Datalink Options

Bit	Type	Function	Default
Bit 7	R/W	RXDMASIG	0
Bit 6	R/W	RFRACE1	0
Bit 5	R/W	TXDMASIG	0
Bit 4	R/W	TFRACE1	0
Bit 3	R/W	RDLINTE	0
Bit 2	R/W	RDLEOME	0
Bit 1	R/W	TDLINTE	0
Bit 0	R/W	TDLUDRE	0

This register allows software to configure the datalink options.

RXDMASIG:

The RXDMASIG bit selects the internal HDLC receiver (RFDL) data-received interrupt (INT) and end-of-message (EOM) signals to be output on the RDLINT[x] and RDLEOM[x] pins. When RXDMASIG is set to logic 1, the RDLINT[x] and RDLEOM[x] output pins can be used by a DMA controller to process the datalink. When RXDMASIG is set to logic 0, the RFDL INT and EOM signals are no longer available to a DMA controller; the signals on RDLINT[x] and RDLEOM[x] become the extracted datalink data and clock, RDLSIG[x] and RDLCLK[x]. In this mode, the data stream available on the RDLSIG[x] output corresponds to the extracted datalink from Time Slot 16 or the Time Slot 0 National Use bits depending on the state of the RXSAxEN bits of the Receive TS0 Data Link Enable register. The RFRACE1 bit takes precedent over RXDMASIG.

RFRACE1:

The RFRACE1 bit selects whether a fractional E1 is extracted and made available on the RDLSIG[x] output, or whether the RDLINT/RDLSIG[x] and RDLEOM/RDLCLK[x] pins operate as defined by the RXDMASIG bit. When RFRACE1 is set to logic 1, the contents of the Channel Select registers determine which channels are output on RDLSIG[x] with an aligned burst clock output on RDLCLK[x]. When RFRACE1 is set to logic 0, the RDLINT/RDLSIG[x] and RDLEOM/RDLCLK[x] pins contain the signals selected by the RXDMASIG bit.

TXDMASIG:

The TXDMASIG bit selects the internal HDLC transmitter (XFDL) request for service interrupt (INT) and data underrun (UDR) signals to be output on the TDLINT[x] and TDLUDR[x] pins. When TXDMASIG is set to logic 1, the TDLINT[x] and TDLUDR[x] output pins can be used by a DMA controller to service the datalink. When TXDMASIG is set to logic 0, the XFDL INT and UDR signals are no longer available to a DMA controller; the signals on TDLINT[x] and TDLUDR[x] become the serial datalink data input and clock, TDLSIG[x] and TDLCLK[x]. In this mode an external controller is responsible for formatting the data stream presented on the TDLSIG[x] input to correspond to the datalink in Time Slot 16 or the Time Slot 0 National Use bits. If the TRAN block Configuration DLEN bit is logic 1 and the TRAN block Configuration SIGEN bit is a logic 0, the TDLSIG data stream is inserted into Time Slot 16 and the TDLCLK[x] pin is a 50% duty cycle 64 kHz clock; otherwise, the TDLSIG[x] data stream is inserted into the Time Slot 0 National Use positions enabled by the TXSAxEN bits. The TFRACE1 bit takes precedent over TXDMASIG

In the default case TDLCLK[x] is a bursted 4 kHz clock and TDLSIG[x] is inserted into the TS0 Sa4 bit.

TFRACE1:

The TFRACE1 bit selects whether a fractional E1 is inserted into a subset of the channels of each frame via the TDLSIG[x] input, or whether the TDLINT/TDLSIG[x] and TDLUDR/TDLCLK[x] pins operate as defined by the TXDMASIG bit. When TFRACE1 is set to logic 1, the channel data is expected on TDLSIG[x], sampled on the rising edge of a burst clock provided on TDLCLK[x]. The channels inserted are determined by the Channel Select registers; all others are inserted through BTPCM[x]. When TFRACE1 is set to logic 0, the TDLINT/TDLSIG[x] and TDLUDR/TDLCLK[x] pins contain the signals selected by the TXDMASIG bit.

RDLINTE:

The RDLINTE bit enables the RFDL received-data interrupt to also generate an interrupt on the microprocessor interrupt, INTB. This allows a single microprocessor to service the RFDL without needing to interface to the DMA control signals. When RDLINTE is set to logic 1, an event causing an interrupt in the RFDL (which is visible on the RDLINT output pin when RXDMASIG is logic 1) also causes an interrupt to be generated on the INTB output. When RDLINTE is set to logic 0, an interrupt event in the RFDL does not cause an interrupt on INTB.

RDLEOME:

The RDLEOME bit enables the RFDL end-of-message interrupt to also generate an interrupt on the microprocessor interrupt, INTB. This allows a single microprocessor to service the RFDL without needing to interface to the DMA control signals. When RDLEOME is set to logic 1, an end-of-message event causing an EOM interrupt in the RFDL (which is visible on the RDLEOM output pin when RXDMASIG is logic 1) also causes an interrupt to be generated on the INTB output. When RDLEOME is set to logic 0, an EOM interrupt event in the RFDL does not cause an interrupt on INTB. NOTE: within the RFDL, an end-of-message event causes an interrupt on both the EOM and INT RFDL interrupt outputs. See the Operation section for further details on using the RFDL.

TDLINTE:

The TDLINTE bit enables the XFDL request for service interrupt to also generate an interrupt on the microprocessor interrupt, INTB. This allows a single microprocessor to service the XFDL without needing to interface to the DMA control signals. When TDLINTE is set to logic 1, an request for service interrupt event in the XFDL (which is visible on the TDLINT output pin when TXDMASIG is logic 1) also causes and interrupt to be generated on the INTB output. When TDLINTE is set to logic 0, an interrupt event in the XFDL does not cause an interrupt on INTB.

TDLUDRE:

The TDLUDRE bit enables the XFDL transmit data underrun interrupt to also generate an interrupt on the microprocessor interrupt, INTB. This allows a single microprocessor to service the XFDL without needing to interface to the DMA control signals. When TDLUDRE is set to logic 1, an underrun event causing an interrupt in the XFDL (which is visible on the TDLUDR output pin when TXDMASIG is logic 1) also causes and interrupt to be generated on the INTB output. When TDLUDRE is set to logic 0, an underrun event in the XFDL does not cause an interrupt on INTB.

Upon reset of the EQUAD, these bits are cleared to zero.

Register 003H, 083H, 103H, 183H: Receive Interface Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	BPV	0
Bit 4	R/W	RDNINV	0
Bit 3	R/W	RDPINV	0
Bit 2	R/W	RUNI	0
Bit 1	R/W	RFALL	0
Bit 0		Unused	X

This register enables the Receive Interface to handle the various input waveform formats.

BPV:

The BPV bit enables only bipolar violations to indicate line code violations and be accumulated in the PMON LCV Count Registers. When BPV is set to logic 1, BPVs (which are not part of a valid HDB3 signature if HDB3 line coding is used) generate an LCV indication and increment the PMON LCV counter. When BPV is set to logic 0, both BPVs (which are not part of a valid HDB3 signature if HDB3 line coding is used) and excessive zeros generate an LCV indication and increment the PMON LCV counter. Excessive zeros is a sequence of zeros greater than 3 bits long for both AMI and HDB3 encoded signals.

RDPINV,RDNINV:

The RDPINV and RDNINV bits enable the Receive Interface to logically invert the signals received on multifunction pins RDP/RDD[x] and RDN/RLCV[x], respectively. When RDPINV is set to logic 1, the interface inverts the signal on the RDP/RDD[x] input. When RDPINV is set to logic 0, the interface passes the RDP/RDD[x] signal unaltered. When RDNINV is set to logic 1, the interface inverts the signal on the RDN/RLCV[x] input. When RDNINV is set to logic 0, the interface passes the RDN/RLCV[x] signal unaltered.

RUNI:

The RUNI bit enables the interface to receive unipolar digital data and line code violation indications on the multifunction pins RDP/RDD[x] and RDN/RLCV[x]. When RUNI is set to logic 1, the RDP/RDD[x] and RDN/RLCV[x] multifunction pins become the data and line code violation inputs, RDD[x] and RLCV[x], sampled on the selected RCLKI[x] edge. When RUNI is set to logic 0, the RDP/RDD[x] and RDN/RLCV[x] multifunction pins become the positive and negative pulse inputs, RDP[x] and RDN[x], sampled on the selected RCLKI[x] edge.

RFALL:

The RFALL bit enables the Receive Interface to sample the multifunction pins on the falling RCLKI[x] edge. When RFALL is set to logic 1, the interface is enabled to sample either the RDD[x] and RLCV[x] inputs, or the RDP[x] and RDN[x] inputs, on the falling RCLKI[x] edge. When RFALL is set to logic 0, the interface is enabled to sample the inputs on the rising RCLKI[x] edge.

Register 004H, 084H, 104H, 184H: Transmit Interface Configuration

Bit	Type	Function	Default
Bit 7	R/W	FIFOBYP	0
Bit 6	R/W	TAISEN	0
Bit 5	R/W	TDNINV	0
Bit 4	R/W	TDPINV	0
Bit 3	R/W	TUNI	0
Bit 2	R/W	FIFOFULL	0
Bit 1	R/W	TRISE	0
Bit 0	R/W	TRZ	0

This register enables the Transmit Interface to generate the required digital output waveform format.

FIFOBYP:

The FIFOBYP bit enables the transmit bipolar input signals to DJAT to be bypassed around the FIFO to the bipolar outputs. When jitter attenuation is not being used the DJAT FIFO can be bypassed to reduce the delay through the transmitter section by typically 24 bits. When FIFOBYP is set to logic 1, the bipolar inputs to DJAT are routed around the FIFO and directly to the bipolar outputs. When FIFOBYP is set to logic 0, the bipolar transmit data passes through the DJAT FIFO.

Note that when FIFOBYP is set to a logic 1, the OCLKSEL1 bit in the Transmit Timing Options register must also be set to logic 1.

TAISEN:

The TAISEN bit enables the interface to generate an unframed all-ones AIS alarm on the TDP/TDD[x] and TDN[x] multifunction pins. When TAISEN is set to logic 1 and TUNI is set to logic 0, the bipolar TDP[x] and TDN[x] outputs are forced to pulse alternately, creating an all-ones signal; when TAISEN and TUNI are both set to logic 1, the unipolar TDD[x] output is forced to all-ones. When TAISEN is set to logic 0, the TDP/TDD[x] and TDN[x] multifunction outputs operate normally. The transition to transmitting AIS on the TDP[x] and TDN[x] outputs is done in such a way as to not introduce any bipolar violations.

TDPINV,TDNINV:

The TDPINV and TDNINV bits enable the E1 Transmit Interface to logically invert the signals output on the TDP/TDD[x] and TDN/TFLG [x] multifunction pins, respectively. When TDPINV is set to logic 1, the TDP/TDD[x] output is inverted. When TDPINV is set to logic 0, the TDP/TDD[x] output is not inverted. When TDNINV is set to logic 1, the TDN/TFLG[x] output is inverted. When TDNINV is set to logic 0, the TDN/TFLG[x] output is not inverted.

TUNI:

The TUNI bit enables the transmit interface to generate unipolar digital outputs on the TDP/TDD[x] and TDN/TFLG[x] multifunction pins. When TUNI is set to logic 1, the TDP/TDD[x] and TDN/TFLG[x] multifunction pins become the unipolar outputs TDD[x] and TFLG[x], updated on the selected TCLKO[x] edge. When TUNI is set to logic 0, the TDP/TDD[x] and TDN/TFLG[x] multifunction pins become the bipolar outputs TDP[x] and TDN[x], also updated on the selected TCLKO[x] edge.

FIFOFULL:

The FIFOFULL bit determines the indication given on the TFLG[x] output pin. When FIFOFULL is set to logic 1, the TFLG[x] output indicates when the Digital Jitter Attenuator's FIFO is within 4 bit positions of becoming full. When FIFOFULL is set to logic 0, the TFLG[x] output indicates when the Digital Jitter Attenuator's FIFO is within 4 bit positions of becoming empty.

TRISE:

The TRISE bit configures the interface to update the multifunction outputs on the rising edge of TCLKO[x]. When TRISE is set to logic 1, the interface is enabled to update the TDP/TDD[x] and TDN/TFLG[x] output pins on the rising TCLKO[x] edge. When TRISE is set to logic 0, the interface is enabled to update the outputs on the falling TCLKO[x] edge.

TRZ:

The TRZ bit configures the interface to transmit bipolar return-to-zero formatted waveforms. When TRZ is set to logic 1, the interface is enabled to generate the TDP[x] and TDN[x] output signals as RZ waveforms with duration equal to half the TCLKO[x] period. When TRZ is set to logic 0, the interface is enabled to generate the TDP[x] and TDN[x] output signals as NRZ waveforms with duration equal to the TCLKO[x] period, updated on the selected edge of TCLKO[x]. The TRZ bit can only be used when TUNI and TRISE are set to logic 0.

When the system is reset, the contents of the register are set to logic 0, enabling the Transmit Interface to output NRZ formatted positive and negative pulse data on the TDP[x] and TDN[x] outputs, updated on the falling TCLKO[x] edge.

Register 005H, 085H, 105H, 185H: Transmit Backplane Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	BTFPREF	0
Bit 4		Unused	X
Bit 3	R/W	BTXCLK	0
Bit 2		Unused	X
Bit 1	R/W	BTX2RAIL	0
Bit 0	R/W	BTXMFP	0

This register allows software to configure the Transmit backplane interface format.

BTFPREF:

The BTFPREF bit selects the source of the input frame pulse. When BTFPREF is set to logic 1, BTFP[1] is used as the input transmit frame pulse for the associated interface. If BTFPREF is set to logic 0, BTFP[4:1] are used as the input transmit frame pulses for the associated interface. Note that when BTFPREF is set to a logic 1, the corresponding BTCLK[x] must be phase aligned to BTCLK[1] to ensure proper sampling of BTFP[1].

The BTFPREF bit in register 005H has no effect if MENB is a logic 0. In this case, MTFP is used to generate internal frame pulses for each quadrant.

BTXCLK:

The BTXCLK bit selects the source of the TRAN transmit clock input signal. When BTXCLK is set to logic 1, the TRAN transmit clock is driven with the 2.048MHz recovered PCM output clock (RCLKO[x]) from the receiver section. When BTXCLK is set to logic 0, the TRAN transmit clock is driven with the 2.048MHz backplane transmit clock (BTCLK[x]).

BTX2RAIL:

The BTX2RAIL bit selects whether the backplane transmit data signal presented to the transmitter on the multifunction inputs BTPCM/BTDP[x] and BTSIG/BTDN[x] are in either dual-rail or single-rail format. When BTX2RAIL is set to logic 1, the multifunction pins become the BTDP[x] and BTDN[x]

dual-rail inputs, which bypass the TRAN and input directly into the jitter attenuator. It is expected that the framing bits be already inserted into the dual-rail streams before they are input on BTDP[x] and BTDN[x]. When BTX2RAIL is set to logic 0, the multifunction pins become the BTPCM[x] and BTSIG[x] digital inputs.

BTXMFP:

The BTXMFP bit selects the type of backplane frame alignment signal presented to the transmitter BTFP[x] input. When BTXMFP is set to logic 1, BTFP[x] must be brought high to mark bit 1 of frame 1 of every 16 frame signaling multiframe and brought low following bit 1 of frame 1 of every 16 frame CRC multiframe. This mode allows both multiframe alignments to be independently controlled using the single BTFP[x] signal. Note that if the signaling and CRC multiframe alignments are coincident, BTFP[x] must pulse high for 1 BTCLK[x] cycle at a multiple of 16 frames. When BTXMFP is set to logic 0, a rising edge on the BTFP[x] indicates the first bit in each frame.

When the multiplexed transmit backplane is selected (MENB is low), the BTXMFP bit must be set to the same value in all four quadrants of the EQUAD. The MTFP pin is used in a similar way as BTFP[x] but is only sampled on the clock cycles corresponding to the first multiplexed PCM stream (destined for transmitter number one). MTFP must be brought high to mark bit 1 of frame 1 of the first multiplexed PCM stream (destined for transmitter number one) of every 16 frame signaling multiframe and brought low following bit 1 of frame 1 of the first multiplexed PCM stream of every 16 frame CRC multiframe. All four interfaces will have the same frame alignment.

Upon reset of the EQUAD, these bits are cleared to zero.

Register 006H, 086H, 106H, 186H: Transmit Framing Options

Bit	Type	Function	Default
Bit 7	R/W	PATHCRC	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	TXSA4EN	1
Bit 3	R/W	TXSA5EN	0
Bit 2	R/W	TXSA6EN	0
Bit 1	R/W	TXSA7EN	0
Bit 0	R/W	TXSA8EN	0

PATHCRC:

The PATHCRC bit allows upstream block errors to be preserved in the transmit CRC bits. If PATHCRC is a logic 1, the CRC-4 bits are modified to reflect any bit values in BTPCM[x] which have changed prior to transmission. When PATHCRC is set to logic 0, the TRAN block is allowed to generate a new CRC-4 value which overwrites the incoming CRC-4 word. For the PATHCRC bit to be effective, the BTXMFP bit of the Transmit Backplane Options register must be a logic 1; otherwise, the identification of the incoming CRC-4 bits would be impossible. The PATHCRC bit only takes effect if the GENCRC bit of the TRAN Configuration register (44H) is a logic 1 and either the INDIS or FDIS bit in the same register are set to logic1.

TXSA4EN, TXSA5EN, TXSA6EN, TXSA7EN and TXSA8EN:

The TXSAxEN bits control the insertion of a data link into the Time Slot 0 National Use bits (Sa4 through Sa8).

These bits only have effect if the TRAN block Configuration DLEN bit is logic 0 or if the TRAN block Configuration SIGEN bit is logic 1. The TXSAxEN bits take priority over the INDIS and FDIS bits of the TRAN block Configuration register. The data link bits are still inserted if either INDIS or FDIS is logic 1.

If the TXDMASIG bit is a logic 1, the data link bits are sourced by the internal HDLC transmitter; otherwise, the bits are sourced from the TDLSIG[x] pin. If the TXSA4EN bit is logic 1, the TDLSIG[x] value is written into bit 4 of Time Slot 0 of non-frame alignment signal frames. If the TXSA8EN bit is logic 1, the TDLSIG[x] value is written into bit 8 of Time Slot 0 of non-frame alignment

signal frames. The other enable bits operate in an analogous fashion. A clock pulse is generated on TDLCLK[x] for each enable that is logic 1. Any combination of enable bits is allowed, resulting in a data rate between 4 kbit/s and 20 kbit/s. Clearing all enable bits disables TS0 insertion. Any National Use bits which are not included in the data link are sourced from either BTPCM[x] or the TRAN block International/National Control register.

Upon reset of the EQUAD, all bits are logic 0 except TXSA4EN. By default, a 4 kbit/s data link is inserted into Sa4 from the TDLSIG[x] input.

Register 007H, 087H, 107H, 187H: Transmit Timing Options

Bit	Type	Function	Default
Bit 7	R/W	HSBPSEL	0
Bit 6	R/W	XCLKSEL	0
Bit 5	R/W	OCLKSEL1	0
Bit 4	R/W	OCLKSEL0	0
Bit 3	R/W	PLLREF1	0
Bit 2	R/W	PLLREF0	0
Bit 1	R/W	TCLKISEL	0
Bit 0	R/W	SMCLKO	0

This register allows software to configure the options of the transmit timing section.

HSBPSEL:

The HSBPSEL bit selects the source of the high-speed clock used in the ELST, SIGX and TPSC blocks. This allows the EQUAD to interface to higher rate backplanes (>2.048MHz) that are externally gapped; however, the instantaneous backplane clock frequency must not exceed 3.0MHz. When HSBPSEL is set to logic 1, the XCLK input signal is divided by 2 and used as the high-speed clock to these blocks. XCLK must be driven with 49.152MHz. When HSBPSEL is set to logic 0, the block high-speed clock is driven with the internal 16.384MHz clock source selected by the XCLKSEL bit.

XCLKSEL:

The XCLKSEL bit selects the source of the high-speed clock used in the CDRC, FRMR, and PMON blocks. When XCLKSEL is set to logic 1, the XCLK input signal is used as the high-speed clock to these blocks. XCLK must be driven with 16.384MHz. When XCLKSEL is set to logic 0, the block high-speed clock is driven with XCLK divided by 3. XCLK must be driven with 49.152MHz.

OCLKSEL1, OCLKSEL0:

The OCLKSEL[1:0] bits select the source of the Digital Jitter Attenuator FIFO output clock signal. When OCLKSEL1 is set to logic 1, the DJAT FIFO output clock is driven with the input data clock driving the DJAT ICLK input. In this

mode the jitter attenuation is disabled and the input clock must be jitter-free. When OCLKSEL1 is set to logic 0, the DJAT FIFO output clock is driven with either the TCLKI[x] input clock or an internal smooth 2.048MHz clock, as selected by the OCLKSEL0 bit. When OCLKSEL0 is set to logic 1, the DJAT FIFO output clock is driven with the TCLKI[x] input clock. When OCLKSEL0 is set to logic 0, the DJAT FIFO output clock is driven with the internal smooth 2.048 MHz clock selected by the TCLKISEL and SMCLKO bits.

In the case where the FIFOBYP bit in the Transmit Interface Configuration register is set to a logic 1, the OCLKSEL1 but must be set to a logic 1.

PLLREF1, PLLREF0:

The PLLREF[1:0] bits select the source of the Digital Jitter Attenuator phase locked loop reference signal as follows:

PLLREF1	PLLREF0	Source of PLL Reference
0	0	Transmit clock used by TRAN (either the 2.048MHz BTCLK[x] or the 2.048MHz RCLKO[x], as selected by the BTXCLK register bit)
0	1	BTCLK[x] input
1	0	RCLKO[x] output
1	1	TCLKI[x] input

TCLKISEL,SMCLKO:

The TCLKISEL and SMCLKO bits select the source of the internal smooth 2.048MHz and 16.384MHz output clock signals. When TCLKISEL and SMCLKO are set to logic 0, the internal 2.048MHz clock signal is driven by the smooth 2.048MHz clock source generated by DJAT. When TCLKISEL is set to logic 0 and SMCLKO is set to logic 1, the internal 2.048MHz clock signal is driven by the TCLKI[x] input signal divided by 8, and the internal 16.384MHz clock signal is driven by the TCLKI[x] input signal. When TCLKISEL and SMCLKO are set to logic 1, the internal 2.048MHz clock signal is driven by the XCLK input signal divided by 8, and the internal 16.384MHz clock signal is driven by the XCLK input signal. The combination of TCLKISEL set to logic 1 and SMCLKO set to logic 0 should not be used.

The following table illustrates the required bit settings for these various clock sources to affect the transmitted data:

Table 2 -

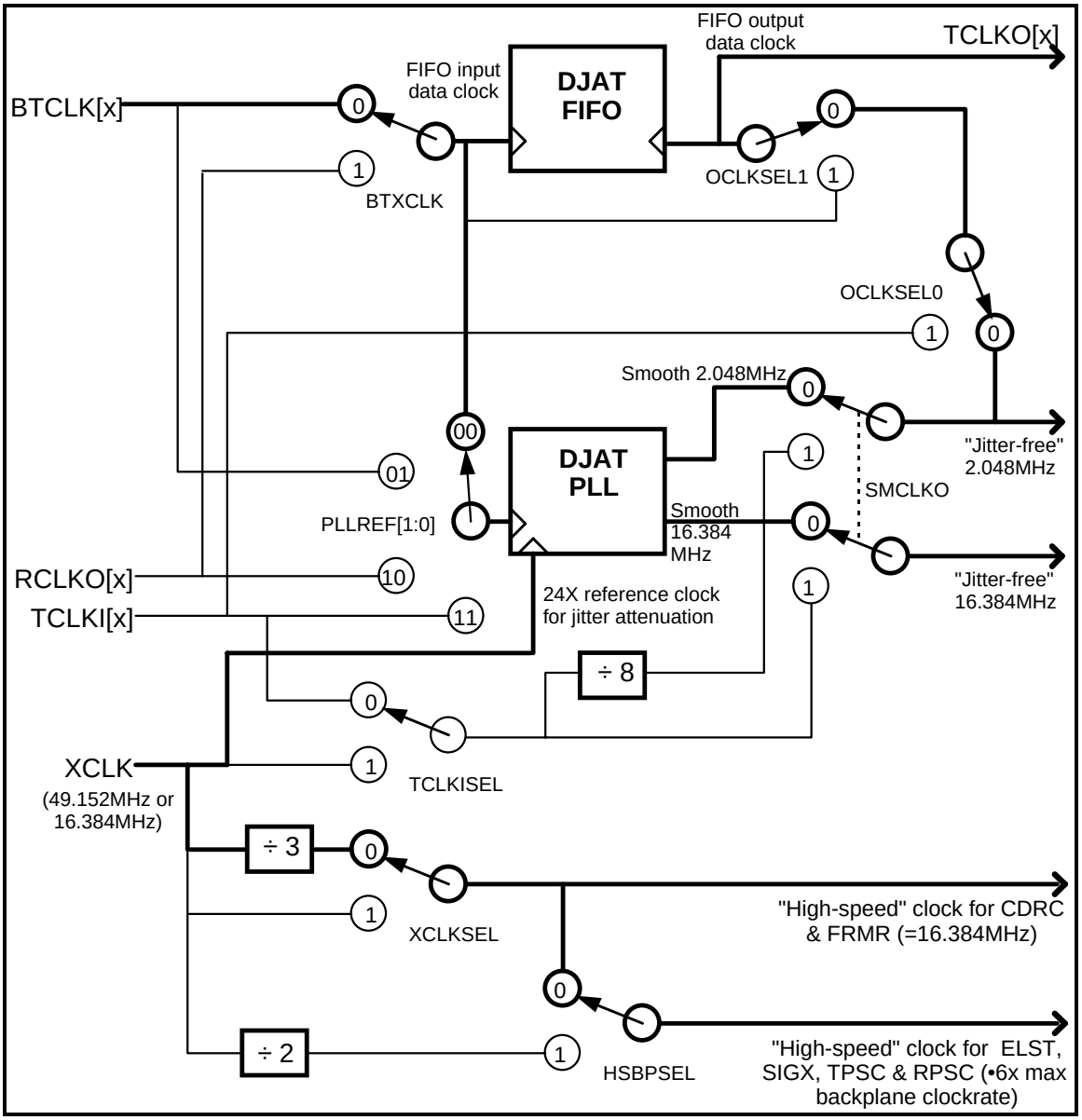
Input Transmit Data	Bit Settings	XCLK Freq	Effect on Output Transmit Data
Backplane transmit data timed to 2.048 MHz BTCLK[x].	HSBPSEL =0 XCLKSEL =0 OCLKSEL1 =0 OCLKSEL0 =0 PLLREF1 =0 PLLREF0 =X TCLKISEL =0 SMCLKO =0 PLLREF1 =1 PLLREF0 =0 PLLREF1 =1 PLLREF0 =1	49.152MHz	Jitter attenuated. TCLKO[x] is a smooth 2.048 MHz. TCLKO[x] referenced to BTCLK[x]. TCLKO[x] referenced to RCLKO[x]. TCLKO[x] referenced to TCLKI[x].
Backplane transmit data timed to >2.048MHz backplane clock. BTCLK[x] is externally "gapped".	HSBPSEL =1 XCLKSEL =0 OCLKSEL1 =0 OCLKSEL0 =0 PLLREF1 =0 PLLREF0 =X TCLKISEL =0 SMCLKO =0 PLLREF1 =1 PLLREF0 =0 PLLREF1 =1 PLLREF0 =1	49.152MHz	Jitter attenuated. TCLKO[x] is a smooth 2.048MHz. TCLKO[x] referenced to externally "gapped" transmit clock. TCLKO[x] referenced to RCLKO. TCLKO[x] referenced to TCLKI.
Backplane transmit data timed to BTCLK[x].	HSBPSEL =0 XCLKSEL =0 OCLKSEL1 =1 OCLKSEL0 =X PLLREF1 =X PLLREF0 =X TCLKISEL =0 SMCLKO =0 XCLKSEL =1 TCLKISEL =1 SMCLKO =1 DJAT SYNC =0	49.152MHz 16.384MHz	No jitter attenuation. TCLKO[x] is equal to internal transmit clock, either BTCLK[x], gapped BTCLK[x], or RCLKO[x]. Same as above.

Input Transmit Data	Bit Settings	XCLK Freq	Effect on Output Transmit Data
Backplane transmit data timed to BTCLK[x].	HSBPSEL =0 XCLKSEL =0 OCLKSEL1 =0 OCLKSEL0 =1 PLLREF1 =X PLLREF0 =X TCLKISEL =0 SMCLKO =0 XCLKSEL =1 TCLKISEL =1 SMCLKO =1	49.152MHz 16.384MHz	No jitter attenuation. TCLKO[x] is equal to TCLKI[x] (useful for higher rate MUX applications). Same as above.
Backplane transmit data timed to BTCLK[x].	HSBPSEL =0 XCLKSEL =0 OCLKSEL1 =0 OCLKSEL0 =0 PLLREF1 =X PLLREF0 =X TCLKISEL =0 SMCLKO =1 XCLKSEL =1	49.152MHz 16.384MHz	TCLKI[x] is a jitter-free 16.384MHz clock. TCLKO[x] is equal to TCLKI[x]÷8.[1] Same as above.
Backplane transmit data timed to BTCLK[x].	HSBPSEL =0 XCLKSEL =1 OCLKSEL1 =0 OCLKSEL0 =0 PLLREF1 =X PLLREF0 =X TCLKISEL =1 SMCLKO =1	jitter-free 16.384MHz	XCLK is a jitter-free 16.384MHz clock. TCLKO[x] is equal to XCLK÷8.[1]

1. The register bits SYNC, CENT, and LIMIT in the DJAT Configuration Register must be set to logic 0 in these configurations.

Upon reset of the EQUAD, these bits are cleared to zero, selecting digital jitter attenuation with TCLKO[x] referenced to the backplane transmit clock, BTCLK[x]. Figure 8 illustrates the various bit setting options, with the reset condition highlighted.

Figure 8 - Transmit Timing Options



This diagram illustrates clock configurations for when the RCLKOSEL bit is set to logic 0. See the Operations - Receiver Jitter Attenuation section for DJAT clock configurations when RCLKOSEL is set to logic 1.

The DJAT requires a 49.152MHz clock; if a 16.384MHz clock is used for XCLK, then the DJAT will not function and should be bypassed.

Register 008H, 088H, 108H, 188H: Interrupt Source

Bit	Type	Function	Default
Bit 7	R	DJAT	0
Bit 6	R	PARITY	0
Bit 5	R	FRMR/SA	0
Bit 4	R	PMON	0
Bit 3	R	ELST	0
Bit 2	R	RFDL	0
Bit 1	R	XFDL	0
Bit 0	R	CDRC	0

This register allows software to determine the block which produced the interrupt on the INTB output pin. The FRMR/SA bit is a logic 1 if either the FRMR or the SACI bit (register 009H, Receive TS0 Data Link Enable register) is the source of the interrupt.

Reading this register does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

Register 009H, 089H, 109H, 189H: Receive TS0 Data Link Enables

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	SACE	0
Bit 5	R	SACI	0
Bit 4	R/W	RXSA4EN	1
Bit 3	R/W	RXSA5EN	0
Bit 2	R/W	RXSA6EN	0
Bit 1	R/W	RXSA7EN	0
Bit 0	R/W	RXSA8EN	0

SACE:

The SACE bit enables the generation of an interrupt whenever there is a change in the National bits that are not extracted to form a data link. Changes in the National bits are not debounced, i.e. the interrupt is generated immediately when the current value of the National bits differs from the previous value. The value of the National bits can be read in the FRMR International/National Bits Register.

SACI:

The SACI bit is set to logic one whenever there is a change in the National bits that are not extracted to form a data link. The SACI bit is cleared following a read of this register.

RXSA4EN, RXSA5EN, RXSA6EN, RXSA7EN and RXSA8EN:

The RXSAxEN bits control the extraction of a data link from the received Time Slot 0 National Use bits (Sa4 through Sa8).

If RXDMASIG bit is set to logic one, the data link bits are terminated by the internal HDLC receiver. If RXDMASIG is set to logic 0, the data link is presented on RDLSIG[x]. If the RXSA4EN is logic 1, the RDLSIG[x] value is extracted from bit 4 of Time Slot 0 of non-frame alignment signal frames. If the RXSA8EN is logic 1, the RDLSIG[x] value is extracted from bit 8 of Time Slot 0 of non-frame alignment signal frames. The other enable bits operate in an analogous fashion. A clock pulse is generated on RDLCLK[x] for each enable

that is logic 1. Any combination enable bits is allowed resulting in a data rate between 4 kbit/s and 20 kbit/s.

If all RXSAxEN (where x is the values 4 to 8 inclusive) bits are set to logic 0, Timeslot 16 is extracted and treated as a data link. If RXDMASIG is set to logic 0, Timeslot16 is made available on the RDLSIG[x] output and RDLCLK[x] is an associated 64 kHz clock. If RXDMASIG is logic 1, the data link is terminated by the HDLC receiver and the RDLINT/RDLSIG[x] and RDLEOM/RDLCLK[x] pins operate as a data link interrupt (RDLINT[x]) and a end-of-message (RDLEOM[x]) indication.

Note that the RFRACE1 bit will force fractional E1 channel outputs on RDLINT/RDLSIG[x] and RDLEOM/RDLCLK[x] if it is set to logic 1 as it has the highest priority over the control of these outputs.

Upon reset of the EQUAD, all bits are logic 0 except RXSA4EN. By default, a 4 kbit/s data link is extracted from Sa4 and presented on the RDLSIG output.

Register 00AH, 08AH, 10AH, 18AH: Master Diagnostics

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	PAYLB	0
Bit 4	R/W	LINELB	0
Bit 3		Unused	X
Bit 2	R/W	DDLB	0
Bit 1		Unused	X
Bit 0	R/W	TXDIS	0

This register allows software to enable diagnostic modes.

PAYLB:

The PAYLB bit selects the payload loopback mode, where the received data output from the ELST is internally connected to the transmit data input of the TRAN. The data read out of ELST is timed to the transmitter clock, and the transmit frame alignment is used to synchronize the output frame alignment of ELST. During payload loopback, the data output on BRPCM[x] is forced to logic 1. When PAYLB is set to logic 1, the payload loopback mode is enabled. When PAYLB is set to logic 0, the loopback mode is disabled.

LINELB:

The LINELB bit selects the line loopback mode, where the recovered positive and negative pulse outputs from the CDRC block are internally connected to the digital inputs of the DJAT. When LINELB is set to logic 1, the line loopback mode is enabled. When LINELB is set to logic 0, the line loopback mode is disabled. Note that when line loopback is enabled, the Timing Options Register settings should be reviewed to ensure the options are such that data will pass error-free and "jitter"-free through DJAT (typically, the default setting, 00H, for register 7 will be appropriate for line loopback).

DDLB:

The DDLB bit selects the diagnostic digital loopback mode, where the transmit side outputs from DJAT are internally connected to the receive side inputs. When DDLB is set to logic 1, the diagnostic digital loopback mode is

enabled. When DDLB is set to logic 0, the diagnostic digital loopback mode is disabled.

The diagnostic digital loopback mode will operate with CDRC clock recovery enabled or disabled and in unipolar or bipolar mode.

TXDIS:

The TXDIS bit provides a method of suppressing the output of the transmitter. When TXDIS is set to logic 1, the digital output of TRAN is disabled by forcing it to logic 0. When TXDIS is set to logic 0, the digital output of TRAN is not suppressed. Zeroing of the transmitter takes place before HDB3 encoding. In order to generate an all-zero's output, TXDIS and AMI encoding (in the E1 TRAN Configuration register) should be set.

Upon reset of the EQUAD, these register bits are cleared to zero.

Register 00BH, 20BH: EQUAD Master Test

Bit	Type	Function	Default
Bit 7	W	TST	X
Bit 6	R/W	A_TM[8]	X
Bit 5	R/W	A_TM[7]	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	0
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to select EQUAD test features. All bits, except for PMCTST and A_TM[8:7] are reset to zero by a hardware reset of the EQUAD; a software reset of the EQUAD does not affect the state of the bits in this register. Refer to the Test Features Description section for more information.

TST:

The TST bit performs a function similar to the PMCTST bit (see below), but does not select A_TM[8:7] internally.

A_TM[8]:

The state of the A_TM[8] bit internally replaces the input address line A[8] when PMCTST is set. This allows for more efficient use of the PMC manufacturing test vectors.

A_TM[7]:

The state of the A_TM[7] bit internally replaces the input address line A[7] when PMCTST is set. This allows for more efficient use of the PMC manufacturing test vectors.

PMCTST:

The PMCTST bit is used to configure the EQUAD for PMC's manufacturing tests. When PMCTST is set to logic 1, the EQUAD microprocessor port becomes the test access port used to run the PMC manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and is cleared by setting CSB to logic 1.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic 1, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the EQUAD to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit only has effect if either the IOTST or PMCTST bit is set. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each block in the EQUAD for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

HIZIO,HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the EQUAD . While the HIZIO bit is a logic 1, all output pins of the EQUAD except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

Register 00CH: EQUAD Revision/Chip ID/Global PMON Update

Bit	Type	Function	Default
Bit 7	R	TYPE[2]	0
Bit 6	R	TYPE[1]	0
Bit 5	R	TYPE[0]	1
Bit 4	R	ID[4]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	1

The version identification bits, ID[4:0], are set to a fixed value representing the version number of the EQUAD.

The chip identification bits, TYPE[2:0], is set to logic 1 representing the EQUAD.

Writing any value to this register causes all performance monitor counters to be updated simultaneously.

Register 00DH, 08DH, 10DH, 18DH: Framer Reset

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	RESET	0

RESET:

The RESET bit implements a software reset to the corresponding quadrant of the EQUAD. If the RESET bit is a logic 1, the individual framer is held in reset. This bit is not self-clearing; therefore, a logic 0 must be written to bring the framer out of reset. Holding the framer in a reset state effectively puts it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus deasserting the software reset.

Register 00EH, 08EH, 10EH, 18EH: Phase Status Word (LSB)

Bit	Type	Function	Default
Bit 7	R	PSB[7]	X
Bit 6	R	PSB[6]	X
Bit 5	R	PSB[5]	X
Bit 4	R	PSB[4]	X
Bit 3	R	PSB[3]	X
Bit 2	R	PSB[2]	X
Bit 1	R	PSB[1]	X
Bit 0	R	PSB[0]	X

This register contains the least significant byte, PSB[7:0], of the 9-bit phase status word. The 9-bit phase status word indicates the relative phase difference between the received E1 line timing (available on RCLKO[x]) and system timing. By utilizing the value of the phase status word, the system timing can be locked to the receive line timing via an external software controlled phase-locked-loop.

The least significant 8 bits contained in this register indicate a count value (0-255) of the number of system backplane clock cycles between successive 125µs frame pulses. The most significant 5 bits (PSB[7:3]) represent a time slot number (0-31) and the least significant 3 bits (PSB[2:0]) represent the bit number within the timeslot (0-7). The count value corresponds to the location within the system frame where the receive line-timed frame pulse occurred. If the received line clock frequency is higher on average than the system clock frequency, the phase status word value will be seen to decrease during successive register reads. If the received line clock frequency is lower on average than the system clock frequency, the phase status word value will be seen to increase during successive register reads.

The 9th bit of the Phase Status Word indicates the "frame count" and will toggle when two successive 8-bit counter values straddle a frame boundary. The PSB[8] bit will toggle when the bit and timeslot count indicated by PSB[7:0] exceeds timeslot 31, bit 7 or the count goes below timeslot 0, bit 0. This is determined by comparing the PSB[7:6] bits of the current phase status word value to those of the previous word value; PSB[8] is toggled only under the following conditions (all other bit value transitions leave PSB[8] unchanged):

Table 3 -

Previous PSB[7:6]	Current PSB[7:6]	Effect on PSB[8]
00	11	toggle
11	00	toggle

The contents of the Phase Status Word registers (address 00EH and 00FH for framer number 1) are internally updated on each receive line data frame pulse; a write to either register address (00EH or 00FH for framer number 1) must be performed to freeze the contents before this register and the Phase Status Word (MSB) register can be read. The correct sequence for reading the contents of the Phase Status Word of framer number 1 are:

1. Write to register address 00EH or 00FH

2. Read register address 00FH (read Phase Status Word MSB)

3. Read register address 00EH (read Phase Status Word LSB)

This write-before-read is analogous to the latching of performance monitor counter values in PMON, and is required to ensure that the phase status word value remains valid during the µP read. It is important to read the MSB register before the LSB register because, once the Phase Status Word (LSB) register has been read, the phase status word counter is unfrozen and the contents may change immediately.

Register 00FH, 08FH, 10FH, 18FH: Phase Status Word (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	PSB[8]	X

This register contains the most significant bit of the 9-bit phase status word.

The PSB[8] bit toggles when the bit and timeslot count (from the Phase Status Word LSB register) exceeds time slot 31, bit 7 or goes below time slot 0, bit 0.

The contents of the Phase Status Word registers are internally updated on each receive line data frame pulse; a write to either Phase Status Word register address must be performed to freeze the contents before this register and the Phase Status Word (MSB) register can be read. The correct sequence for reading the contents of the Phase Status Word are:

1. Write to either Phase Status Word register
2. Read Phase Status Word MSB
3. Read Phase Status Word LSB

This write-before-read is analogous to the latching of performance monitor counter values in PMON, and is required to ensure that the phase status word value remains valid during the µP read. It is important to read the MSB register before the LSB register because, once the Phase Status Word (LSB) register has been read, the phase status word counter is unfrozen and the contents may change immediately.

Register 010H, 090H, 110H, 190H: CDRC Configuration

Bit	Type	Function	Default
Bit 7	R/W	AMI	0
Bit 6	R/W	LOS1	0
Bit 5	R/W	LOS0	0
Bit 4	R/W	DCR	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	ALGSEL	0
Bit 1	R/W	O162	0
Bit 0		Unused	X

AMI:

The active high AMI bit disables HDB3 decoding. With AMI low, an HDB3 signature on the RP and RN inputs is substituted with four zeros on the DRPCM output. The AMI bit has no affect on the RPCM output.

LOS1, LOS0

The loss of signal threshold is set by the state of the AMI, LOS1 and LOS0 bits:

AMI	LOS1	LOS0	Threshold (PCM periods)
0	0	0	10
1	0	0	15
X	0	1	31
X	1	0	63
X	1	1	175

If the number of consecutive spaces *exceeds* the programmed threshold, loss of signal is declared.

DCR:

Asserting the DCR bit disables clock recovery. With DCR high, the recovered clock (RCLKO[x]) is derived from RCLKI[x] instead of being recovered from the RDP[x] and RDN[x] inputs.

Reserved:

The reserved bit must be cleared to logic 0 for correct operation.

ALGSEL:

The algorithm select (ALGSEL) bit determines the DPLL phase adjustment algorithm. A logic 0 selects the original phase adjustment algorithm which has 0.41 UIpp of high frequency jitter tolerance. When ALGSEL is logic 1, the high frequency jitter tolerance is 0.50 UIpp, but the low frequency tolerance is approximately 20% lower than the first algorithm.

O162:

If the AMI bit is logic 0, the ITU-T Recommendation O.162 compatibility select bit (O162) allows selection between two line code definitions:

1. If O162 is a logic 0, a line code violation is indicated if the serial stream does not match the verbatim HDB3 definition given in Recommendation G.703. A bipolar violation that is not part of an HDB3 signature or a bipolar violation in an HDB3 signature that is the same polarity as the last bipolar violation results in a line code violation indication.

2. If O162 is a logic 1, a line code violation is indicated if a bipolar violation is of the same polarity as the last bipolar violation, as per ITU-T Recommendation O.162.

Register 011H, 091H, 111H, 191H: CDRC Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	LCVE	0
Bit 6	R/W	LOSE	0
Bit 5	R/W	HDB3E	0
Bit 4	R/W	Z4DE	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The CDRC Interrupt Enable register allows the setting of specific events to cause an interrupt on the INTB pin.

The Z4DE, HDB3E, LOSE, and LCVE bits of this register are interrupt enable bits used to select which of the indications (four consecutive zeros, HDB3 pattern, loss of signal, or line code violation) will generate an interrupt when their status changes.

The occurrence of any of these events will generate an interrupt if there is a logic 1 in the corresponding bit position. When the EQUAD is reset, Z4DE, HDB3E, LOSE, and LCVE bits are set to logic 0, disabling any interrupt generation.

Register 012H, 092H, 112H, 192H: CDRC Interrupt Status

Bit	Type	Function	Default
Bit 7	R	LCVI	X
Bit 6	R	LOSI	X
Bit 5	R	HDB3I	X
Bit 4	R	Z4DI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	LOS	X

The LCVI, LOSI, HDB3I and Z4DI bits indicate which of the status events have occurred since the last read of this register. A logic 1 indicates the corresponding event was detected. These bits are cleared when the CDRC Interrupt Status register is read.

LCVI:

The LCVI bit is asserted if a line code violation is detected. If the AMI bit of the CDRC Configuration Register is a logic 1, LCVI becomes a logic 1 if two consecutive marks are of the same polarity (i.e. on the same pin, RDP or RDN). If the AMI and O162 bits of the CDRC Configuration Register are both logic 0, LCVI becomes a logic 1 if a bipolar violation (BPV) is of the same polarity as the previous BPV or if the BPV is not preceded by two spaces. If the AMI bit is a logic 0 and the O162 bit is a logic 1, LCVI becomes a logic 1 if two consecutive bipolar violations are of the same polarity.

LOSI:

The LOSI bit is set high when the LOS status bit changes state.

HDB3I:

The HDB3I bit is set high if an HDB3 signature, which is a bipolar violation of the opposite polarity of the previous bipolar violation following two spaces, is detected in the received data stream.

Z4DI:

The Z4DI bit is set high if four consecutive spaces occur.

LOS:

The LOS bit is the loss of signal status. It is a logic 1 if the number of consecutive spaces exceeds the programmed threshold. The status is deasserted upon the reception of a single mark.

Register 013H, 093H, 113H, 193H: CDRC Alternate Loss of Signal Status

Bit	Type	Function	Default
Bit 7	R/W	ALTLOSE	0
Bit 6	R	ALTLOSI	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	ALTLOS	X

The alternate loss of signal status provides a more stringent criteria for the deassertion of the alarm.

ALTLOSE:

If the ALTLOSE bit is a logic 1, an interrupt is generated when the ALTLOS status bit changes state.

ALTLOSI:

The LOSI bit is set high when the ALTLOS status bit changes state. It is cleared when this register is read.

ALTLOS:

The ALTLOS bit is asserted when the number of consecutive zeros exceeds the threshold specified by the CDRC Configuration register. The ALTLOS bit is deasserted only after 255 bit periods during which no sequence of four zeros has been received.

Registers 014H, 094H, 114H and 194H: Channel Select (0 to 7)

Bit	Type	Function	Default
Bit 7	R/W	CH[7]	0
Bit 6	R/W	CH[6]	0
Bit 5	R/W	CH[5]	0
Bit 4	R/W	CH[4]	0
Bit 3	R/W	CH[3]	0
Bit 2	R/W	CH[2]	0
Bit 1	R/W	CH[1]	0
Bit 0	R/W	CH[0]	0

Registers 015H, 095H, 115H and 195H: Channel Select (8 to 15)

Bit	Type	Function	Default
Bit 7	R/W	CH[15]	0
Bit 6	R/W	CH[14]	0
Bit 5	R/W	CH[13]	0
Bit 4	R/W	CH[12]	0
Bit 3	R/W	CH[11]	0
Bit 2	R/W	CH[10]	0
Bit 1	R/W	CH[9]	0
Bit 0	R/W	CH[8]	0

Registers 016H, 096H, 116H and 196H: Channel Select (16 to 23)

Bit	Type	Function	Default
Bit 7	R/W	CH[23]	0
Bit 6	R/W	CH[22]	0
Bit 5	R/W	CH[21]	0
Bit 4	R/W	CH[20]	0
Bit 3	R/W	CH[19]	0
Bit 2	R/W	CH[18]	0
Bit 1	R/W	CH[17]	0
Bit 0	R/W	CH[16]	0

Registers 017H, 097H, 117H and 197H: Channel Select (24 to 31)

Bit	Type	Function	Default
Bit 7	R/W	CH[31]	0
Bit 6	R/W	CH[30]	0
Bit 5	R/W	CH[29]	0
Bit 4	R/W	CH[28]	0
Bit 3	R/W	CH[27]	0
Bit 2	R/W	CH[26]	0
Bit 1	R/W	CH[25]	0
Bit 0	R/W	CH[24]	0

These registers determine which timeslots (TS) are presented on RDLSIG[x] or inserted from TDLSIG[x] when the RFRACE1 or TFRACE1 register bit is set to logic 1 respectively.

If the RFRACE1 register bit is a logic 1, each channel, overhead, or datalink timeslot for which the associated CH[x] bit is set (e.g. CH[16] corresponds to TS16) will be presented on the RDLSIG[x] output. The RDLCLK[x] output will generate a pulse for each extracted bit.

If the TFRACE1 register bit is a logic 1, the serial stream input on TDLSIG[x] will replace the channel timeslot from BTPCM[x] for which the associated CH[x] bit is set. The TDLCLK[x] output will generate a pulse to clock in each defined bit. Note that if CH[0] is set to logic 1, the TDLSIG[x] input will overwrite any framing and overhead data that would otherwise be inserted into TS0 by the TRAN block. If CH[16] is set to logic 1, the TDLSIG[x] input will be inserted into TS16 regardless of the settings of the SIGEN and DLEN bits of the TRAN Configuration register.

Register 018H, 098H, 118H, 198H: DJAT Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OVRI	0
Bit 0	R	UNDI	0

This register contains the indication of the DJAT FIFO status.

OVRI:

The OVRI bit is asserted when an attempt is made to write data into the FIFO when the FIFO is already full. When OVRI is a logic 1, an overrun event has occurred.

UNDI:

The UNDI bit is asserted when an attempt is made to read data from the FIFO when the FIFO is already empty. When UNDI is a logic 1, an underrun event has occurred.

Register 019H, 099H, 119H, 199H: DJAT Reference Clock Divisor (N1) Control

Bit	Type	Function	Default
Bit 7	R/W	N1[7]	0
Bit 6	R/W	N1[6]	0
Bit 5	R/W	N1[5]	1
Bit 4	R/W	N1[4]	0
Bit 3	R/W	N1[3]	1
Bit 2	R/W	N1[2]	1
Bit 1	R/W	N1[1]	1
Bit 0	R/W	N1[0]	1

This register defines an 8-bit binary number, N1, which is one less than the magnitude of the divisor used to scale down the DJAT PLL reference clock input. The REF divisor magnitude, (N1+1), is the ratio between the frequency of REF input and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL and, if the SYNC bit in the DJAT Configuration register is high, will also reset the FIFO.

Upon reset of the EQUAD, the default value of N1 is set to decimal 47 (2FH).

Consult the Operations section for clarification of divisor selection criteria.

Register 01AH, 09AH, 11AH, 19AH: DJAT Output Clock Divisor (N2) Control

Bit	Type	Function	Default
Bit 7	R/W	N2[7]	0
Bit 6	R/W	N2[6]	0
Bit 5	R/W	N2[5]	1
Bit 4	R/W	N2[4]	0
Bit 3	R/W	N2[3]	1
Bit 2	R/W	N2[2]	1
Bit 1	R/W	N2[1]	1
Bit 0	R/W	N2[0]	1

This register defines an 8-bit binary number, N2, which is one less than the magnitude of the divisor used to scale down the DJAT smooth output clock signal. The output clock divisor magnitude, (N2+1), is the ratio between the frequency of the smooth output clock and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL and, if the SYNC bit is high, will also reset the FIFO.

Upon reset of the EQUAD, the default value of N2 is set to decimal 47 (2FH).

Consult the Operations section for clarification of divisor selection criteria.

Register 01BH, 09BH, 11BH, 19BH: DJAT Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	1
Bit 4	R/W	CENT	0
Bit 3	R/W	UNDE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	SYNC	1
Bit 0	R/W	LIMIT	1

This register controls the operation of the DJAT FIFO read and write pointers and controls the generation of interrupt by the FIFO status.

Reserved:

This bit should be written to a logic 1 for proper operation.

CENT:

The CENT bit allows the FIFO to self-center its read pointer, maintaining the pointer at least 4 UI away from the FIFO being empty or full. When CENT is set to logic 1, the FIFO is enabled to self-center for the next 384 transmit data bit period, and for the first 384 bit periods following an overrun or underrun event. If an EMPTY or FULL alarm occurs during this 384 UI period, then the period will be extended by the number of UI that the EMPTY or FULL alarm persists. During the EMPTY or FULL alarm conditions, data is lost. When CENT is set to logic 0, the self-centering function is disabled, allowing the data to pass through uncorrupted during EMPTY or FULL alarm conditions. *The SYNC bit must be set to logic 0 in order to set the CENT bit to logic 1.*

OVRE,UNDE:

The OVRE and UNDE bits control the generation of an interrupt on the microprocessor INTB pin when a FIFO error event occurs. When OVRE or UNDE is set to logic 1, an overrun event or underrun event, respectively, is allowed to generate an interrupt on the INTB pin. When OVRE or UNDE is set to logic 0, the FIFO error events are disabled from generating an interrupt.

SYNC:

The SYNC bit enables the PLL to synchronize the phase delay between the FIFO input and output data to the phase delay between reference clock input and smooth output clock at the PLL. For example, if the PLL is operating so that the smooth output clock lags the reference clock by 24 UI, then the synchronization pulses that the PLL sends to the FIFO will force its output data to lag its input data by 24 UI.

LIMIT:

The LIMIT bit enables the PLL to limit the jitter attenuation by enabling the FIFO to increase or decrease the frequency of the smooth output clock whenever the FIFO is within one unit interval (UI) of overflowing or underflowing. This limiting of jitter ensures that no data is lost during high phase shift conditions. When LIMIT is set to logic 1, the PLL jitter attenuation is limited. When LIMIT is set to logic 0, the PLL is allowed to operate normally.

Upon reset of the EQUAD, the LIMIT and SYNC bits are set to logic 1, and the OVRE, UNDE, and CENT bits are set to logic 0.

Register 01CH, 09CH, 11CH, 19CH: ELST Configuration

Bit	Type	Function	Default
Bit 7	R/W	ACCEL	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	IR	1
Bit 0	R/W	OR	1

This register controls the format of the expected input frame to the ELST block and the format of the generated output frame from the ELST block.

ACCEL:

The ACCEL bit is used for production test purposes only. THE ACCEL BIT MUST BE PROGRAMMED TO LOGIC 0 FOR NORMAL OPERATION.

IR:

The IR bit selects the input frame format. The IR bit must be set to logic 1 to properly handle the E1 frame format being input into the ELST. SETTING IR TO LOGIC 0 IS A RESERVED SETTING AND SHOULD NOT BE USED.

OR:

The OR bit selects the output frame format. The OR bit must be set to logic 1 to properly generate the E1 frame format output from the ELST. SETTING OR TO LOGIC 0 IS A RESERVED SETTING AND SHOULD NOT BE USED.

Register 01DH, 09DH, 11DH, 19DH: ELST Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	SLIPE	0
Bit 1	R	SLIPD	X
Bit 0	R	SLIPI	X

SLIPE:

The SLIPE bit position is an interrupt enable that when set, allows the INT output to go HIGH when a slip occurs. When the block is reset the SLIPE bit position is cleared and interrupt generation is disabled.

SLIPD:

The SLIPD bit indicates the direction of the last slip. If the Interrupt Status Register is read and the SLIPD bit is a logic 1 then the last slip was due to the frame buffer becoming full. If the Interrupt Status Register is read and the SLIPD bit is a logic 0 then the last slip was due to the frame buffer becoming empty.

SLIPI:

The SLIPI bit is set if a slip occurred since the last read of the Interrupt Status register. The SLIPI bit is cleared just after the Interrupt Status register read operation.

Register 01EH, 09EH, 11EH, 19EH: ELST Idle Code

Bit	Type	Function	Default
Bit 7	R/W	D7	1
Bit 6	R/W	D6	1
Bit 5	R/W	D5	1
Bit 4	R/W	D4	1
Bit 3	R/W	D3	1
Bit 2	R/W	D2	1
Bit 1	R/W	D1	1
Bit 0	R/W	D0	1

The contents of the IDLE CODE register replace the timeslot data in the BRPCM serial data stream when the E1 framer is out of frame and the TRKEN bit in the Receive Options register is a logic 1. Since the transmission of all ones timeslot data is a common requirement, the IDLE CODE register is set to all ones on a reset condition. Bit 7 is the first to be transmitted.

The writing of the idle code pattern is asynchronous with respect to the output data clock. One timeslot of idle code data will be corrupted if the register is written to when the framer is out of frame.

Register 020H, 0A0H, 120H, 1A0H: FRMR Frame Alignment Options

Bit	Type	Function	Default
Bit 7	R/W	CRCEN	0
Bit 6	R/W	CASDIS	0
Bit 5	R/W	AFAA	0
Bit 4	R/W	CHKSEQ	0
Bit 3	R/W	CASA	0
Bit 2	R/W	REFR	0
Bit 1	R/W	REFCRCE	0
Bit 0	R/W	REFRDIS	0

This register selects the various framing formats and framing algorithms supported by the FRMR block.

CRCEN:

The CRCEN bit enables the FRMR to frame to the CRC multiframe. When the CRCEN bit is logic 1, the FRMR searches for CRC multiframe alignment and monitors for errors in the alignment. A logic 0 in the CRCEN bit position disables searching for multiframe and suppresses the CRCE, CMFER, and FEBE FRMR status's, forcing them to logic 0 and forcing OOCMF to a logic 1.

CASDIS:

The CASDIS bit enables the FRMR to frame to the Channel Associated Signaling multiframe when set to a logic 0. When CAS is enabled, the FRMR searches for signaling multiframe alignment and monitors for errors in the alignment. A logic 1 in the CASDIS bit position disables searching for multiframe and suppresses the OOSMF and the SMFER FRMR outputs, forcing them to logic 0.

AFAA:

The AFAA bit enables an alternate framing algorithm. If AFAA is a logic zero, frame alignment is declared after a correct FAS, a logic 1 in bit 2 of time slot 0 of the next frame and finally another FAS in the third frame are found. If one of the conditions fails, the next bit position is checked for valid framing. If AFAA is a logic one, the framing is similar to the above, but adds a "hold-off" feature. If bit2 or the second 7-bit FAS conditions fail, the same byte location

is checked again in the subsequent frames before checking the next bit position for frame alignment.

CHKSEQ:

The CHKSEQ bit enables the use of the check sequence to verify the correct frame alignment in the presence of random imitative frame alignment signals. A logic 1 in the CHKSEQ bit position enables the use of the check sequence algorithm in addition to the basic frame find algorithms; a logic 0 disables the use of the check sequence algorithm.

CASA:

The CASA bit selects one of the two algorithms used to find Channel Associated Signaling multiframe alignment. A logic 0 in the CASA bit position selects the G.732-compatible algorithm; a logic 1 selects the alternate framing algorithm.

REFR:

A transition from logic 0 to logic 1 in the REFR bit position forces the re-synchronization to a new frame alignment. The bit must be cleared to logic 0, then set to logic 1 again to generate subsequent re-synchronizations.

REFCRCE:

The REFCRCE bit enables excessive CRC errors (• 915 errors in one second) to force a re-synchronization to a new frame alignment. Setting the REFCRCE bit position to logic 1 enables reframe due to excessive CRC errors; setting the REFCRCE bit to logic 0 disables CRC errors from causing a reframe.

REFRDIS:

The REFRDIS bit disables reframing under any error condition once frame alignment has been found; reframing can be initiated by software via the REFR bit. A logic 1 in the REFRDIS bit position causes the FRMR to remain "locked in frame" once initial frame alignment has been found. A logic 0 allows reframing to occur based on the various error criteria (FER, excessive CRC errors, etc.). Note that while the FRMR remains locked in frame due to REFRDIS=1, a received AIS will not be detected since the FRMR must be out-of-frame to detect AIS.

Register 021H, 0A1H, 121H, 1A1H: FRMR Maintenance Mode Options

Bit	Type	Function	Default
Bit 7	R/W	FASC	0
Bit 6	R/W	BIT2C	0
Bit 5	R/W	SMFASC	0
Bit 4	R/W	T16C	0
Bit 3	R/W	RADEB	0
Bit 2	R/W	RMADEB	0
Bit 1	R	CMFACT	X
Bit 0	R	EXCRCE	X

FASC:

The FASC bit selects the criterion used to declare loss of frame alignment signal: a logic 0 in the FASC bit position enables declaration of loss of frame alignment when 3 consecutive frame alignment patterns have been received in error; a logic 1 in the FASC bit position enables declaration of loss of frame when 4 consecutive frame alignment pattern errors are detected.

BIT2C:

The BIT2C bit enables the additional criterion that loss of frame is declared when bit 2 in time slot 0 of NFAS frames has been received in error on 3 consecutive occasions: a logic 1 in the BIT2C position enables declaration of loss of frame alignment when bit 2 is received in error; a logic 0 in BIT2C enables declaration of loss of frame alignment based on the setting of FASC, only.

SMFASC:

The SMFASC bit selects the criterion used to declare loss of signaling multiframe alignment signal: a logic 0 in the SMFASC bit position enables declaration of loss of signaling multiframe alignment when 2 consecutive multiframe alignment patterns have been received in error; a logic 1 in the SMFASC bit position enables declaration of loss of signaling multiframe when 2 consecutive multiframe alignment patterns have been received in error or when time slot 16 contains logic 0 in all bit positions for 1 or 2 multiframes based on the criterion selected by T16C.

T16C:

The T16C bit selects the criterion used to declare loss of signaling multiframe alignment signal when enabled by the SMFASC: a logic 0 in the T16C bit position enables declaration of loss of signaling multiframe alignment when time slot 16 contains logic 0 in all bit positions for 1 multiframe; a logic 1 in the T16C bit position enables declaration of loss of signaling multiframe when time slot 16 contains logic 0 in all bit positions for 2 consecutive signaling multiframes.

RADEB:

The RADEB bit selects the amount of debouncing applied to the Remote Alarm Indication before the RRA is allowed to change state: a logic 0 in the RADEB bit position enables the RRA output to change to the logic value contained in the Remote Alarm bit position (bit 3 of NFAS frames) when the received Remote Alarm bit value has been in the same state for 2 consecutive NFAS frames; a logic 1 in the RADEB bit position enables the RRA output to change when the Remote Alarm bit has been in the same state for 3 consecutive NFAS frames.

RMADEB:

The RMADEB bit selects the amount of debouncing applied to the Remote Signaling Multiframe Alarm Indication before the RRMA is allowed to change state: a logic 0 in the RMADEB bit position enables the RRMA output to change to the logic value contained in the Remote Signaling Multiframe Alarm bit position (bit 6 of time slot 16 of frame 0 of the signaling multiframe) when the received Remote Signaling Multiframe Alarm bit value has been in the same state for 2 consecutive signaling multiframes; a logic 1 in the RMADEB bit position enables the RRMA output to change when the Remote Signaling Multiframe Alarm bit has been in the same state for 3 consecutive signaling multiframes.

CMFACT:

The CMFACT bit is an active high status bit indicating that the CRC Multiframe Find algorithm has been active for more than 8ms, thereby initiating a reframe if the CRCEN bit is set to logic 1. The CMFACT bit is reset to logic 0 after the register is read.

EXCRCE:

The EXCRCE bit is an active high status bit indicating that excessive CRC evaluation errors (i.e. •915 error in one second) have occurred, thereby initiating a reframe if enabled by the REFCRCE bit of the Frame Alignment Options register. The EXCRCE bit is reset to logic 0 after the register is read.

Register 022H, 0A2H, 122H, 1A2H: FRMR Framing Status Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	OOFE	0
Bit 5	R/W	OOSMFE	0
Bit 4	R/W	OOCMFE	0
Bit 3	R/W	COFAE	0
Bit 2	R/W	FERE	0
Bit 1	R/W	SMFERE	0
Bit 0	R/W	CMFERE	0

OOFE, OOSMFE and OOCMFE:

A logic one in bits OOFE, OOSMFE and OOCMFE enables the generation of an interrupt on a change of state of OOF, OOSMF and OOCMF bits respectively of the FRMR Framing Status register.

COFAE:

A logic one in the COFAE bit enables the generation of an interrupt when the position of the frame alignment has changed.

FERE:

A logic one in the FERE bit enables the generation of an interrupt when an error has been detected in the frame alignment signal.

SMFERE:

A logic one in the SMFERE bit enables the generation of an interrupt when an error has been detected in the signaling multiframe alignment signal.

CMFERE:

A logic one in the CMFERE bit enables the generation of an interrupt when an error has been detected in the CRC multiframe alignment signal.

Register 023H, 0A3H, 123H, 1A3H: FRMR Maintenance/Alarm Status Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	RRAE	0
Bit 6	R/W	RRMAE	0
Bit 5	R/W	AISDE	0
Bit 4	R/W	T16AISDE	0
Bit 3	R/W	REDE	0
Bit 2	R/W	AISE	0
Bit 1	R/W	FEBEE	0
Bit 0	R/W	CRCEE	0

RRAE, RRMAE, AISDE, T16AISDE, REDE and AISE:

A logic one in bits RRAE, RRMAE, AISDE, T16AISDE, REDE or AISE enables the generation of an interrupt on a change of state of the RRA, RRMA, AISD, T16AISD, RED and AIS bits respectively of the FRMR Maintenance/Alarm Status register.

FEBEE:

When the FEBEE bit is a logic one, an interrupt is generated when a logic zero is received in the Si bits of frames 13 or 15.

CRCEE:

When the CRCEE bit is a logic one, an interrupt is generated when calculated CRC differs from the received CRC remainder.

Register 024H, 0A4H, 124H, 1A4H: FRMR Framing Status Interrupt Indication

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	OOFI	X
Bit 5	R	OOSMFI	X
Bit 4	R	OOCMFI	X
Bit 3	R	COFAI	X
Bit 2	R	FERI	X
Bit 1	R	SMFERI	X
Bit 0	R	CMFERI	X

A logic 1 in any bit position of this register indicates which framing status generated an interrupt by changing state.

OOFI, OOSMFI, OOCMFI, and COFAI:

OOFI, OOSMFI, OOCMFI, and COFAI indicate when the corresponding status has changed state from logic 0 to logic 1 or vice-versa.

FERI, SMFERI, CMFERI:

FERI, SMFERI, CMFERI indicate when a framing error, signaling multiframe error or CRC multiframe error event has been detected; these bits will be set if one or more errors have occurred since the last register read.

The interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the state of the framer. The contents of this register are cleared to logic 0 after the register is read; the interrupt is also cleared if it was generated by any of the Framing Status outputs.

Register 025H, 0A5H, 125H, 1A5H: FRMR Maintenance/Alarm Status Interrupt Indication

Bit	Type	Function	Default
Bit 7	R	RRAI	X
Bit 6	R	RRMAI	X
Bit 5	R	AISDI	X
Bit 4	R	T16AISDI	X
Bit 3	R	REDI	X
Bit 2	R	AISI	X
Bit 1	R	FEBEI	X
Bit 0	R	CRCEI	X

A logic 1 in any bit position of this register indicates which maintenance or alarm status generated an interrupt by changing state.

RRAI, RRMAI, AISDI, T16AISDI, REDI, and AISI:

RRAI, RRMAI, AISDI, T16AISDI, REDI, and AISI indicate when the corresponding FRMR Maintenance/Alarm Status register bit has changed state from logic 0 to logic 1 or vice-versa.

FEBEI:

The FEBEI bit becomes a logic one when a logic zero is received in the Si bits of frames 13 or 15.

CRCEI:

The CRCEI bit becomes a logic one when a calculated CRC differs from the received CRC remainder.

The bits in this register are set by a single error event.

The interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the state of the framer. The contents of this register are cleared to logic 0 after the register is read; the interrupt is also cleared if it was generated by one of the Maintenance/Alarm Status events.

Register 026H, 0A6H, 126H, 1A6H: FRMR Framing Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	OOF	X
Bit 5	R	OOSMF	X
Bit 4	R	OOCMF	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	8MSDIS	0
Bit 0	R/W	MFASDIS	0

Reading this register returns the current state value of the OOF, OOSMF and OOCMF FRMR framing status.

OOF:

The OOF bit is a logic one when basic frame alignment has been lost. The OOF bit goes to a logic zero once frame alignment has been regained.

OOSMF:

The OOSMF bit is a logic one when the signaling multiframe alignment has been lost. The OOSMF bit becomes a logic zero once signaling multiframe has been regained.

OOCMF:

The OOCMF bit is a logic one when the CRC multiframe alignment has been lost. The OOCMF bit becomes a logic zero once CRC multiframe has been regained.

8MSDIS:

The 8MSDIS bit controls the ability of the 8 ms timer to initiate a reframe when CRC multi-frame alignment cannot be found. When 8MSDIS is set to logic 0, the 8 ms timer will initiate a reframe when the CRC Multi-frame Find algorithm has been active for more than 8 ms. When 8MSDIS is set to logic 1, the 8 ms timer will not initiate a reframe when the CRC Multi-frame Find algorithm has been active for more than 8 ms.

This bit is intended to be used for compatibility with ITU-T G.706 section 4.2, note 2.

MFASDIS:

The MFASDIS bit controls the ability of the MFAS errors to cause a loss of CRC Multiframe. When MFASDIS is a logic 0, 4 consecutive MFASs received in error will cause a loss of CRC Multiframe, indicated by OOCMF = 1 and OOF = 1. When MFASDIS is a logic 1, CRC Multiframe alignment, once found, will not be lost unless there is a loss of basic frame alignment or excessive CRC errors (> 915 per second) occur. This bit should be set to logic 1 for compliance to ITU-T G.706.

Register 027H, 0A7H, 127H, 1A7H: FRMR Maintenance/Alarm Status

Bit	Type	Function	Default
Bit 7	R	RRA	X
Bit 6	R	RRMA	X
Bit 5	R	AISD	X
Bit 4	R	T16AISD	X
Bit 3	R	RED	X
Bit 2	R	AIS	X
Bit 1		Unused	X
Bit 0		Unused	X

Reading this register returns the current state value of the RRA, RRMA, AISD, T16AISD, RED, and AIS maintenance/alarm statuses.

RRA:

The RRA bit is a logic one when the "A" bit (bit 3 in time slot 0 of the non-frame alignment signal frame) has been a logic one for 2 or 3 consecutive non-frame alignment signal frames, as determined by the RADEB bit. The RRA output is updated every two frames.

RRMA:

The RRMA bit is a logic one when the "Y" bit (bit 6 in time slot 16 in frame 0 of the signaling multiframes) has been a logic one for 2 or 3 consecutive signaling multiframes, as determined by the RMADEB bit. The RRMA bit is updated every 16 frames.

AISD:

The AISD bit is a logic one after an unframed pattern of all ones with less than 3 zeros in two consecutive frame times (512 bits) has been detected. The AISD bit is updated every 512 bit times.

TS16AISD:

The TS16AISD is a logic one after an all-ones byte has been detected in time slot 16 for 2 consecutive frames while out of signaling multiframe alignment.

RED:

The RED bit is a logic one if an out of frame condition has persisted for 100 ms. The RED bit returns to a logic zero when a out of frame condition has been absent for 100 ms.

AIS:

The AIS bit is a logic one when an out of frame all-ones condition has persisted for 100 ms. The AIS bit returns to a logic zero when the AIS condition has been absent for 100 ms.

Register 028H, 0A8H, 128H, 1A8H: FRMR International/National Bits

Bit	Type	Function	Default
Bit 7	R	Si1	X
Bit 6	R	Si0	X
Bit 5	R	RAWRA	X
Bit 4	R	Sn0	X
Bit 3	R	Sn1	X
Bit 2	R	Sn2	X
Bit 1	R	Sn3	X
Bit 0	R	Sn4	X

Reading this register returns the current bit value of the International and National bits collected over 2 consecutive frames. The Si1 bit position corresponds to the value contained in the International bit position in the FAS frame; the Si0, RAWRA, and Sn[4:0] bit positions correspond to the values contained in the International, Remote Alarm Indication, and National bit positions in the NFAS frame. This register is updated after time slot 0 of every NFAS frame and the contents are valid for 2 frames (250µs). The contents of this register are latched during the read, however the individual bits should not be considered to constitute a byte value (i.e. the 5 national bits should not be considered as indicating 1 of 32 possible values since it is possible that the individual bits are not all from the same time instant due to the asynchronous nature of the microprocessor reads). If the bits are to be interpreted as binary values, care should be taken to ensure a coherent set of bit values by reading the register at least twice.

The Si0, RAWRA and Sn0-Sn4 bits map to the TSO NFAS as follows:

Bit Position							
1	2	3	4	5	6	7	8
Si0	1	RAWRA	Sn0	Sn1	Sn2	Sn3	Sn4

Register 029H, 0A9H, 129H, 1A9H: FRMR Extra Bits

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	X3	X
Bit 2	R	RAWRMA	X
Bit 1	R	X1	X
Bit 0	R	X0	X

Reading this register returns the current bit value of the Extra bits and the Remote Signaling Multiframe Alarm collected from time slot 16 of frame 0 of signaling multiframes. The X3, RAWRMA, X1, X0 bit positions corresponds to the value contained in bit positions 5, 6, 7, and 8 in time slot 16 of frame 0 of the signaling multiframe. This register is updated once per signaling multiframe (the contents remain valid for 2ms). If the X3, X1, X0 bits are to be interpreted as binary values, care should be taken to ensure a coherent set of bit values by reading the register at least twice.

Register 02AH, 0AAH, 12AH, 1AAH: FRMR CRC Error Counter - LSB

Bit	Type	Function	Default
Bit 7	R	CRCE7	X
Bit 6	R	CRCE6	X
Bit 5	R	CRCE5	X
Bit 4	R	CRCE4	X
Bit 3	R	CRCE3	X
Bit 2	R	CRCE2	X
Bit 1	R	CRCE1	X
Bit 0	R	CRCE0	X

This register contains the least significant byte of the 10-bit CRC error counter value, updated every second.

Register 02BH, 0ABH, 12BH, 1ABH: FRMR CRC Error Counter - MSB

Bit	Type	Function	Default
Bit 7	R	OVR	0
Bit 6	R	NEWDATA	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	CRCE9	X
Bit 0	R	CRCE8	X

This register contains the most significant two bits of the 10-bit CRC error counter value, updated every second.

NEWDATA:

The NEWDATA flag bit indicates that the counter register contents have been updated with a new count value accumulated over the last 1 second interval. It is set to logic 1 when the CRC error counter data is transferred into the counter registers, and is reset to logic 0 when this register is read. This bit can be polled to determine the 1 second timing boundary used by the FRMR.

OVR:

The OVR flag bit indicates that the counter register contents have not been read within the last 1 second interval, and therefore have been over-written. It is set to logic 1 if CRC error counter data is transferred into the counter registers before the previous data has been read out, and is reset to logic 0 when this register is read.

This CRC error count is distinct from that of PMON because it is guaranteed to be an accurate count of the number of CRC error in one second; whereas, PMON relies on externally initiated transfers which may not be one second apart.

Register 02CH, 0ACH, 12CH, 1ACH: TS16 AIS Alarm Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	TS16AISE	0
Bit 5	R	TS16AISI	X
Bit 4	R	T16AIS	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

Reading this register returns the current value of the time slot 16 AIS status.

The TS16 AIS alarm algorithm accumulates the occurrences of TS16AISD (TS16 AIS detection) events. TS16AISD is defined as two consecutive all ones time slot 16 bytes while out of signaling multiframe. Each interval with a valid TS16 AIS presence indication increments an interval counter which declares TS16 AIS Alarm when 22 valid intervals have been accumulated. An interval with no valid TS16 AIS presence indication decrements the interval counter; the TS16 AIS Alarm declaration is removed when the counter reaches 0. This algorithm provides a 99.1% probability of declaring an TS16 AIS Alarm within 3.1 ms after loss of signaling multiframe detection in the presence of a 10^{-3} mean bit error rate.

TS16AISE:

If the TS16AISE bit is a logic 1, an interrupt is generated when the TS16AIS status bit changes state.

TS16AISI:

The TS16AISI bit is set high when the TS16AIS status bit changes state. It is cleared when this register is read.

TS16AIS:

The TS16AIS bit is a logic one when an all ones condition has persisted in time slot 16 for 3 ms. The bit returns to a logic zero when the time slot 16 AIS condition has been absent for 3 ms.

Register 030H, 0B0H, 130H, 1B0H: TPSC Block Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	IND	0
Bit 0	R/W	PCCE	0

This register allows selection of the microprocessor read access type and output enable control for the Transmit Per-channel Serial Controller.

IND:

The IND bit controls the microprocessor access type: either indirect or direct. The IND bit must be set to logic 1 for proper operation. When the EQUAD is reset, the IND bit is set low, disabling the indirect access mode.

PCCE:

The PCCE bit enables the per-timeslot functions. When the PCCE bit is set to a logic 1, each timeslot's Data Control byte and IDLE Code byte are passed on to the TRAN block. When the PCCE bit is set to logic 0, the per-timeslot functions are disabled.

Register 031H, 0B1H, 131H, 1B1H: TPSC Block µP Access Status

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

BUSY:

The BUSY bit in the Status register is high while a µP access request is in progress. The BUSY bit goes low timed to an internal high-speed clock rising edge after the access has been completed. During normal operation, the Status Register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 480 ns.

Register 032H, 0B2H, 132H, 1B2H: TPSC Block Timeslot Indirect Address/Control

Bit	Type	Function	Default
Bit 7	R/W	R/WB	0
Bit 6	R/W	A6	0
Bit 5	R/W	A5	0
Bit 4	R/W	A4	0
Bit 3	R/W	A3	0
Bit 2	R/W	A2	0
Bit 1	R/W	A1	0
Bit 0	R/W	A0	0

This register allows the µP to access the internal TPSC registers addressed by the A[6:0] bits and perform the operation specified by the R/WB bit. Writing to this register with a valid address and R/WB bit initiates an internal µP access request cycle. The R/WB bit selects the operation to be performed on the addressed register: when R/WB is set to a logic 1, a read from the internal TPSC register is requested; when R/WB is set to a logic 0, an write to the internal TPSC register is requested.

Register 033H, 0B3H, 133H, 1B3H: TPSC Block Timeslot Indirect Data Buffer

Bit	Type	Function	Default
Bit 7	R/W	D7	0
Bit 6	R/W	D6	0
Bit 5	R/W	D5	0
Bit 4	R/W	D4	0
Bit 3	R/W	D3	0
Bit 2	R/W	D2	0
Bit 1	R/W	D1	0
Bit 0	R/W	D0	0

This register contains either the data to be written into the internal TPSC registers when a write request is initiated or the data read from the internal TPSC registers when a read request has completed. During normal operation, if data is to be written to the internal registers, the byte to be written must be written into this Data register before the target register's address and R/WB=0 is written into the Address/Control register, initiating the access. If data is to be read from the internal registers, only the target register's address and R/WB=1 is written into the Address/Control register, initiating the request. After 480 ns, this register will contain the requested data byte.

The internal TPSC registers control the per-timeslot functions on the Transmit PCM data, provide the per-timeslot Transmit IDLE Code, and provide the per-timeslot Transmit signaling control and the alternate signaling bits. The functions are allocated within the registers as follows:

20H	Data Control byte for Time Slot 0
21H	Data Control byte for Time Slot 1
22H	Data Control byte for Time Slot 2
• • •	• • •
3EH	Data Control byte for Time Slot 30
3FH	Data Control byte for Time Slot 31
40H	IDLE Code byte for Time Slot 0
41H	IDLE Code byte for Time Slot 1
42H	IDLE Code byte for Time Slot 2
• • •	• • •
5EH	IDLE Code byte for Time Slot 30
5FH	IDLE Code byte for Time Slot 31

The bits within each control byte are allocated as follows:

TPSC Internal Registers 20-3FH: Data Control byte

Bit	Type	Function
Bit 7	R/W	SUBS
Bit 6	R/W	DS[0]
Bit 5	R/W	DS[1]
Bit 4	R/W	SIGSRC
Bit 3	R/W	A'
Bit 2	R/W	B'
Bit 1	R/W	C'
Bit 0	R/W	D'

SUBS, DS[1], and DS[0]:

The SUBS, DS[1], and DS[0] bits select one of the following data manipulations to be performed on the timeslot:

SUBS	DS[0]	DS[1]	Function
0	0	0	OFF - no change to PCM timeslot data
0	0	1	ADI - data inversion on timeslot bits 1,3,5,7
0	1	0	ADI - data inversion on timeslot bits 2,4,6,8
0	1	1	INV - data inversion on all timeslot bits
1	0	X	Data substitution on - IDLE code replaces PCM timeslot data
1	1	0	Data substitution on - A-Law digital milliwatt pattern* replaces TPCM timeslot data.
1	1	1	Data substitution on - µ-Law digital milliwatt pattern* replaces TPCM timeslot data.

* The A-Law digital milliwatt pattern used is that defined in Recommendation G.711 for A-law:

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
0	0	1	1	0	1	0	0
0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1
0	0	1	1	0	1	0	0
1	0	1	1	0	1	0	0
1	0	1	0	0	0	0	1
1	0	1	0	0	0	0	1
1	0	1	1	0	1	0	0

* The µ-Law digital milliwatt pattern used is that defined in Recommendation G.711 for µ-law:

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
0	0	0	1	1	1	1	0
0	0	0	0	1	0	1	1
0	0	0	0	1	0	1	1
0	0	0	1	1	1	1	0
1	0	0	1	1	1	1	0
1	0	0	0	1	0	1	1
1	0	0	0	1	0	1	1
1	0	0	1	1	1	1	0

SIGSRC:

The SIGSRC bit is valid only if Channel Associated Signaling (CAS) is selected in the TRAN Configuration Register; otherwise, it is ignored. When valid, the SIGSRC bit selects the source of the timeslot signaling bits: if SIGSRC is a logic 0, the signaling bits are taken from the incoming BTSIG stream in the format specified by the SIGEN and DLEN bits in the TRAN Configuration Register; if SIGSRC is a logic 1, the signaling bits are taken from the A',B',C', and D' bit .

TPSC Internal Registers 40-5FH: IDLE Code byte

Bit	Type	Function
Bit 7	R/W	IDLE7
Bit 6	R/W	IDLE6
Bit 5	R/W	IDLE5
Bit 4	R/W	IDLE4
Bit 3	R/W	IDLE3
Bit 2	R/W	IDLE2
Bit 1	R/W	IDLE1
Bit 0	R/W	IDLE0

The contents of the IDLE Code byte register are substituted for the timeslot data on BTPCM when the SUBS bit in the PCM Control Byte is set to a logic 1 and the DS[0] bit in the PCM Control Byte is set to a logic 0. The IDLE Code is transmitted from MSB (bit 7) to LSB (bit 0).

Register 034H, 0B4H, 134H, 1B4H: XFDL Block Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	EOM	0
Bit 3	R/W	INTE	0
Bit 2	R/W	ABT	0
Bit 1	R/W	CRC	0
Bit 0	R/W	EN	0

EOM:

The EOM bit indicates that the last byte of data written in the XFDL Transmit Data register is the end of the present data packet. If the CRC bit is set then the 16-bit FCS word is appended to the last data byte transmitted and a continuous stream of flags is generated. The EOM bit is automatically cleared before transmission of the next data packet begins.

INTE:

The INTE bit enables the generation of an interrupt via the TDLINT[x] output. Setting the INTE bit to logic 1 enables the generation of an interrupt; setting INTE to logic 0 disables the generation of an interrupt. If the TDLINTE bit is also set to logic 1 in the Datalink Options register, the interrupt generated on the TDLINT[x] output is also generated on the microprocessor INTB pin.

ABT:

The Abort (ABT) bit controls the sending of the 7 consecutive ones HDLC abort code. Setting the ABT bit to a logic 1 causes the 11111110 code to be transmitted after the last byte from the XFDL Transmit Data Register is transmitted. Aborts are continuously sent until this bit is reset to a logic 0.

CRC:

The CRC enable bit controls the generation of the ITU-T-CRC frame check sequence (FCS). Setting the CRC bit to logic 1 enables the ITU-T-CRC generator and the appends the 16 bit FCS to the end of each message. When the CRC bit is set to logic 0, the FCS is not appended to the end of the

message. The CRC type used is the ITU-T-CRC with generator polynomial = $x^{16} + x^{12} + x^5 + 1$. The high order bit of the FCS word is transmitted first.

EN:

The enable bit (EN) controls the overall operation of the XFDL block. When the EN bit is set to a logic 1, the XDFL block is enabled and flag sequences are sent until data is written into the XFDL Transmit Data register. When the EN bit is set to logic 0, the XFDL block is disabled.

Register 035H, 0B5H, 135H, 1B5H: XFDL Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	INT	1
Bit 0	R/W	UDR	0

INT:

The INT bit indicates when the XFDL block is ready to accept a new data byte for transmission. The INT bit is set to a logic 1 when the previous byte in the Transmit Data register has been loaded into the parallel to serial converter and a new byte can be written into the XFDL Transmit Data register. The INT bit is set to a logic 0 while new data is in the Transmit Data register. The INT bit is not disabled by the INTE bit in the configuration register.

UDR:

The UDR bit indicates when the XFDL block has underrun the data in the XFDL Transmit Data register. The UDR bit is set to a logic 1 if the parallel to serial conversion of the last byte in the XFDL Transmit Data register has completed before the new byte was written into the XFDL Transmit Data register. Once an underrun has occurred, the XFDL transmits an ABORT, followed by a flag, and waits to transmit the next valid data byte. If the UDR bit is still set after the transmission of the flag the XFDL will continuously transmit the all-ones idle pattern. The UDR bit can only be cleared by writing a logic 0 to the UDR bit position in this register.

Register 036H, 0B6H, 136H, 1B6H: XFDL Transmit Data

Bit	Type	Function	Default
Bit 7	R/W	TD7	X
Bit 6	R/W	TD6	X
Bit 5	R/W	TD5	X
Bit 4	R/W	TD4	X
Bit 3	R/W	TD3	X
Bit 2	R/W	TD2	X
Bit 1	R/W	TD1	X
Bit 0	R/W	TD0	X

Data written to this register is serialized and transmitted on the facility data link least significant bit first. The XFDL block signals when the next data byte is required by setting the TDLINT[x] output high (if enabled) and by setting the INT bit in the Status register high. When INT and/or TDLINT[x] is set, the Transmit Data register must be written with the new data within 4 data bit periods to prevent the occurrence of an underrun.

Register 038H, 0B8H, 138H, 1B8H: RFDL Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	TR	0
Bit 0	R/W	EN	0

TR:

Setting the terminate reception bit (TR) forces the RFDL block to immediately terminate the reception of the current LAPD frame, empty the FIFO, clear the interrupts, and begin searching for a new flag sequence. The RFDL handles the TR input in the same manner as if the EN bit had been cleared and then set. The TR bit in the Configuration register will reset itself after a rising and falling edge have occurred on the CLK input to the RFDL block once the write to this register has completed and WRB goes inactive. If the Configuration register is read after this time, the TR bit value returned will be zero.

EN:

The enable bit (EN) controls the overall operation of the RFDL block. When set, the RDFL block is enabled; when reset the RFDL block is disabled. When the block is disabled, the FIFO and interrupts are all cleared, however, the programming of the RFDL Interrupt Control/Status register is not affected. When the block is enabled, it will immediately begin looking for flags.

The RFDL block handles the TR input in the same manner as clearing and setting the EN bit, therefore, the RFDL state machine will begin searching for flags and an interrupt will be generated when the first flag is detected.

Register 039H, 0B9H, 139H, 1B9H: RFDL Interrupt Control/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTC1	0
Bit 1	R/W	INTC0	0
Bit 0	R	INT	0

INTC1,INTC0:

The INTC1 and INTC0 bits control when an interrupt is asserted based on the number of received data bytes in the FIFO as follows:

INTC1	INTC0	Description
0	0	Disable interrupts (All sources)
0	1	Enable interrupt when FIFO receives data
1	0	Enable interrupt when FIFO has 2 bytes of data
1	1	Enable interrupt when FIFO has 3 bytes of data

INT:

The INT bit reflects the status of the external RDLINT[x] interrupt unless the INTC1 and INTC0 bits are set to disable interrupts. In that case, the RDLINT[x] output is forced to 0 and the INT bit of this register will reflect the state of the internal interrupt latch.

In addition to the FIFO fill status, interrupts are also generated for EOM (end of message), OVR (FIFO overrun), detection of the abort sequence while not receiving all ones and on detection of the first flag while receiving all ones. The interrupt is reset by a RFDL Receive Data Register read that empties the FIFO, unless the cause of the interrupt was due to a FIFO overrun. The interrupt due to

a FIFO overrun is cleared by a RFDL Status register read, by disabling the block, or by setting TR high.

The contents of this register should only be changed when the RFDL block is disabled to prevent any erroneous interrupt generation.

Register 03AH, 0BAH, 13AH, 1BAH: RFDL Status

Bit	Type	Function	Default
Bit 7	R	FE	1
Bit 6	R	OVR	0
Bit 5	R	FLG	0
Bit 4	R	EOM	0
Bit 3	R	CRC	0
Bit 2	R	NVB2	1
Bit 1	R	NVB1	1
Bit 0	R	NVB0	1

The FLG and EOM bits in this register contain values which correspond to the last byte read from the RFDL Data Register.

FE:

The FIFO Empty bit (FE) is high when the last FIFO entry is read and goes low when the FIFO is loaded with new data.

OVR:

The Receiver Overrun bit (OVR) is set when data is written over unread data in the FIFO. This bit is not reset until after the RFDL Status register is read. While OVR is high, the RFDL and FIFO are held in the reset state, causing the FLG and EOM bits in the status register to be reset also.

FLG:

The flag bit (FLG) is set if the RFDL has detected the presence of the LAPD flag sequence (01111110) in the data. FLG is reset only when the LAPD abort sequence (01111111) is detected in the data or when the RFDL is disabled. This bit is passed through the FIFO with the Data so that the status of this bit will correspond to the data just read from the RFDL Data Register. The reception of bit-oriented codes over the data link will also force an abort due to its eight ones pattern.

EOM:

The End of Message bit (EOM) follows the RDLEOM[x] output. It is set when:

1) The last byte in the LAPD frame (EOM) is being read from the Receive Data Register,

2) An abort sequence is detected while not in the receiving all-ones state and the byte, written to the FIFO due to the detection of the abort sequence, is being read from the FIFO,

3) The first flag has been detected and the dummy byte, written into the FIFO when the RFDL changes from the receiving all-ones state to the receiving flags state, is being read from the FIFO,

4) Immediately on detection of FIFO overrun.

The EOM bit is passed through the FIFO with the Data so that the status of this bit will correspond to the data just read from the RFDL Data Register.

CRC:

The CRC bit is set if a CRC error was detected in the last received HDLC frame. The CRC bit is only valid when EOM is logic 1 and FLG is a logic 1 and OVR is a logic 0.

NVB[2:0]:

The NVB[2:0] bit positions indicate the number of valid bits in the RFDL Receive Data Register byte. It is possible that not all of the bits in the RFDL Receive Data Register are valid when the last data byte is read since the data frame can be any number of bits in length and not necessarily an integral number of bytes. The RFDL Receive Data Register is filled starting from the MSB bit position (RD7) and the data bits are shifted to lower bit positions as more bits are received, with one to eight data bits being valid. The number of valid bits is equal to 1 plus the value of NVB[2:0]. An NVB[2:0] value of 000 binary indicates that only the FE bit in this register is valid. An NVB[2:0] value of 011 indicates that RD[7:4] contain valid data bits where RD4 is the data bit that was received first. NVB[2:0] is only valid when the EOM bit is a logic 1 and the FLG bit is a logic 1 and the OVR bit is a logic 0.

On an interrupt generated from the detection of the first flag, reading the RFDL Status register will return invalid NVB[2:0] and CRC bits, even though the EOM bit is logic 1 and the FLG bit is logic 1.

If the Receive Data register is read while there is no valid data, then a FIFO underrun condition occurs. The underrun condition is reflected in the Status register by forcing all bits to logic zero on the first Status register read

immediately following the Received Data register read which caused the underrun condition.

Register 03BH, 0BBH, 13BH, 1BBH: RFDL Receive Data

Bit	Type	Function	Default
Bit 7	R	RD7	X
Bit 6	R	RD6	X
Bit 5	R	RD5	X
Bit 4	R	RD4	X
Bit 3	R	RD3	X
Bit 2	R	RD2	X
Bit 1	R	RD1	X
Bit 0	R	RD0	X

The RFDL Receive Data Register is filled starting from the MSB bit position (RD7) and the data bits are shifted to lower bit positions as more bits are received, with one to eight data bits being valid. The number of valid bits is equal to 1 plus the value of NVB[2:0] from the RFDL Status Register. An NVB[2:0] value of 111 indicates that RD[7:0] contain valid data bits where RD0 corresponds to the first bit of the serial byte received by the RFDL.

These registers are actually 4 level FIFOs. If data is available, the FE bit in the RFDL Status register is low. If INTC[1:0] (in the RFDL Interrupt Control/Status register) is set to 01, this register must be read within 31 data bit periods to prevent an overrun. If INTC[1:0] is set to 11, this register must be read within 15 data bit periods.

When an overrun is detected, an interrupt is generated and the FIFO is held cleared until the Status register is read. When the LAPD abort sequence (01111111) is detected in the data an ABORT interrupt is generated and the data that has been shifted into the serial to parallel converter is written into the FIFO.

A read of this register increments the FIFO pointer at the end of the read. If this register read causes a FIFO underrun, then the pointer is inhibited from incrementing. The underrun condition will be signaled in the next RFDL Status register read by returning all zeros.

Registers 03CH, 0BCH, 13CH and 1BCH: Interrupt ID/Clock Monitor

Bit	Type	Function	Default
Bit 7	R	INT4	0
Bit 6	R	INT3	0
Bit 5	R	INT2	0
Bit 4	R	INT1	0
Bit 3	R	BTCLKA	0
Bit 2	R	TCLKIA	0
Bit 1	R	BRCLKA	0
Bit 0	R	RCLKIA	0

These registers provide interrupt identification and activity monitoring on EQUAD clocks. The framer which caused the INTB output to transition low can be identified by reading register 03CH - the INTx bits in register 0BCH, 13CH, and 1BCH are invalid. The INTx bit in register 03CH will be high if the xth framer caused the interrupt. The Interrupt Source registers of that framer can then be used to find which block within the framer generated the interrupt.

When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. These registers should be read at periodic intervals to detect clock failures.

INT4, INT3, INT2, INT1:

The INTx bit will be high if the xth framer (the framer corresponding to the input pin BTCLK[x]) caused the INTB pin to transition low.

BTCLKA:

The BTCLK active (BTCLKA) bit monitors for low to high transitions on the BTCLK[x] input. BTCLKA is set high on a rising edge of BTCLK[x], and is set low when this register is read.

TCLKIA:

The TCLKI active (TCLKIA) bit monitors for low to high transitions on the TCLKI[x] input. TCLKIA is set high on a rising edge of TCLKI[x], and is set low when this register is read.

BRCLKA:

The BRCLK active (BRCLKA) bit monitors for low to high transitions on the BRCLK input. BRCLKA is set high on a rising edge of BRCLK, and is set low when this register is read.

RCLKIA:

The RCLKI active (RCLKA) bit monitors for low to high transitions on the RCLKI[x] input. RCLKIA is set high on a rising edge of RCLKI[x], and is set low when this register is read.

Registers 03DH, 0BDH, 13DH and 1BDH: Backplane Parity Configuration and Status

Bit	Type	Function	Default
Bit 7	R/W	BTPTYP	0
Bit 6	R/W	BTPRTYE	0
Bit 5	R	BTPCMPI	X
Bit 4	R	BTSIGPI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	BRPTYP	0
Bit 0	R/W	BRPRTYE	0

These registers provide control and status reporting of data integrity checking on the backplane buses. Parity bits in the first bit position of TS0 (henceforth called the PRTY-bit position) represents parity over the previous frame (excluding the parity bit) for the PCM and SIG data streams. BRX2RAIL must be set to logic 0.

BTPTYP:

The transmit backplane parity type (BTPTYP) bit sets even or odd parity in the transmit streams. If BTPTYP is a logic zero, then the expected parity value in the PRTY-bit position of BTPCM[x] and BTSIG[x] is even, thus it is a one if the number of ones in the previous frame (excluding the PRTY-bit) is odd. If BTPTYP is a logic one, then the expected parity value in the PRTY-bit position of BTPCM[x] and BTSIG[x] is odd, thus it is a one if the number of ones in the previous frame (excluding the PRTY-bit) is even.

BTPRTYE:

The BTPRTYE bit enables transmit parity interrupts. When set a logic one, parity errors on inputs BTPCM[x] and BTSIG[x] are indicated by the BTPCMI and BTSIGI bits, respectively, and by the INTB output. When set to logic zero, parity errors are indicated by the BTPCMI and BTSIGI status bits but are not indicated on the INTB output.

BTPCMI:

The BTPCMI bit indicates if a parity error has been detected on the BTPCM[x] input. This bit is cleared when this register is read. Odd or even parity is selected by the BTPTYP bit.

BTSIGI:

The BTSIGI bit indicates if a parity error has been detected on the BTSIG[x] input. This bit is cleared when this register is read. Odd or even parity is selected by the BTPTYP bit.

BRPTYP:

The receive backplane parity type (BRPTYP) bit sets even or odd parity in the receive streams. If BRPTYP is a logic zero, then the parity value in the PRTY-bit position of BRPCM[x] and BRSIG[x] is even, thus it is a one if the number of ones in the previous frame (excluding the PRTY-bit) is odd. If BRPTYP is a logic one, then the parity value in the PRTY-bit position of BRPCM[x] and BRSIG[x] is odd, thus it is a one if the number of ones in the previous frame (excluding the PRTY-bit) is even. BRPTYP only has effect if BRPRTYE is a logic one.

BRPRTYE:

The BRPRTYE bit enables receive parity insertion. When set a logic one, parity is inserted into the PRTY-bit position of the BRPCM[x] and BRSIG[x] streams. When set to logic zero, the data in the PRTY-bit position passes through unaltered.

Register 040H, 0C0H, 140H, 1C0H: SIGX Block Configuration

Bit	Type	Function	Default
Bit 7	R/W	ACCEL	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	MTKC	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	IND	0
Bit 0	R/W	PCCE	0

This register allows selection of the microprocessor access type, and allows enabling of the per-timeslot configuration registers.

ACCEL:

The ACCEL bit is used to enable an accelerated test mode for production purposes only. For proper operation the ACCEL bit must be set to logic 0.

MTKC:

The master trunk conditioning bit, MTKC, enables trunk conditioning for all timeslots, regardless of per-timeslot settings. A logic 1 in the MTKC bit position enables master trunk conditioning. Data from all of the timeslot Trunk Conditioning Data registers (40H to 5FH) is output onto the data stream BRPCM and the per-timeslot signaling trunk conditioning bits A',B',C' and D' are output onto the signaling data stream BRSIG. The MTKC bit is ORed with the per-timeslot trunk conditioning enable bits in the Per-Timeslot Configuration Registers to form the applied per-timeslot trunk conditioning enables. When the EQUAD is reset, the MTKC bit is set to logic 0, disabling master trunk conditioning.

The MTKC bit is independent of the TRKEN bit of the EQUAD Receive Options register and takes precedence over it. If TRKEN is a logic 1, an out-of-frame condition causes the contents of the ELST Idle Code register to placed in all time slots on BRPCM. BRSIG presents the frozen signaling. If MTKC is a logic 1, each BRPCM and BRSIG time slot may have an unique idle code.

Reserved:

The reserved bit must be programmed to logic 0 for proper operation.

IND:

The IND bit controls the microprocessor access type: either indirect or direct. The IND bit must be set to logic 1 for proper operation. When the EQUAD is reset, the IND bit is set low, disabling the indirect access mode.

PCCE:

The PCCE bit enables the per-timeslot functions. When the PCCE bit is set to a logic 1, data inversion, trunk conditioning and signaling debouncing are performed on a per-timeslot basis. When the PCCE bit is set to logic 0, the per-timeslot functions are disabled.

Upon reset of the EQUAD, the ACCEL, MTKC, IND, and PCCE bits are all set to logic 0 disabling µP indirect access and per-timeslot functions.

Register 041H, 0C1H, 141H, 1C1H: SIGX Block µP Access Status

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

BUSY:

The BUSY bit in the Status register is high while a µP access request is in progress. The BUSY bit goes low timed to an internal high-speed clock rising edge after the access has been completed. During normal operation, the Status Register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 480 ns.

Register 042H, 0C2H, 142H, 1C2H: SIGX Block Time Slot Indirect Address/Control

Bit	Type	Function	Default
Bit 7	R/W	R/WB	X
Bit 6	R/W	A6	X
Bit 5	R/W	A5	X
Bit 4	R/W	A4	X
Bit 3	R/W	A3	X
Bit 2	R/W	A2	X
Bit 1	R/W	A1	X
Bit 0	R/W	A0	X

This register allows the µP to access to internal SIGX registers addressed by the A[6:0] bits and perform the operation specified by the R/WB bit. Writing to this register with a valid address and R/WB bit initiates an internal µP access request cycle. The R/WB bit selects the operation to be performed on the addressed register: when R/WB is set to a logic 1, a read from the internal SIGX register is requested, when R/WB is set to a logic 0, a write to the internal SIGX register is requested.

Register 043H, 0C3H, 143H, 1C3H: SIGX Block Time Slot Indirect Data Buffer

Bit	Type	Function	Default
Bit 7	R/W	D[7]	X
Bit 6	R/W	D[6]	X
Bit 5	R/W	D[5]	X
Bit 4	R/W	D[4]	X
Bit 3	R/W	D[3]	X
Bit 2	R/W	D[2]	X
Bit 1	R/W	D[1]	X
Bit 0	R/W	D[0]	X

In the case of an indirect write, the Indirect Data Register holds the value that will be written to the desired register when a write is initiated via the Timeslot Indirect Address Register. In the case of an indirect read, the Indirect Data Register will hold the contents of the indirectly addressed register, when the read has been completed. Please refer below to the per-timeslot register descriptions for the expected bit formats.

The signaling and per-timeslot functions are allocated within the registers as follows:

21H	Signaling Data Register for Time Slot 1
22H	Signaling Data Register for Time Slot 2
• • •	• • •
2FH	Signaling Data Register for Time Slot 15
31H	Signaling Data Register for Time Slot 17
• • •	• • •
3EH	Signaling Data Register for Time Slot 30

3FH	Signaling Data Register for Time Slot 31
40H	PCM Trunk Conditioning byte for Time Slot 0
41H	PCM Trunk Conditioning byte for Time Slot 1
• • •	• • •
5EH	PCM Trunk Conditioning byte for Time Slot 30
5FH	PCM Trunk Conditioning byte for Time Slot 31
60H	Configuration and Signaling Trunk Conditioning data for Time Slot 0
61H	Configuration and Signaling Trunk Conditioning data for Time Slot 1
• • •	• • •
7EH	Configuration and Signaling Trunk Conditioning for Time Slot 30
7FH	Configuration and Signaling Trunk Conditioning for Time Slot 31

SIGX Indirect Registers 33 (21H)- 47 (2FH) - Segment 2: Typical Timeslot Signaling Data Register (TSs 1-15)

Bit	Type	Function	Default
Bit 7	R	A TS ‘n+16’	X
Bit 6	R	B TS ‘n+16’	X
Bit 5	R	C TS ‘n+16’	X
Bit 4	R	D TS ‘n+16’	X
Bit 3	R	A TS ‘n’	X
Bit 2	R	B TS ‘n’	X
Bit 1	R	C TS ‘n’	X
Bit 0	R	D TS ‘n’	X

SIGX Indirect Registers 49 (31H)- 63 (3FH) - Segment 2: Typical Timeslot Signaling Data Register (TSs 17-31)

Bit	Type	Function	Default
Bit 7	R	A TS ‘n-16’	X
Bit 6	R	B TS ‘n-16’	X
Bit 5	R	C TS ‘n-16’	X
Bit 4	R	D TS ‘n-16’	X
Bit 3	R	A TS ‘n’	X
Bit 2	R	B TS ‘n’	X
Bit 1	R	C TS ‘n’	X
Bit 0	R	D TS ‘n’	X

SIGX Indirect Registers 64 (40H) - 95 (5FH) - Segment 3: Typical Per-Timeslot PCM Trunk Conditioning Data Register

Bit	Type	Function	Default
Bit 7	R/W	TCD[7]	X
Bit 6	R/W	TCD[6]	X
Bit 5	R/W	TCD[5]	X
Bit 4	R/W	TCD[4]	X
Bit 3	R/W	TCD[3]	X
Bit 2	R/W	TCD[2]	X
Bit 1	R/W	TCD[1]	X
Bit 0	R/W	TCD[0]	X

When trunk conditioning is enabled, PCM trunk conditioning bits TCD[7:0] replace timeslot bits 1 through 8 respectively for the referenced timeslot. TS0 and TS16 can be replaced with trunk conditioning data.

10.1 SIGX Indirect Registers 96 (60H) - 127 (7FH) - Segment 4: Typical Per-Timeslot Configuration and Signaling Trunk

Conditioning Data Register

Bit	Type	Function	Default
Bit 7	R/W	RINV[1]	X
Bit 6	R/W	RINV[0]	X
Bit 5	R/W	RTKCE	X
Bit 4	R/W	RDEBE	X
Bit 3	R/W	A’	X
Bit 2	R/W	B’	X
Bit 1	R/W	C’	X
Bit 0	R/W	D’	X

RINV[1:0]:

The RINV[1:0] bits select whether the output BRPCM stream is entirely or selectively inverted. The bit mapping is as follows.

00 - do not invert

01 - invert even bits (2,4,6,8)

10 - invert odd bits (1,3,5,7)

11 - invert all bits

RTKCE:

The RTKCE bit enables per-timeslot data stream and signal stream trunk conditioning. A logic 1 in this bit position enables trunk conditioning while a logic 0 disables trunk conditioning. When RTKCE is enabled, per-timeslot trunk conditioning data from one of the timeslot Trunk Conditioning Data Registers (one of 40H to 5FH) is output onto the data stream, BRPCM. In addition, the per-timeslot signaling trunk conditioning bits A’,B’,C’ and D’ are output onto the signaling data stream, BRSIG.

RDEBE:

The RDEBE bit enables debouncing of timeslot signaling bits. A logic 1 in this bit position enables signaling debouncing while a logic 0 disables it. When debouncing is selected, per-timeslot signaling transitions are ignored until two consecutive, equal values are sampled.

A',B',C' and D':

A',B',C' and D' are the per-timeslot signaling trunk conditioning bits. When trunk conditioning is enabled, these bits are used as signaling data, instead of the extracted timeslot signaling bits, and are output onto the BRSIG output.

To enable the RINV[1:0], RTKCE and RDEBE bits, the PCCE bit in the SIGX Configuration Register must be set to logic 1. When these bits are enabled, bits RINV[1:0] and RDEBE are ORed with their primary input equivalents to generate the applied configuration signals.

Register 044H, 0C4H, 144H, 1C4H: TRAN Configuration

Bit	Type	Function	Default
Bit 7	R/W	AMI	0
Bit 6	R/W	SIGEN	1
Bit 5	R/W	DLEN	1
Bit 4	R/W	GENCRC	0
Bit 3	R/W	FDIS	0
Bit 2	R/W	FEBEDIS	0
Bit 1	R/W	INDIS	0
Bit 0	R/W	XDIS	0

AMI:

The AMI bit enables AMI line coding when set to logic 1; when it is set to logic 0, the HDB3 line coding is enabled.

SIGEN, DLEN:

The SIGEN and DLEN bits select the signaling data source for Time Slot 16 (TS16) as follows:

SIGEN	DLEN	MODE
0	0	Signaling insertion disabled. TS16 data is taken directly from the input BTPCM[x] TS16.
0	1	CCS enabled. TS16 data is taken directly from the TDLSIG[x] input or from the HDLC/LAPD transmitter.
1	0	Reserved.
1	1	CAS enabled. TS16 data is taken from either BTSIG[x] stream or from the TPSC Data Control byte as selected on a per-timeslot basis via the SIGSRC bit. The format of the BTSIG[x] input data stream is shown in the "Functional Timing" section.

When channel associated signaling (CAS) is enabled, the format of the input BTSIG stream is selected by the DLEN bit. A logic 1 in the DLEN bit position selects the PMC compatible format in which the BTSIG stream contains the signaling data nibble in the lower four bits of the time slot byte. A logic 0 in the DLEN bit position is reserved and should not be used.

GENCRC:

The GENCRC bit enables generation of the CRC multiframe when set to logic 1. When enabled, the TRAN generates the CRC multiframe alignment signal, calculates and inserts the CRC bits, and if enabled by FEBEDIS, inserts the FEBE indication in the spare bit positions. The CRC bits transmitted during the first sub-multiframe (SMF) are indeterminate and should be ignored. The CRC bits calculated during the transmission of the 'n'th SMF (SMF n) are transmitted in the following SMF (SMF n+1). When GENCRC is set to logic 0, the CRC generation is disabled. The CRC bits are then set to the logic value contained in the Si[1] bit position in the International/National Bit Control Register and bit 1 of the NFAS frames are set to the value of Si[0] bit if enabled by INDIS, or, if not enabled by INDIS, are taken directly from BTPCM[x]. When BTPCM[x] or Si[1] are transmitted in lieu of the calculated CRC bits, there is no delay of one SMF (i.e., the BTPCM[x] bits received in SMF n are transmitted in the same SMF). The same applies when substituting Si[1] in place of the calculated CRC bits.

FDIS:

The FDIS bit value controls the generation of the framing alignment signal. A logic 1 in the FDIS bit position disables the generation of the framing pattern in TS0 and allows the incoming data on BTPCM[x] to pass through the TRAN transparently. A logic 0 in FDIS enables the generation of the framing pattern, replacing TS0 of frames 0,2,4,6,8,10,12,14 with the frame alignment signal, and if enabled by INDIS, replacing TS0 of frames 1,3,5,7,9,11,13,15 with the contents of the International/National Bits Control Register. When FDIS is a logic 1, framing is globally disabled and the values in controls bits GENCRC, FEBEDIS, INDIS, and XDIS are ignored.

Note that the above is true only if the AIS bit in the TRAN Transmit Alarm/Diagnostic Control register is a logic 0. If AIS is logic 1, the output bit stream becomes all ones unconditionally.

INDIS, GENCRC and FEBEDIS:

The INDIS bit controls the insertion of the International and National bits into TS0. When INDIS is set to logic 0, the contents of the TRAN International/National Bit Control register are inserted into TS0; when INDIS

is a logic 1, the contents of the TRAN International/National Bit Control register are ignored and the values for those bit positions in the output stream are taken directly from the BTPCM[x] stream. When INDIS and FDIS are logic 0, the bit values used for the International and National bits are dependent upon the values of the GENCRC and FEBEDIS configuration bits, as shown in the following table:

GENCRC	FEBEDIS	Source of International/National bits
0	X	Bit position Si[1] in the International/National Control Register is used for the International bit in the frame alignment signal (FAS) frames and the Si[0] bit in the non-frame alignment signal (NFAS) frames if INDIS is logic 0. TPCM replaces Si[1:0] if INDIS is logic 1. Bit positions Sn[4:0] in the register are used for the National bits in NFAS frames.
1	0	The calculated CRC bits are used for the International bit in the FAS frames and the generated CRC multiframe alignment signal and the FEBE bits are used for the International bit in the NFAS frames. Bit positions Sn[4:0] in the TRAN International/National Control register are used for the National bits in NFAS frames.
1	1	The calculated CRC bits are used for the International bit in the FAS frames and the generated CRC multiframe alignment signal is used for the International bit in the NFAS frames, with the Si[1:0] bits in the International/National Control Register used for the spare bits. Bit positions Sn[4:0] in the register are used for the National bits in NFAS frames.

XDIS:

If FDIS is logic 0 and SIGEN is logic 1, the XDIS bit controls the insertion of the Extra bits in TS16 of frame 0 of the signaling multiframe as follows. When XDIS is set to a logic 0, the contents of the TRAN Extra Bits Control Register are inserted into TS16, frame 0; when XDIS is a logic 1, the contents of the register are ignored and the values for those bits positions in the output

stream are taken directly from the BTPCM[x] stream. i.e., When XDIS and FDIS are logic 0, and SIGEN is logic 1, the X1,X3,X4 bit values from the TRAN Extra Bits Control Register are used for the Extra bits in TS16 of frame 0 of the signaling multiframe.

When the EQUAD is reset, the contents of this register are set to logic 0, except SIGEN and DLEN which are set to logic 1.

Register 045H, 0C5H, 145H, 1C5H: TRAN Transmit Alarm/Diagnostic Control

Bit	Type	Function	Default
Bit 7	R/W	MTRK	0
Bit 6	R/W	FPATINV	0
Bit 5	R/W	SPLRINV	0
Bit 4	R/W	SPATINV	0
Bit 3	R/W	REMAIS	0
Bit 2	R/W	MFAIS	0
Bit 1	R/W	TS16AIS	0
Bit 0	R/W	AIS	0

MTRK:

The MTRK bit forces trunk conditioning (i.e., idle code substitution and signaling substitution) when MTRK is a logic 1. This has the same effect as setting data substitution to IDLE code on time slots 1-15 and 17-31 (setting bits SUBS and DS[0] to binary 10 in time slots 1-15 and 17-31) and sourcing the signaling data from the TPCSC stream, if SIGEN is logic 1. When SIGEN is logic 0, TS16 will be treated the same as time slots 1-15 and 17-31 and will contain data sourced from TIDL. TS0 data is determined by the control bits associated with it and is independent of the value of MTRK.

FPATINV:

The FPATINV bit is a diagnostic control bit. When set to logic 1, FPATINV forces the frame alignment signal (FAS) written into TS0 to be inverted (i.e., the correct FAS, 0011011, is substituted with 1100100); when set to logic 0, the FAS is unchanged.

SPLRINV:

The SPLRINV bit is a diagnostic control bit. When set to logic 1, SPLRINV forces the "spoiler bit" written into bit 2 of TS0 of NFAS frames to be inverted (i.e., the spoiler bit is forced to 0); when set to logic 0, the spoiler bit is unchanged.

SPATINV:

The SPATINV bit is a diagnostic control bit. When set to logic 1, SPATINV forces the signaling multiframe alignment signal written into bits 1-4 of TS16

of frame 0 of the signaling multiframe to be inverted (i.e., the correct signaling multiframe alignment signal, 0000, is substituted with 1111); when set to logic 0, the signaling multiframe alignment signal is unchanged.

REMAIS:

The REMAIS bit controls the transmission of the remote Alarm Indication Signal. A logic 1 in the REMAIS bit position causes bit 3 of NFAS frames to be forced to logic 1; otherwise, bit 3 of NFAS frames is a logic 0.

MFAIS:

The MFAIS bit controls the transmission of the signaling multiframe Alarm Indication Signal. A logic 1 in the MFAIS bit position causes the y-bit (bit 6) of TS16 of frame 0 of the signaling multiframe to be forced to logic 1; otherwise, the y-bit is a logic 0.

TS16AIS:

The TS16AIS bit controls the transmission of the Time Slot 16 Alarm Indication Signal (all-ones in TS16). A logic 1 in the TS16AIS bit position forces TS16 of all frames in the output stream to logic 1.

AIS:

The AIS bit controls the transmission of the Alarm Indication Signal (unframed all-ones). A logic 1 in the AIS bit position forces the output streams to logic 1.

When the EQUAD is reset, the contents of this register are set to logic 0.

Register 046H, 0C6H, 146H, 1C6H: TRAN International/National Control

Bit	Type	Function	Default
Bit 7	R/W	Si[1]	1
Bit 6	R/W	Si[0]	1
Bit 5		Unused	X
Bit 4	R/W	Sn[4]	1
Bit 3	R/W	Sn[3]	1
Bit 2	R/W	Sn[2]	1
Bit 1	R/W	Sn[1]	1
Bit 0	R/W	Sn[0]	1

Sn[4:0]:

Bits 4 to 0 of this register are substituted in bit positions 4 to 8, respectively, of TS0 of each NFAS frame when framing generation (FDIS = 0) and International/National bit control (INDIS = 0) is enabled. When FDIS or INDIS is logic 1, the contents of this register are ignored and replaced with the values received on the BTPCM[x] input.

The bits Sn[4:0] correspond to the 5 National bits; these can be programmed to any value and are inserted into the National bit positions in the NFAS frames when enabled by INDIS.

Si[1:0]:

The bits Si[1] and Si[0] correspond to the International bits. The Si[1] and Si[0] bits can be programmed to any value and will be inserted into bit 1 of each FAS frame and NFAS frame, respectively, when the block is configured for frame generation, INDIS is set to logic 0, and CRC multiframe generation is disabled. When CRC multiframe generation is enabled, both Si[1] and Si[0] are ignored if FEBE indication is enabled; if FEBEDIS is a logic 1 and INDIS = 0, the values programmed in the Si[1] and Si[0] bit positions are inserted into the spare bit locations of frame 13 and frame 15, respectively, of the CRC multiframe. If both FEBEDIS and INDIS are logic 1, then data from BTPCM[x] replaces the Si[0] and Si[1] bits in the CRC multiframe.

The Si[1], Si[0], and Sn[4:0] bits should be programmed to a logic 1 when not being used to carry information.

When the EQUAD is reset, the contents of the register are set to logic 1.

Register 047H, 0C7H, 147H, 1C7H: TRAN Extra Bits Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	X[1]	1
Bit 2		Unused	X
Bit 1	R/W	X[3]	1
Bit 0	R/W	X[4]	1

X[4:3,1]:

The X[1], X[3], and X[4] bits control the value programmed in the X[1], X[3], and X[4] bit locations (bits 5,7, and 8) in TS16 of frame 0 of the signaling multiframe, when enabled by XDIS. The X[1], X[3], and X[4] bits should be programmed to a logic 1 when not being used to carry information.

When the EQUAD is reset, the contents of the register are set to logic 1.

Register 048H, 0C8H, 148H, 1C8H: PMON Control/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	XFER	0
Bit 0	R	OVR	0

This register contains status information indicating when counter data has been transferred into holding registers and indicating whether the holding registers have been overrun. Configuration for PMON interrupt enable is also available in this register.

INTE:

The INTE bit controls the generation of a microprocessor interrupt when the transfer clock has caused the counter values to be stored in the holding registers. A logic 1 bit in the INTE position enables the generation of an interrupt ; a logic 0 bit in the INTE position disables the generation of an interrupt.

XFER:

The XFER bit indicates that a transfer of counter data has occurred. A logic 1 in this bit position indicates that a latch request, initiated by writing to one of the counter register locations, was received and a transfer of the counter has occurred. A logic 0 indicates that no transfer has occurred. The XFER bit is cleared (acknowledged) by reading this register.

OVR:

The OVR bit is the overrun status of the holding registers. A logic 1 in this bit position indicates that a previous interrupt has not been acknowledged before the next transfer clock has been issued and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. The OVR bit is cleared by reading this register.

10.2 Registers 049-04FH, 0C9H-0CFH, 149H-14FH, 1C9H-1CFH: Latching Performance Data

All the Performance Data registers in one framer are updated as a group by writing to any of the PMON block count registers (addresses 049H-04FH for framer 1, 0C9H-0CFH for framer 2, 149H-14FH for framer 3, and 1C9H-1CFH for framer 4). A write to any one of these locations loads performance data in the associated PMON block into the internal holding registers (it is necessary to write to one, and only one, count register address to latch all the count data register values into the holding registers and to reset all the counters for each polling cycle for the associated framer). Alternately, the Performance Data registers for all four framers are updated by writing to the Revision/Chip ID/Global PMON Update register (address 00CH). The data contained in the holding registers can then be subsequently read by microprocessor accesses into the PMON block count register address space. The latching of count data, and subsequent resetting of the counters, is synchronized to the internal event timing so that no events are missed.

The PMON is loaded with new performance data within 3.5 recovered clock periods of the latch performance data register write. With nominal line rates, the PMON registers should not be polled until 1.71µsec have elapsed from the "latch performance data" register write.

When the EQUAD is reset, the contents of the PMON count registers are unknown until the first latching of performance data is performed.

Register 049H, 0C9H, 149H, 1C9H: Framing Bit Error Count

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	FER[6]	X
Bit 5	R	FER[5]	X
Bit 4	R	FER[4]	X
Bit 3	R	FER[3]	X
Bit 2	R	FER[2]	X
Bit 1	R	FER[1]	X
Bit 0	R	FER[0]	X

This register indicates the number of framing bit error events that occurred during the previous accumulation interval. The FER counts are suppressed when the FRMR has lost frame alignment (OOF in the FRMR Framing Status register is set).

Register 04AH, 0CAH, 14AH, 1CAH: Far End Block Error Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 04BH, 0CBH, 14BH, 1CBH: Far End Block Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

These registers indicate the number of far end block error events that occurred during the previous accumulation interval. The FEBE counts are suppressed when the FRMR has lost frame alignment (OOF in the FRMR Framing Status register is set).

Register 04CH, 0CCH, 14CH, 1CCH: CRC Error Count LSB

Bit	Type	Function	Default
Bit 7	R	CRCE[7]	X
Bit 6	R	CRCE[6]	X
Bit 5	R	CRCE[5]	X
Bit 4	R	CRCE[4]	X
Bit 3	R	CRCE[3]	X
Bit 2	R	CRCE[2]	X
Bit 1	R	CRCE[1]	X
Bit 0	R	CRCE[0]	X

Register 04DH, 0CDH, 14DH, 1CDH: CRC Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	CRCE[9]	X
Bit 0	R	CRCE[8]	X

These registers indicate the number of CRC error events that occurred during the previous accumulation interval. CRC error events are suppressed when the FRMR is out of CRC-4 multiframe alignment (OOCMF bit in the FRMR Framing Status register is set).

Register 04EH, 0CEH, 14EH, 1CEH: Line Code Violation Count LSB

Bit	Type	Function	Default
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

Register 04FH, 0CFH, 14FH, 1CFH: Line Code Violation Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	LCV[12]	X
Bit 3	R	LCV[11]	X
Bit 2	R	LCV[10]	X
Bit 1	R	LCV[9]	X
Bit 0	R	LCV[8]	X

These registers indicate the number of LCV error events that occurred during the previous accumulation interval. An LCV event is defined as the occurrence of a Bipolar Violation or Excessive Zeros. The counting of Excessive Zeros can be disabled by the BPV bit of the Receive Interface Configuration register.

11 TEST FEATURES DESCRIPTION

Simultaneously asserting the CSB, RDB and WRB inputs causes all output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the EQUAD. Test mode registers (as opposed to normal mode registers) are mapped into addresses 200H-3FFH.

Test mode registers may also be used for board testing. When all of the constituent Telecom System Blocks within the EQUAD are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. Reading unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. Writeable test mode register bits are not initialized upon reset unless otherwise noted.

11.1 Test Mode 0

In test mode 0, the EQUAD allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface.

To enable test mode 0, the IOTST bit in the Test Mode Select Register is set to logic 1 and the following addresses must be written with 00H: 211H, 219H, 21DH, 221H, 231H, 235H, 239H, 241H, 245H, 291H, 299H, 29DH, 2A1H, 2B1H, 2B5H, 2B9H, 2C1H, 2C5H, 311H, 319H, 31DH, 321H, 331H, 335H, 339H, 341H, 345H, 391H, 399H, 39DH, 3A1H, 3B1H, 3B5H, 3B9H, 3C1H, and 3C5H. Also, to enable input and output signals to propagate through the interface blocks, the value 00H must be written to addresses 001H, 002H, 003H, 004H, 081H, 082H, 083H, 084H, 101H, 102H, 103H, 104H, 181H, 182H, 183H, and 184H. The value 02H must be written to addresses 007H, 087H, 107H, and 187H.

Reading the following address locations returns the values for the indicated inputs :

Table 4 -

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
210H				RDP[1]	RDN[1]	RCLKI[1]		
218H				XCLK	TCLKI[1]			
21CH	BRFPI	BRCLK						
244H	[1]	BTPCM			BTSIG[1]			TDLSIG[1]
246H				MENB	BTFP[1]			BTCLK[1]
290H					RDP[2]	RDN[2]	RCLKI[2]	
298H					XCLK	TCLKI[2]		
29CH	BRFPI	BRCLK						
2C4H		BTPCM[2]			BTSIG[2]			TDLSIG[2]
2C6H				MENB	BTFP[2]			BTCLK[2]
310H					RDP[3]	RDN[3]	RCLKI[3]	
318H					XCLK	TCLKI[3]		
31CH	BRFPI	BRCLK						
344H		BTPCM[3]			BTSIG[3]			TDLSIG[3]
346H				MENB	BTFP[3]			BTCLK[3]
390H					RDP[4]	RDN[4]	RCLKI[4]	
398H					XCLK	TCLKI[4]		
39CH	BRFPI	BRCLK						
3C4H		BTPCM[4]			BTSIG[4]			TDLSIG[4]
3C6H				MENB	BTFP[4]			BTCLK[4]

Writing the following address locations forces the outputs to the value in the corresponding bit position:

Table 5 -

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
210H		INTB[1]						RCLKO[1]
212H							BRPCM[1], MRD	BRSIG[1]
218H	INTB[1]					TCLKO[1]	TDN[1]	TDP[1]
21CH		INTB[1]						
220H					RFP[1]			
223H								INTB[1]

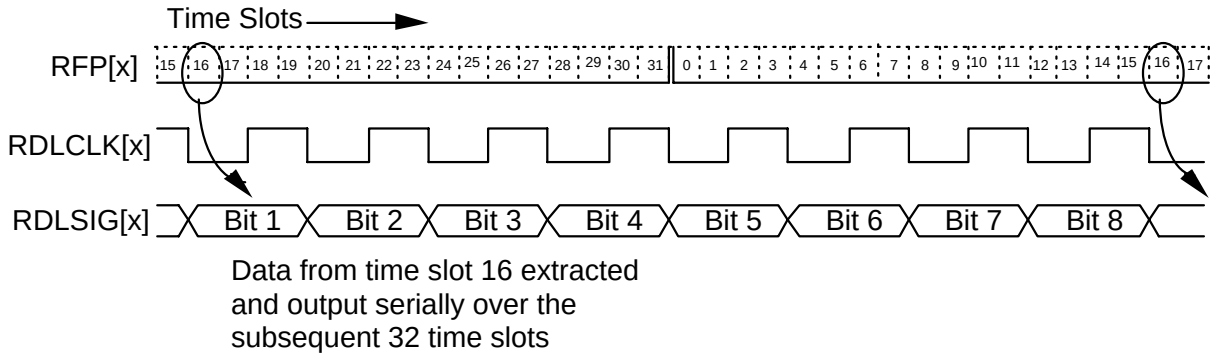
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
238H							RDLCLK[1]	RDLSIG[1]
240H					BRFPO[1]			
244H								TDLCLK[1]
290H		INTB[1]						RCLKO[2]
292H							BRPCM[2]	BRSIG[2]
298H	INTB[1]					TCLKO[2]	TDN[2]	TDP[2]
29CH		INTB[1]						
2A0H					RFP[2]			
2A3H								INTB[1]
2B8H							RDLCLK[2]	RDLSIG[2]
2C0H					BRFPO[2]			
2C4H								TDLCLK[2]
310H		INTB[1]						RCLKO[3]
312H							BRPCM[3]	BRSIG[3]
318H	INTB[1]					TCLKO[3]	TDN[3]	TDP[3]
31CH		INTB[1]						
320H					RFP[3]			
323H								INTB[1]
338H							RDLCLK[3]	RDLSIG[3]
340H					BRFPO[3]			
344H								TDLCLK[3]
390H		INTB[1]						RCLKO[4]
392H							BRPCM[4]	BRSIG[4]
398H	INTB[1]					TCLKO[4]	TDN[4]	TDP[4]
39CH		INTB[1]						
3A0H					RFP[4]			
3A3H								INTB[1]
3B8H							RDLCLK[4]	RDLSIG[4]
3C0H					BRFPO[4]			
3C4H								TDLCLK[4]

Notes:

1. Writing a logic 1 to any of the block interrupt signals asserts the INTB output low.

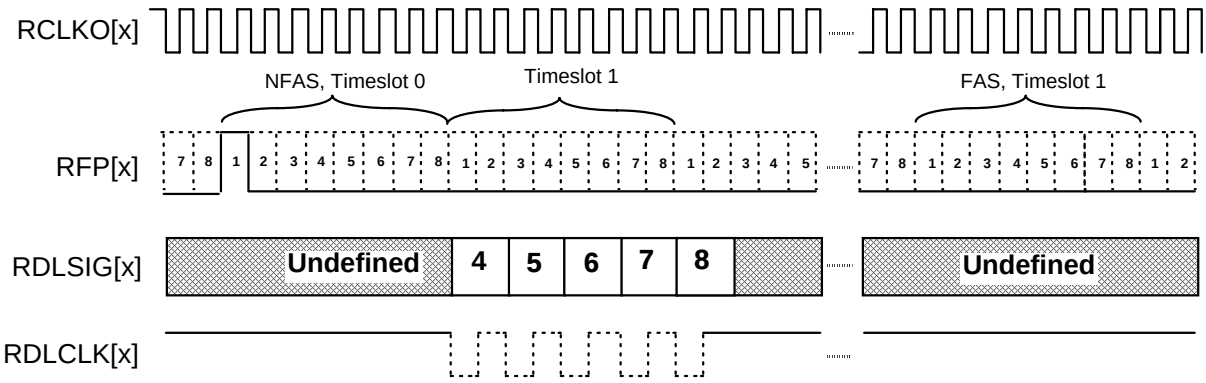
12 FUNCTIONAL TIMING

Figure 9 - TS16 Receive Datalink Interface



When TS16 is selected as the source of the receive datalink (RXDMASIG=0 and all of RXSAxEN=0), the 64 kbit/s TS16 data is presented on RDLSIG[x] with an accompanying RDLCLK[x] with a period of 4 time slots. The data on RDLSIG[x] is generated on the falling edge of RDLCLK[x]. For the RFP timing shown above, the SRSMFP and SRCMFP register bits are set to logic 0.

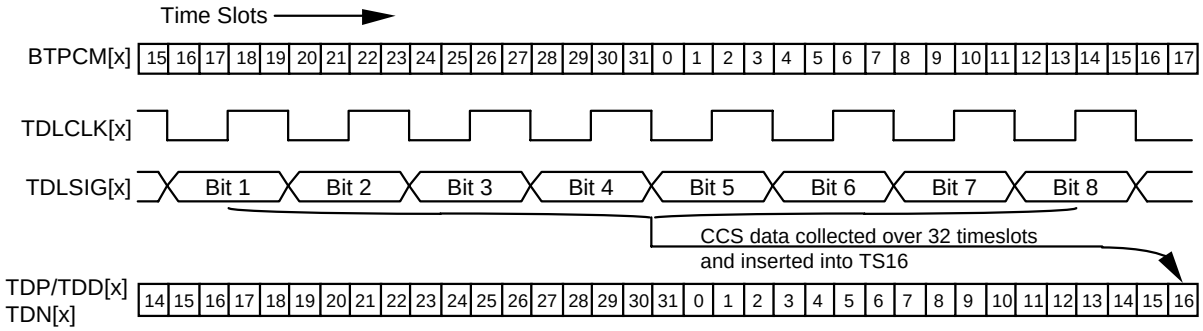
Figure 10 - TS0 Receive Datalink Interface



When TS0 is selected as the source of the receive datalink (RXDMASIG=0 and at least one RXSAxEN bit is a logic 1), the National Use bit of TS0 of the NFAS frames data is presented on RDLSIG[x] with an accompanying RDLCLK[x]. A clock pulse is generated on RDLCLK[x] for each National Use bit on RDLSIG[x] which has the associated enable (RXSAxEN, x=4 to 8) set to logic 1. Depending on the settings of the RXSAxEN bits, the effective bit rate of the data link may

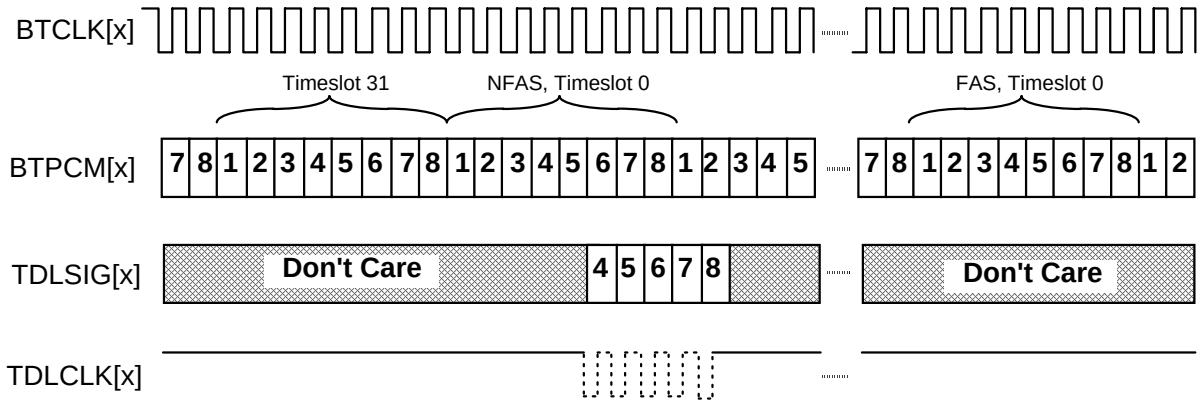
range between 4 bit/s and 20 kbit/s. RDLSIG[x] is generated on the falling edge of RDLCLK[x]. For the diagram shown above, the SRSMFP and SRCMFP register bits are set to logic 0. The timing with respect to RCLKO[x] shown here is valid only if the RCLKOSEL bit is set to logic 0.

Figure 11 - TS16 Transmit Datalink Interface



When Common Channel Signaling (CCS) data sourced from TDLSIG[x] is selected (DLEN=1, SIGEN=0 and TXDMASIG=0), TDLCLK[x] is active, producing one cycle every 4 time slots, aligned to the incoming BTPCM[x]. The data on TDLSIG[x] is sampled on the rising edge of TDLCLK[x] and put directly into TS16 on the outgoing data stream.

Figure 12 - TS0 Transmit Datalink Interface

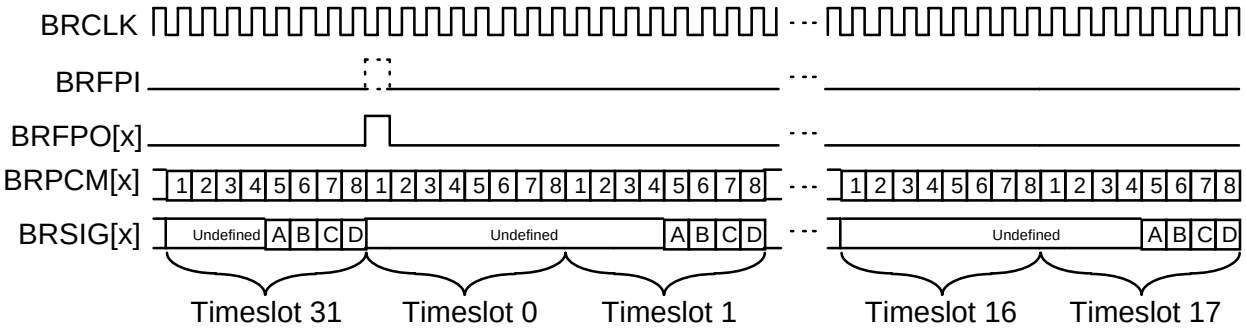


When the TS0 maintenance datalink is active (DLEN=0 or SIGEN=1, TXDMASIG=0, at least one TXSAxEN bit is a logic 1), the data presented on TDLSIG[x] is inserted into the National Use bits of the NFAS frames. A clock pulse is generated on TDLCLK[x] for each National Use bit on TDLSIG[x] which has the associated enable (TXSAxEN, x=4 to 8) set to logic 1. If the enable is

logic 0, the specific bit value is sourced from the TRAN block International/National Control register. Depending on the settings of the TXSAxEN bits, the effective bit rate of the data link may range between 4 bit/s and 20 kbit/s. TDLSIG[x] is sampled on the rising edge of TDLCLK[x]. Note that the TDLSIG[x] data is shifted from the corresponding BTPCM[x] data by 2 bits.

12.1 Receive Backplane Interface

Figure 13 - ROHM=0, BRX2RAIL=0, BRXSMFP=0 and BRXCMFP=0



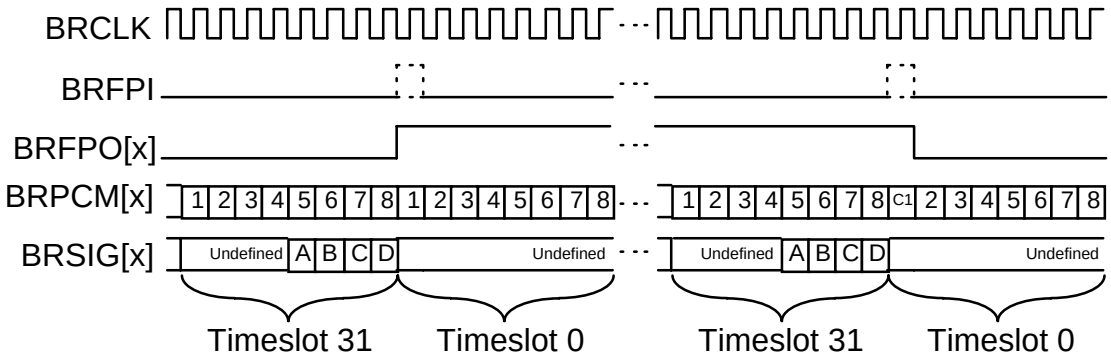
The Receive Backplane is configured to generate 2048 kbit/s, single-rail formatted data with frame alignment indication. The Receive Backplane Options register is programmed to BRX2RAIL=0, BRXSMFP=0 and BRXCMFP=0.

The BRFPI input pulse need not exist every frame; only one is required to align the backplane signals. If no BRFPI pulse has been presented since reset, the outputs will assume an arbitrary alignment.

If ROHM=0, BRXSMFP=0 and BRXCMFP=1, the BRFPO[x] signal pulses high only during the first bit of the first frame in the CRC multiframe.

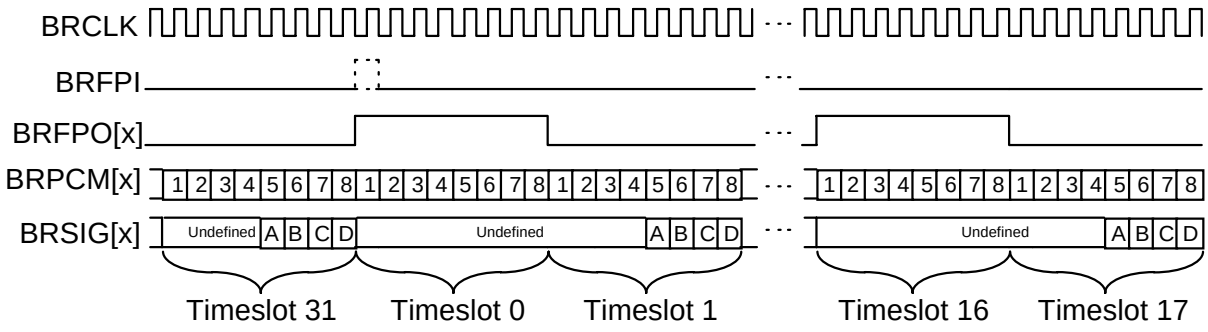
If ROHM=0, BRXSMFP=1 and BRXCMFP=0, the BRFPO[x] signal pulses high only during the first bit of the frame containing the signaling multiframe alignment signal.

Figure 14 - Receive composite multiframe output (BRXSMFP=1 and BRXCMFP=1)



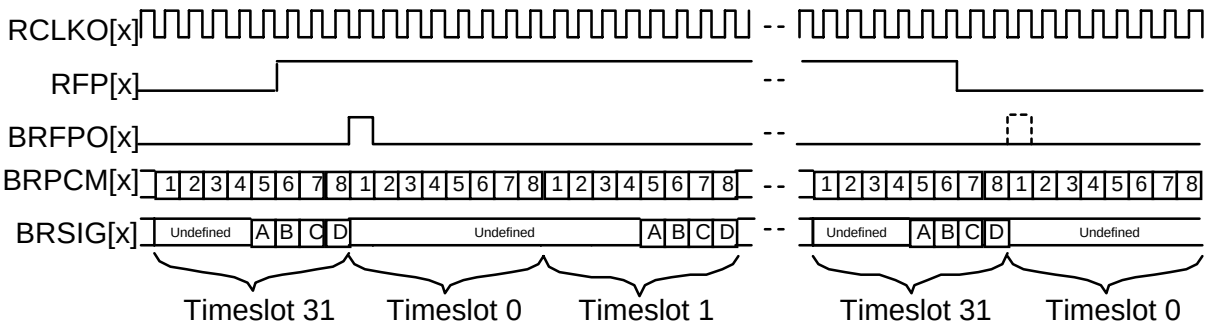
If ROHM=0, BRXSMFP=1 and BRXCMFP=1, the BRFPO[x] signal becomes high on the falling BRCLK edge marking the beginning of bit 1 of frame 1 of every 16 frame signaling multiframe and returns low on the falling BRCLK edge marking the end of bit 1 of frame 1 of every 16 frame CRC multiframe.

Figure 15 - Receive overhead output (ROHM=1)



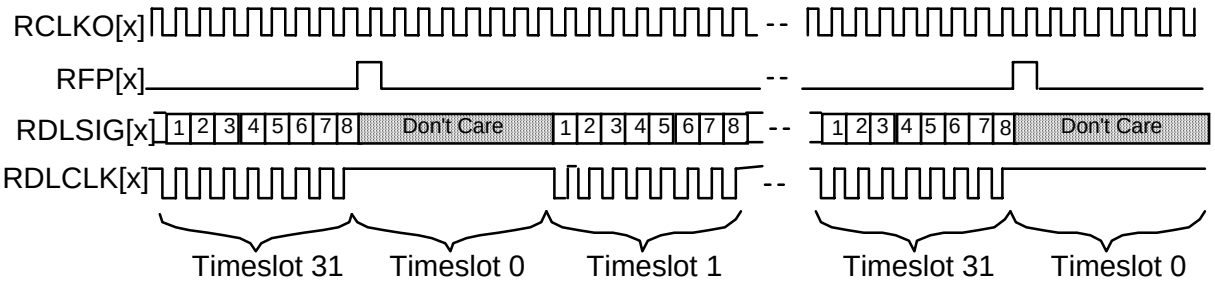
If the ROHM bit is logic 1, the BRFPO[x] signal marks the overhead by becoming high during timeslots 0 and 16, as in Figure 15.

Figure 16 - ELSTBYP=1, SRSMFP=1, SRCMFP=1, BRXSMFP=1, BRXCMFP=0



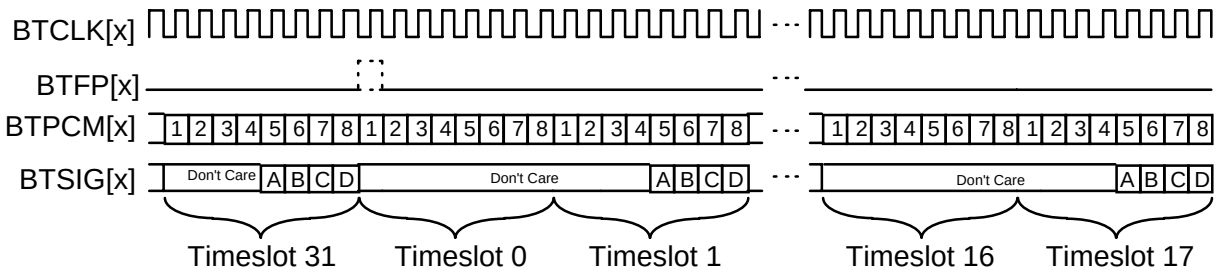
The Receive Backplane is configured to generate single-rail formatted data with frame alignment indication and with the ELST bypassed (ELSTBYP=1). The Receive Options register is programmed to SRSMFP=1 and SRCMFP=1, the Receive Backplane Options register is programmed to BRXSMFP=1 and BRXCMFP=0. In this case, the backplane output signals are timed off of the output clock RCLKO[x] instead of the input clock BRCLK. RFP marks (though offset by 3 bits) the start of each signaling multiframe, and the start of each CRC multiframe.

Figure 17 - Receive Channel Interface



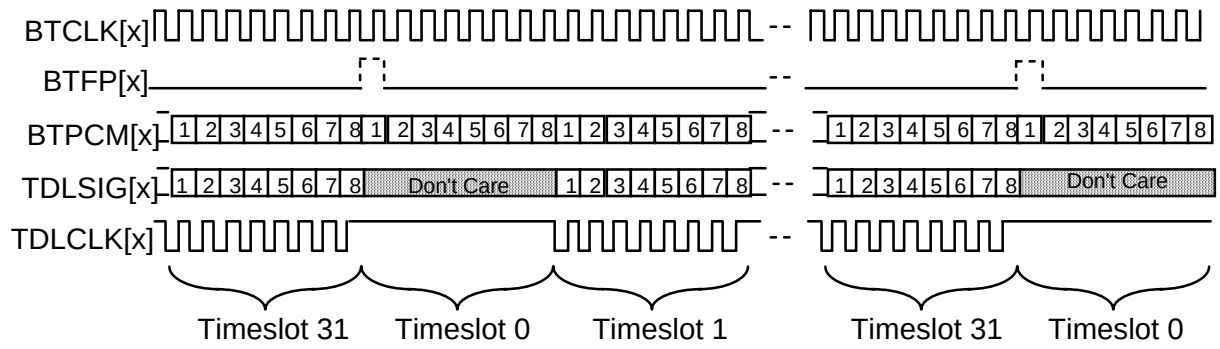
The RFRACE1 bit in the Datalink Options register is set to logic 1. The CH[1] and CH[31] register bits in the Channel Select registers are set to logic 1 and the CH[0] register bit is set to logic 0. Channels 1 and 31 are presented on RDLSIG[x]. RDLCLK[x] is gapped so that it is only active for the channels with the associated CH[x] bit set. As shown here, the SRCMFP and SRSMFP bits in the Receive Options register are set to logic 0.

Figure 18 - Transmit Backplane Interface



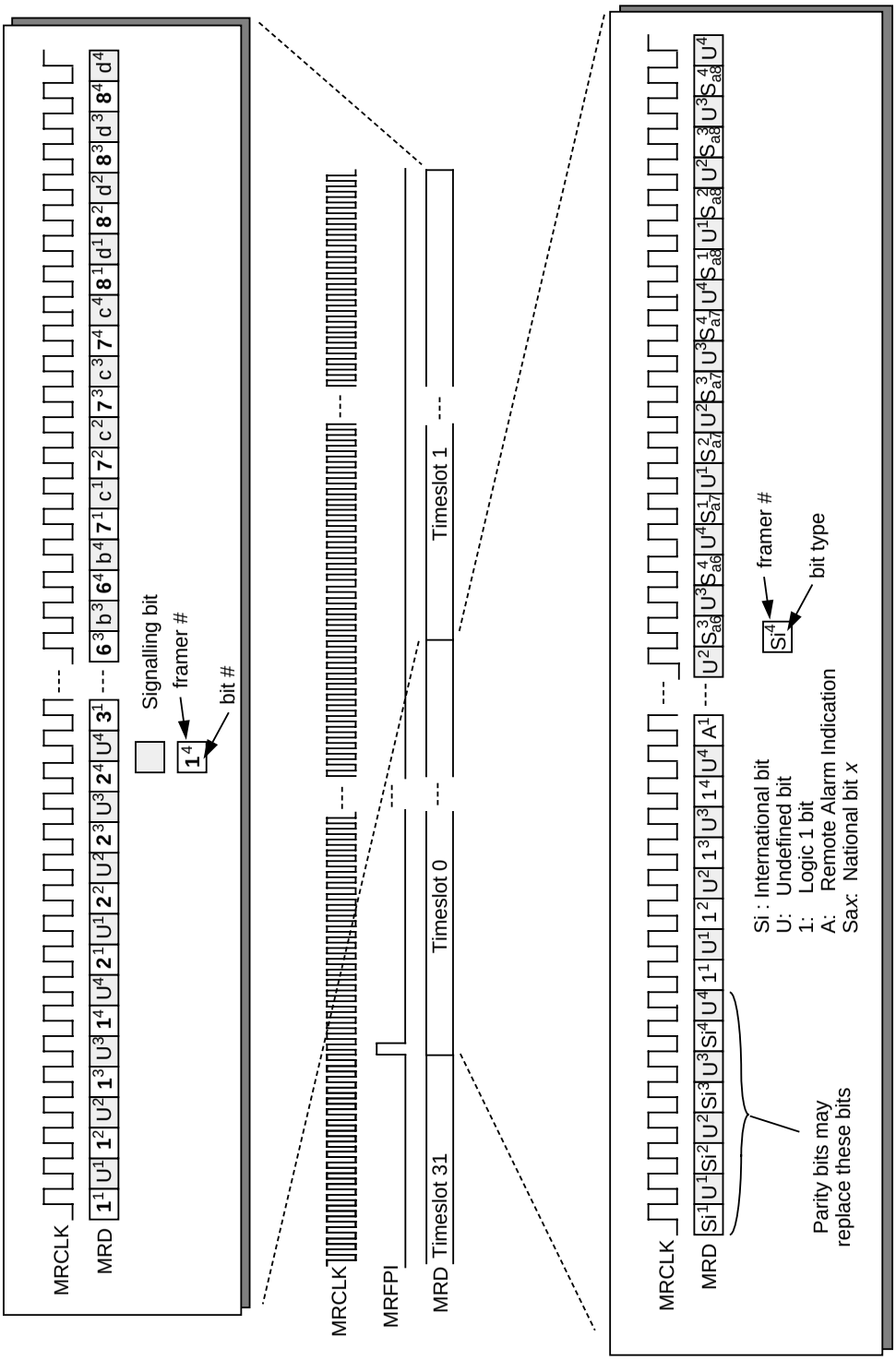
The Transmit Backplane is configured to receive 2048 kbit/s, single-rail formatted data with frame alignment indication. The Transmit Backplane Options register is programmed to BTXCLK=0, BTX2RAIL=0, BTXMFP=0. (If BTXMFP=1, the BTFP[x] input must be brought high to mark bit 1 of frame 1 of every 16 frame signaling multiframe and brought low following bit 1 of frame 1 of every 16 frame CRC multiframe. This mode allows both multiframe alignments to be independently controlled using the single BTFP[x] signal. Note that if the signaling and CRC multiframe alignments are coincident, BTFP[x] must pulse high for 1 BTCLK[x] cycle every 16 frames.

Figure 19 - Transmit Channel Interface



The TFRACE1 bit in the Datalink Options register is set to logic 1. The CH[1] and CH[31] register bits in the Channel Select registers are set to logic 1 and the CH[0] register bit is set to logic 0. TDLCLK[x] is gapped so that it is only active for the channels with the associated CH[x] bit set. Data for channels 1 and 31 are expected on TDLSIG[x].

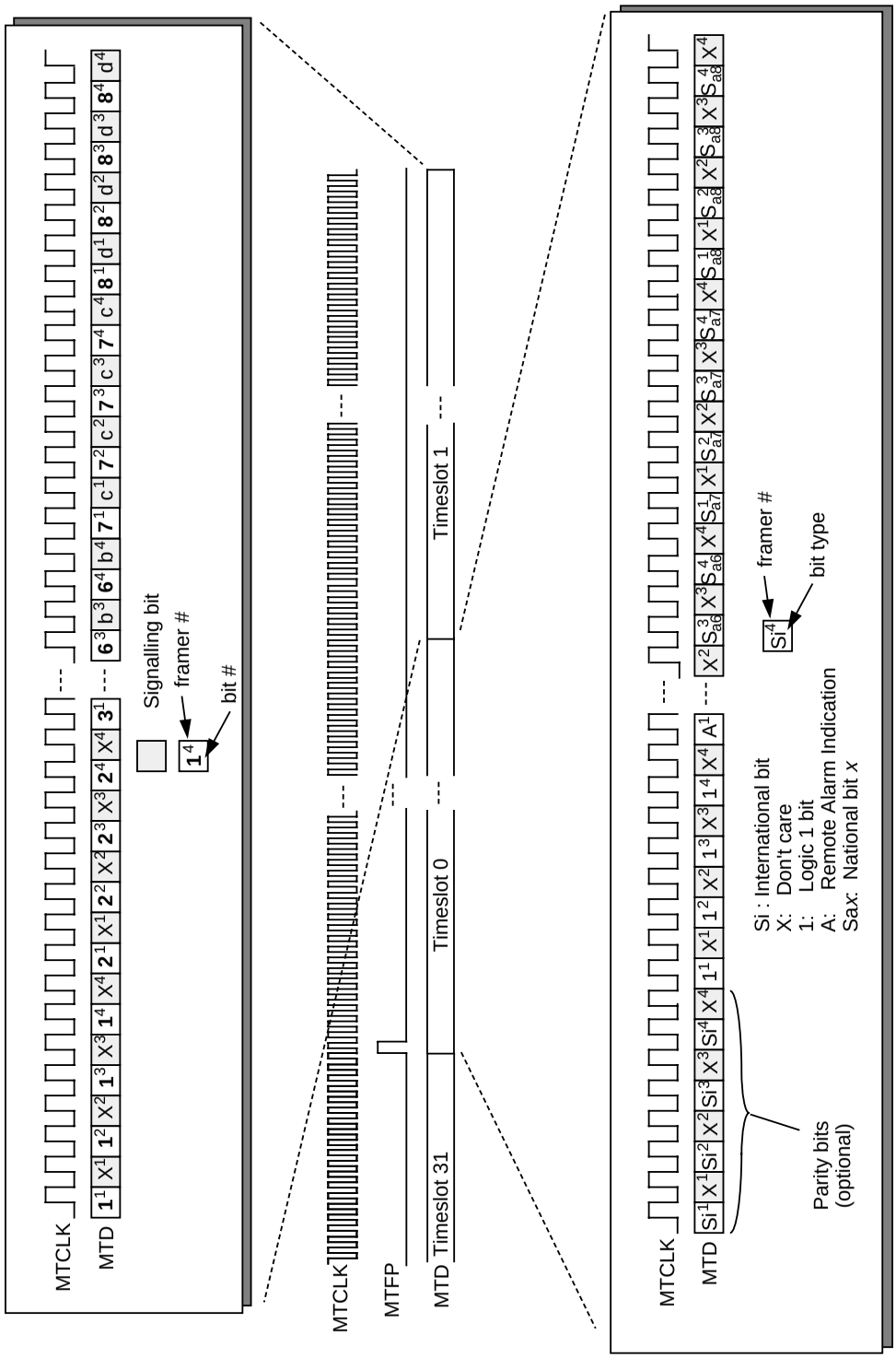
Figure 20 - Multiplexed Receive Backplane Interface



The Receive Backplane is configured to generate bit interleaved 16.384MHz data. PCM and signaling for all four receivers are presented on a single pin, MRD. The superscripts represent the index of the particular E1 stream. The Receive Backplane Options register for each receiver is programmed to BRX2RAIL=0 and the MENB input is low. The preceding figure shows the expected outputs if all four E1 framers are outputting NFAS frames.

If the BRPTYPE bit in the Backplane Parity Configuration and Status register is set to logic 1, the backplane receive parity is enabled. The International bit (Si bit) of the PCM data stream in each frame is replaced by the parity value calculated over the previous frame (not counting the parity bit of the previous frame). The parity bit of each SIG stream follows the parity bit of the PCM data stream.

Figure 21 - Multiplexed Transmit Backplane Interface



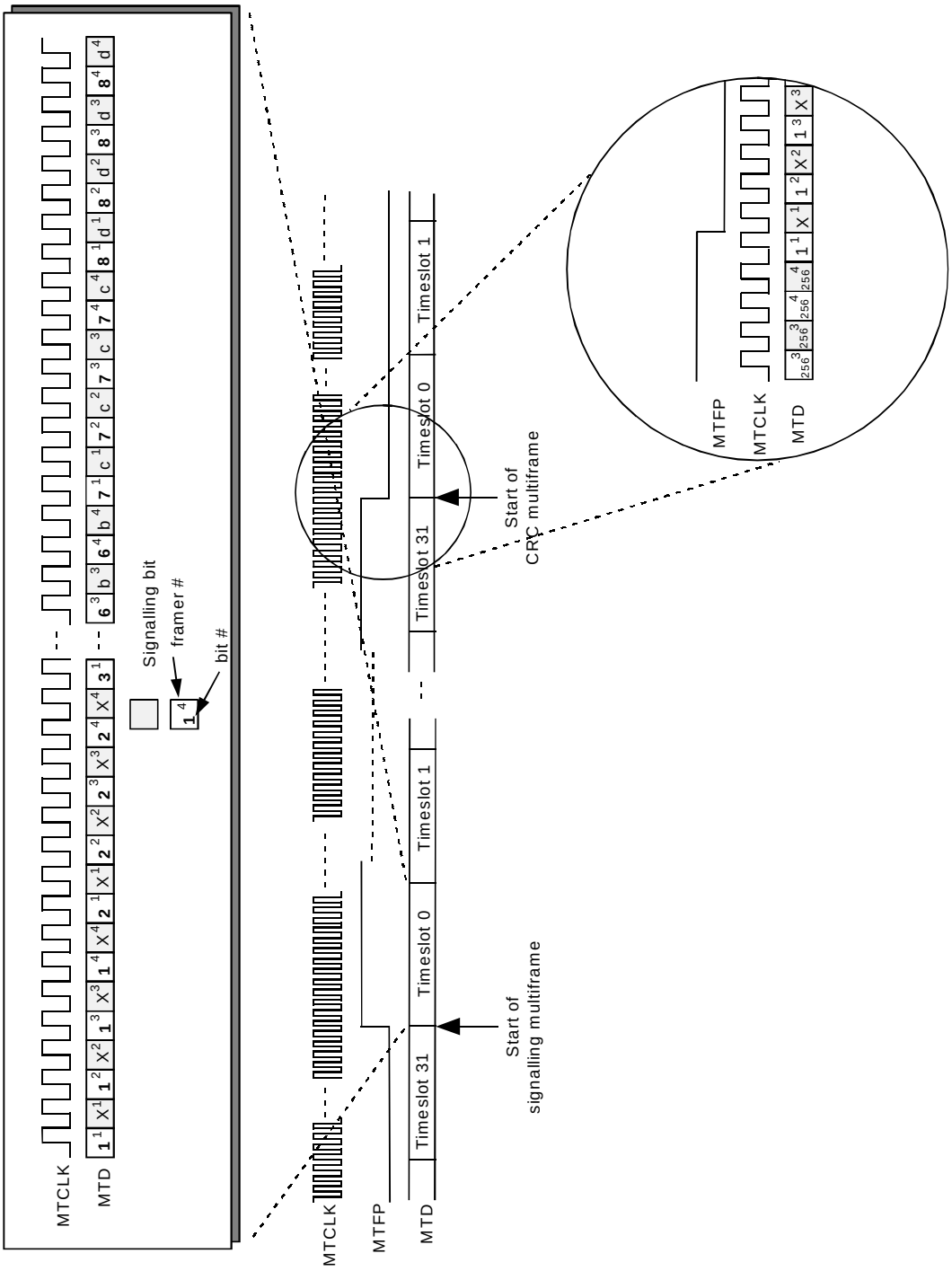
The Transmit Backplane is configured to expect bit interleaved 16.384MHz data. PCM and signaling for all four receivers are presented on a single pin, MTD. The superscripts represent the index of the particular E1 stream. The Transmit Backplane Options register for each receiver is programmed with BRX2RAIL=0. For input frame pulses shown in the preceding figure, BTXMFP=0. The MENB input is low.

Note that in normal operation, where the TRAN block inserts all the TS0 overhead, the PCM inputs on MTD are "don't cares" for TS0 and TS16. The preceding diagram shows the TS0 bits for timing reference purposes only.

If the backplane transmit parity is enabled, the International bit (Si bit) position of the PCM data stream in each frame should contain the PCM parity bit. The parity bit of each SIG stream follows the parity bit of the PCM data stream.

In the case where MENB=0 and BTXMFP=1, the input MTFP marks the start of the signaling multiframe and the start of the CRC multiframe as described in the description of the Transmit Backplane Options register. The waveforms for this case are shown in Fig. 21.

Figure 22 - Multiplexed Transmit Backplane Interface with BTXMFP=1



13 OPERATION

After a system reset (either via the RSTB pin or via the RESET register bit), the EQUAD will default to the following settings:

Table 6 - Configuring the EQUAD from Reset

Setting	Receiver Section	Transmitter Section
Framing Format	Basic G.704 without CRC multiframe. Channel Associated Signaling is enabled.	Basic G.704 without CRC multiframe. Channel Associated Signaling is enabled.
Line Code	HDB3	HDB3
E1 interface	• Pins RDP/RDD[x] and RDN/RLCV[x] active as digital inputs RDP[x] and RDN[x]	• TDP[x], TDN[x] outputs NRZ data updated on falling TCLKO[x] edge
System Backplane	• BRPCM[x], BRSIG[x] active • BRFPO[x] indicates frame pulses	• BTPCM[x] active • BTSIG[x] inactive • BTFP[x] indicates frame alignment
Data Link	• internal RFDL disabled • RDLSIG[x] and RDLCLK[x] outputs present the Sa4 bit of TS0.	• internal XFDL disabled • TDLCLK[x] output, TDLSIG[x] input inserted into Sa4 bit of TS0.
Options	• ELST not bypassed • RFP[x] indicates frame pulses	•
Timing Options	Not applicable	• Digital jitter attenuation enabled, with TCLKO[x] referenced to BTCLK[x]
Diagnostics	• All diagnostic modes disabled	• All diagnostic modes disabled

13.1 Using the Internal FDL Transmitter

Upon reset of the EQUAD, the XFDL should be disabled by setting the EN bit in the XFDL Configuration Register to logic 0. If data is not ready to be transmitted, the TDLINT[x] output should also be masked by setting the INTE bit to logic 0.

When using the internal HDLC transmitter, the XFDL Configuration Register should be initialized for transmission: if the FCS is desired, the CRC bit should be set to logic 1; if the block is to be used in interrupt driven mode, interrupts should be enabled by setting the INTE bit to logic 1. Finally, the XFDL can be enabled by setting the EN bit to logic 1. If no message is sent after the EN bit is set to logic 1, continuous flags will be sent.

The XFDL can be used in a polled, interrupt driven, or DMA-controlled mode for the transfer of frame data. In the polled mode, the TDLINT[x] and TDLUDR[x] outputs of the XFDL are not used, and the processor controlling the XFDL must periodically read the XFDL Status Register to determine when to write to the XFDL Transmit Data Register. In the interrupt driven mode, the processor controlling the XFDL uses either the TDLINT[x] output, or the main processor INTB output and the interrupt source registers, to determine when to write to the XFDL Transmit Data Register. In the DMA controlled mode, the TDLINT[x] output of the XFDL is used as a DMA request input to the DMA controller, and the TDLUDR[x] output is used as an interrupt to the processor to allow handling of exceptions. The TDLUDR[x] output can also be enabled to generate a processor interrupt through the common INTB output via the TDLUDRE bit in the Datalink Options register.

Polled Mode

If the XFDL data transfer is operating in the polled mode (TXDMASIG, TFRACE1, TDLINTE, and TDLUDRE bits in the Datalink Options Register are set to logic 0), then a timer periodically starts up a service routine, which should process data as follows:

1. Read the XFDL Interrupt Status Register and poll the UDR and INT bits.

2. If UDR=1, then clear the UDR bit in the XFDL Interrupt Status Register to logic 0, and restart the current frame. Go to step 1.

3. If INT=1, then:

   a) If there is still data to send, then write the next data byte to the XFDL Transmit Data Register;

b) If all bytes in the frame have been sent, then set the EOM bit in the XFDL Configuration Register to logic 1.

4. If EOM bit was set to logic 1 in step 3b, then:

   a) Read the XFDL Interrupt Status Register and check the UDR bit.

   b) If UDR=1 then reset the UDR bit in the XFDL Interrupt Status Register and the EOM bit in the XFDL Configuration Register to logic 0, and retransmit the last frame.

5. Go to step 1.

Interrupt Mode

In the case of interrupt driven data transfer, the TDLINT[x] output is connected to the interrupt input of the processor, and the interrupt service routine should process the data exactly as described above for the polled mode. The INTE bit in the XFDL Configuration Register must be set to logic 1. Alternately, the INTB output can be connected to the interrupt input of the processor if the TDLINTE bit of the Datalink Options Register is set to logic 1. If this mode is used, additional polling of the Interrupt ID/Clock Monitor and Master Interrupt Source registers must be performed to identify the cause of the interrupt before the initiating the interrupt service routine.

DMA-Controlled Mode

The XFDL can also be used with a DMA controller to process the frame data. In this case, the TDLUDR[x] output is connected to the processor interrupt input. The TDLINT[x] output of the XFDL is connected to the DMA request input of the DMA controller. The INTE bit in the XFDL Configuration Register must be set to logic 1 before enabling the XFDL. The DMA controller writes a data byte to the XFDL whenever the TDLINT[x] output is high. If there is a problem during transmission and an underrun condition occurs, then the TDLUDR[x] output goes high and the processor is interrupted. The processor can then halt the DMA controller, reset the UDR bit in the XFDL Interrupt Status Register, reset the frame data pointers, and restart the DMA controller to resend the data frame. After the message transmission is completed, the DMA controller must initiate a write to set the EOM bit in the XFDL Configuration Register and then verify that TDLUDR[x] is not set prior to setting EOM.

13.2 Using the Internal FDL Receiver

On power up of the EQUAD, the RFDL should be disabled by setting the EN bit in the Configuration Register to logic 0. The RFDL Interrupt Control/Status Register should then be initialized to select the FIFO buffer fill level at which an interrupt will be generated.

After the Interrupt Control/Status Register has been written to, the RFDL can be enabled at any time by setting the EN bit in the Configuration Register to logic 1. When the RFDL is enabled, it will assume that the link status is idle (all ones) and immediately begin searching for flags. When the first flag is found, an interrupt will be generated (if enabled), and the byte received before the first flag was detected will be written into the FIFO buffer. Because the FLG and EOM bits are passed through the buffer, this dummy write allows the RFDL Status Register to accurately reflect the current state of the data link. A RFDL Status Register read after a RFDL Data Register read of the dummy byte will return EOM as logic 1 and FLG as logic 1. The first interrupt and data byte read after the RFDL is enabled (or TR bit set to logic 1) is an indication of the link status, and the data byte should therefore be discarded. It is up to the controlling processor to keep track of the link state as idle (all ones or bit-oriented messages active) or active (flags received).

The RFDL can be used in a polled, interrupt driven, or DMA controlled mode for the transfer of frame data.

Polled Mode

In the polled mode, the RDLINT[x] and RDLEOM[x] outputs of the RFDL are not used, and the processor controlling the RFDL must periodically read the RFDL Interrupt/Status to determine when to read the Data Register. If the RFDL data transfer is operating in the polled mode, entry to the service routine is from a timer. The processor service routine should process the data in the following order:

1. Poll the INT bit in the RFDL Interrupt/Status Register until it is set to logic 1. Once INT is set to logic 1, then proceed to step 2.

2. Read the RFDL Data Register.

3. Read the RFDL Status Register to check for the following:

   a) If OVR=1, then discard the current frame and go to step 1.

   ELSE

b) If FLG=0 (i.e. an abort has been received) and the link state was active, then set the link state to inactive, discard the current frame, and go to step 1.

c) If FLG=1 and the link state was inactive, then set the link state to active, discard the last data byte, and go to step 1.

ELSE

d) Save the last data byte read.

e) If EOM=1, then read the CRC and NVB[2:0] bits of the RFDL Status Register to process the frame properly.

f) If FE=0, then go to step 2, else go to step 1.

The link state is typically a local software variable. The link state is inactive if the RFDL is receiving all ones or receiving bit-oriented codes which contain a sequence of eight ones. The link state is active if the RFDL is receiving flags or data.

Interrupt Mode

In the interrupt driven mode, the processor controlling the RFDL uses either the RDLINT[x] output, or the main processor INTB output (RDLINTE bit of the Datalink Options Register is set to logic 1), the Interrupt ID/Clock Monitor, and the Interrupt Source Registers, to determine when to read the Data Register. The RXDMASIG bit in the Datalink Options Register should be set to logic 1. RDLINTE of the same register should be set to logic 1 if the INTB output is used as the interrupt source. The processor interrupt service routine should process the data in the following order:

1. Wait for an interrupt originating from the RFDL. Once the interrupt is set, then proceed to step 2.

2. Read the RFDL Data Register.

3. Read the RFDL Status Register to check for the following:

   a) If OVR=1, then discard the current frame and go to step 1.

   ELSE

   b) If FLG=0 (i.e. an abort has been received) and the link state was active, then set the link state to inactive, discard the current frame, and go to step 1.

c) If FLG=1 and the link state was inactive, then set the link state to active, discard the last data byte, and go to step 1.

ELSE

d) Save the last data byte read.

e) If EOM=1, then read the CRC and NVB[2:0] bits of the RFDL Status Register to process the frame properly.

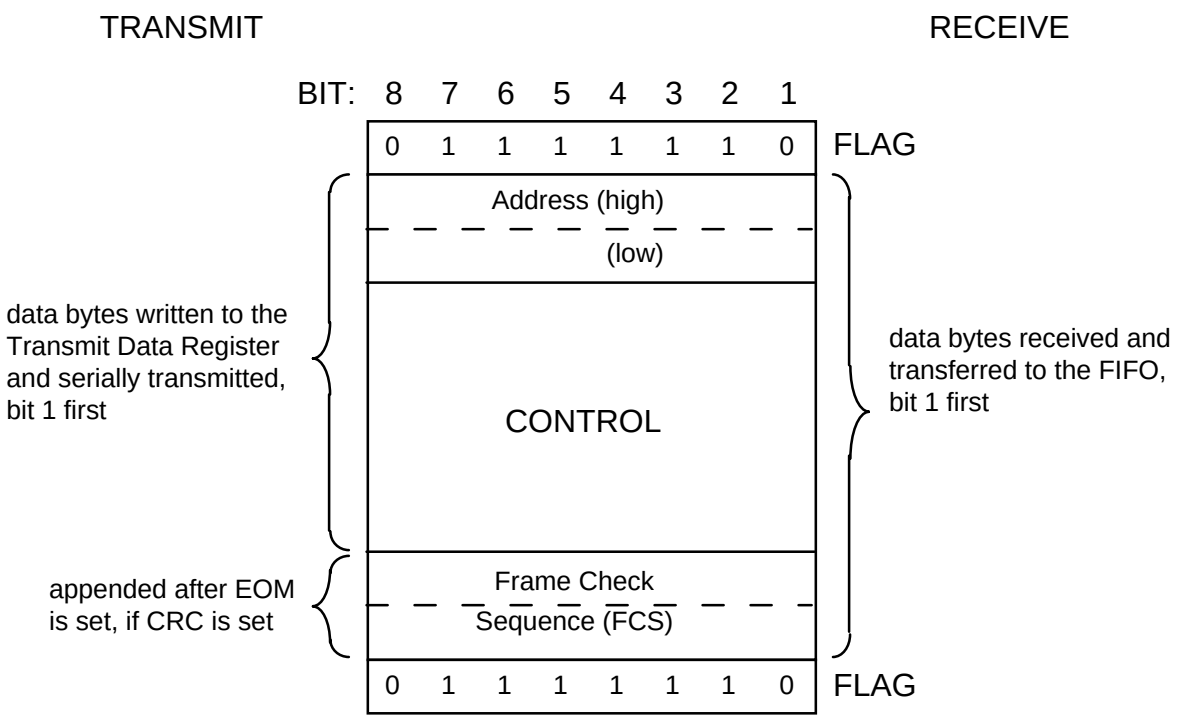
f) If FE=0, then go to step 2, else go to step 1.

DMA-Controlled Mode

The RFDL can also be used with a DMA controller to process the frame data. In the DMA controlled mode, the RDLINT[x] output of the RFDL is used as a DMA request input to the DMA controller, and the RDLEOM[x] output is used as an interrupt to the processor to allow handling of exceptions and as an indication of when to process a frame. The RXDMASIG bit of the Datalink Options Register should be set to logic 1.

The RDLINT[x] output of the RFDL is connected through a gate to the DMA request input of the DMA controller to optionally inhibit the DMA request if the RDLEOM[x] output is high. The DMA controller reads the data bytes from the RFDL whenever the RDLINT[x] output is high. When the current byte read from the Data Register is the last byte in a frame (due to an end-of-message or an abort), or an overrun condition occurs, then the RDLEOM[x] output goes high. The DMA controller is inhibited from reading any more bytes, and the processor is interrupted. The processor can then halt the DMA controller, read the Status Register, process the frame, and finally reset the DMA controller to process the data for the next frame. The RDLEOM[x] output can optionally be enabled to generate a processor interrupt through the common INTB output via the RDLEOME bit in the Datalink Options register, rather than tying the RDLEOM[x] output directly to the microprocessor. This allows a central microprocessor controlling the EQUAD operation to also respond to conditions affecting the DMA servicing of RFDL. When using the INTB output, the central processor must poll the Interrupt ID/Clock Monitor, and the Interrupt Source Registers to identify the source of the interrupt before beginning any interrupt service routine.

Figure 23 - Typical Data Frame



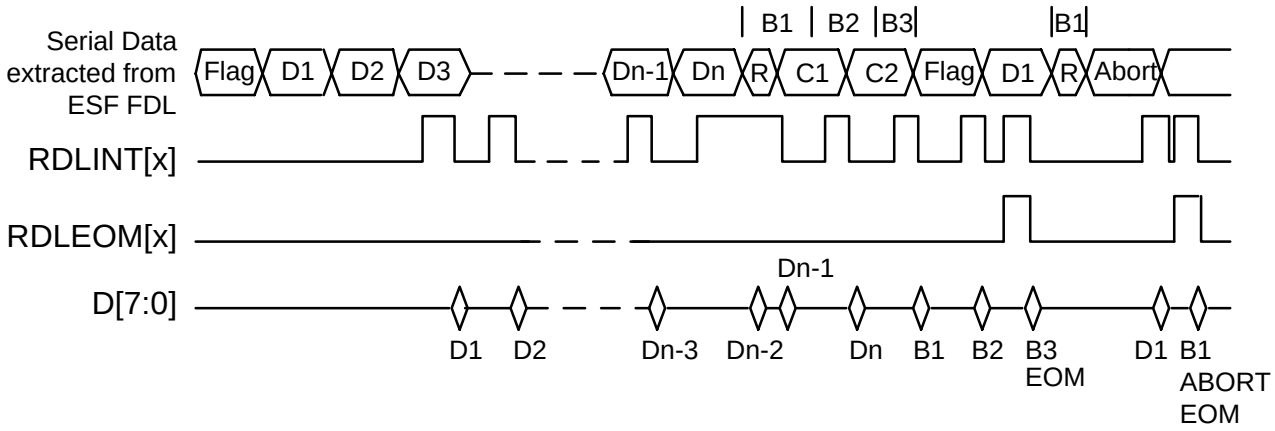
Bit 1 is the first serial bit to be transmitted or received.

Both the address and control bytes must be supplied by an external processor and are shown for reference purposes only.

Key used on subsequent diagrams:

Flag	- flag sequence (01111110)
Abort	- abort sequence (01111111)
D1 - Dn	- n frame data bytes
R	- remainder bits (less than 8)
C1, C2	- CRC-CCITT information
B1, B2, B3	- groupings of 8 bits

Figure 24 - RFDL Normal Data and Abort Sequence



This diagram shows the relationship between RFDL inputs and outputs for the case where interrupts are programmed to occur when one byte is present in the FIFO buffer. The RFDL is assumed to be operating in the interrupt driven mode. Each read shown is composed of two register reads: first a read of the RFDL Data Register, followed by a read of the RFDL Status Register. A read of the RFDL Data Register sets the RDLINT[x] output to low if no more data exists in the FIFO buffer. The status of the FE bit returned in the RFDL Status Register read will indicate the FIFO buffer fill status as well. The RFDL Data Register read Dn-2 is shown to occur after two bytes have been written into the buffer. The RDLINT[x] output does not go low after the first RFDL Data Register read because a data byte still remains to be read. The RDLINT[x] output goes low after RFDL Data Register read Dn-1. The FE bit will be logic 0 in RFDL Status Register read Dn-2 and logic 1 in RFDL Status Register read Dn-1.

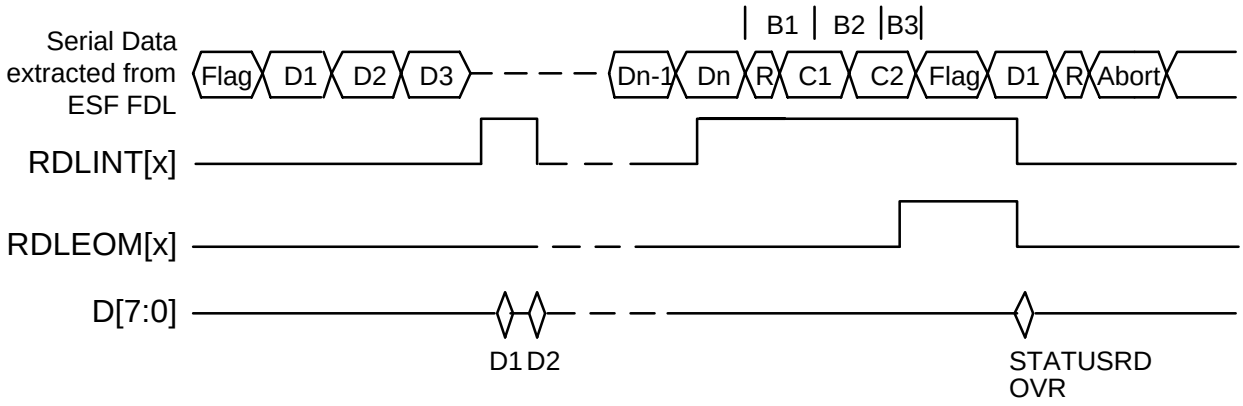
The RDLEOM[x] output goes high as soon as the last byte in the frame is read from the RFDL Data Register. The RDLINT[x] output will go low if the FIFO buffer is empty. The next RFDL Status Register read will return a value of logic 1 for the EOM and FLG bits, and cause the RDLEOM[x] output of the RFDL to return low.

In the next frame, the first data byte is received, and after a delay of ten bit periods, it is written to the FIFO buffer, and read by the processor after the interrupt. When the abort sequence is detected, the data received up to the abort is written to the FIFO buffer and an interrupt generated. The processor then reads the partial byte from the RFDL Data Register and the RDLEOM[x] output is set high. The processor then reads the RFDL Status Register which will return a value of logic 1 for the EOM and FLG bits, and set the RDLEOM[x]

output low. The FIFO buffer is not cleared when an abort is detected. All bytes received up to the abort are available to be read.

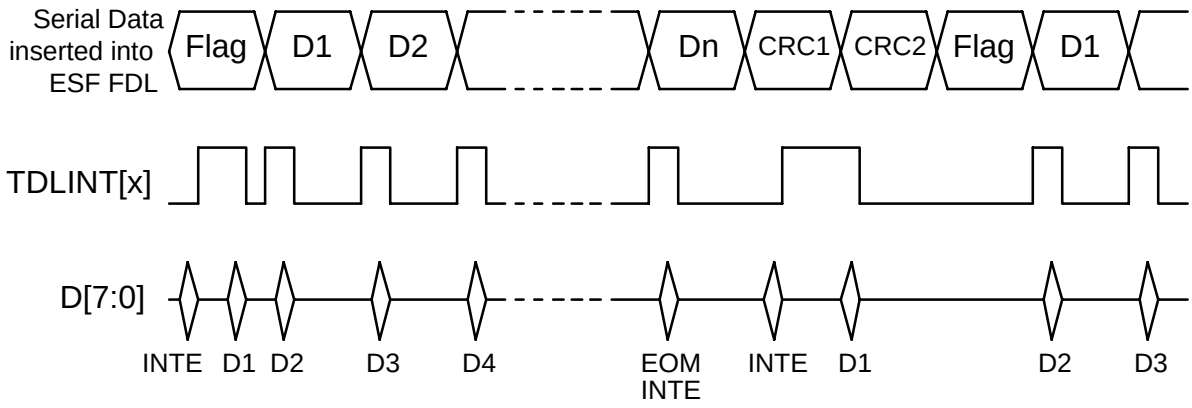
After an abort, the RFDL state machine will be in the receiving all ones state, and the data link status will be idle. When the first flag is detected, a new interrupt will be generated, with a dummy data byte loaded into the FIFO buffer, to indicate that the data link is now active.

Figure 25 - RFDL FIFO Overrun



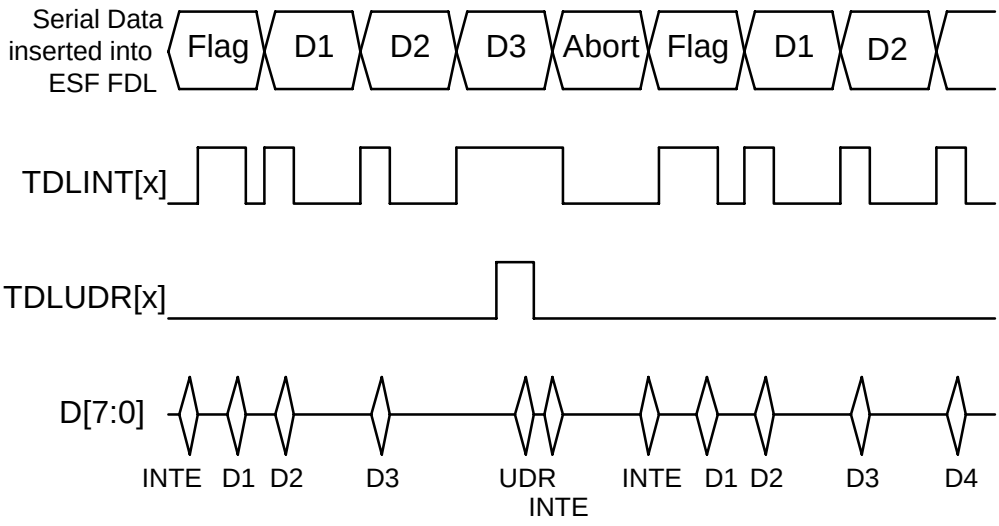
This diagram shows the relationship between RFDL inputs and outputs for the case where interrupts are programmed to occur when two data bytes are present in the FIFO buffer. Each read is composed of two register reads, as described above. In this example, data is not read by the end of B2. An overrun occurs since unread data (Dn-3) has been overwritten by B1. This sets the RDLEOM[x] output high, and resets both the RFDL and the FIFO buffer. The RFDL is held disabled until the RFDL Status Register is read. The start flag sequence is not detected since the RFDL is still held disabled when it occurs. Consequently, the RFDL will ignore the entire frame including the abort sequence (since it has not occurred in a valid frame or during flag reception, according to the RFDL).

Figure 26 - XFDL Normal Data Sequence



This diagram shows the relationship between XFDL inputs and outputs for the case where interrupts and CRC are enabled for regular data transmission. The process is started by setting the INTE bit in the XFDL Configuration Register to logic 1, thus enabling the TDLINT[x] signal. When TDLINT[x] goes high, the interrupt service routine is started, which writes the first byte (D1) of the data frame to the XFDL Transmit Data Register. When this byte begins to be shifted out on the data link, TDLINT[x] goes high. This restarts the interrupt service routine, and the next data byte (D2) is written to the XFDL Transmit Data Register. When D2 begins to be shifted out on the data link, TDLINT[x] goes high again. This cycle continues until the last data byte (Dn) of the frame is written to the XFDL Transmit Data Register. When Dn begins to be shifted out on the data link, TDLINT[x] again goes high. Since all the data has been sent, the interrupt service routine sets the EOM bit in the XFDL Configuration Register to logic 1. The TDLINT[x] interrupt should also be disabled at this time by setting the INTE bit in the XFDL Configuration Register to logic 0. The XFDL will then shift out the two-byte CRC word and closing flag, which ends the frame. Whenever new data is ready, the TDLINT[x] signal can be re-enabled by setting the INTE bit in the XFDL Configuration Register to logic 1, and the cycle starts again.

Figure 27 - XFDL Underrun Sequence



This diagram shows the relationship between XFDL inputs and outputs in the case of an underrun error. An underrun error occurs if the XFDL finishes transmitting the current message byte before the processor writes the next byte into the XFDL Transmit Data Register; that is, the processor fails to write data to the XFDL in time. In this example, data is not written to the XFDL within the time-out period after TDLINT[x] goes high at the beginning of the transmission of byte D3. The TDLUDR[x] interrupt becomes active at this point, and an abort, followed by a flag, is sent out on the data link. Meanwhile, the processor must clear the TDLUDR[x] interrupt by setting the UDR bit in the XFDL Interrupt Status Register to logic 0. The TDLINT[x] interrupt should also be disabled at this time by setting the INTE bit in the XFDL Configuration Register to logic 0. The data frame can then be restarted as usual, by setting the INTE bit logic to 1. Transmission of the frame then proceeds normally.

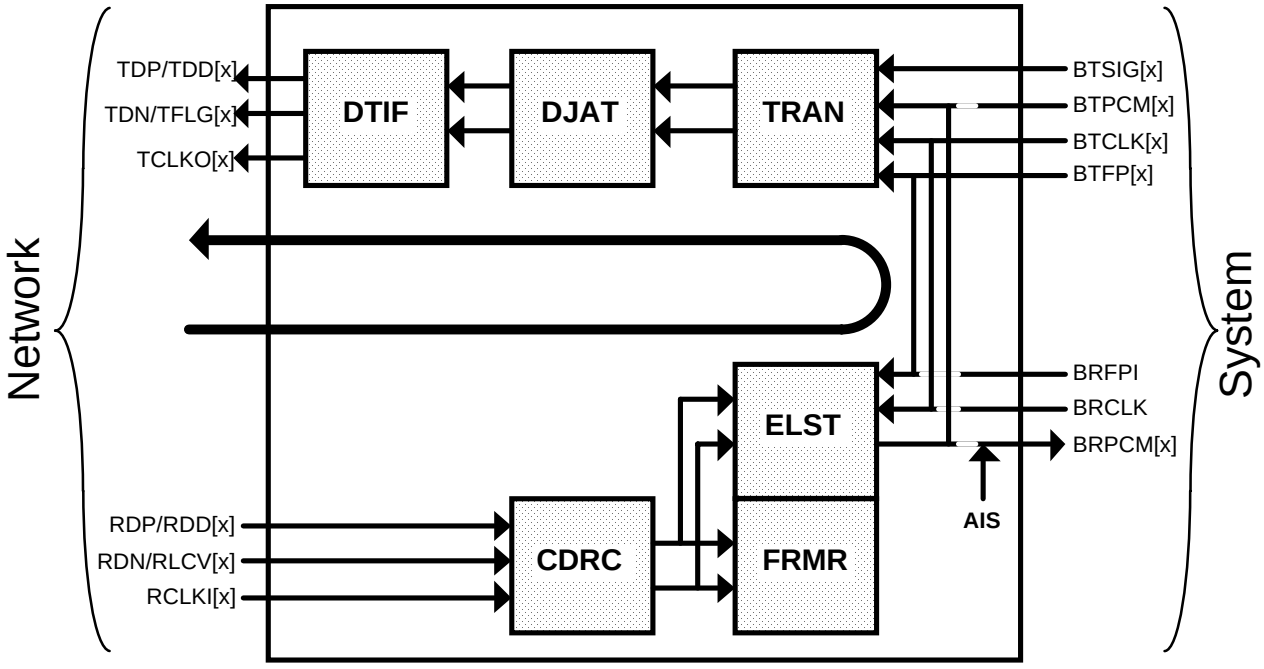
13.3 Using the Loopback Modes

The EQUAD provides three loopback modes to aid in network and system diagnostics. The network loopbacks (PAYLOAD and LINE) can be initiated at any time via the microprocessor interface, but are usually initiated once an inband loopback activate code is detected. The system loopback (Diagnostic) can be initiated at any time by the system via the microprocessor interface to check the path of system data through the transceiver.

13.3.1 Payload Loopback

When PAYLOAD loopback (PAYLB) is initiated by writing 20H to the Master Diagnostics Register (00AH) and disabling the TPSC by clearing the PCCE bit in the TPSC Configuration Register (030H) to 0, the framer is configured to internally connect the output of the ELST to the PCM input of TRAN. Payload loopback will only function if there is a valid BTCLK input signal and a valid BTFP signal (alternatively, BTFP can be tied either high or low). BTFP cannot, though, be derived from the BRFPO output of the loopbacked channel. The data is read out of ELST timed to the transmitter clock, and the transmit frame alignment indication is used to synchronize the output frame alignment of ELST. Note that the BTSIG[x] stream is still presented to the TRAN; therefore, the SIGEN and DLEN bits of the TRAN Configuration register should be cleared to logic 0 if the signaling is to be looped back. The BTSIG[x], BTCLK[x] and BTFP[x] signals must be active during payload loopback. Conceptually, the data flow through a single E1 framer in this loopback condition can be shown as follows:

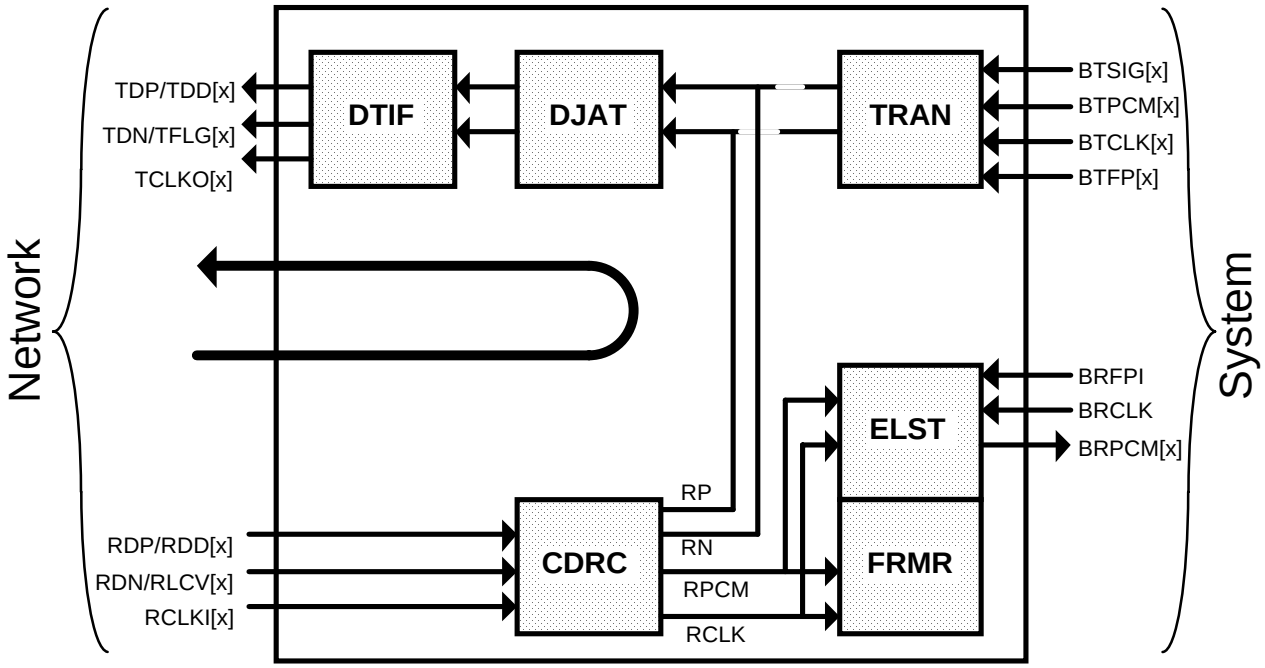
Figure 28 - Payload Loopback



13.3.2 Line Loopback

When LINE loopback (LINELB) is initiated by writing 10H to the Master Diagnostics Register, the framer is configured to internally connect the dual-rail positive and negative line data pulses output from CDRC to the dual-rail inputs of DJAT. If either the transmit or receive is in unipolar mode, the appropriate line decoding or encoding is performed. Conceptually, the data flow through a single framer in this loopback condition can be shown as follows:

Figure 29 - Line Loopback



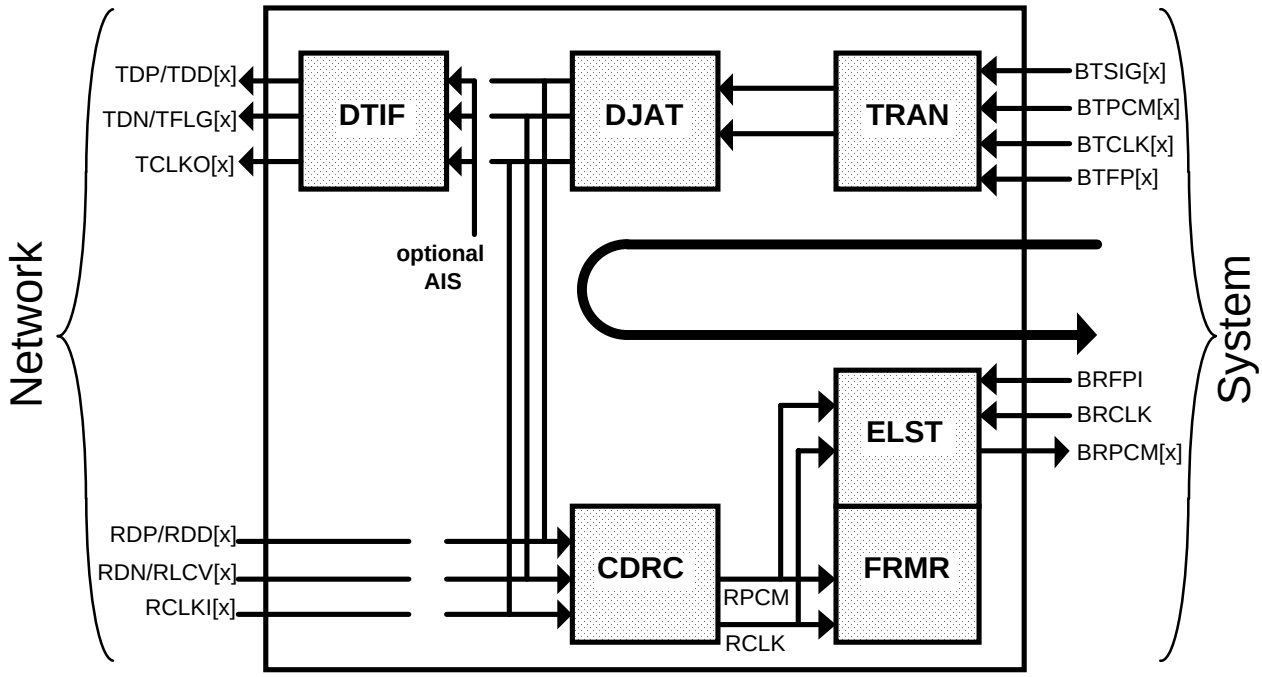
13.3.3 Diagnostic Digital Loopback

When Diagnostic digital loopback (DDLB) is initiated by writing 04H to the Master Diagnostics Register, the framer is configured to internally connect the data and clock outputs from the DJAT to the CDRC. When the framer is configured for dual-rail operation (RUNI=0, TUNI=0), the dual-rail positive and negative data pulses output from DJAT are connected to the dual-rail inputs of CDRC.

Clock recovery can be enabled or disabled in the CDRC and diagnostic digital loopback will also operate when the framer is configured for single-rail operation (RUNI=1, TUNI=1).

Conceptually, the data flow through a single framer in this loopback condition can be shown as follows:

Figure 30 - Diagnostic Digital Loopback



13.4 Using the Per-Channel Serial Controllers

13.4.1 Initialization

Before the TPSC block can be used, a proper initialization of the internal registers must be performed to eliminate erroneous control data from being produced on the block outputs. The output control streams should be disabled by setting the PCCE bit in the TPSC Configuration Register to logic 0. Then, all 64 locations of the TPSC must be filled with valid data. Finally, the output streams can be enabled by setting the PCCE bit in the TPSC Configuration Register to logic 1.

13.4.2 Direct Access Mode

Direct access mode to the TPSC is not used in the EQUAD. However, direct access mode is selected by default whenever the EQUAD is reset. The IND bit within the TPSC Configuration Register must be set to logic 1 after a reset is applied.

13.4.3 Indirect Access Mode

Indirect access mode is selected by setting the IND bit in the TPSC Configuration Register to logic 1. When using the indirect access mode, the status of the BUSY indication bit should be polled to determine the status of the microprocessor access: when the BUSY bit is logic 1, the TPSC is processing an access request; when the BUSY bit is logic 0, the TPSC has completed the request.

The indirect write programming sequence for the TPSC is as follows:

1. Check that the BUSY bit in the TPSC µP Access Status Register is logic 0.
2. Write the timeslot data to the TPSC Timeslot Indirect Data Buffer register.
3. Write RWB=0 and the timeslot address to the TPSC Timeslot Indirect Address/Control Register.
4. Poll the BUSY bit until it goes to logic 0. The BUSY bit will go to logic 1 immediately after step 3 and remain at logic 1 until the request is complete.
5. If there is more data to be written, go back to step 1.

The indirect read programming sequence for the TPSC is as follows:

1. Check that the BUSY bit in the TPSC µP Access Status Register is logic 0.
2. Write RWB=1 and the timeslot address to the TPSC Timeslot Indirect Address/Control Register.
3. Poll the BUSY bit, waiting until it goes to a logic 0. The BUSY bit will go to logic 1 immediately after step 2 and remain at logic 1 until the request is complete.
4. Read the requested timeslot data from the TPSC Timeslot Indirect Data Buffer register.

5. If there is more data to be read, go back to step 1.

13.5 Using the Digital Jitter Attenuator

The key to using DJAT lies in selecting the appropriate divisors for the phase comparison between the selected reference clock and the generated smooth TCLKO.

13.5.1 Default Application

Upon reset, the EQUAD default condition provides jitter attenuation with TCLKO[x] referenced to the transmit clock, BTCLK[x]. The DJAT SYNC bit is also logic 1 by default. DJAT is configured to divide its input clock rate, BTCLK[x], and its output clock rate, TCLKO[x], both by 48, which is the maximum length of the FIFO. These divided down clock rates are then used by the phase comparator to update the DJAT DPLL. The phase delay between BTCLK[x] and TCLKO[x] is synchronized to the physical data delay through the FIFO. For example, if the phase delay between BTCLK[x] and TCLKO[x] is 12UI, the FIFO will be forced to lag its output data 12 bits from its input data.

The default mode works well with the transmit backplane running at 2.048MHz.

13.5.2 Data Burst Application

In applications where a higher transmit backplane rate with external gapping is used, a few factors must be considered to adequately filter the resultant TCLKO[x] into a smooth 2.048MHz clock. The magnitude of the phase shifts in the incoming bursty data can be too large to be properly attenuated by the PLL alone. However, the magnitudes, and the frequency components of these phase shifts are known, and are most often multiples of 8 kHz.

When using a gapped higher rate clock, the phase shifts of the input clock with respect to the generated TCLKO[x] in this case can be large, but when viewed over a longer period, such as a frame, there is little net phase shift. Therefore, by choosing the divisors appropriately, the large phase shifts can be filtered out, leaving a stable reference for the DPLL to lock onto. In this application, the N1 and N2 divisors should be changed to FFH (i.e. divisors of 256). Consequently, the frequency of the clock inputs to the phase discriminator in the PLL is 8 kHz. The DJAT SYNC option must be disabled, since the divisor magnitude of 256 is not an integer multiple of the FIFO length, 48.

The self-centering circuitry of the FIFO should be enabled by setting the CENT register bit. This sets up the FIFO read pointer to be at least 4 UI away from the

end of the FIFO registers, and then disengages. Should variations in the frequency of input clock or the output clock cause the read pointer to drift to within one unit interval of FIFO overflow or underflow, the pointer will be incrementally pushed away by the LIMIT control without any loss of data.

With SYNC disabled, CENT and LIMIT enabled, the maximum tolerable phase difference between the bursty input clock and the smooth TCLKO is 40UI. Phase wander between the two clock signals is compensated for by the LIMIT control.

13.5.3 Elastic Store Application

In multiplex applications where the jitter attenuation is not required, the DJAT FIFO can be used to provide an elastic store function. For example, in a M12 application, the data is written into the FIFO at 2.048MHz and the data is read out of the FIFO with a gapped E2 rate clock applied on TCLKI[x]. In this configuration, the Timing Options OCLKSEL[1:0] bits should be programmed to 01, the TCLKISEL bit should be programmed to 1, and the SMCLKO bit should be programmed to 1. Also, the DJAT SYNC and LIMIT bits should be disabled and the CENT bit enabled. This provides the maximum phase difference between the input clock and the gapped output clock of 40UI. The maximum jitter and wander between the two clocks is 8UIpp.

13.5.4 Alternate TCLKO Reference Application

In applications where TCLKO[x] is referenced to an Nx8 kHz clock source applied on TCLKI[x], DJAT can be configured by programming the output clock divisor, N2, to FFH and the input clock divisor, N1, to the value (N-1). The resultant input clocks to the phase comparator are both 8kHz. The DJAT SYNC and LIMIT bits should be disabled in this configuration.

13.5.5 Changing the Jitter Transfer Function

The DJAT phase lock loop has a single order low pass jitter transfer function. By default, the corner frequency is 8.8 Hz. The corner may be moved by the appropriate selection of clock divisors:

$$f_c = \frac{2048\ \text{kHz}}{1536\pi(N2+1)}$$

where f_c = corner frequency

N2 = value in the Output Clock Divisor Control register

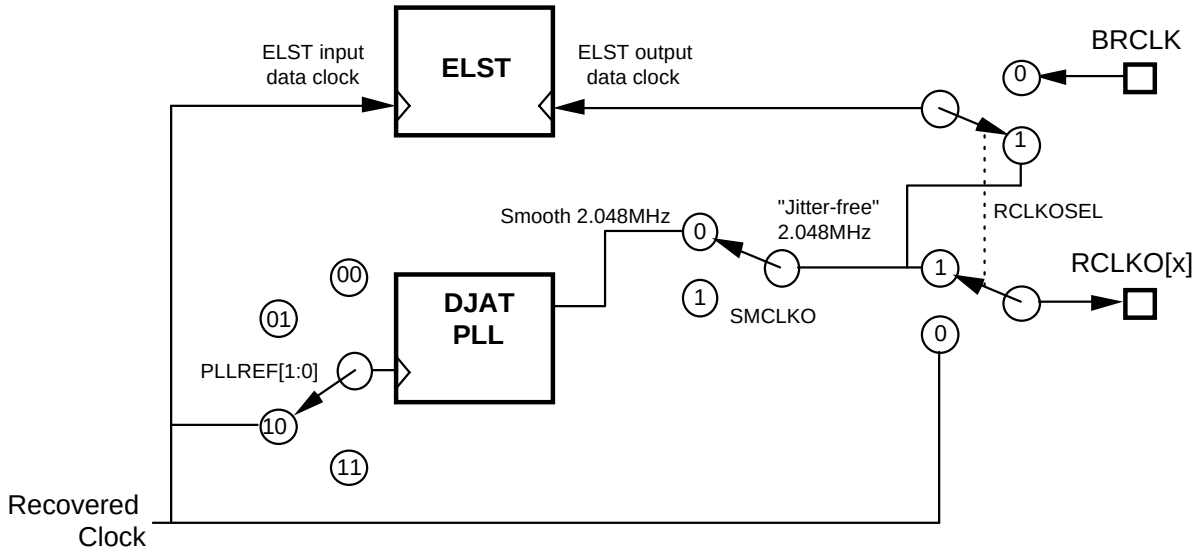
Ensure the Reference Clock Divisor Control value (N1) is also modified to satisfy:

$$\frac{f_{REF}}{N1+1} = \frac{2048\ \text{kHz}}{N2+1}$$

13.5.6 Receiver Jitter Attenuation

The combination of the receive elastic store and the digital phase locked loop may be used to attenuate jitter in the receive direction by locking the elastic store output clock to the recovered clock. The following diagram illustrates the concept.

Fig. 30 Timing Options for Receiver Jitter Attenuation

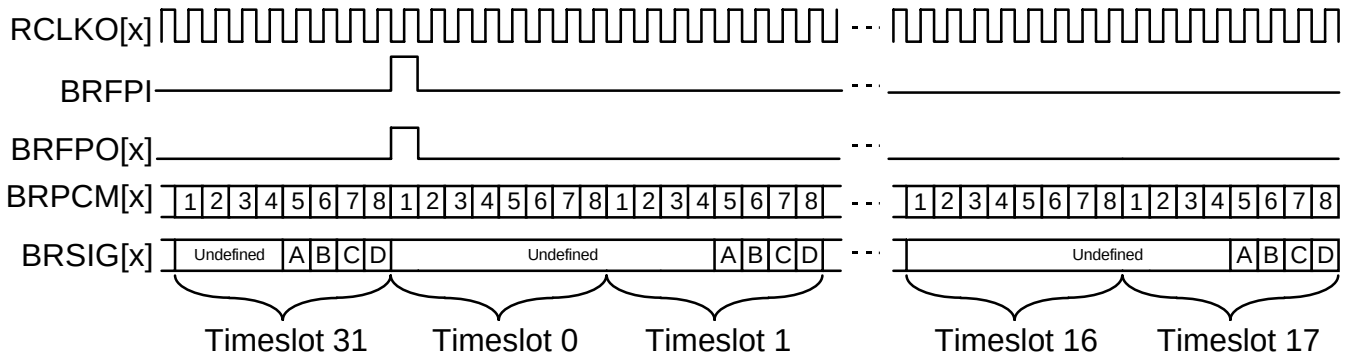


The jitter on the recovered clock is absorbed by the two frame slip buffer in the elastic store. BRPCM[x], BRSIG[x], and BRFPO[x] are updated on the falling edge of RCLKO[x].

The framing alignment on BRPCM[x] and BRSIG[x] is still set by the BRFPI input. However, BRFPI must now be timed with respect to the individual output clock RCLKO[x] instead of BRCLK for each quadrant of the EQUAD in which RCLKOSEL is set to logic 1. A possible configuration would have RCLKOSEL set to logic 1 in only one quadrant and BRFPI timed to that quadrant's RCLKO. The same RCLKO can then be connected to BRCLK which will be used as the timing reference for all the other quadrants which will have RCLKOSEL set to logic 0. Otherwise, if backplane frame alignment is not necessary, RCLKOSEL can be set to logic 1 in every quadrant and BRFPI should be tied low.

Figure 31 shows the functional waveforms for a configuration where RCLKOSEL is set to logic 1 in quadrant x. BRFPI and all the backplane outputs are timed to RCLKO[x].

Figure 31 - Receive Backplane Interface with RCLKOSEL = 1



It should also be noted that RFP[x] can no longer be sampled by RCLKO[x] since RCLKO[x] is a smoothed version of the recovered clock, and RFP[x] is timed by the unsmoothed recovered clock.

Register bits TRSLIP and ELSTBYP in the Receive Options register and BRX2RAIL in the Receive Backplane Options register must be cleared to logic 0 for proper operation. The DJAT Configuration register should be cleared to all zeros to disable the LIMIT and SYNC bits. Note that the DJAT PLL is no longer in the transmit path. Therefore, the FIFOBYP bit of the Transmit Interface Configuration register must be set. to logic 1.

13.6 Using the Performance Monitor Counter Values

All PMON block event counters are of sufficient length so that the probability of counter saturation over a one second interval at a 10^{-3} BER is less than 0.001%. The odds of any one of the counters saturating during a one second sampling interval go up as the BER increases. At some point, the probability of counter saturation reaches 50%. This point varies, depending upon the framing format and the type of event being counted. The BER at which the probability of counter saturation reaches 50% is shown below for various counters:

Table 7 -

Counter	BER
LCV	4.0×10^{-3}
FER	4.0×10^{-3}
CRCE	cannot saturate
FEBE	cannot saturate

Below these 50% points, the relationship between the BER and the counter event count (averaged over many one second samples) is essentially linear. Above the 50% point, the relationship between BER and the average counter event count is highly non-linear due to the likelihood of counter saturation. Figure 32-Figure 34 show this relationship for various counters and framing formats. These graphs can be used to determine the BER, given the average event count. In general, if the BER is above 10^{-3}, the average counter event count cannot be used to determine the BER without considering the statistical effect of occasional counter saturation.

Figure 32 - LCV Count vs. BER

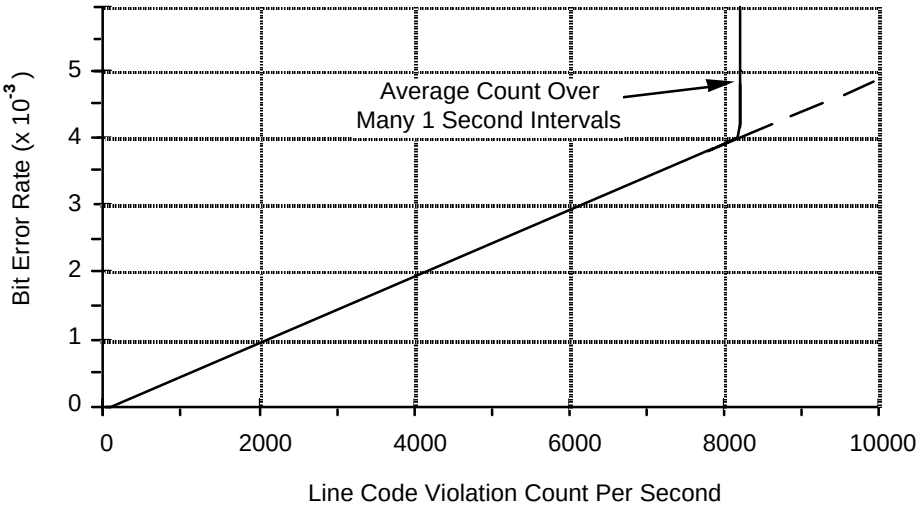
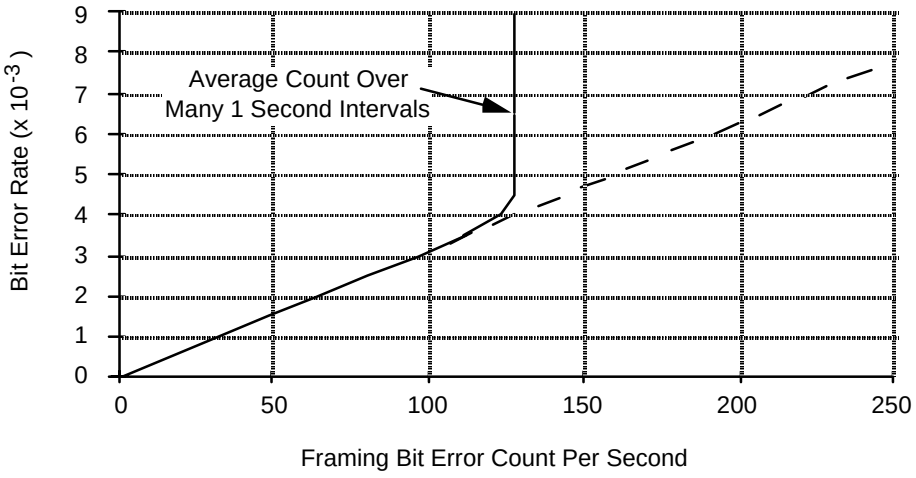


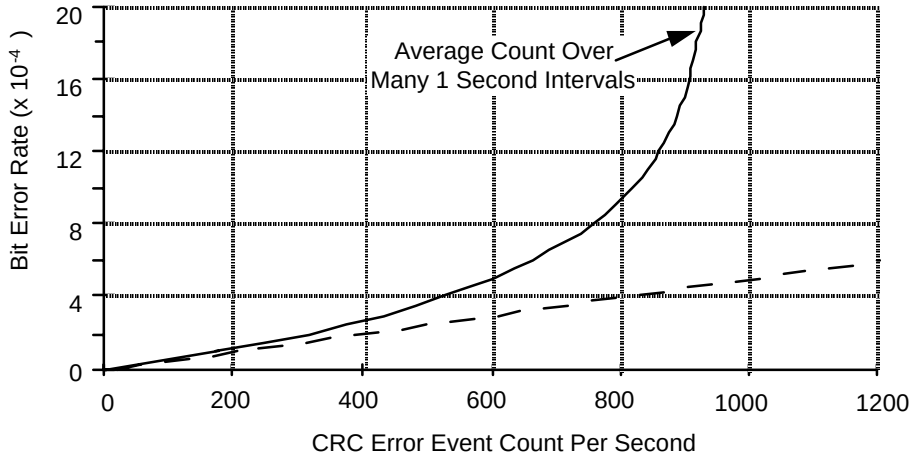
Figure 33 - FER Count vs. BER



Since the maximum number of CRC sub-multiframes that can occur in one second is 1000, the 10-bit FEBE and CRCE counters cannot saturate in one second. Despite this, there is not a linear relationship between BER and CRC-4 block errors due to the nature of the CRC-4 calculation. At BERs below 10^{-4}, there tends to be no more than one bit error per sub-multiframe, so the number of CRC-4 errors is generally equal to the number of bit errors, which is directly related to the BER. However, at BERs above 10^{-4}, each CRC-4 error is often due to more than one bit error. Thus, the relationship between BER and CRCE

count becomes non-linear above a 10^{-4} BER. This must be taken into account when using CRC-4 counts to determine the BER. Since FEBEs are indications of CRCEs at the far end, and are accumulated identically to CRCEs, the same explanation holds for the FEBE event counter.

Figure 34 - CRCE Count vs. BER



13.7 Reset Procedure

In the SIGX block that there is a small state machine which will not clear itself out if it happens to get in an all-ones state. The result is that the SIGX remains frozen after a reset. The probability that this state will occur is very small, about 1 in 3600 or about 0.028 percent probability of occurrence. If the SIGX function is not being used, then this condition is a don't care.

To prevent this state from occurring hold the BRCLK and the BTCLK[4:1] signals low for at least 65ns (greater than one cycle of an 8x clock) after a hardware or software reset. If ELSTBYP is to be set, do not do so within 65ns of a hardware or software reset.

For designs where it is not possible to implement the above hardware solution, the software solution is to perform a self-test after every reset. This self-test routine would use the TPSC functional block to source known signaling data, which would be looped back to the SIGX. If the SIGX can detect changes in the signaling data, then the SIGX block is okay; if it cannot detect changes in the signaling data, then a reset must be performed and the self-test repeated (until the SIGX is okay).

Here are the suggested steps to be taken after every reset (software or hardware reset) of an EQUAD in which the SIGX functional block is being used. This procedure should be performed on each quadrant in the EQUAD.

1) Initialize all indirect registers (including TS0 and TS16). The data control registers contained in PCSC for TS0 and TS16 should not be written to.

2) Perform the reset (software or hardware).

   A software reset is performed by setting then clearing the RESET bit in Register 00DH, 08Dh, 10DH or 18DH (depending on the quadrant). A hardware reset is performed by asserting the RSTB pin low, then deasserting high.

   The reset will make all the EQUAD's normal mode registers revert to their default state as described in the EQUAD databook section entitled "REGISTER DESCRIPTION." This default state enables the EQUAD to operate as described in the EQUAD databook section entitled "Configuring the EQUAD from Reset." Note that indirect registers contained in the SIGX and PCSC are not affected by a reset.

3) Configure and enable the PCSC functional block for the self-test.

   The method of accessing the indirect registers within the PCSC functional block is explained in the EQUAD databook section entitled "Using the Per-Channel Serial Controllers."

   The PCSC should be configured as follows:

   a) Set the IND bit in quadrant 1 Register 030H (0B0H, 130H or 1B0H for quadrants 2, 3 and 4) to a logic one. This will enable access to the PCSC indirect registers.

   b) Program the PCSC indirect registers such that, for all channels, the Data Control byte is equal to F5H. The IDLE Code bytes can be left (they are don't-cares). This will configure the PCSC to insert µ-Law Digital Milliwatt patterns into all channels, and to insert a signaling state of ABCD=0101.

   c) Set the PCCE bit in quadrant 1 Register 030H (0B0H, 130H, 1B0H for quadrants 2, 3 and 4) to a logic one. This will enable the PCSC to perform the functions configured in step (b) above.

4) Configure the SIGX functional block for the self-test.

The method of accessing the indirect registers within the SIGX functional block is the same as that explained in the EQUAD databook section entitled "Using the Per-Channel Serial Controllers."

The SIGX should be configured as follows:

a) Set the IND bit in quadrant 1 register 040H (0C0H, 140H or 1C0H for quadrants 2, 3 or 4) to a logic one. This will enable accesses to the SIGX indirect registers.

b) Program the SIGX indirect registers such that, for timeslots 1-15 and 17-31 the per-timeslot Configuration and Signaling Trunk Conditioning data registers contain 10H. This will configure the SIGX to debounce the received signaling states as explained in the RDEBE bit description.

c) Set the PCCE bit in register 040H (0C0H, 140H, 1C0H) to a logic one. This will enable the SIGX to perform the functions configured in step (b) above.

5) Configure for Diagnostic Digital Loopback. To accomplish this:

a) Program quadrant 1 Register 00AH (08AH, 10AH or 18AH for quadrants 2, 3 or 4) to 04H. This will enable the Diagnostic Digital Loopback mode of the EQUAD which internally loops back the transmit data to the receive circuitry. This mode is sometimes called a "local" loopback.

b) Program Register 10H (090H, 110H, 190H) to default value of 00H and Register 44H (0C4H, 144H, 1C4H) to 70H for CRC generation. Program register 20H to 80H to enable CRC framing. This will enable the receiver to accept the HDB3-encoded signal sourced by the transmitter.

6) Disable Elastic Store.

This can be done by bypassing elastic store. To do this, program Register 00H (080H, 100H, 180H) to a value of 20H.

7) Wait until the FRMR functional block is solidly in-frame.

This can be determined by polling the OOF, OOSMF and OOCMF bits in Register 026H (0A6H, 126H, 1A6H) and the OOFI, OOSMFI and OOCMFI bits in Register 024H (0A4H, 124H, 1A4H). When the OOF, OOSMF and OOCMF bits are low (logic zero) for two consecutive polls, and the OOFI, OOSMFI and OOCMFI bits are low (logic zero) on the second consecutive poll, then you can assume that the FRMR functional block of the current quadrant of the EQUAD has found a stable frame alignment pattern.

8) Further wait until at least five signaling multiframes have been received (> 10 ms) to give SIGX time to unfreeze and debounce the signaling data.

9) Verify that the SIGX signaling data registers contain the expected value (that transmitted by the PCSC functional block). If not, return to Step (1). This is accomplished by reading the SIGX typical timeslot signaling for timeslots 1-15 and 17-31. The values returned should contain 55H -- if not, return to Step (1).

10) Change the signaling data transmitted by the PCSC for all channels. A value of FFH should be written to the PCSC Data Control byte for timeslots 1-15 and 17-31. This will configure the PCSC to insert a signaling state of ABCD=1111.

11) Wait until at least three signaling multiframes have been received (> 6 ms) to give SIGX time to extract and debounce the new signaling data.

12) Verify that the SIGX signaling data registers contain the new values. If not, return to Step (1).

    This is accomplished by reading the SIGX Typical Timeslot Signaling Data Registers for timeslots 1-15, 17-31. The values returned should contain FFH. If not, return to Step (1).

13) The self-test passed -- The EQUAD is ready for operation.

    The EQUAD can now be configured for the desired application. It is allowable to reconfigure the PCSC and SIGX functional blocks.

Every time a reset (software or hardware) occurs, the above procedure, Steps (1) through (13), should be performed for each quadrant in the EQUAD.

14 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on VDD with Respect to GND	-0.5V to +7.0V
Voltage on Any Pin	VSS-0.5V to VDD+0.5V
Static Discharge Voltage	±1000 V

15 CAPACITANCE

Table 8 - EQUAD Capacitance

Symbol	Parameter	Typical	Units	Conditions
Cin	Input Capacitance	5	pF	T_A = 25°C, f = 1 MHz
Cout	Output Capacitance	5	pF	T_A = 25°C, f = 1 MHz
Cbidir	Bidirectional Capacitance	5	pF	T_A = 25°C, f = 1 MHz

16 D.C. CHARACTERISTICS

TA= -40° to +85°C, VDD=5V ±10%

Table 9 - EQUAD D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
PHA, PHD	Power Supply	4.5	5	5.5	Volts	
V_{IL}	Input Low Voltage	-0.5		0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage	2.0		V_{DD}+0.5	Volts	Guaranteed Input HIGH Voltage
V_{OL}	Output or Bidirectional Low Voltage		0.1	0.4	Volts	V_{DD} = min, I_{OL} = -4 mA for D[7:0] and MRD and -2 mA for others[3]
V_{OH}	Output or Bidirectional High Voltage	V_{DD} - 1.0	4.5		Volts	V_{DD} = min, I_{OL} = 4 mA for D[7:0] and MRD and 2 mA for others[3]
V_{T+}	Reset Input High Voltage	3.5			Volts	
V_{T-}	Reset Input Low Voltage			0.6	Volts	
V_{TH}	Reset Input Hysteresis Voltage		1.4		Volts	
I_{ILPU}	Input Low Current[1,3]	+100	+350	+525	µA	V_{IL} = GND

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IHPU}	Input High Current[1,3]	-10	0	+10	µA	$V_{IH} = V_{DD}$
I_{IL}	Input Low Current[2,3]	-10	0	+10	µA	V_{IL} = GND
I_{IH}	Input High Current[2,3]	-10	0	+10	µA	$V_{IH} = V_{DD}$
I_{DDOP}	Operating Current		47	80	mA	V_{DD} = 5.5 V, Outputs Unloaded, XCLK = 49.152 MHz BTCLK[4:1] = 2.048MHz

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistors.
2. Input pin or bidirectional pin without internal pull-up resistors
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

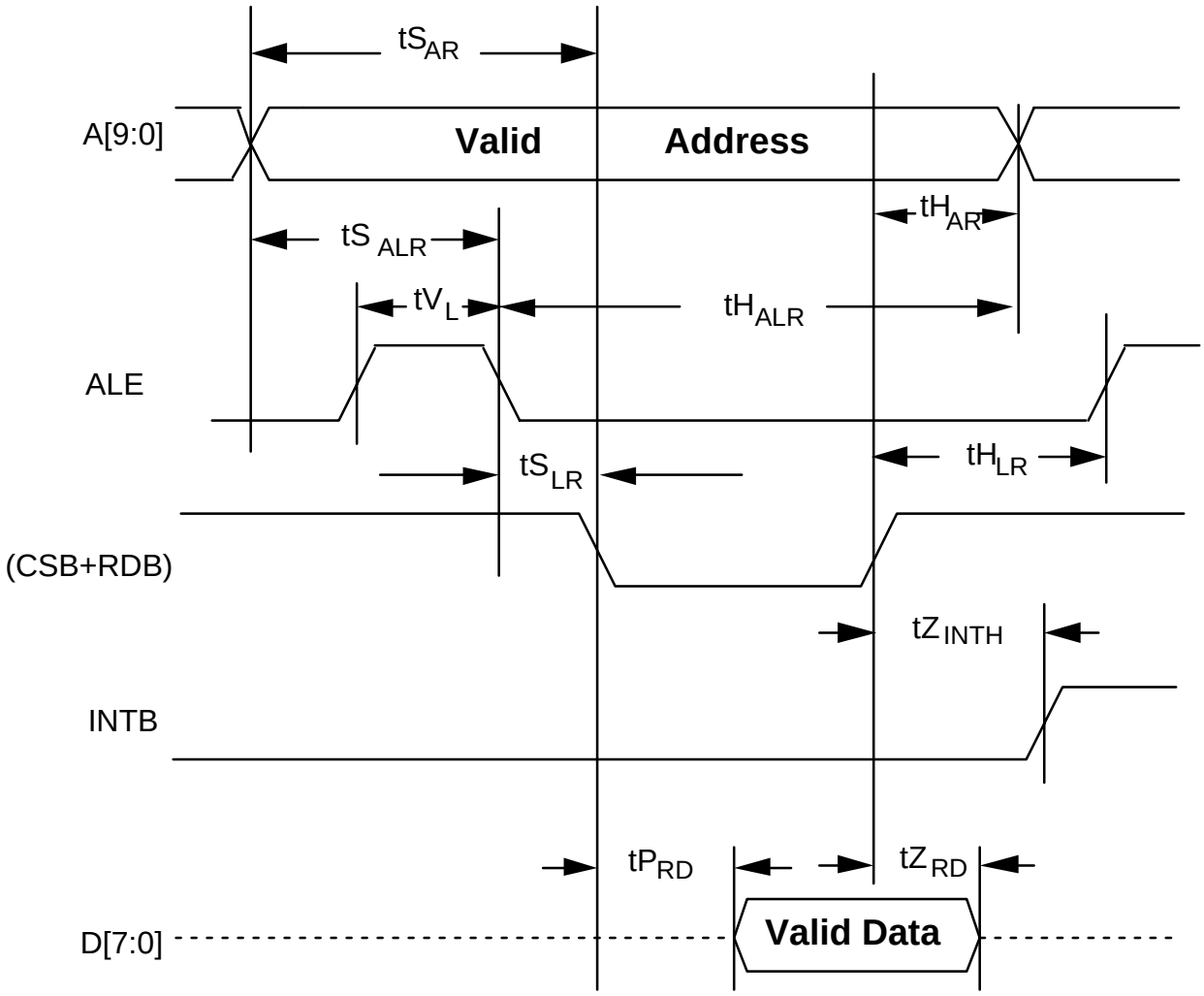
17 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

TA= -40° to +85°C, VDD=5V ±10%

Table 10 - Microprocessor Read Access (Figure 35)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	10		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	10		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		80	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to INTB high		50	ns

Figure 35 - Microprocessor Read Access Timing



Notes on Microprocessor Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 50 pF load on the Microprocessor Interface data bus, (D[7:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

4. Microprocessor Interface timing applies to normal mode register accesses only.

5. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

6. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

7. In non-multiplexed address/data bus architectures ALE should be held high and parameters tS_{ALR}, tH_{ALR}, tV_L, tS_{LR} and tH_{LR} are not applicable.

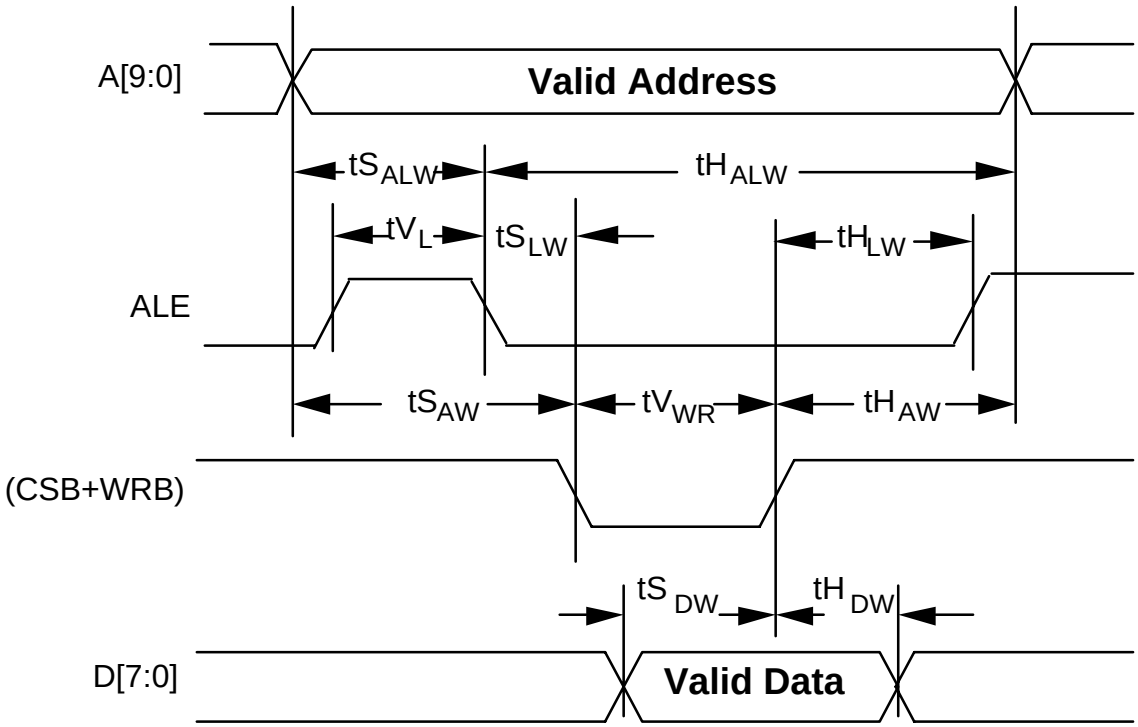
8. Parameter tH_{AR} is not applicable when address latching is used.

9. Output tristate delay is the time in nanoseconds from the 1.4 Volt point of the reference signal to ±300mV of the termination voltage on the output. The test load is 50Ω to 1.4V in parallel with 10 pf to GND.

Table 11 - Microprocessor Write Access (Figure 36)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_L	Valid Latch Pulse Width	20		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 36 - Microprocessor Write Access Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. Microprocessor Interface timing applies to normal mode register accesses only.
3. In non-multiplexed address/data bus architectures, ALE should be held high and parameters tS_{ALW}, tH_{ALW}, tV_L, tS_{LW} and tH_{LW} are not applicable.
4. Parameters tH_{AW} and tS_{AW} are not applicable if address latching is used.
5. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

18 EQUAD I/O TIMING CHARACTERISTICS

TA= -40° to +85°C, VDD=5V ±10%

Table 12 - Backplane Transmit Input Timing, MENB Input High (Figure 37)

Symbol	Description	Min	Max	Units
f_{BTCLK}	Backplane Transmit Clock Frequency[1,2](Typically 2.048 MHz ± 50 ppm)		2.1	MHz
tD_{BTCLK}	Backplane Transmit Clock Duty Cycle	30	70	%
tS_{TCLK}	BTCLK[x] to Backplane Input Set-up Time[7]	20		ns
tH_{TCLK}	BTCLK[x] to Backplane Input Hold Time[8]	20		ns

Figure 37 - Backplane Transmit Input Timing Diagram

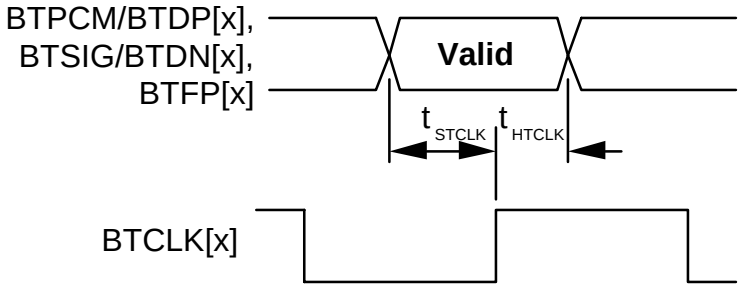


Table 13 - Backplane Transmit Input Timing, MENB Input Low (Figure 37)

Symbol	Description	Min	Max	Units
t_{MTCLK}	Backplane Transmit Clock Frequency[2,3](Typically 16.384 MHz ± 50 ppm)		16.8	MHz
tD_{MTCLK}	Backplane Transmit Clock Duty Cycle	40	60	%
tS_{MTCLK}	MTCLK to Backplane Input Set-up Time[7]	10		ns
tH_{MTCLK}	MTCLK to Backplane Input Hold Time[8]	3		ns

Figure 38 - Backplane Transmit Input Timing Diagram

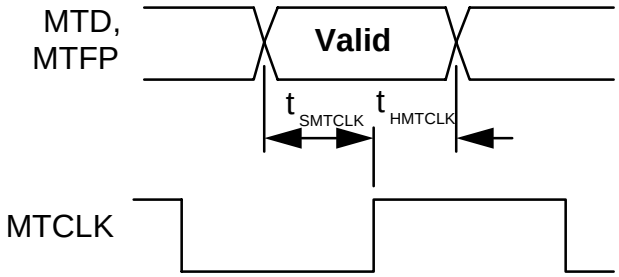


Table 14 - XCLK=49.152 MHz Input (Figure 39)

Symbol	Description	Min	Max	Units
t_{LXCLK}	XCLK Low Pulse Width[4]	8		ns
t_{HXCLK}	XCLK High Pulse Width[4]	8		ns
t_{XCLK}	XCLK Period (typically 1/49.152 MHz)[5]	20		ns

Figure 39 - XCLK=37.056 MHz Input Timing

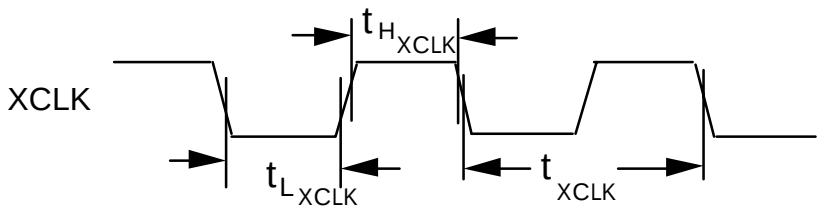


Table 15 - TCLKI Input (Figure 40

Symbol	Description	Min	Max	Units
$f1_{TCLKI}$	TCLKI[x] Frequency (when used for DJAT REF or for mux operation), typically 2.048 MHz± 50 ppm[2,6]		2.10	MHz
$f2_{TCLKI}$	TCLKI[x] Frequency (when DJAT PLL not used), typically 16.384 MHz		16.8	MHz
t_{HTCLKI}	TCLKI[x] High Duration[6]	100		ns
t_{LTCLKI}	TCLKI[x] Low Duration[6]	100		ns

Figure 40 - TCLKI Input Timing

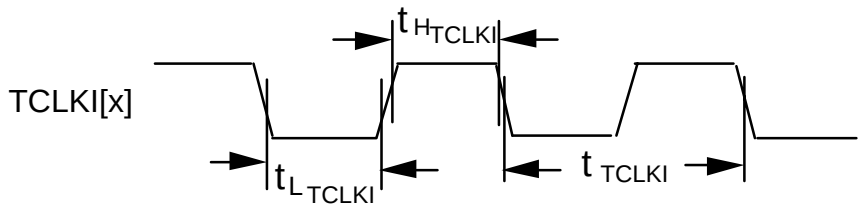
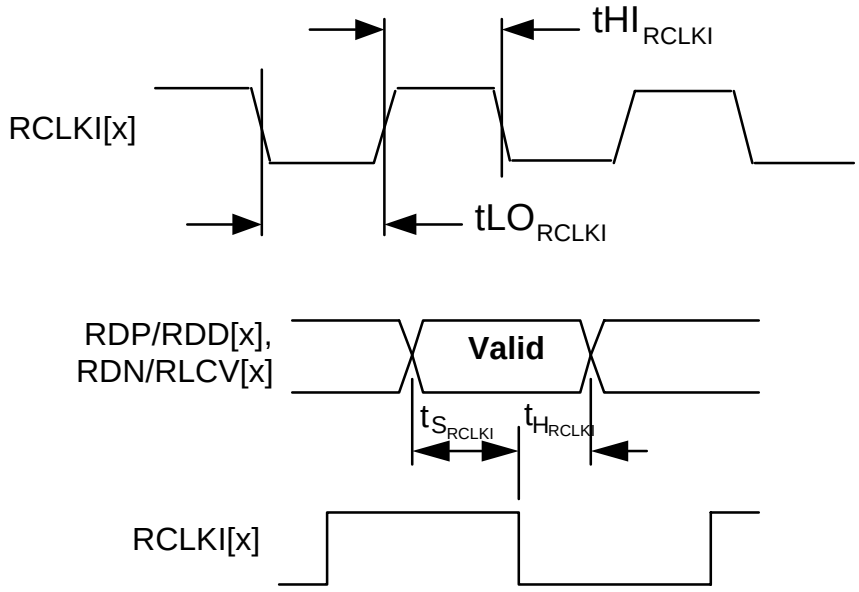


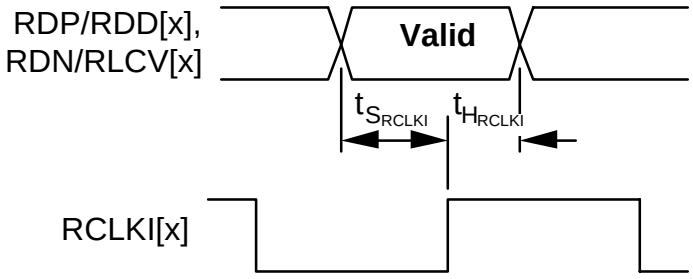
Table 16 - Digital Receive Interface Input Timing (Figure 41)

Symbol	Description	Min	Max	Units
f_{RCLKI}	Digital Receive Clock RCLKI[x] Frequency (nominally 2.048 MHz ± 50 ppm)[2]		2.1	MHz
tLO_{RCLKI}	RCLKI[x] Low Duration	145[2]		ns
tHI_{RCLKI}	RCLKI[x] High Duration	145[2]		ns
tS_{RCLKI}	RCLKI[x] to NRZ Receive Input Set-up Time[7]	20		ns
tH_{RCLKI}	RCLKI[x] to NRZ Receive Input Hold Time[8]	20		ns
tW_{RDPN}	RZ Receive Input Pulse Width[2,4]	200	300	ns

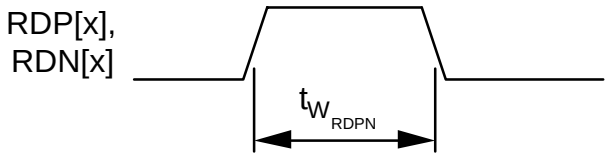
Figure 41 - Digital Receive Interface Input Timing Diagram



With RFALL bit =1, DCR or RUNI=1



With RFALL bit =0, DCR or RUNI=1



With DCR=0 & RUNI=0

Table 17 - Transmit Data Link Input Timing (Figure 42)

Symbol	Description	Min	Max	Units
tS_{DIN}	TDLCLK[x] to TDLSIG[x] Input Set-up Time[7]	80		ns
tH_{DIN}	TDLCLK[x] to TDLSIG[x] Input Hold Time[8]	20		ns

Figure 42 - Transmit Data Link Input Timing Diagram

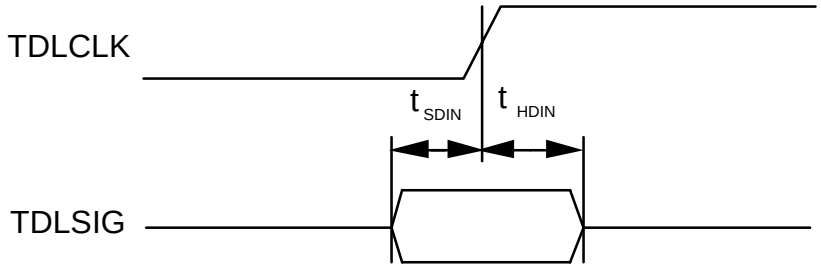


Table 18 - Backplane Receive Timing, MENB Input High (Figure 43)

Symbol	Description	Min	Max	Units
t_{SBRFPI}	BRCLK to BRFPI Input Set-up Time[7]	20		ns
t_{HBRFPI}	BRCLK to BRFPI Input Hold Time[8]	20		ns
t_{PBRCLK}	BRCLK to Backplane Output Signals Propagation Delay[9,10]		50	ns
$f1_{BRCLK}$	BRCLK freq. - Reg 07H HSBPSEL=0[2]		2.41	MHz
$f2_{BRCLK}$	BRCLK freq. - Reg 07H HSBPSEL=1[2]		3.00	MHz

Figure 43 - Backplane Receive Timing Diagram

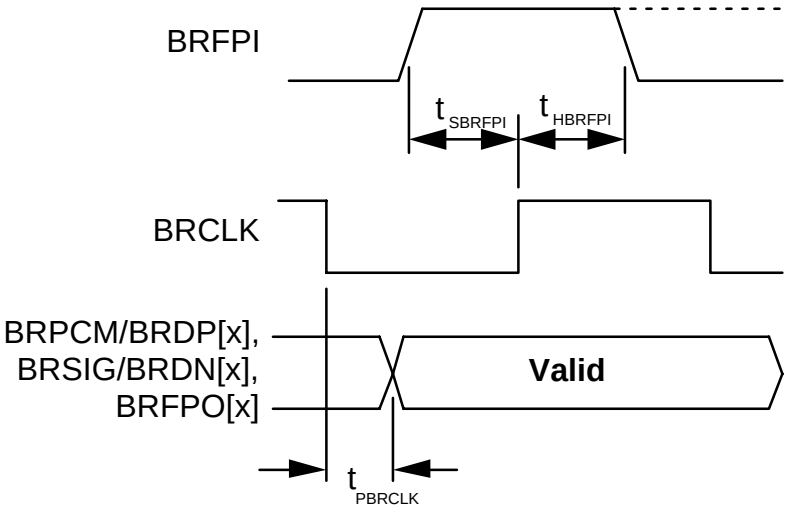


Table 19 - Backplane Receive Timing, MENB Input High, RCLKOSEL = 1 (Figure 44)

Symbol	Description	Min	Max	Units
$t_{SBRFPIO}$	RCLKO to BRFPI Input Set-up Time[7]	25		ns
$t_{HBRFPIO}$	RCLKO to BRFPI Input Hold Time[8]	20		ns
$t_{PBRCLKO}$	RCLKO to Backplane Output Signals Propagation Delay[9,10]		50	ns

Figure 44 - Backplane Receive Timing (RCLKOSEL = 1) Diagram

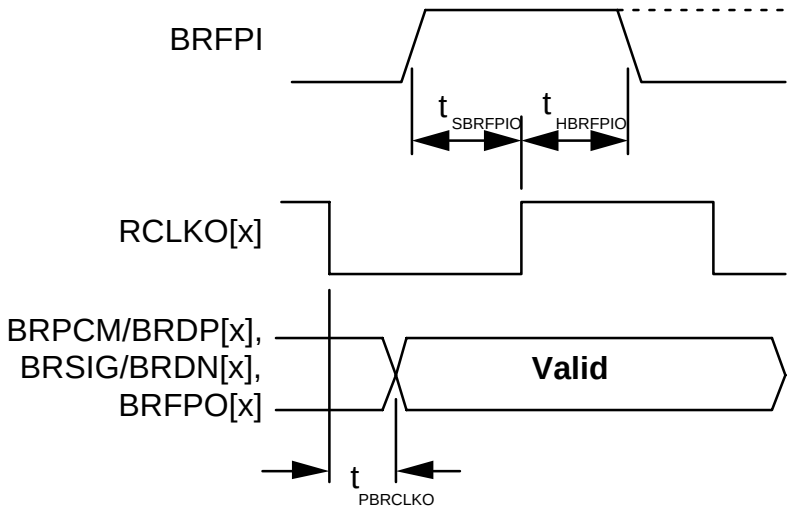


Table 20 - Multiplexed Backplane Receive Timing, MENB Input Low (Figure 45)

Symbol	Description	Min	Max	Units
t_{SMRFPI}	MRCLK to MRFPI Input Set-up Time[7]	10		ns
t_{HMRFPI}	MRCLK to MRFPI Input Hold Time[8]	2		ns
t_{PMRD}	BRCLK to MRD Propagation Delay[9,10]		25	ns

Figure 45 - Multiplexed Backplane Receive Timing Diagram

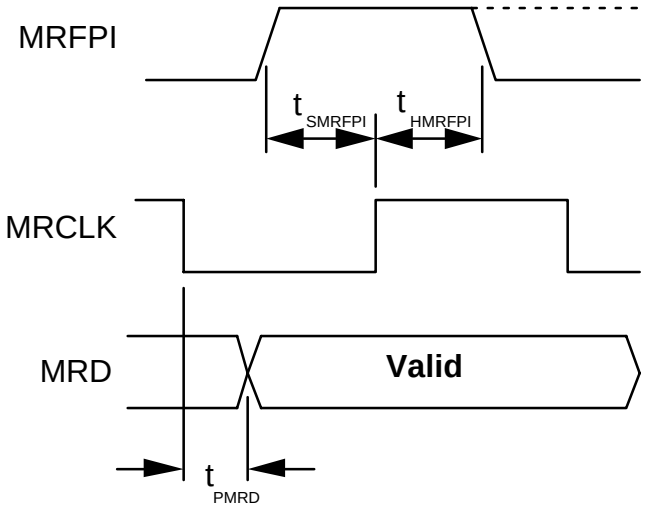


Table 21 - Receive Data Link Output Timing (Figure 46)

Symbol	Description	Min	Max	Units
$t_{PRDLCLK}$	RDLCLK[x] to RDLSIG[x] Propagation Delay[9,10]		50	ns

Figure 46 - Receive Data Link Output Timing Diagram

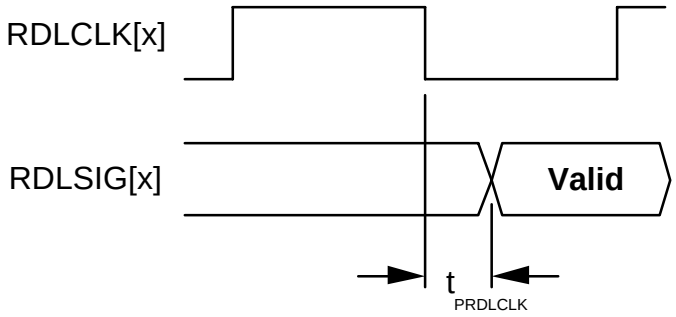


Table 22 - Recovered Frame Pulse Output Timing (Figure 47)

Symbol	Description	Min	Max	Units
t_{PRFP}	RCLKO[x] to Recovered Frame Pulse (RFP[x]) Propagation Delay (RCLKOSEL = 0)[9,10]		50	ns

Figure 47 - Recovered Frame Output Timing Diagram

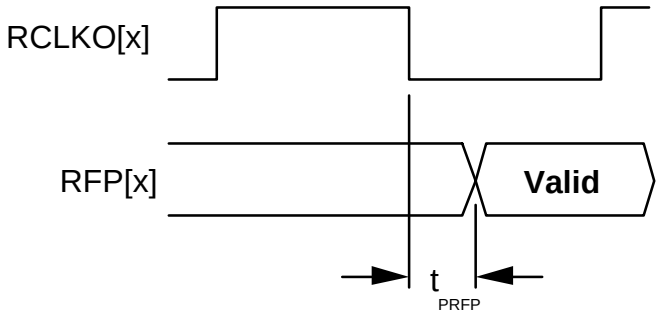
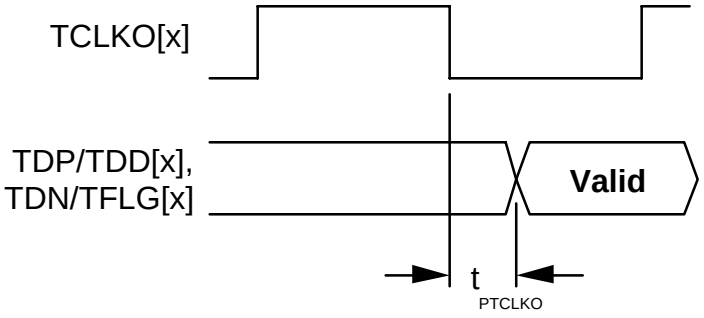


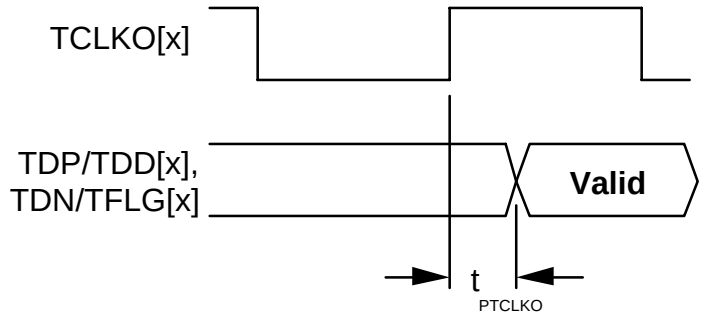
Table 23 - Transmit Interface Output Timing (Figure 48)

Symbol	Description	Min	Max	Units
t_{PTCLKO}	TCLKO[x] to Digital Transmit Data Output Signals Propagation Delay[9,10]		50	ns

Figure 48 - Transmit Interface Output Timing Diagram



With TRISE bit=0



With TRISE bit= 1

Table 24 - Transmit Data Link DMA Interface Output Timing (Figure 49)

Symbol	Description	Min	Max	Units
tP_{TINT}	Transmit Data Register Serviced (WRB low) to TDLINT[x] Low Propagation Delay[9,10]		50	ns
tP_{TUDR}	XFDL UDR bit written low (WRB high) to TDLUDR[x] Low Propagation Delay[9,10]		50	ns

Figure 49 - Transmit Data Link DMA Interface Output Timing Diagram

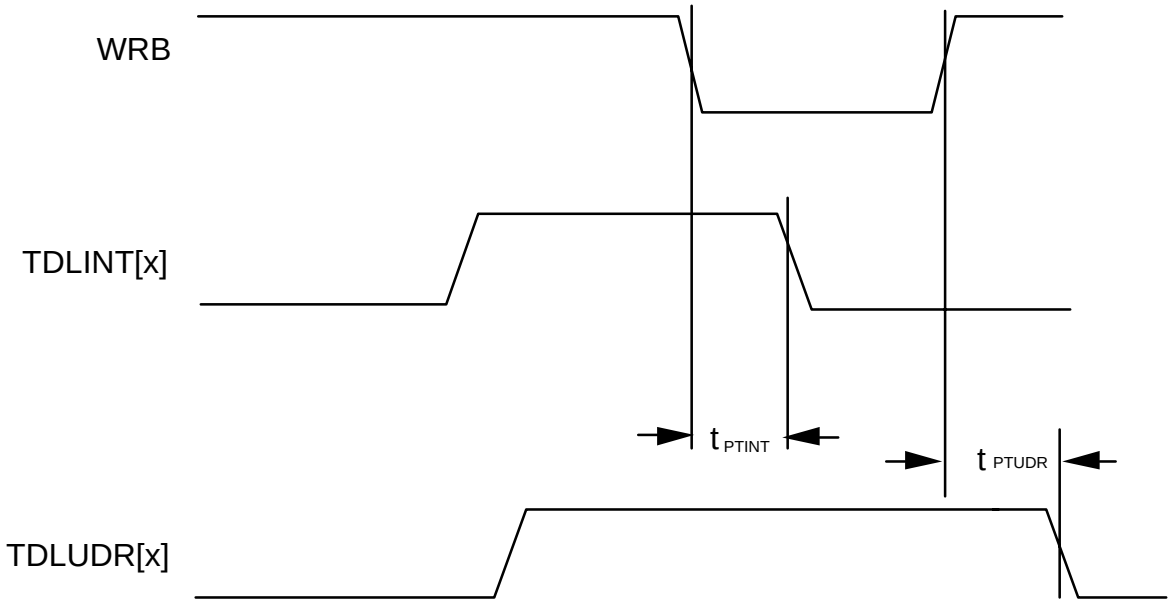
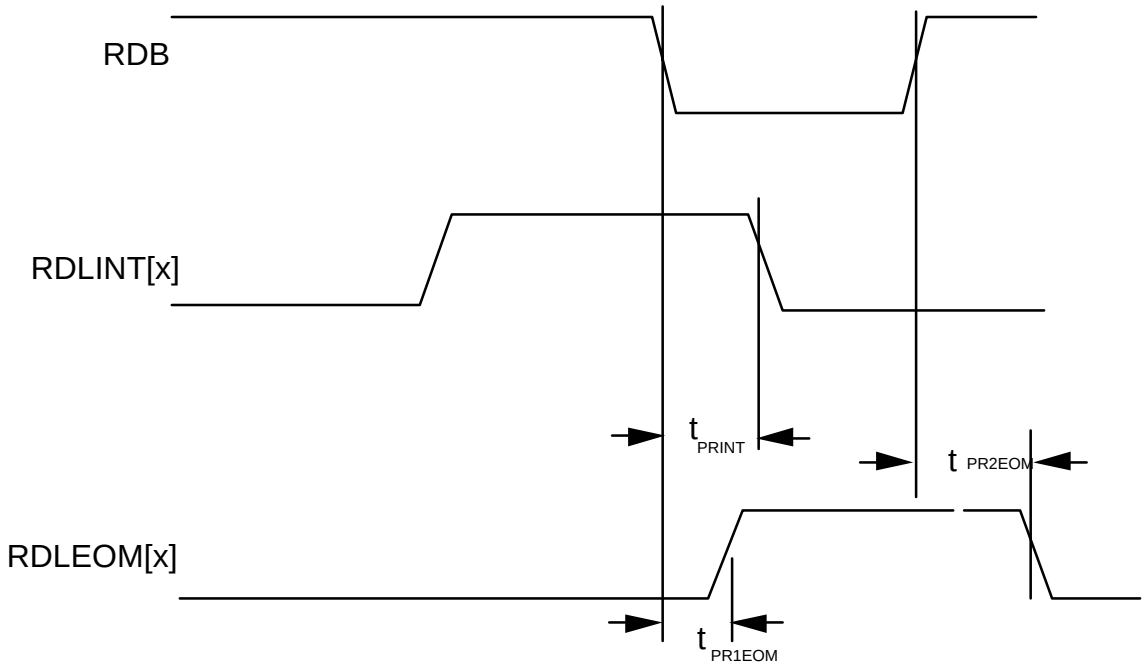


Table 25 - Receive Data Link DMA Interface Output Timing (Figure 50)

Symbol	Description	Min	Max	Units
tP_{RINT}	Receive Data Register Serviced (RDB low) to RDLINT[x] Low Propagation Delay[9,10]		70	ns
tP_{R1EOM}	Receive Data Register Serviced (RDB low) to RDLEOM[x] High Propagation Delay[9,10]		80	ns
tP_{R2EOM}	Receive Status Register Serviced (RDB high) to RDLEOM[x] Low Propagation Delay[9,10]		50	ns

Figure 50 - Receive Data Link DMA Interface Output Timing Diagram



Notes on Input Timing:

1. BTCLK[x] can be a jittered clock signal subject to the minimum and maximum instantaneous frequencies and duty cycles shown.

2. Guaranteed by design for nominal XCLK input frequencies (49.152 MHz ± 50 ppm or 16.384 MHz ± 50 ppm).

3. MTCLK can be a jittered clock signal subject to the minimum and maximum instantaneous frequencies and duty cycles shown. These specifications correspond to nominal XCLK input frequencies.

4. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

5. XCLK accuracy is ± 50 ppm.

6. TCLKI[x] can be a jittered clock signal subject to the minimum high and low durations tH_{TCLKI}, tL_{TCLKI}. These durations correspond to nominal XCLK input frequencies.

7. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

8. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

9. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

10. Output propagation delays are specified with a 50 pF load.

19 ORDERING AND THERMAL INFORMATION

Table 26 - EQUAD Ordering Information

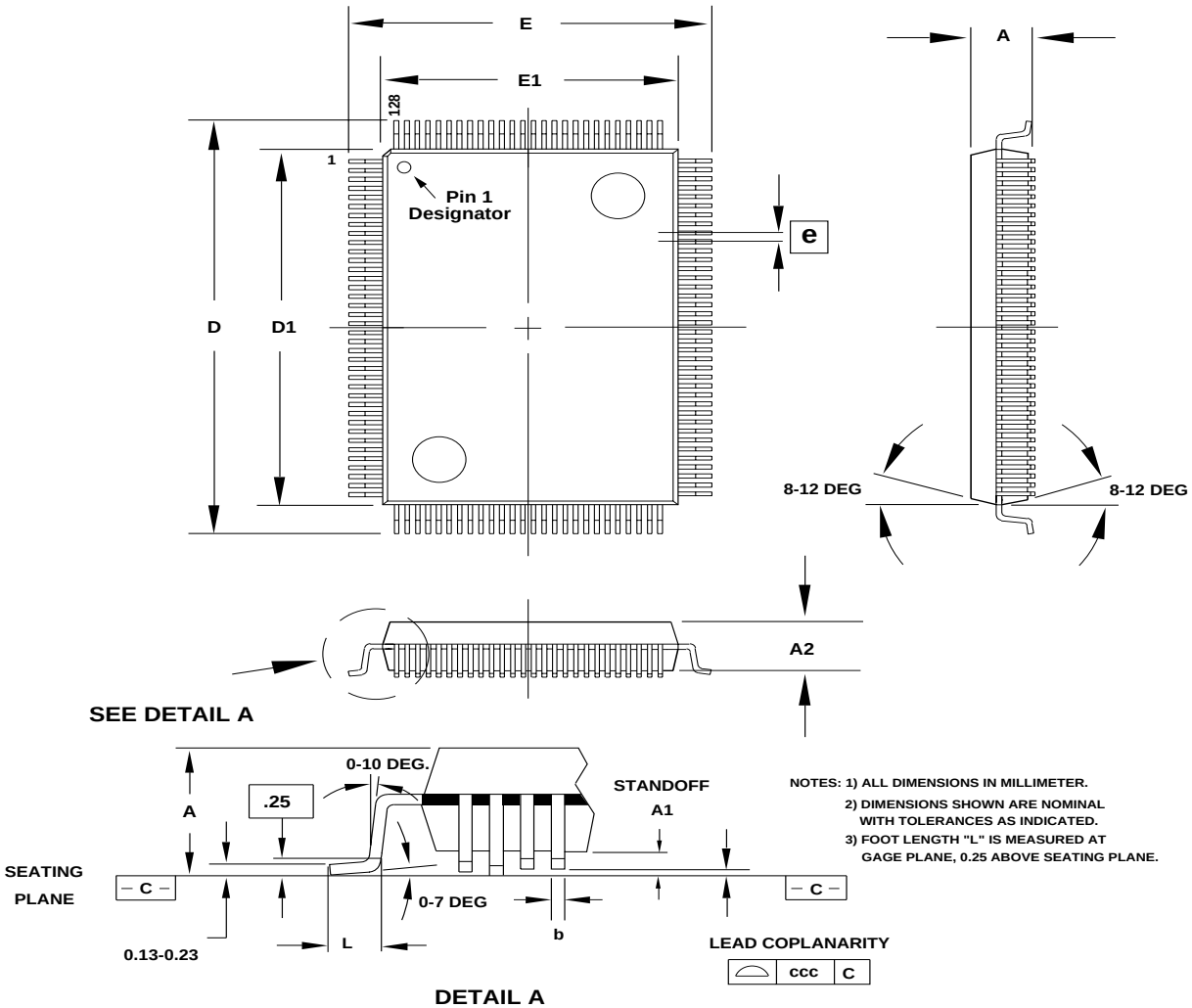
PART NO	Description
PM6344-RI	128 Plastic Quad Flat Pack (PQFP)

Table 27 - EQUAD Thermal Information

PART NO.	AMBIENT TEMPERATURE	Theta Ja	Theta Jc
PM6344-RI	-40°C to 85°C	50 °C/W	16 °C/W

20 MECHANICAL INFORMATION

Figure 51 - 128 Pin Copper Leadframe Plastic Quad Flat Pack (R Suffix)



PACKAGE TYPE: 128 PIN METRIC RECTANGULAR PLASTIC QUAD FLATPACK-MQFP											
BODY SIZE: 14 x 20 x 2.7 MM											
Dim.	A	A1	A2	D	D1	E	E1	L	e	b	ccc
Min.	2.82	0.25	2.57	22.95	19.90	16.95	13.90	0.73		0.17	
Nom.			2.70	23.20	20.00	17.20	14.00	0.88	0.50	0.22	
Max.	3.40	0.53	2.87	23.45	20.10	17.45	14.10	1.03		0.27	0.10

NOTES

NOTES

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