Low Cost Monolithic 12-Bit D/A Converter

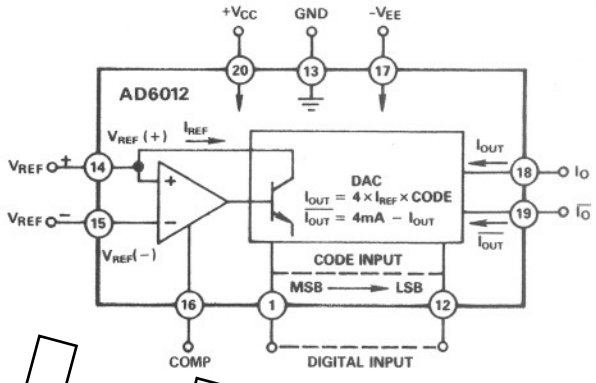
AD6012

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FEATURES

- 1/2LSB max Differential Linearity Error Over Temperature
- 250ns Typical Settling Time
- Full Scale Current 4mA
- High Speed Multiplying Capability
- TTL/CMOS/ECL/HTL Compatible
- High Output Compliance: −5V to +10V
- Complementary Current Outputs
- Low Power Consumption: 230mW

AD6012 FUNCTIONAL BLOCK DIAGRAM



20-PIN DUAL-IN-LINE PACKAGE

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PRODUCT DESCRIPTION

The AD6012 is an industry standard monolithic 12-bit digital-to-analog converter. Complementary current output and high speed multiplying capability make the AD6012 useful in a wide range of applications such as video displays, process control circuitry and fast A/D converters. The 6012 is the first D/A to achieve 12-bit differential linearity without the use of thin film resistors or active trimming. The 6012's unique circuit design insures monotonicity without the precision trimming associated with most other 12-bit DAC architectures.

The AD6012 is packaged in a 20-pin plastic DIP. The maximum differential linearity error of the AD6012N is guaranteed to be less than ±1LSB (±0.025%). Although tested and specified at ±15V, the AD6012 works well over a wide range of power supply voltages. Performance is essentially independent of supply voltage over the range of +5 volts, −12 volts to ±18 volts.

Guaranteed monotonicity and low cost make the AD6012 an ideal choice for high volume applications requiring fine local resolution. Typical applications include printer graphics and video displays. These applications need a minimum of 12 bits of resolution, although conformance to an ideal straight line from zero to full scale is less important.

PRODUCT HIGHLIGHTS

1. A segmented design technique guarantees monotonicity without the requirement of ultra precise internal components. Resistor tolerances can be as much as 8 times lower than that of conventional R-2R DAC designs while maintaining monotonicity over temperature. This advantage has been used in the AD6012 to provide 12-bit differential linearity over temperature without the use of laser trimmed thin film resistors.
2. The high output current of 4mA full scale accommodates the use of lower load impedances required in higher speed applications. Relatively high output voltages are obtained when small load impedances are used to minimize the output RC time constant.
3. Fully complementary current outputs effectively double the peak-to-peak output swing.
4. Less board space is used by the single width 20-pin dual-in-line package. Most other 12-bit DACs are packaged in larger 24-pin DIPs requiring more than twice the board area of the AD6012.
5. Reference circuit slew rate of 8mA/μs typical accommodates high speed multiplication applications.
6. The AD6012 is compatible with the industry standard 6012 in both pinout and specifications.

ORDERING INFORMATION

Model	Package	Temperature Range	Differential Nonlinearity
AD6012N	20-Pin Plastic DIP	0 to +70°C	±0.025%

SPECIFICATIONS (typical @ $+V_{CC} = +15V$, $-V_{EE} = -15V$, $I_{REF} = 1mA$ over specified temperature range unless otherwise specified)

MODEL	AD6012N MIN	TYP	MAX	UNITS
DATA INPUTS (Pins 1 to 12)				
TTL or 5 Volt CMOS				
Input Voltage				
Bit ON Logic "1"	+2.0			V
Bit OFF Logic "0"			+0.8	V
Logic Current (each bit)				
$V_{IN} = -5V$ to $+18V$			40	μA
RESOLUTION	12		12	Bits
OUTPUT				
Full Scale Current	3.935	3.999	4.063	mA
$V_{REF} = 10.000V$, $T_A = 25°C$				
$R_1 = R_2 = 10.000k\Omega$				
Full Scale Symmetry Error			±2.0	μA
Zero Scale Current			0.1	μA
Capacitance		20		pF
Compliance Voltage[1]				
$R_{OUT} > 10M\Omega$ typ	−5		+10	V
RELATIVE ACCURACY (error relative to full scale) T_{min} to T_{max}			±0.05	% FS
DIFFERENTIAL NONLINEARITY		±1/2	±1 (±0.025% FS)	LSB
	MONOTONICITY GUARANTEED			
FULL SCALE TEMPCO		10	40	ppm/°C
SETTLING TIME TO 1/2LSB				
All Bits ON-to-OFF or OFF-to-ON				
$T_A = 25°C$		250	500	ns
PROPAGATION DELAY				
50% to 50%		25	50	ns
TEMPERATURE RANGE				
Specified	0		70	°C
Operating	−25		+85	°C
POWER REQUIREMENTS				
Current				
$V_{CC} = +5V$ dc to $+15V$ dc		5.7	8.5	mA
$V_{EE} = -15V$		−13.7	−18	mA
Voltage				
V_{CC}	+4.5		+18	V
V_{EE}	−18		−10.8	V
POWER SUPPLY SENSITIVITY				
$V_{CC} = +13.5V$ to $+16.5V$,				
$V_{EE} = -15V$		±0.0005	±0.001	%FS/%
$V_{EE} = -13.5V$ to $-16.5V$,				
$V_{CC} = +15V$		±0.00025	±0.001	%FS/%
REFERENCE CURRENT RANGE	0.2	1.0	1.1	mA
REFERENCE BIAS CURRENT	0	−0.5	−2.0	μA
REFERENCE INPUT SLEW RATE				
$R_{IN} = 800\Omega$	4.0	8.0		mA/μs
POWER DISSIPATION				
$V_{CC} = +5V$, $V_{EE} = -15V$		234	312	mW
$V_{CC} = +15V$, $V_{EE} = -15V$		291	397	mW
PACKAGE OPTION[2]		N20A		

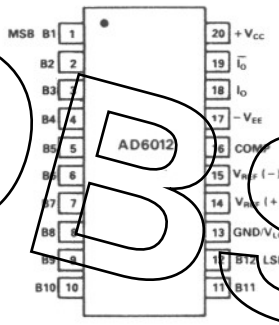
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NOTES
[1]D.N.L. specifications guaranteed over compliance range.
[2]See Section 19 for package outline information.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0 to +70°C
Storage Temperature	−65°C to +125°C
Power Supply Voltage	±18V
Logic Inputs	−5V to +18V
Voltage at Current Output Pins	−8V to +12V
Reference Inputs	$+V_{CC}$ to $-V_{EE}$, ±18V max Differential
Reference Input Current	1.25mA

PIN CONFIGURATION



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FUNCTIONAL DESCRIPTION

The segmented design of the AD6012, shown in the functional block diagram, insures that there are no significant differential nonlinearities in the transfer characteristic. The eight major carries of the most significant bits are not subject to the gross differential nonlinearities that can occasionally occur in an R-2R type DAC. This advantage is due to the fundamentally different way that the current is handled in an AD6012.

In a conventional R-2R type DAC, when the input code is incremented past a major carry, a current representing the new code is substituted for the sum of all the less significant bit currents that were previously on. To avoid any nonlinearities, the two total currents must be extremely well matched. In the case of the MSB major carry in a 12-bit DAC, the match must be better than one part in 2048 to maintain monotonicity. However, in the AD6012, a new current is never substituted for the sum of several smaller ones, but redirected through alternate channels and incremented one step at a time.

For example, consider the MSB carry in an AD6012. In the initial state of 011111111111 as shown in the functional block diagram, the switches in the segment generator are set in such a way that currents I_0, I_1 and I_2 are steered directly into the noninverting output I_{OUT}. In addition, a portion of I_3 is directed through the 9-bit DAC that is controlled by the 9 least significant bits into I_{OUT}. With the 9LSBs set to "1", all of the I_3 current is directed to I_{OUT} except for the 1/512 that goes to ground through the right-most transistor in the 9-bit DAC. After the input word is changed to 100000000000, the segment decoder switch for I_3 will be all the way to the right, the switch for I_4 will be in the middle, and all the switches in the 9-bit DAC will be to the left. I_{OUT} will be composed of I_0, I_1, I_2 and I_3. None of I_4 will be directed into I_{OUT} until a higher code is reached. In other words, I_3 is now steered directly to I_{OUT} instead of being divided by a factor of 511/512 in the 9-bit DAC. Since no major current substitution occurs, there is less chance of a large nonlinearity at this transition than in a comparable R-2R DAC.

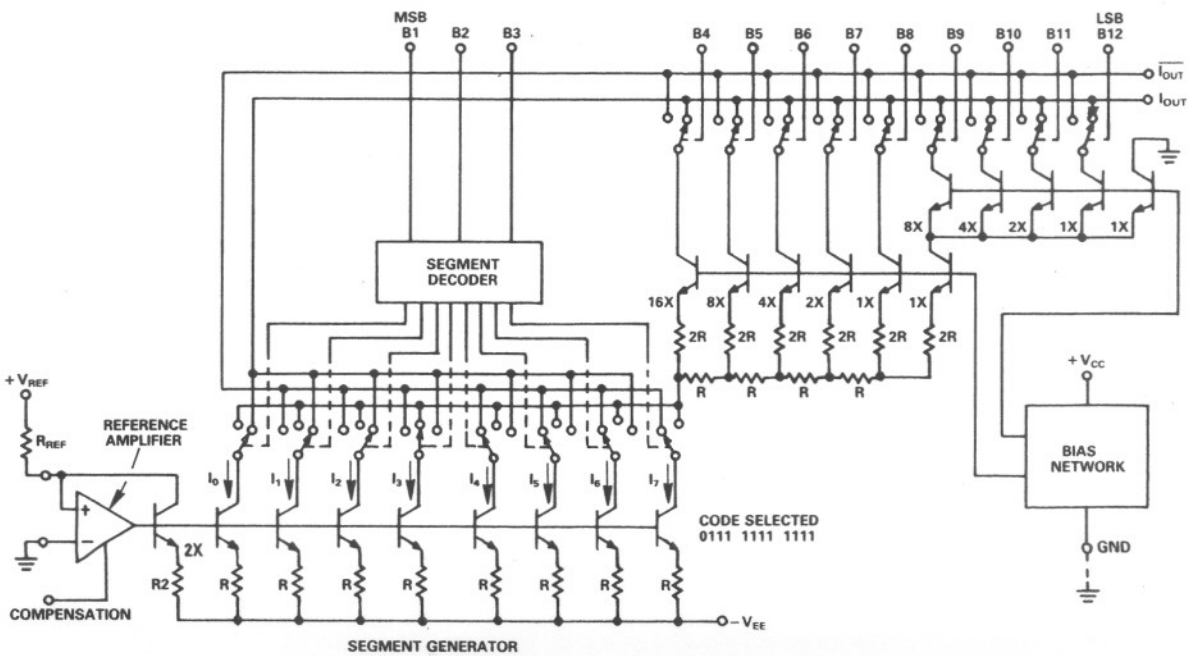


Figure 1. AD6012 Functional Block Diagram

RELATIVE ACCURACY VS. DIFFERENTIAL NON-LINEARITY

Analog Devices defines relative accuracy as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn between the lowest code output voltage and the highest code output voltage) for any bit combination. Relative accuracy is often referred to as nonlinearity. The DAC transfer function shown in Figure 2a has a bow that results in a maximum relative accuracy error of 3LSB. This must be distinguished from a differential linearity error. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 4mA full scale output, a change of 1LSB in digital input code should result in a 0.98μA change in the analog output current (1LSB = 4mA × 1/4096 = 0.98μA). If in actual use, however, a 1LSB change in the input code results in a change of only 0.24μA (1/4LSB) in output current, the differential linearity error would be 0.74μA or 3/4LSB.

The DAC of Figure 1 has very good differential linearity in spite of the poor relative accuracy. Conversely, the DAC of Figure 2 has very good relative accuracy but poor differential linearity. The anomaly in the middle of the transfer function is the result of a positive differential linearity error followed by a negative differential linearity error greater than 1LSB. A negative output step for an increase in digital input code is referred to as nonmonotonic behavior. In general, if a DAC has a differential linearity error specification greater than 1LSB, it may be non-monotonic at one or more of the major carries. In most cases the worst differential linearity error will occur at the MSB transition point.

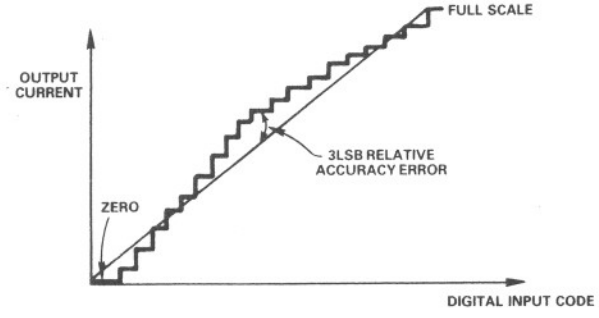


Figure 2a. Relative Accuracy Error

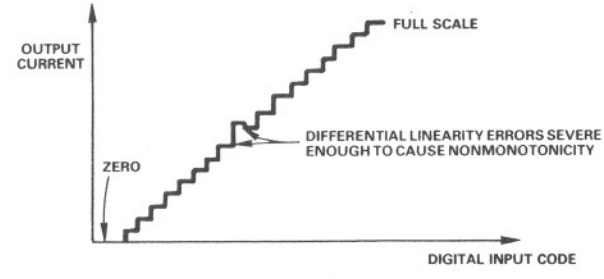


Figure 2b. Example of Nonmonotonic Behavior

As noted in the functional description, the 6012's unique design minimizes differential linearity errors at the transition points of the 3MSBs. This results in a tight specification on maximum differential nonlinearity over temperature. The AD6012N is specified at ±1LSB. Differential linearity is verified on all AD6012s with 100% final testing.

In many converter applications, uniform step size (or minimum differential linearity error) is more important than conformance to an ideal straight line. Twelve-bit converters are usually needed for high resolution rather than high linearity as evidenced by the fact that few transducers are more linear than 0.1%. This is also true in video graphics, where the human eye has difficulty discerning nonlinearity of less than 5%. The AD6012 is especially well suited for these applications since it has inherently low differential linearity error.

For applications requiring 12 bits of resolution and more accuracy than 0.05%, the AD565A and AD566A are recommended. These units feature 0.012% (1/2LSB) max accuracy error over temperature.

ANALOG CIRCUIT CONNECTIONS

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L, AD517L, AD741L, AD301AL, AD OP-07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). Unipolar zero will typically be within ±0.1LSB (plus op amp offset), and full scale accuracy will be within 0.5% (1.5% max).

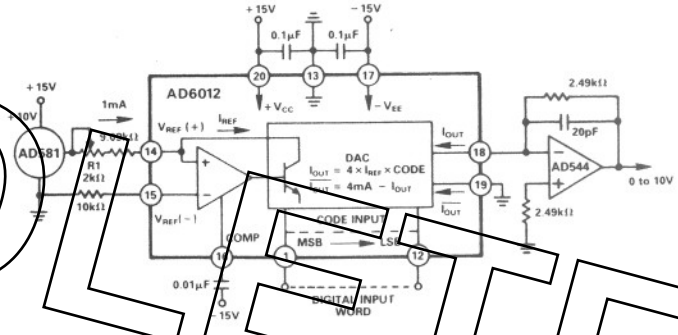


Figure 3. Unipolar 0 to 10V

FIGURE 3 UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. The following trim adjustment may not be necessary if the application can tolerate up to ±1 1/2% gain error.

Gain Adjust

Turn all bits ON and adjust 2kΩ gain trimmer R1, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.24V full scale is desired (exactly 2.5mV/bit), adjust R1 until the output is 10.2375 volts.

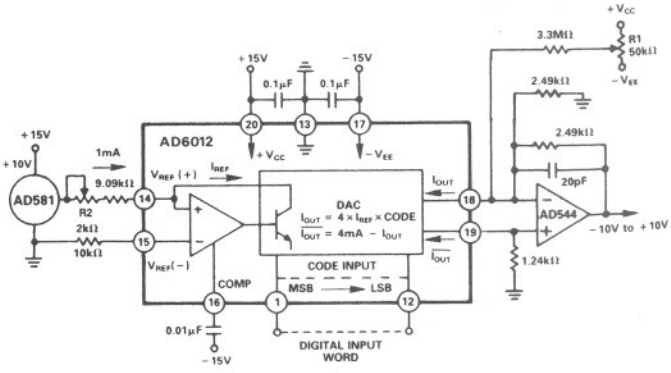


Figure 4. Bipolar −10V to +10V

FIGURE 4 BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from −10.000 to +9.995 volts, with positive full scale occurring with all bits ON (all 1s).

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Step I . . . Offset Adjust
Turn OFF all bits except the MSB. Adjust 50kΩ trimmer R1 to give 0.000 volts output.

Step II . . . Gain Adjust
Turn ON all bits. Adjust 2kΩ gain trimmer R2 to give a reading of +9.995 volts. Turn OFF all bits. The output should read −10.000 volts. It may be necessary to repeat steps 1 and 2 for the optimal calibration.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

OTHER VOLTAGE RANGES

The AD6012 can be easily configured for other voltage ranges by using either larger or smaller gain setting resistors and/or an offset resistor from the precision reference. For example, by substituting 1.24kΩ for the 2.49kΩ resistors and 625Ω for the 1.24kΩ resistor in Figure 4, the output voltage swing will be ±5V. A similar modification on the unipolar circuit of Figure 3 will yield an output voltage range of 0 to +5V.

In addition, the complement of the output voltage can be achieved by switching I_{OUT} and $\overline{I_{OUT}}$. Starting with the unipolar connection in Figure 3 and switching the outputs results in an output voltage swing of +10V to 0V. Specifically, an input of all zeros causes an output of +9.9976V, and all ones causes 0V. Going one step farther and shifting the output by the addition of a 2.49kΩ resistor from $\overline{I_{OUT}}$ to the 10V reference results in an output voltage going from 0 to −9.9976V. This circuit is shown in Figure 5.

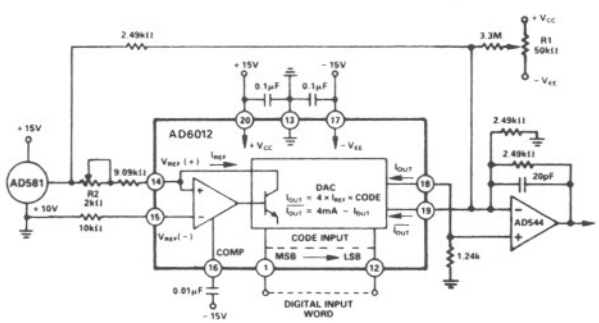


Figure 5. Negative Unipolar 0V to −10V

POWER SUPPLY DECOUPLING

As in any video speed circuit, low impedance ground returns and decoupled power supplies are critical for proper circuit operation. A minimum of 0.1μF bypass capacitor is recommended on the positive and negative supplies. In circuits with at least 400mV headroom on the negative supply, settling time can be enhanced with the RC decoupling circuit shown below:

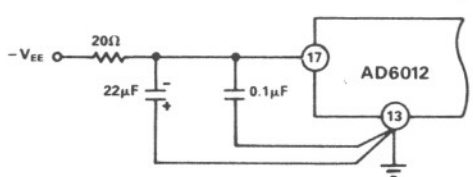


Figure 6.

OUTPUT VOLTAGE COMPLIANCE

The AD6012 has a typical output compliance range from −5V to +10V. The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, there is an equivalent output impedance of 10MΩ in parallel with 25pF at the output terminal which produces an equivalent error current if the voltage deviates from analog common. This is a linear effect which does not change with input code. Operation beyond the compliance limits may cause either output stage saturation or breakdown which results in nonlinear performance. Compliance limits are not affected by the positive power supply, but are a function of output current and negative supply, as shown in Figure 7.

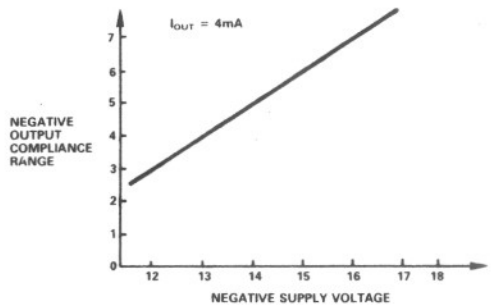


Figure 7. Typical Negative Compliance Range vs. Negative Supply

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DIRECT UNBUFFERED VOLTAGE OUTPUT FOR CABLE DRIVING

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. Figure 8 shows a connection using the gain and bipolar offset resistors to give a ±5V bipolar swing. In this situation, the digital code is complementary binary. Other combinations of gain and offset resistors can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 to −4mA output current and using the 10V reference voltage for bipolar offset. For example, setting R_X = 555Ω gives a ±1 volt range with a 500Ω equivalent output impedance.

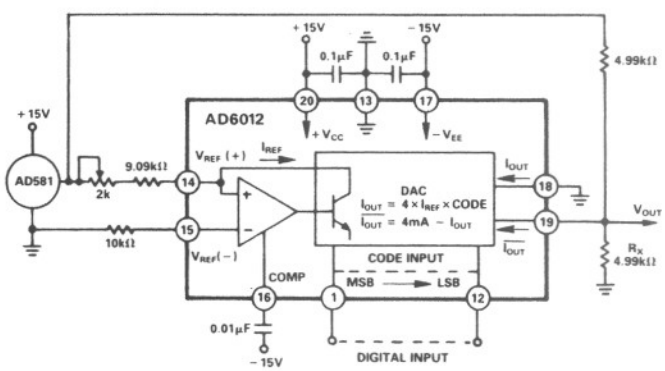


Figure 8. Unbuffered Bipolar Voltage Output

This connection is especially useful for direcly driving a long cable at high speed. Using a 51Ω resistor for R_X would allow interface to a 50Ω cable with a ±100mV full scale swing. Settling time would be very fast since the load impedance matches the characteristic impedance of the cable.

REFERENCE AMPLIFIER CONNECTIONS

The current into the reference amplifier at pin 14 must be approximately 1mA to realize the full scale output current of 4mA. If a dc reference is used, a 0.01μF compensation capacitor should be connected between pin 16 and $-V_{EE}$. However, for ac reference applications, a minimum value is often used for the compensation capacitor to maximize bandwidth. The value of this capacitor is dependent upon the equivalent resistance at pin 14. The values to maximize bandwidth without oscillation are as follows:

R14 Equiv. (kΩ)	C16 (pF)
10	50
5	25
2	10
1	5
0.5	0

HIGH SPEED 12-BIT A/D CONVERTERS

The fast settling characteristics of the AD6012 make it ideal for high speed successive approximation A/D converters.

Shown in Figure 9 is a configuration using standard components; this system completes a full 12-bit conversion in 8.5μs unipolar or bipolar. This converter will have 12 bits of resolution and have a typical gain T.C. of 10ppm/°C.

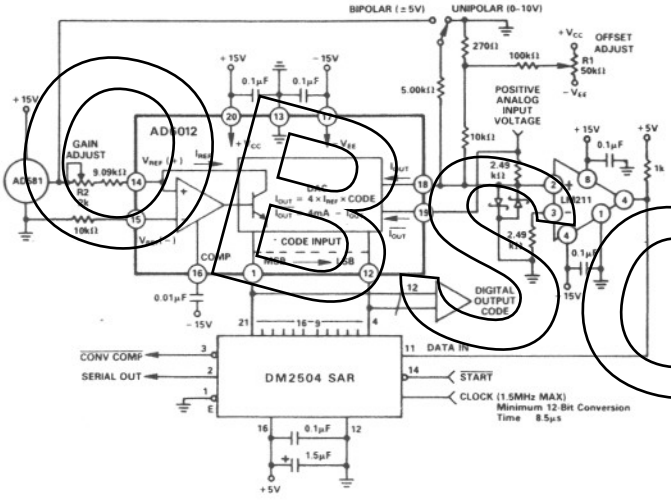


Figure 9. Analog-to-Digital Converter

In the unipolar mode, the system range is 0 to 9.9976 volts, with each bit having a value of 2.44mV. For true conversion accuracy, an A/D converter should be trimmed so that a given bit code output results from input levels from 1/2LSB below to 1/2LSB above the exact voltage which that code represents. Therefore, the converter zero point should be trimmed with an input voltage of +1.22mV; trim R1 until the LSB just begins to appear in the output code (all other bits "0"). For full scale, use an input voltage of +9.9963 volts (10 volts – 1LSB – 1/2LSB); then trim R2 until the LSB just begins to appear (all other bits "1").

The bipolar signal range is −5.0 to +4.9976 volts. Bipolar offset trimming is done by applying a −4.9988V input signal and trimming R1 for the LSB transition (all other bits "0"). Full scale is set by applying +4.9963 volts and trimming R2 for the LSB transition (all other bits "1").

For fastest operation, the impedance at the comparator summing node must be minimized. However, lowering the impedance will reduce the voltage signal to the comparator (at an equivalent impedance at the summing node of 1kΩ, 1LSB = 1.0mV) to the point that comparator performance will be sacrificed. The contribution to this impedance from the DAC will be approximately 10MΩ.

To prevent dynamic errors, the input signal should have a low dynamic source impedance, such as that of the AD509 high speed op amp.

D/A CONVERTER DISPLAYS

In Figure 10, a latched AD6012 is shown as a CRT deflection controller. Using the resistors shown, the output to the CRT yoke will swing ±110V. With a second AD6012 in the same configuration, both the vertical and horizontal position can be controlled. As in all vector scan schemes, this circuit provides a method of precisely locating the beam with minimum delay between locations. The AD6012 is an ideal choice in these applications since its settling time is only 500ns max. With a frame update time of 1/60th of a second, more than 33 thousand locations can be covered in each frame.

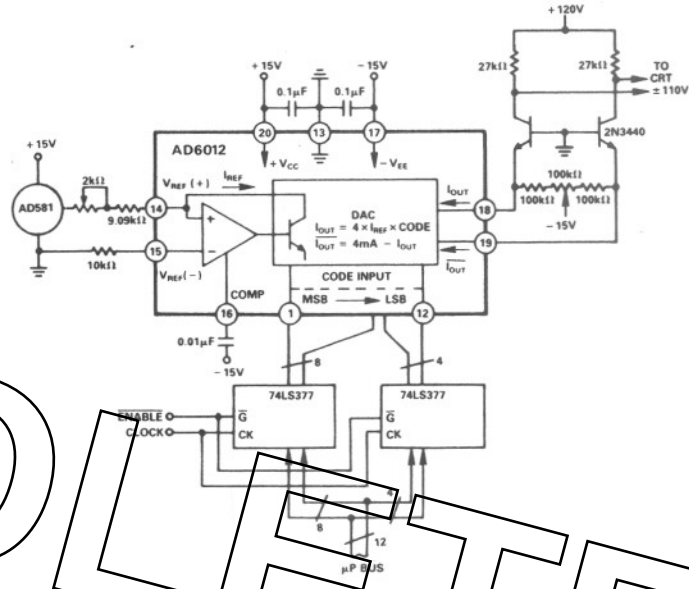
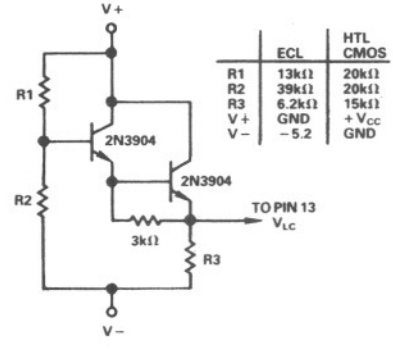


Figure 10. Vector Scan Video CRT Control

In raster scan applications, the AD6012 can be used for the slower vertical sweep. However, the horizontal sweep requires a settling time of 100ns or less to achieve a picture of suitable quality. In either vector or raster scan applications, a third AD6012 can be used for intensity modulation. In addition to its fast settling time, the reference can be clamped to zero whenever "blacker than black" is required (for retrace or lead zeroes in picture field).

LOGIC BIASING

The AD6012 can be used with many different logic families by setting GND/V_{LC} (Pin 13) at two diode drops below the desired logic threshold voltage. When GND/V_{LC} is connected to logic common, the AD6012 inputs interface directly to TTL. Other logic families can be connected directly to the logic inputs by using the logic bias circuit shown in Figure 11.



	ECL	HTL CMOS
R1	13kΩ	20kΩ
R2	39kΩ	20kΩ
R3	6.2kΩ	15kΩ
V+	GND	+V_{CC}
V−	−5.2	GND

Figure 11. HTL, CMOS, or ECL Bias Circuit

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