# SiT5001
## 1-80 MHz MEMS TCXO and VCTCXO

The Smart Timing Choice™

## Features

- Any frequency between 1 and 80 MHz accurate to 6 decimal places
- 100% pin-to-pin drop-in replacement to quartz-based (VC)TCXO
- Frequency stability as low as ±5 ppm. Contact SiTime for tighter stability options
- Ultra low phase jitter: 0.5 ps (12 kHz to 20 MHz)
- Voltage control option with pull range from ±12.5 ppm to ±50 ppm
- LVCMOS compatible output with SoftEdge™ option for EMI reduction
- Voltage control, standby, output enable or no connect modes
- Standard 4-pin packages: 2.5 x 2.0, 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm
- Outstanding silicon reliability of 2 FIT, 10 times better than quartz
- Pb-free, RoHs and REACH compliant

## Applications

- WiFi, 3G, LTE, SDI, Ethernet, SONET, DSL
- Telecom, networking, smart meter, wireless, test instrumentation




## Electrical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Output Frequency Range** | f | 1 | – | 80 | MHz | |
| **Initial Tolerance** | F_init | -1 | – | 1 | ppm | At 25°C after two reflows |
| **Stability Over Temperature** | F_stab | -5 | – | +5 | ppm | Over operating temperature range at rated nominal power supply voltage and load. (*see ordering codes on page 6*) **Contact SiTime for tighter stability options.** |
| **Supply Voltage** | F_vdd | – | 50 | – | ppb | ±10% Vdd (±5% for Vdd = 1.8V) |
| **Output Load** | F_load | – | 0.1 | – | ppm | 15 pF ±10% of load |
| **First year Aging** | F_aging | -2.5 | – | +2.5 | ppm | 25°C |
| **10-year Aging** | | -4.0 | – | +4.0 | ppm | 25°C |
| **Operating Temperature Range** | T_use | -20 | – | +70 | °C | Extended Commercial |
| | | -40 | – | +85 | °C | Industrial |
| **Supply Voltage** | Vdd | 1.71 | 1.8 | 1.89 | V | Contact SiTime for any other supply voltage options. |
| | | 2.25 | 2.5 | 2.75 | V | |
| | | 2.52 | 2.8 | 3.08 | V | |
| | | 2.70 | 3.0 | 3.3 | V | |
| | | 2.97 | 3.3 | 3.63 | V | |
| **Pull Range** | PR | ±12.5, ±25, ±50 | | | ppm | |
| **Upper Control Voltage** | VC_U | Vdd-0.1 | – | – | V | All Vdds. Voltage at which maximum deviation is guaranteed. |
| **Control Voltage Range** | VC_L | – | – | 0.1 | V | |
| **Control Voltage Input Impedance** | Z_vc | 100 | – | – | kΩ | |
| **Frequency Change Polarity** | – | Positive slope | | | – | |
| **Control Voltage -3dB Bandwidth** | V_BW | – | – | 8 | kHz | |
| **Current Consumption** | Idd | – | 31 | 33 | mA | No load condition, f = 20 MHz, Vdd = 2.5V, 2.8V or 3.3V. |
| | | – | 29 | 31 | mA | No load condition, f = 20 MHz, Vdd = 1.8V. |
| **OE Disable Current** | I_OD | – | – | 31 | mA | Vdd = 2.5V, 2.8V or 3.3V, OE = GND, output is Weakly Pulled Down |
| | | – | – | 30 | mA | Vdd = 1.8 V. OE = GND, output is Weakly Pulled Down |
| **Standby Current** | I_std | – | – | 70 | µA | Vdd = 2.5V, 2.8V or 3.3V, $\overline{ST}$ = GND, output is Weakly Pulled Down. |
| | | – | – | 10 | µA | Vdd = 1.8V. $\overline{ST}$ = GND, output is Weakly Pulled Down. |
| **Duty Cycle** | DC | 45 | – | 55 | % | All Vdds |
| **LVCMOS Rise/Fall Time** | Tr, Tf | – | 1.5 | 2 | ns | LVCMOS option. Default rise/fall time, All Vdds, 10% - 90% Vdd. |
| **SoftEdge™ Rise/Fall Time** | | SoftEdge™ Rise/Fall Time Table | | | ns | SoftEdge™ option. Frequency and supply voltage dependent. |
| **Output Voltage High** | VOH | 90% | – | – | Vdd | OH = -7 mA, IOL = 7 mA, (Vdd = 3.3V, 3.0V)<br>IOH = -4 mA, IOL = 4 mA, (Vdd = 2.8V, 2.5V)<br>IOH = -2 mA, IOL = 2 mA, (Vdd = 1.8V) |
| **Output Voltage Low** | VOL | – | – | 10% | Vdd | |
| **Input Voltage High** | VIH | 70% | – | – | Vdd | Pin 1, OE or $\overline{ST}$ |
| **Input Voltage Low** | VIL | – | – | 30% | Vdd | Pin 1, OE or $\overline{ST}$ |
| **Input Pull-up Impedance** | Z_in | – | 100 | 250 | kΩ | |

## Electrical Characteristics (continued)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Startup Time** | T_start | – | – | 10 | ms | Measured from the time Vdd reaches its rated minimum value |
| **OE Enable/Disable Time** | T_oe | – | – | 150 | ns | f = 80 MHz. For other frequencies, T_oe = 100 ns + 3 cycles |
| **Resume Time** | T_resume | – | 6 | 10 | ms | Measured from the time ST pin crosses 50% threshold |
| **RMS Period Jitter** | T_jitt | – | 1.7 | 2 | ps | f = 10 MHz, Vdd = 2.5V, 2.8V or 3.3V |
| | | – | 1.7 | 2 | ps | f = 10 MHz, Vdd = 1.8V |
| **RMS Phase Jitter (random)** | T_phj | – | 0.5 | 1 | ps | f = 10 MHz, Integration bandwidth = 12 kHz to 20 MHz, All Vdds |

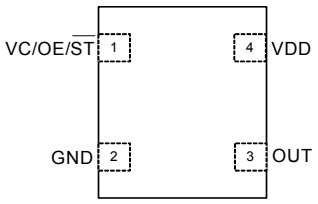
**Note:**

1. All electrical specifications in the above table are measured with 15pF output load, Contact SiTime for higher drive options.

## Pin Configuration

| Pin | Symbol | Functionality | |
|---|---|---|---|
| 1 | VC/OE/$\overline{ST}$/NC | V control | Voltage control |
| | | Output Enable | H or Open[2]: specified frequency output<br>L: output is high impedance. Only output driver is disabled. |
| | | Standby | H or Open[2]: specified frequency output<br>L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I_std. |
| | | NC | No connect (input receiver off) |
| 2 | GND | Power | Electrical and case ground |
| 3 | CLK | Output | Oscillator output |
| 4 | VDD | Power | Power supply voltage |

**Top View**




**Note:**

2. A pull-up resistor of <10 kΩ between OE/ $\overline{ST}$ pin and Vdd is recommended in high noise environment when the device operates in OE/$\overline{ST}$ mode.

## Absolute Maximum

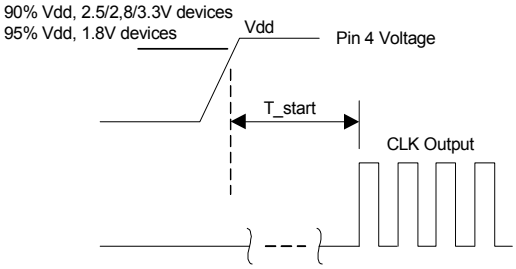
Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

| Parameter | Min. | Max. | Unit |
|---|---|---|---|
| **Storage Temperature** | -65 | 150 | °C |
| **VDD** | -0.5 | 4 | V |
| **Electrostatic Discharge** | – | 2000 | V |
| **Soldering Temperature (follow standard Pb free soldering guidelines)** | – | 260 | °C |

## Environmental Compliance

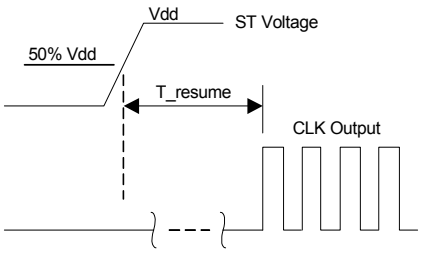
| Parameter | Condition/Test Method |
|---|---|
| **Mechanical Shock** | **MIL-STD-883F, Method 2002** |
| **Mechanical Vibration** | **MIL-STD-883F, Method 2007** |
| **Temperature Cycle** | **JESD22, Method A104** |
| **Solderability** | **MIL-STD-883F, Method 2003** |
| **Moisture Sensitivity Level** | **MSL1 @ 260°C** |

## Timing Diagram




T_start: Time to start from power-off

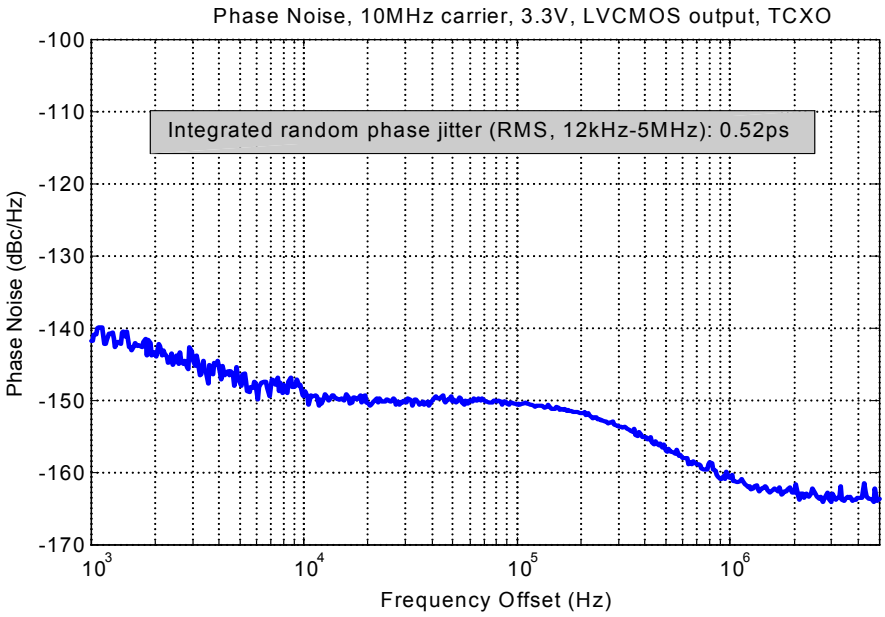
**(ST/OE Mode)**




T_resume: Time to resume from ST

**(ST Mode Only)**

## Phase Noise Plot



## SoftEdge™ Option

The SoftEdge™ output is available as a standard option for the SiT500x family of MEMS (VC)TCXOs. It is typically used for EMI reduction similar to that of the clipped sinewave output common to many quartz based TCXOs.

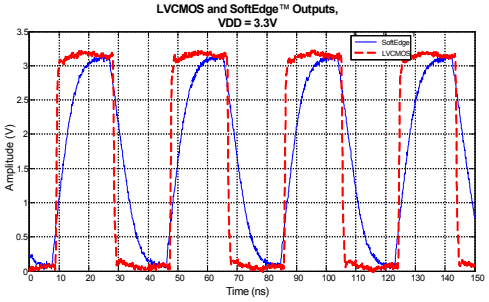
In the SoftEdge™ mode, the slower rise/fall edges of the output waveform reduce the higher clock harmonics in a digital clock signal, minimizing EMI radiation at these harmonics. The table below show the actual rise/fall time in relation to the desired output frequency and the supply voltage with a 10 kΩ / 10pF load. Rail-to-rail swing of the output is maintained for these supported frequencies.

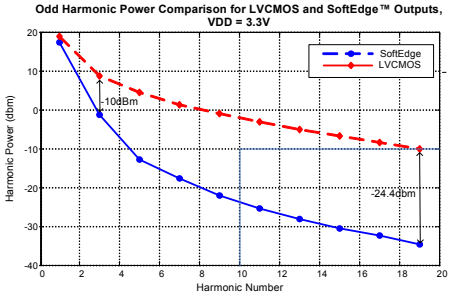
## Rise/Fall Time for SoftEdge™ Option

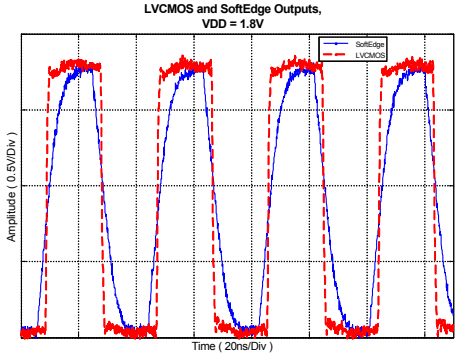
| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Rise/Fall Time** | Tr, Tf | 4.0 | 6.5 | 9.5 | ns | 1-26 MHz, 1.8V, 3.0 and 3.3V, MHz 10k and 10 pF, 20%-80% Vd |
| | | 2.5 | 4.0 | 6.0 | ns | 1-26 MHz, 2.5V and 2.8V, MHz 10k and 10 pF, 20%-80% Vdd |
| | | 1.5 | 3.5 | 5.0 | ns | 26-50 MHz, 1.8V, 3.0V and 3.3V, MHz 10k and 10 pF, 20%-80% Vdd |
| | | 1.5 | 2.5 | 4.5 | ns | 26-50 MHz, 2.5V and 2.8V, MHz 10k and 10 pF, 20%-80% Vdd |

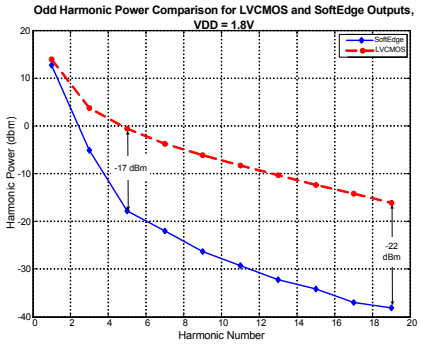
## SoftEdge™ Waveform Examples and Corresponding Harmonics Reduction

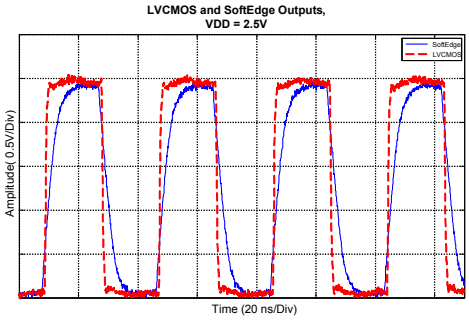
Figures below illustrate the harmonic power reduction as the rise/fall times are slowed from the standard squarewave output to that of the SoftEdge™ output. In general, the 1.8V device shows the lowest harmonics and provides best EMI performance comparing to devices with higher operating voltages.

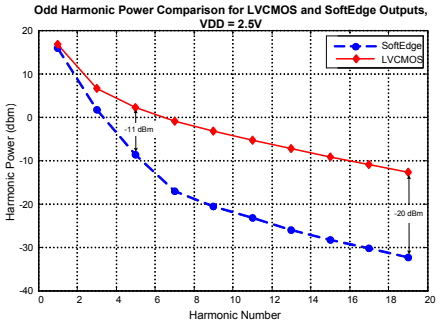


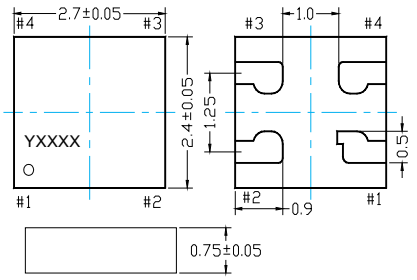
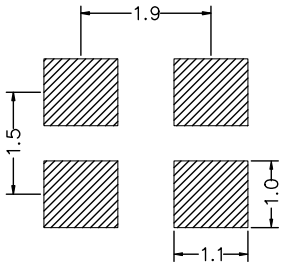
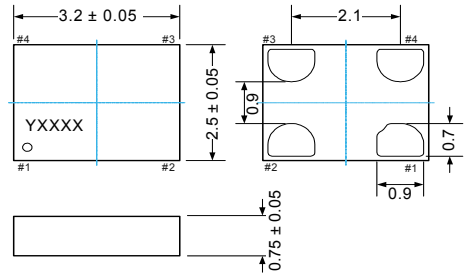
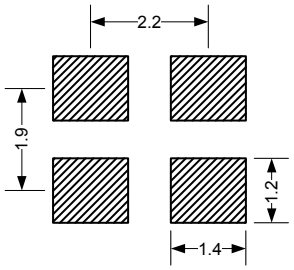
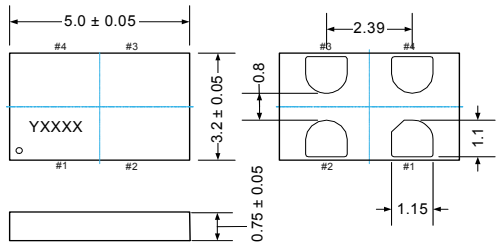
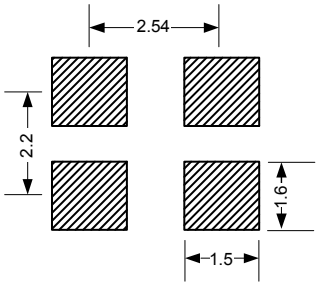
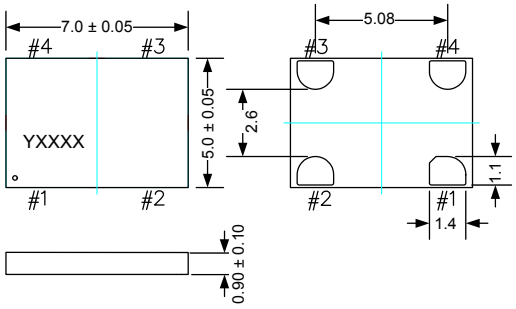
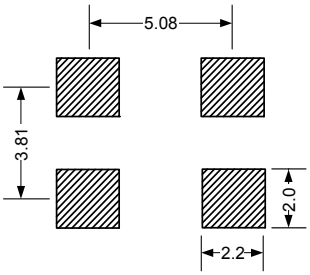



## Dimensions and Patterns

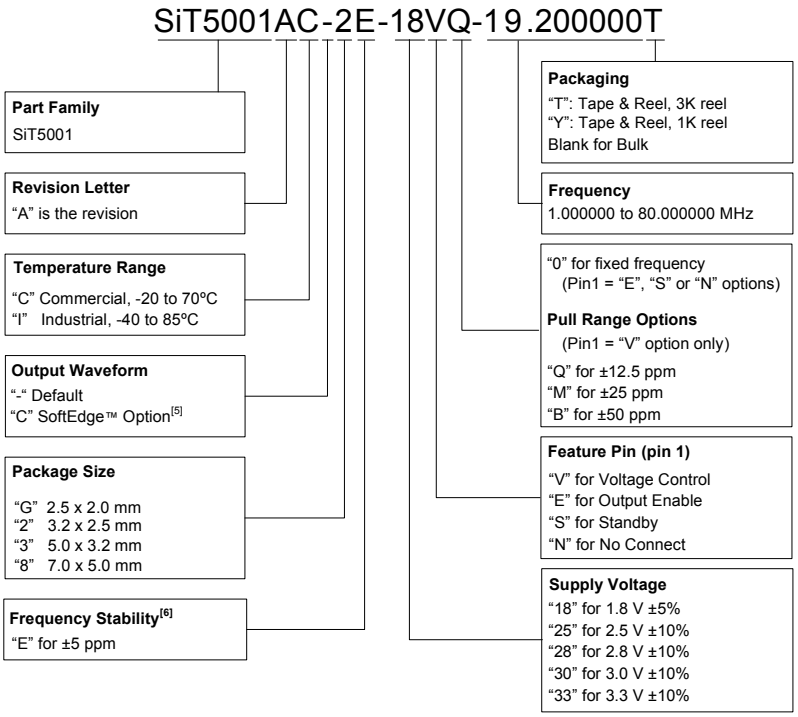
| Package Size – Dimensions (Unit: mm) [3] | Recommended Land Pattern (Unit: mm) [4] |
|---|---|
| **2.7 x 2.4 x 0.75 mm (100% compatible with 2.5 x 2. 0 mm footprint)** | |
|  |  |
| **3.2 x 2.5 x 0.75 mm** | |
|  |  |
| **5.0 x 3.2 x 0.75 mm** | |
|  |  |
| **7.0 x 5.0 x 0.90 mm** | |
|  |  |

**Notes:**

3. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
4. A capacitor of value 0.1 µF between Vdd and GND is recommended.

## Ordering Information

**The Part No. Guide is for reference only. To customize and build an exact part number, use the SiTime Part Number Generator.**




**Notes:**

5. SiTime's SoftEdge™ output waveform with 6 ns rise/fall time reduces EMI and is similar to clipped sine wave in functionality.
6. Contact SiTime for tighter stability options.

## Additional Information

| Document | Description | Download Link |
|---|---|---|
| **Manufacturing Notes** | Tape & Reel dimension, reflow profile and other manufacturing related info | http://www.sitime.com/component/docman/doc_download/85-manufacturing-notes-for-sitime-oscillators |
| **Qualification Reports** | RoHS report, reliability reports, composition reports | http://www.sitime.com/support/quality-and-reliability |
| **Performance Reports** | Additional performance data such as phase noise, current consumption and jitter for selected frequencies | http://www.sitime.com/support/performance-measurement-report |
| **Termination Techniques** | Termination design recommendations | http://www.sitime.com/support/application-notes |
| **Layout Techniques** | Layout recommendations | http://www.sitime.com/support/application-notes |

## Revision History

| Version | Release Date | Change Summary |
|---|---|---|
| 1.0 | 11/12/15 | Final production release<br>• Revised initial tolerance, stability over temperature and first/10 year aging values in the electrical characteristics table<br>• Revised frequency stability option |

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# Supplemental Information

The Supplemental Information section is not part of the datasheet and is for informational purposes only.

# Silicon MEMS Outperforms Quartz

# Silicon MEMS Outperforms Quartz

The Smart Timing Choice™

## Best Reliability

Silicon is inherently more reliable than quartz. Unlike quartz suppliers, SiTime has in-house MEMS and analog CMOS expertise, which allows SiTime to develop the most reliable products. Figure 1 shows a comparison with quartz technology.

**Why is SiTime Best in Class:**

- SiTime's MEMS resonators are vacuum sealed using an advanced EpiSeal™ process, which eliminates foreign particles and improves long term aging and reliability
- World-class MEMS and CMOS design expertise

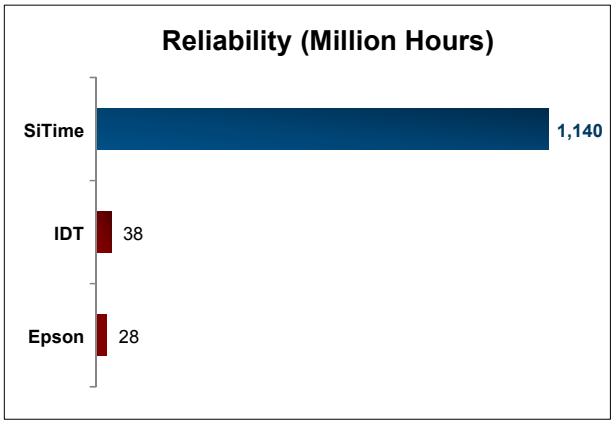



**Figure 1. Reliability Comparison[1]**

## Best Aging

Unlike quartz, MEMS oscillators have excellent long term aging performance which is why every new SiTime product specifies 10-year aging. A comparison is shown in Figure 2.

**Why is SiTime Best in Class:**

- SiTime's MEMS resonators are vacuum sealed using an advanced EpiSeal process, which eliminates foreign particles and improves long term aging and reliability
- Inherently better immunity of electrostatically driven MEMS resonator

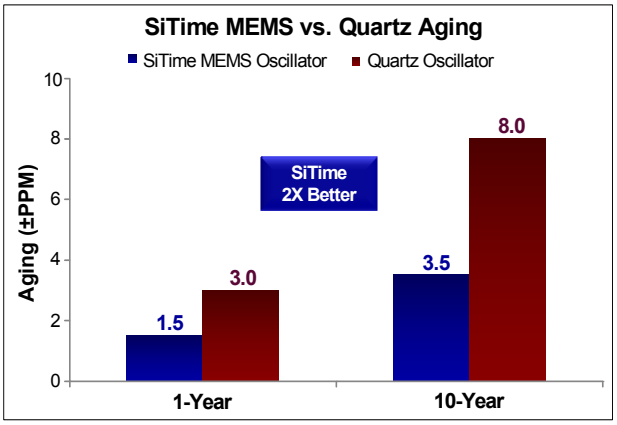



**Figure 2. Aging Comparison[2]**

## Best Electro Magnetic Susceptibility (EMS)

SiTime's oscillators in plastic packages are up to 54 times more immune to external electromagnetic fields than quartz oscillators as shown in Figure 3.

**Why is SiTime Best in Class:**

- Internal differential architecture for best common mode noise rejection
- Electrostatically driven MEMS resonator is more immune to EMS

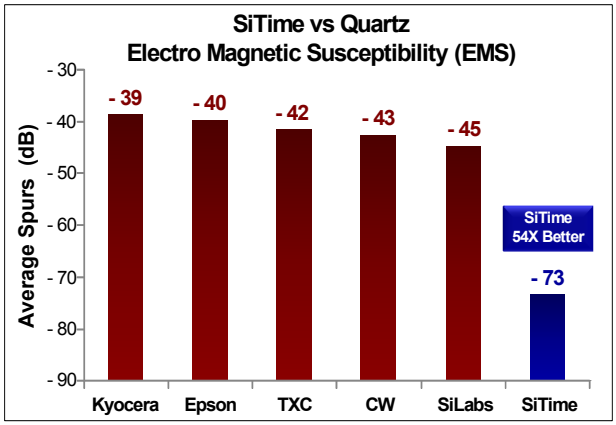



**Figure 3. Electro Magnetic Susceptibility (EMS)[3]**

## Best Power Supply Noise Rejection

SiTime's MEMS oscillators are more resilient against noise on the power supply. A comparison is shown in Figure 4.

**Why is SiTime Best in Class:**

- On-chip regulators and internal differential architecture for common mode noise rejection
- Best analog CMOS design expertise

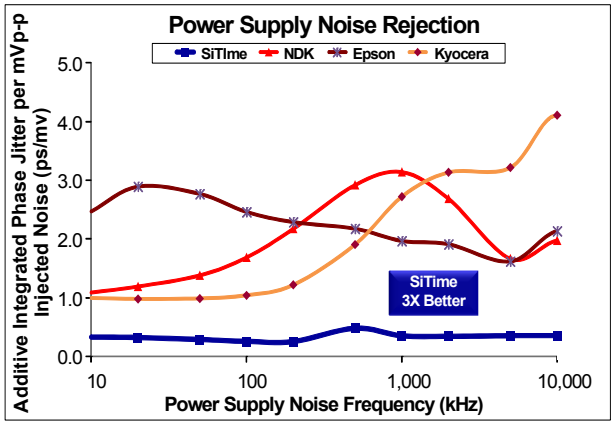



**Figure 4. Power Supply Noise Rejection[4]**

# Silicon MEMS Outperforms Quartz

The Smart Timing Choice™

## Best Vibration Robustness

High-vibration environments are all around us. All electronics, from handheld devices to enterprise servers and storage systems are subject to vibration. Figure 5 shows a comparison of vibration robustness.

**Why is SiTime Best in Class:**

- The moving mass of SiTime's MEMS resonators is up to 3000 times smaller than quartz
- Center-anchored MEMS resonator is the most robust design

## Best Shock Robustness

SiTime's oscillators can withstand at least 50,000 *g* shock. They all maintain their electrical performance in operation during shock events. A comparison with quartz devices is shown in Figure 6.

**Why is SiTime Best in Class:**

- The moving mass of SiTime's MEMS resonators is up to 3000 times smaller than quartz
- Center-anchored MEMS resonator is the most robust design

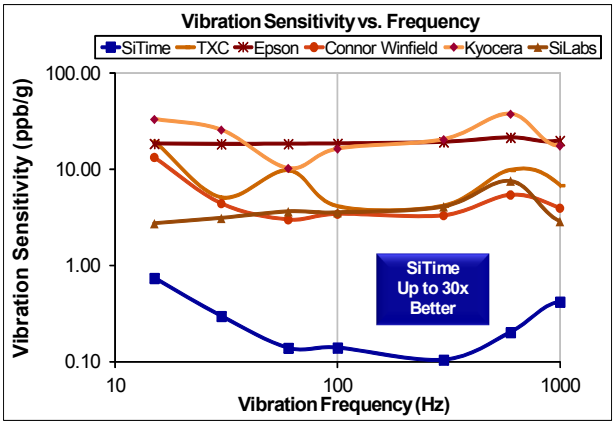



**Figure 5. Vibration Robustness[5]**

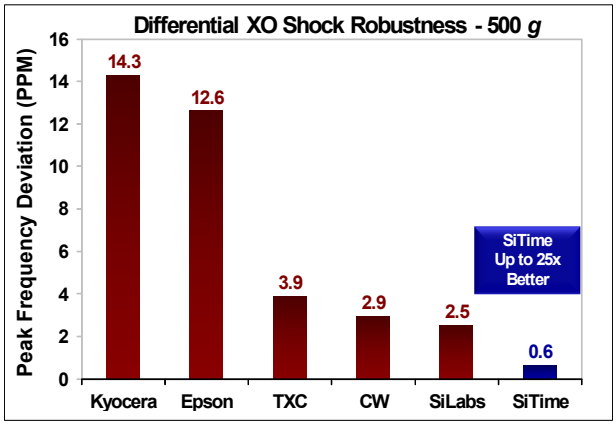



**Figure 6. Shock Robustness[6]**

**Notes:**

1. Data Source: Reliability documents of named companies.
2. Data source: SiTime and quartz oscillator devices datasheets.
3. Test conditions for Electro Magnetic Susceptibility (EMS):
   - According to IEC EN61000-4.3 (Electromagnetic compatibility standard)
   - Field strength: 3V/m
   - Radiated signal modulation: AM 1 kHz at 80% depth
   - Carrier frequency scan: 80 MHz – 1 GHz in 1% steps
   - Antenna polarization: Vertical
   - DUT position: Center aligned to antenna

   **Devices used in this test:**
   SiTime, SiT9120AC-1D2-33E156.250000 - MEMS based - 156.25 MHz
   Epson, EG-2102CA 156.2500M-PHPAL3 - SAW based - 156.25 MHz
   TXC, BB-156.250MBE-T - 3rd Overtone quartz based - 156.25 MHz
   Kyocera, KC7050T156.250P30E00 - SAW based - 156.25 MHz
   Connor Winfield (CW), P123-156.25M - 3rd overtone quartz based - 156.25 MHz
   SiLabs, Si590AB-BDG - 3rd overtone quartz based - 156.25 MHz
4. 50 mV pk-pk Sinusoidal voltage.
   **Devices used in this test:**
   SiTime, SiT8208AI-33-33E-25.000000, MEMS based - 25 MHz
   NDK, NZ2523SB-25.6M - quartz based - 25.6 MHz
   Kyocera, KC2016B25M0C1GE00 - quartz based - 25 MHz
   Epson, SG-310SCF-25M0-MB3 - quartz based - 25 MHz
5. **Devices used in this test:** same as EMS test stated in Note 3.
6. Test conditions for shock test:
   - MIL-STD-883F Method 2002
   - Condition A: half sine wave shock pulse, 500-g, 1ms
   - Continuous frequency measurement in 100 µs gate time for 10 seconds

   **Devices used in this test:** same as EMS test stated in Note 3
7. Additional data, including setup and detailed results, is available upon request to qualified customers. Please contact productsupport@sitime.com.

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