

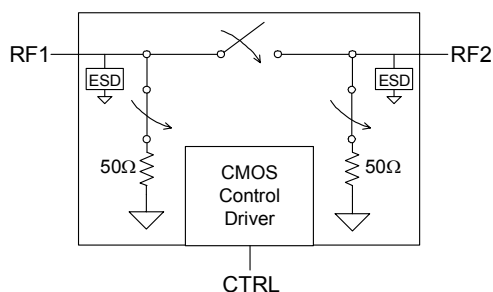
Product Description

The PE4246 RF Switch is designed to cover a broad range of applications from 1 to 5000 MHz. It is non-reflective at both RF1 and RF2 ports. This SPST switch integrates a single-pin CMOS control interface, and provides low insertion loss while operating with extremely low bias from a single +3-volt supply. In a typical application, the high isolation PE4246 can replace multiple RF switches of lesser isolation performance. It is offered in a small 3x3 mm DFN package.

The PE4246 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

Peregrine Specification 71/0008



Absorptive SPST UltraCMOS™ RF Switch: 1 - 5000 MHz

Features

- Non-reflective 50-ohm RF switch
- 50-ohm (0.25 watt) terminations
- High isolation: 55 dB at 1000 MHz, 48 dB at 3000 MHz
- Low insertion loss: 0.8 dB at 1000 MHz, 0.9 dB at 3000 MHz
- High linearity: +33 dBm input 1dB compression point
- CMOS/TTL single-pin control
- Single +3-volt supply operation
- Extremely low bias: 33 μ A @ 3 V
- Available in a 6-lead DFN package

Figure 2. Package Type

6-lead DFN

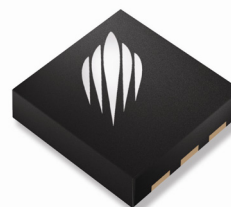


Table 1. Electrical Specifications @ +25 °C, V_{DD} = 3 V (Z_S = Z_L = 50 Ω)

Parameter	Condition	Minimum	Typical	Maximum	Units
Operation Frequency ¹		1		5000	MHz
Operating Power	CTRL=1/CTRL=0			30/24	dBm
Insertion Loss	1-2000 MHz		0.8	1.0	dB
	2000-3000 MHz		0.9	1.1	dB
	3000-4000 MHz		1.0	1.3	dB
	4000-5000 MHz		1.3	1.8	dB
Isolation	1-2000 MHz	49	55		dB
	2000-3000 MHz	45	48		dB
	3000-4000 MHz	43	46		dB
	4000-5000 MHz	40	44		dB
Return Loss	1-5000 MHz	11	20		dB
Input 1 dB Compression ³	1-5000 MHz	30	33		dBm
Input IP3	1-5000 MHz	50			dBm
Video Feedthrough ²				15	mV _{pp}
Switching Time			2		μ s

Notes: 1. Device linearity will begin to degrade below 1 MHz.

2. The DC transient at the output of the switch when the control voltage is switched from Low to High or High to Low in a 50 Ω test set-up, measured with 1ns risetime pulses and 500 MHz bandwidth.

3. Note Absolute Maximum ratings in Table 3.

Figure 3. Pin Configuration

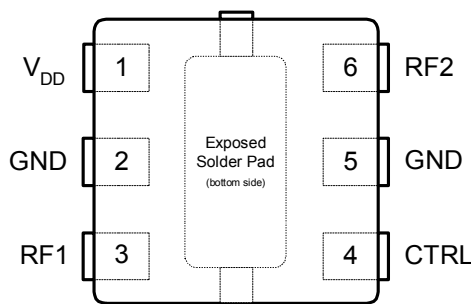


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	V _{DD}	Nominal 3 V supply connection. ¹
2	GND	Ground connection. ³
3	RF1	RF port. ²
4	CTRL	CMOS or TTL logic level: High = RF1 to RF2 signal path Low = RF1 isolated from RF2
5	GND	Ground connection. ³
6	RF2	RF port. ²

Notes: 1. A bypass capacitor should be placed as close as possible to the pin.
2. Both RF pins must be DC blocked by an external capacitor or held at 0 V_{DC}.
3. The exposed pad must be soldered to the ground plane for proper switch performance.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V _{DD}	Power supply voltage	-0.3	4.0	V
V _I	Voltage on CTRL input	-0.3	5.5	V
T _{ST}	Storage temperature	-65	150	°C
P _{IN}	Input power (50 Ω), CTRL=1/CTRL=0		33/24	dBm
V _{ESD}	ESD voltage (Human Body Model)		200	V

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE4246 in the 6-lead 3x3 DFN package is MSL1.

Device Description

The PE4246 high-isolation SPST RF Switch is designed to support a variety of applications where high isolation performance is demanded and a non-reflective input and output is desired. This switch is able to replace multiple lesser performing switches in a very small 3x3 mm DFN footprint.

Table 4. Operating Ranges

Parameter	Min	Typ	Max	Unit
V _{DD} Power Supply	2.7	3.0	3.3	V
I _{DD} Power Supply Current (V _{DD} = 3 V, V _{CTRL} = 3 V)		33	40	μA
T _{OP} Operating temperature	-40		85	°C
Control Voltage High	0.7xV _{DD}		5	V
Control Voltage Low	0		0.3xV _{DD}	V

Table 5. Control Logic Truth Table

Control Voltage	Signal Path
CTRL = CMOS or TTL High	RF1 to RF2
CTRL = CMOS or TTL Low	RF1 isolated from RF2

Control Logic

The control logic input pin (CTRL) is typically driven by a 3-volt CMOS logic level signal, and has a threshold of 50% of V_{DD}. For flexibility to support systems that have 5-volt control logic drivers, the control logic input has been designed to handle a 5-volt logic HIGH signal. (A minimal current will be sourced out of the V_{DD} pin when the control logic input voltage level exceeds V_{DD}.)

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 3.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Typical Performance Data @ 25 °C (Unless Otherwise Noted)

Figure 4. Insertion Loss
T = -40 °C to 85 °C

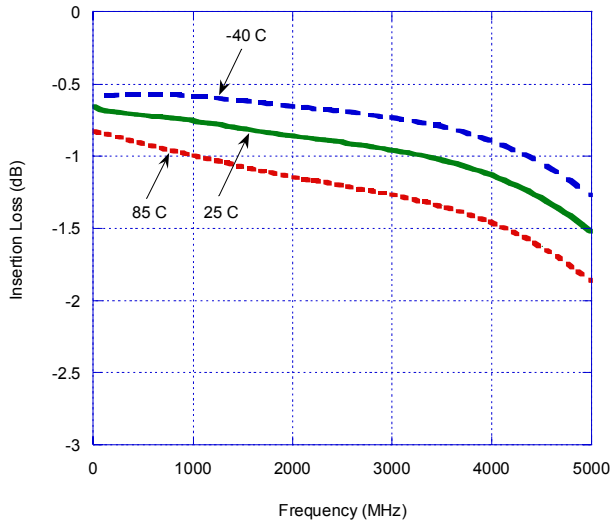


Figure 5. Input 1dB Compression Point and IIP3

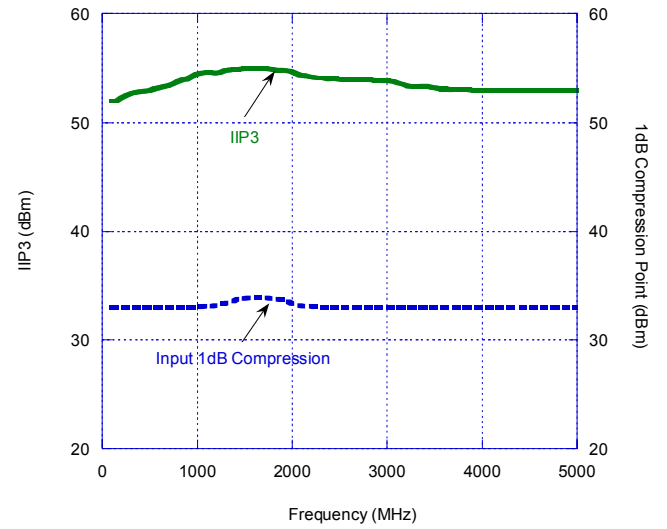
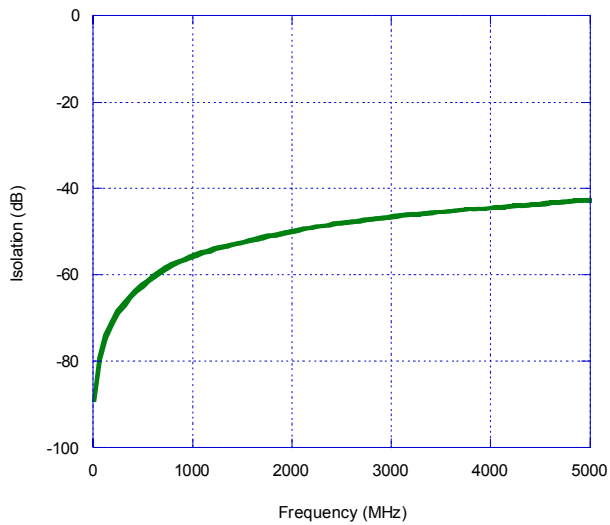


Figure 6. Isolation



Typical Performance Data @ +25 °C

Figure 7. RF1 Return Loss (CTRL = High)

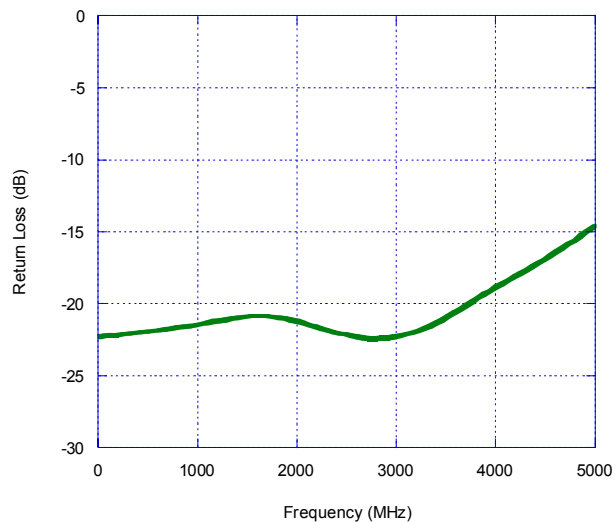


Figure 8. RF2 Return Loss (CTRL = High)

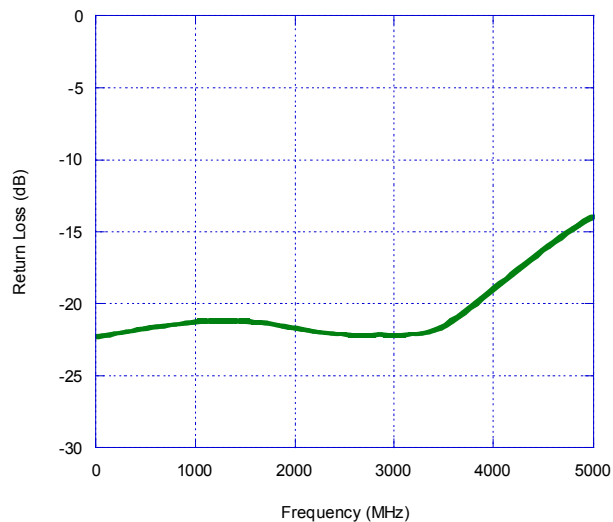


Figure 9. RF1 Return Loss (CTRL = Low)

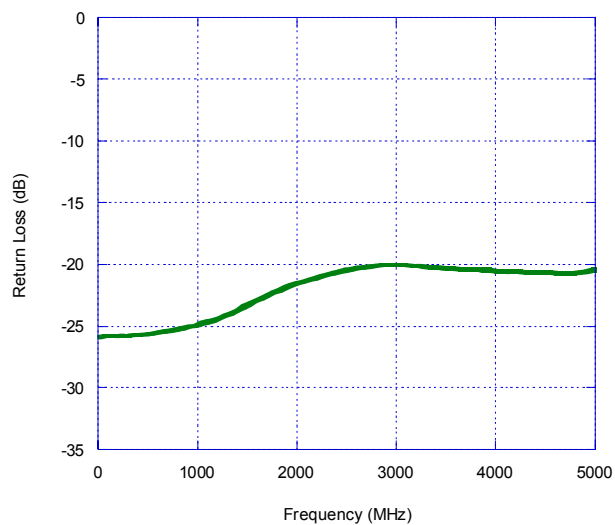
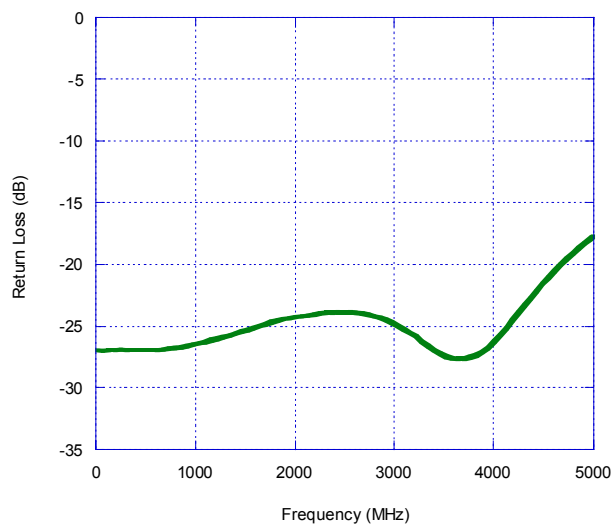


Figure 10. RF2 Return Loss (CTRL = Low)



Evaluation Kit

The SPST Switch Evaluation Kit board was designed to ease customer evaluation of the PE4246 SPST switch. The RF1 port is connected through a 50 Ω transmission line to the top left SMA connector, J1. The RF2 port is connected through a 50 Ω transmission line to the top right SMA connector, J2. A through transmission line connects SMA connectors J3 and J4. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide model with trace width of 0.0476", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0021" and ϵ_R of 4.3. Note that the predominate mode for these transmission lines is coplanar waveguide with a ground plane.

J5 and J6 provide a means for controlling DC and digital inputs to the device. J6-1 is connected to the device V_{DD} input. J5-1 is connected to the device CTRL input. J5-2 and J6-2 are GND connections. A decoupling capacitor (100 pF) is provided on both CTRL and V_{DD} traces. It is the responsibility of the customer to determine proper supply decoupling for their design application. Removing these components from the evaluation board has not been shown to degrade RF performance.

Figure 11. Evaluation Board Layouts

Peregrine Specification 101/0102

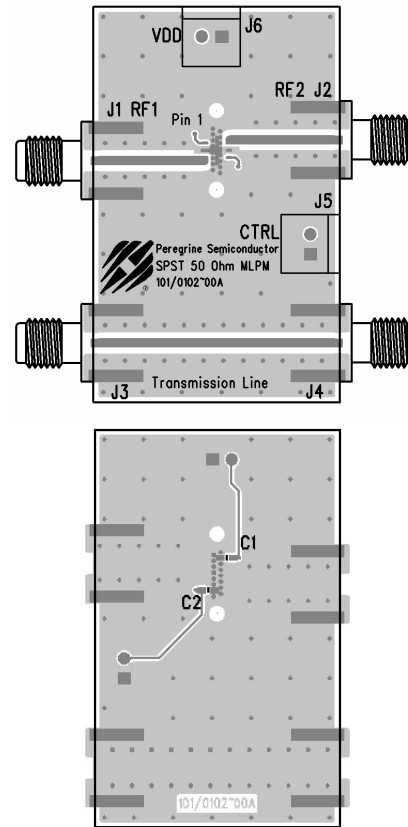


Figure 12. Evaluation Board Schematic

Peregrine Specification 102/0134

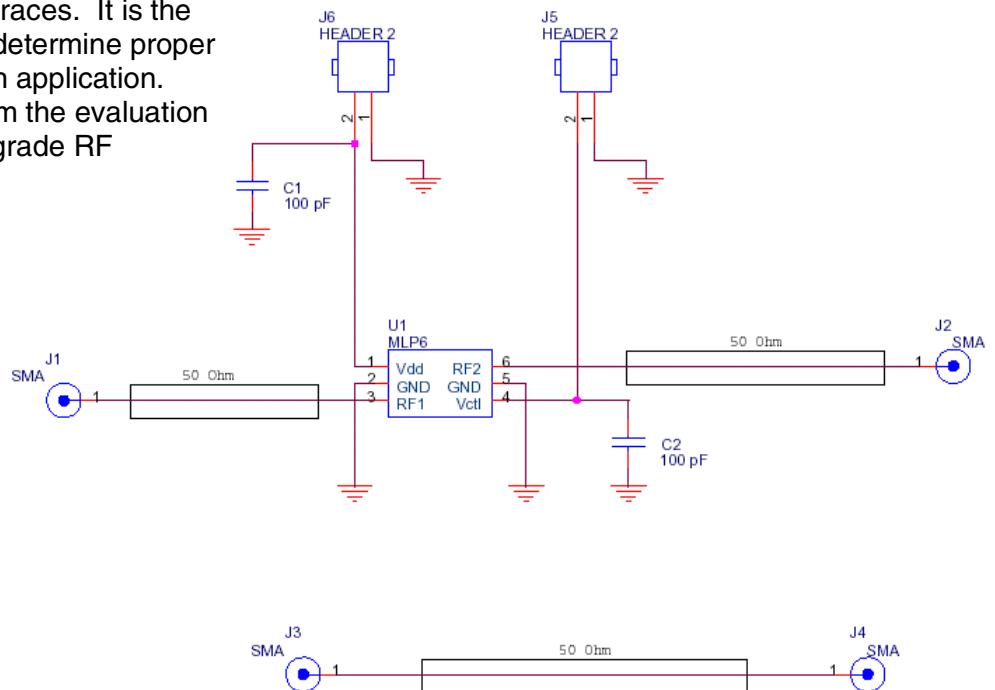
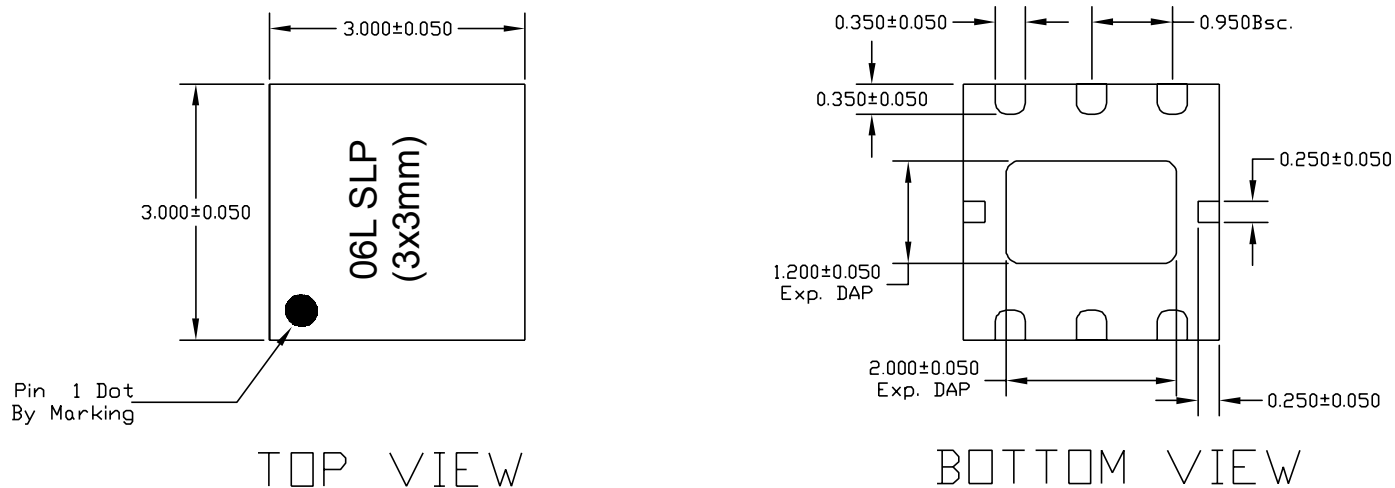


Figure 13. Package Drawing

6-lead DFN



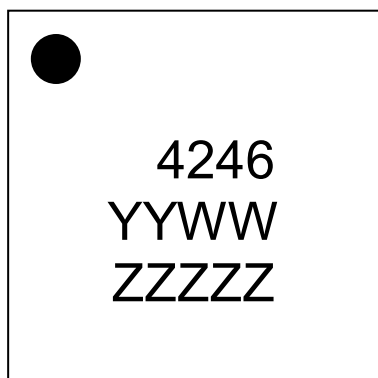
NOTE:

1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS:

		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

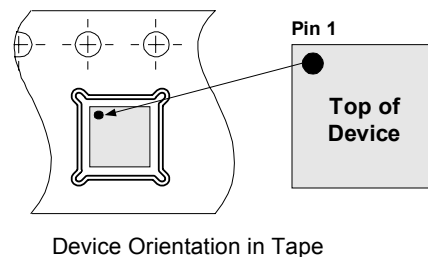
NOTE: The exposed solder pad (on the bottom of the package) is not electrically connected to any other pin (isolated).

Figure 14. Marking Specifications



YYWW = Date Code (last two digits of year and work week)
ZZZZZ = Last five digits of Lot Number

6-lead DFN



Dimension	DFN 3x3 mm
Ao	3.23 ± 0.1
Bo	3.17 ± 0.1
Ko	1.37 ± 0.1
P	4 ± 0.1
W	8 +0.3, -0.1
T	0.254 ± 0.02
R7 Quantity	3000
R13 Quantity	N.A.

NOTES:

1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.2
2. CAMBER IN COMPLIANCE WITH ETA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

Order Code	Part Marking	Description	Package	Shipping Method
4246-51	4246	PE4246G-06DFN 3x3mm-12800F	Green 6-lead 3x3 mm DFN	Tape or loose
4246-52	4246	PE4246G-06DFN 3x3mm-3000C	Green 6-lead 3x3 mm DFN	3000 units / T&R
4246-00	PE4246-EK	PE4246-06DFN 3x3mm-EK	Evaluation Kit	1 / Box

Sales Offices

The Americas

Peregrine Semiconductor Corporation

9380 Carroll Park Drive
San Diego, CA 92121
Tel: 858-731-9400
Fax: 858-731-9499

Europe

Peregrine Semiconductor Europe

Bâtiment Maine
13-15 rue des Quatre Vents
F-92380 Garches, France
Tel: +33-1-4741-9173
Fax : +33-1-4741-9173

High-Reliability and Defense Products

Americas

San Diego, CA, USA
Phone: 858-731-9475
Fax: 848-731-9499

Europe/Asia-Pacific

Aix-En-Provence Cedex 3, France
Phone: +33-4-4239-3361
Fax: +33-4-4239-7227

For a list of representatives in your area, please refer to our Web site at: www.psemi.com

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Peregrine Semiconductor, Asia Pacific (APAC)

Shanghai, 200040, P.R. China
Tel: +86-21-5836-8276
Fax: +86-21-5836-7652

Peregrine Semiconductor, Korea

#B-2607, Kolon Tripolis, 210
Geumgok-dong, Bundang-gu, Seongnam-si
Gyeonggi-do, 463-943 South Korea
Tel: +82-31-728-3939
Fax: +82-31-728-3940

Peregrine Semiconductor K.K., Japan

Teikoku Hotel Tower 10B-6
1-1-1 Uchisaiwai-cho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: +81-3-3502-5211
Fax: +81-3-3502-5213

The information in this data sheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this data sheet are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

The Peregrine name, logo, and UTSi are registered trademarks and UltraCMOS, HaRP, MultiSwitch and DuNE are trademarks of Peregrine Semiconductor Corp.