NTND31200PZ

Small Signal MOSFET

−20 V, −127 mA, Dual P−Channel, 0.65 mm x 0.90 mm x 0.4 mm XLLGA6 Package

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Features

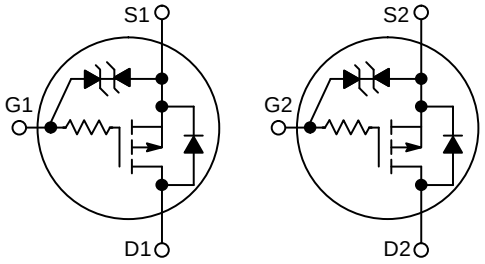
- Dual P−Channel MOSFET
- Offers a Low $R_{DS(ON)}$ Solution in the Ultra Small 0.65 mm × 0.90 mm Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Small Signal Load Switch
- Analog Switch
- High Speed Interfacing
- Optimized for Power Management in Ultra Portable Products

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D Max
−20 V	5.0 Ω @ −4.5 V	−127 mA
	6.0 Ω @ −2.5 V	
	7.0 Ω @ −1.8 V	
	10.0 Ω @ −1.5 V	

P−Channel MOSFET





XLLGA6
Case 713AC

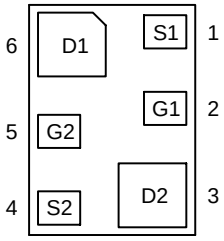
MAXIMUM RATINGS (T_J = 25°C unless otherwise specified)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	−20	V
Gate-to-Source Voltage			V_{GS}	±8	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	−127	mA
		T_A = 85°C		−91	
	t ≤ 5 s	T_A = 25°C		−146	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	125	mW
	t ≤ 5 s			166	
Pulsed Drain Current		t_p = 10 μs	I_{DM}	−488	mA
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode) (Note 2)			I_S	−200	mA
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

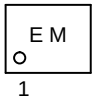
1. Surface-mounted on FR4 board using the minimum recommended pad size, 1 oz Cu.
2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%

PINOUT DIAGRAM



(Bottom View)

MARKING DIAGRAM



E = Specific Device Code
M = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient (Note 3) Steady State t ≤ 5 s	$R_{\theta JA}$	 998 751	°C/W

3. Surface-mounted on FR4 board using the minimum recommended pad size, 1 oz Cu.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA		−20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −5 V	T_J = 25°C			−50	nA
			T_J = 85°C			−200	nA
		V_{GS} = 0 V, V_{DS} = −16 V	T_J = 25°C			−100	
Gate-to-Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±5.0 V				±100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA		−0.4		−1.0	V
Drain-to-Source On Resistance	$R_{DS(ON)}$	V_{GS} = −4.5 V, I_D = −100 mA			2.1	5.0	Ω
		V_{GS} = −2.5 V, I_D = −50 mA			2.7	6.0	
		V_{GS} = −1.8 V, I_D = −20 mA			3.4	7.0	
		V_{GS} = −1.5 V, I_D = −10 mA			4.2	10.0	
Forward Transconductance	g_{FS}	V_{DS} = −5.0 V, I_D = −125 mA			0.35		S
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −10 mA			−0.6	−1.0	V
CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = −15 V			12.8		pF
Output Capacitance	C_{OSS}				2.8		
Reverse Transfer Capacitance	C_{RSS}				2.0		
SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V							
Turn-On Delay Time	$t_{d(ON)}$	V_{GS} = −4.5 V, V_{DD} = −15 V, I_D = −200 mA, R_G = 2.0 Ω			37		ns
Rise Time	t_r				71		
Turn-Off Delay Time	$t_{d(OFF)}$				280		
Fall Time	t_f				171		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Device	Package	Shipping†
NTND31200PZTAG	XLLGA6 (Pb−Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

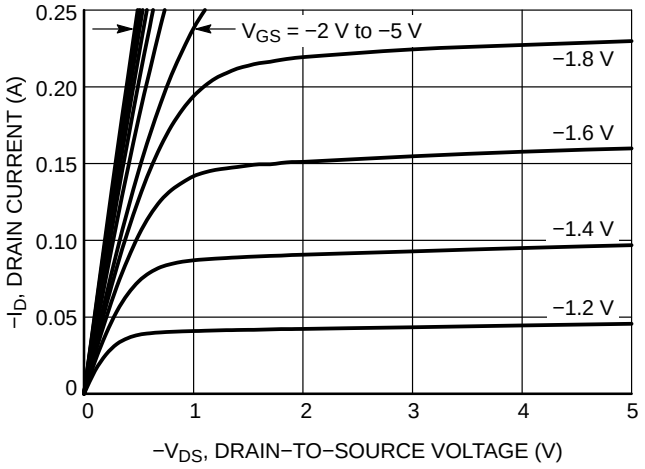


Figure 1. On−Region Characteristics

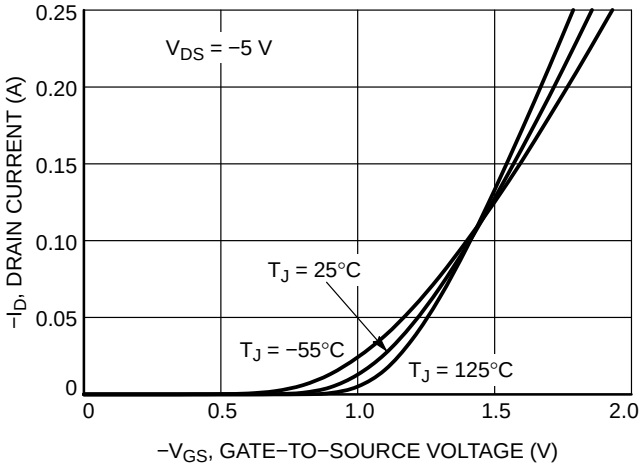


Figure 2. Transfer Characteristics

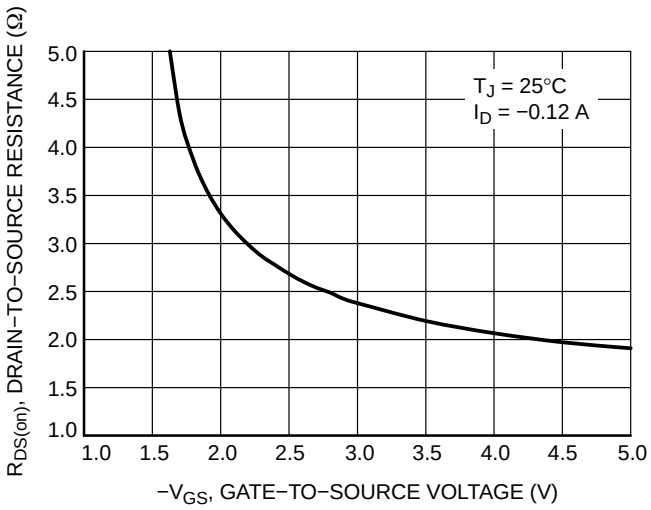


Figure 3. On−Resistance vs. Gate−to−Source Voltage

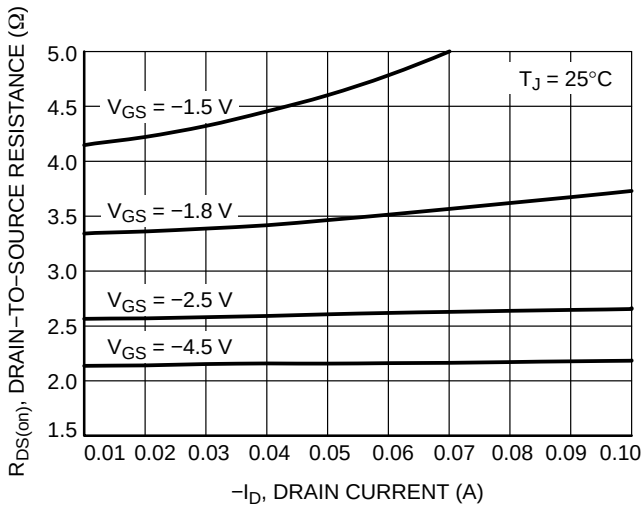


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

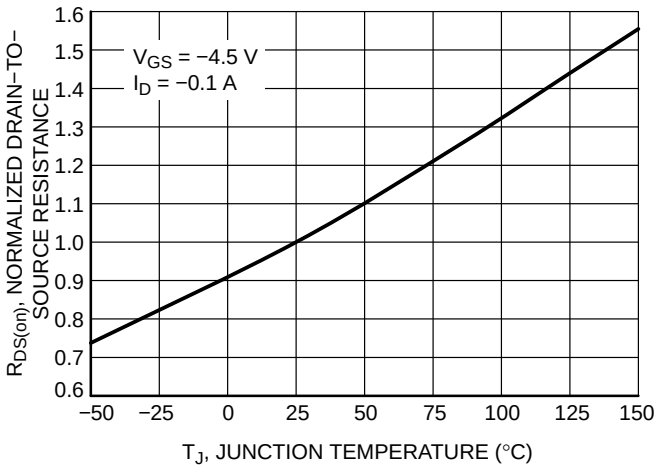


Figure 5. On−Resistance Variation with Temperature

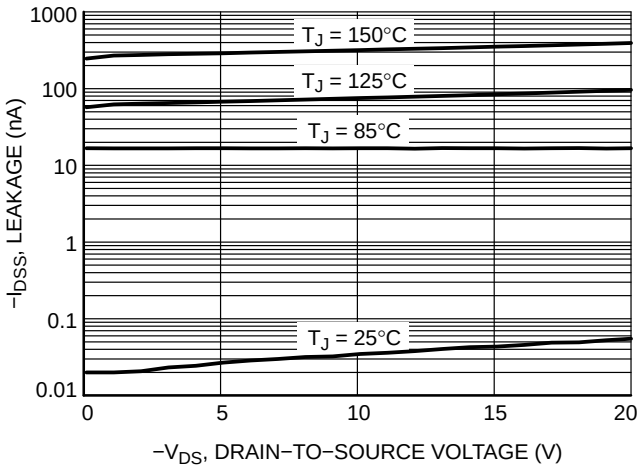


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

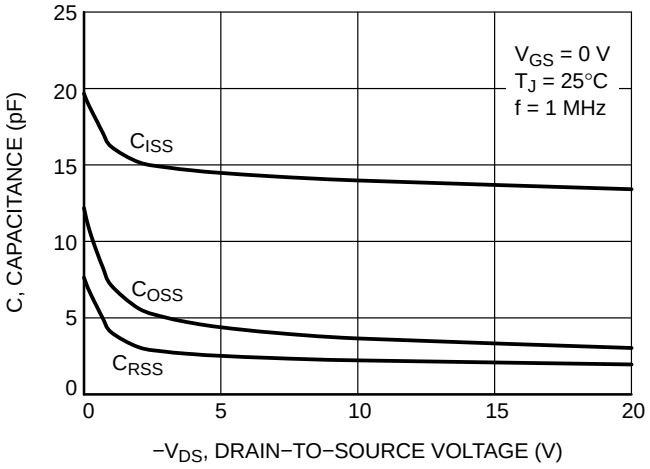


Figure 7. Capacitance Variation

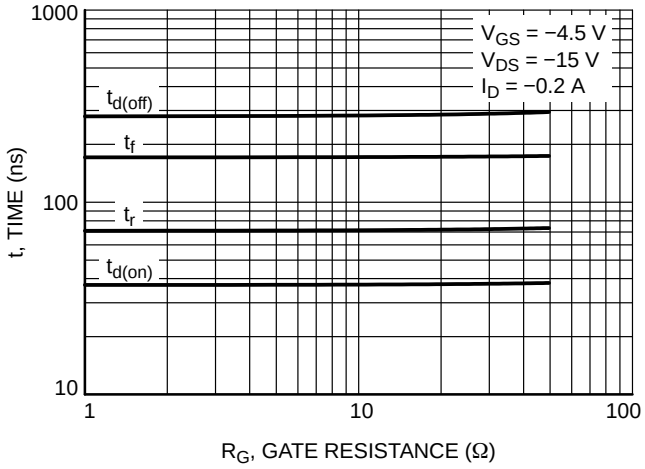


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

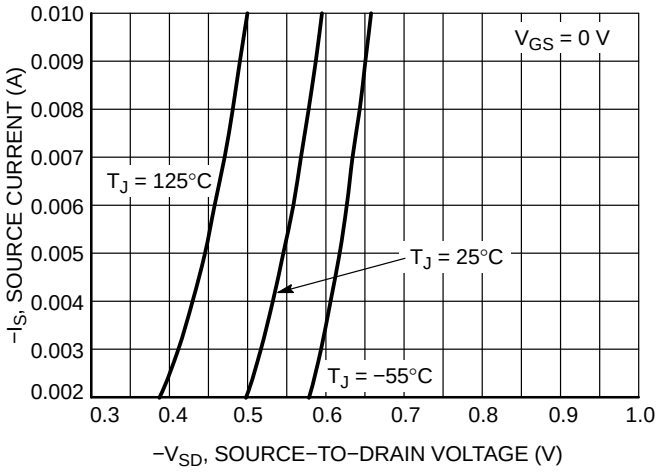


Figure 9. Diode Forward Voltage vs. Current

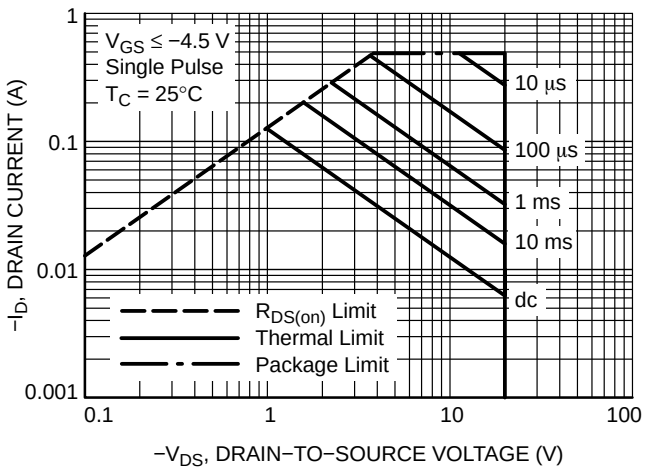


Figure 10. Maximum Rated Forward Biased Safe Operating Area

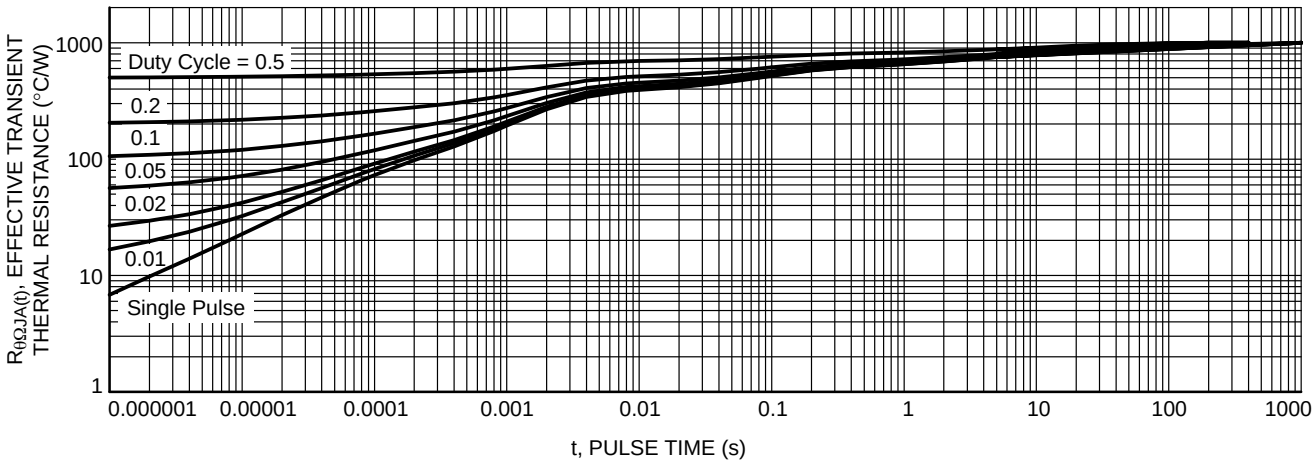
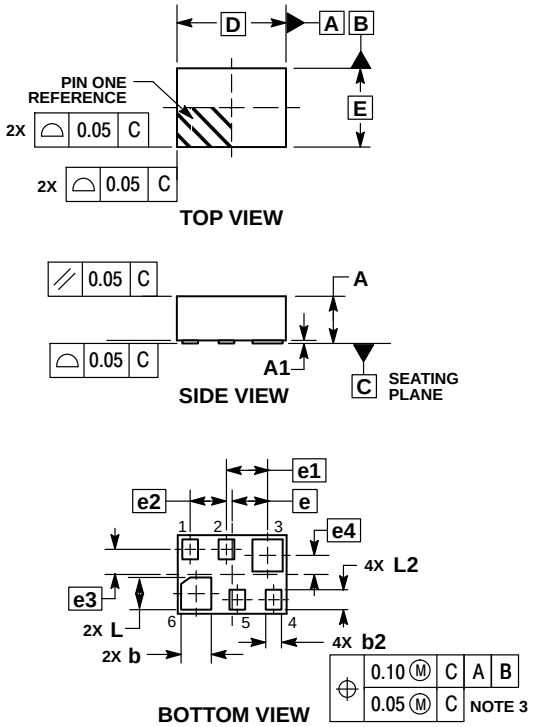


Figure 11. Thermal Response

NTND31200PZ

PACKAGE DIMENSIONS

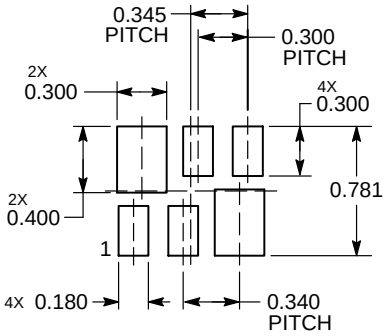
XLLGA6 0.90x0.65
CASE 713AC
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. POSITIONAL TOERANCE APPLIES TO ALL SIX LEADS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.340	0.440
A1	0.000	0.050
b	0.200	0.300
b2	0.080	0.180
D	0.900 BSC	
E	0.650 BSC	
e	0.295 BSC	
e1	0.340 BSC	
e2	0.300 BSC	
e3	0.208 BSC	
e4	0.158 BSC	
L	0.215	0.315
L2	0.115	0.215

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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