DATA SHEET

Part No.	AN12978A
Package Code No.	UBGA015-W-2020

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AN12978A

Monaural BTL amplifier IC with built-in AGC (I^2C bus-control correspondence)

■ Overview

AN12978A is the monaural BTL amplifier which contained the AGC circuit for clip prevention of a speaker output. This IC performs a mode change by the I^2C bus control system. (Standby function ON/OFF change etc.)

■ Features

- Selection by I^2C bus control is possible in the on-level of AGC. (3-bit, 8-step)
- Selection by I^2C bus control is possible in an attack/recovery time of AGC. (attack: 2-bit , recovery: 3-bit)
- The resistance and the capacitor of a detector circuit which were being used for the conventional AGC are unnecessary.
- In order to realize high efficiency of output power, it adopts CMOS power amplifier circuit.
- Built-in shutdown function.
- Built-in Gv-Switch.

■ Applications

- Audio amplifier for mobile, such as a cellular phone

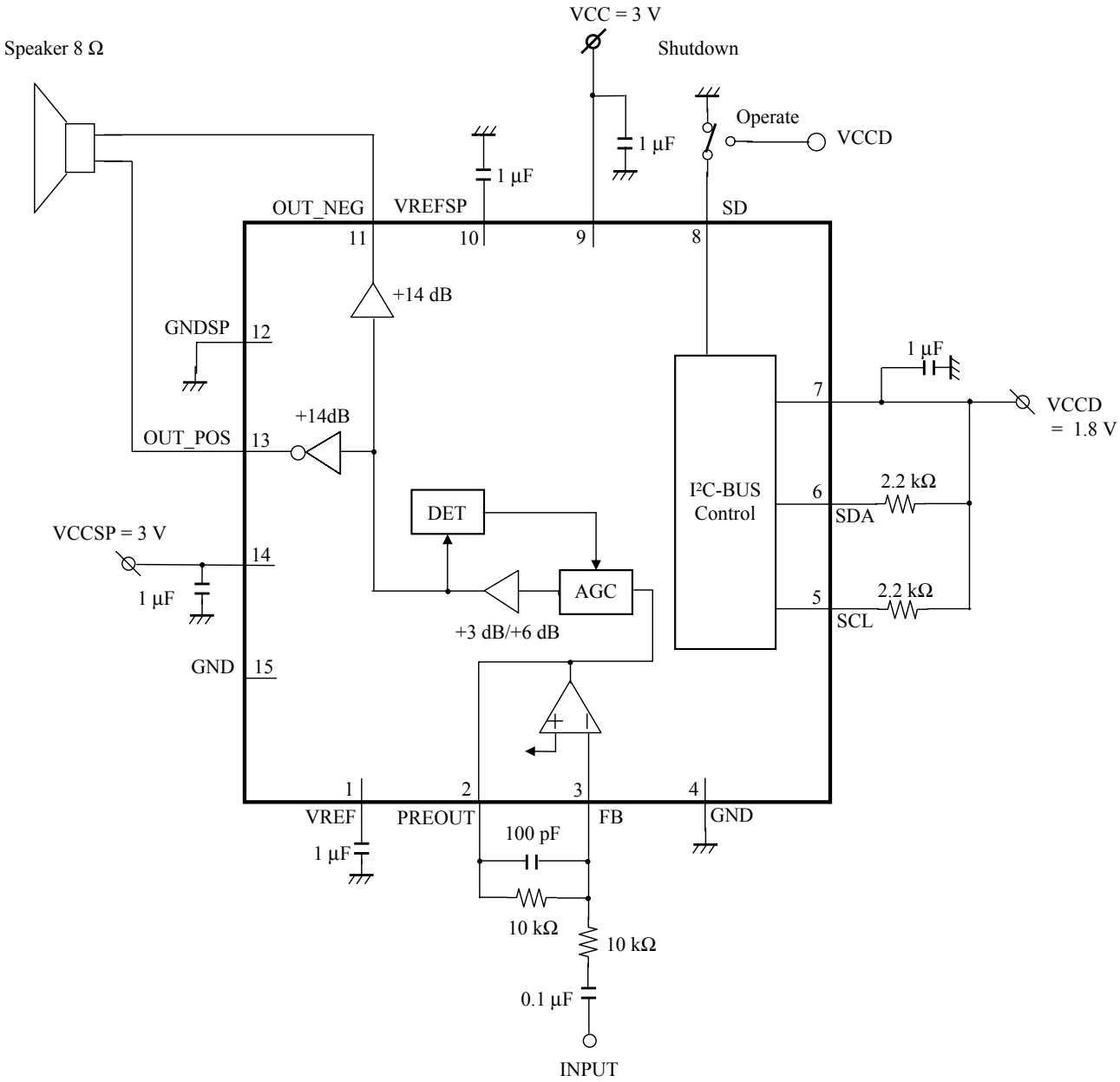
■ Package

- 15 pin Wafer level chip size package (WLCSP)
  Size: 2.0 mm × 2.0 mm (0.5 mm pitch)

■ Type

- Bi-CMOS IC

■ Application Circuit Example (Block Diagram)



Note) 1. This circuit and these circuit constants show an example and do not guarantee the design as a mass-production set.
2. The threshold voltage at 8pin has the VCCD dependency.

■ Pin Descriptions

Pin No.	Pin name	Type	Description
1	VREF	Output	Reference Voltage Output
2	PREOUT	Output	Pre-amplifier Output
3	FB	Input	Pre-amplifier Negative Feedback Input
4	GND	Ground	Ground
5	SCL	Input	SCL Input on I^2C-bus Control
6	SDA	Input / Output	SDA Input on I^2C-bus Control
7	VCCD	Power Supply	Power supply for logic circuit
8	SD	Input	Shutdown Control
9	VCC	Power Supply	Power supply
10	VREFSP	Output	Reference Voltage Output for Speaker Amplifier
11	OUT_NEG	Output	Speaker Output (Negative Phase)
12	GNDSP	Ground	Ground for Speaker Amplifier
13	OUT_POS	Output	Speaker Output (Positive Phase)
14	VCCSP	Power Supply	Power supply for Speaker Amplifier
15	GND	Ground	Ground

■ Absolute Maximum Ratings

A No.	Parameter	Symbol	Rating	Unit	Note
1	Supply voltage	VCC	5.5	V	*1
		VCCD	3.6		
		VCCSP	5.5		
2	Supply current	I_{CC}	—	A	
3	Power dissipation	P_D	120	mW	*2
4	Operating ambient temperature	T_{opr}	–20 to +70	°C	*3
5	Storage temperature	T_{stg}	–55 to +150	°C	*3

Note) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: The power dissipation shown is the value at T_a = 70°C for the independent (unmounted) IC package without a heat sink. When using this IC, refer to the • P_D – T_a diagram in the ■ Technical Data and use under the condition not exceeding the allowable value.

*3: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

■ Operating Supply Voltage Range

Parameter	Symbol	Range	Unit	Note
Supply voltage range	VCC	2.7 to 4.5	V	
	VCCD	1.7 to 2.6		*1
		1.7 to 3.3		*2
	VCCSP	2.7 to 4.5		

Note) 1. The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

2. *1: The values under Fast mode.

*2: The values under Standard mode.

■ Electrical Characteristics at VCC = 3.0 V , VCCD = 1.8 V , VCCSP = 3.0 V

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Conditions	Limits			Unit	Note
				Min	Typ	Max		
Circuit Current								
1	Circuit current at non-signal 1 (VCC)	IVCC1A	VCC = 3.0V, Non-signal STB = OFF, SP = ON, AGC = ON	0.5	2.4	4.5	mA	
2	Circuit current at non-signal 2 (VCCSP)	IVCC2A	VCCSP = 3.0V, Non-signal STB = OFF, SP = ON, AGC = ON	1.0	6.5	15.5	mA	
3	Circuit current at non-signal 3 (VCCD)	IVCC3A	VCCD = 1.8V, Non-signal STB = OFF, SP = ON, AGC = ON	—	0.1	10	µA	
4	Circuit current at standby mode 1 (VCC)	IVCC1B	VCC = 3.0V, Non-signal STB = ON, SP = OFF, AGC = ON	—	0.1	1.0	µA	
5	Circuit current at standby mode 2 (VCCSP)	IVCC2B	VCCSP = 3.0V, Non-signal STB = ON, SP = OFF, AGC = ON	—	0.1	1.0	µA	
6	Circuit current at standby mode 3 (VCCD)	IVCC3B	VCCD = 1.8V, Non-signal STB = ON, SP = OFF, AGC = ON	—	0.1	1.0	µA	
7	Circuit current at speaker save mode 1 (VCC)	IVCC1C	VCC = 3.0 V, Non-signal STB = OFF, SP = OFF, AGC = ON	0.5	2.4	4.5	mA	
8	Circuit current at speaker save mode 2 (VCCSP)	IVCC2C	VCCSP = 3.0 V, Non-signal STB = OFF, SP = OFF, AGC = ON	—	0.3	1.0	mA	
9	Circuit current at speaker save mode 3 (VCCD)	IVCC3C	VCCD = 1.8 V, Non-signal STB = OFF, SP = OFF, AGC = ON	—	0.1	10	µA	
Input/output characteristics								
11	SP reference output level	VSPO	Vin = –31.0 dBV , f = 1 kHz RL = 8 Ω, GAIN = +23 dB	–9.5	–8.0	–6.5	dBV	
12	SP reference output distortion	THSPO	Vin = –31.0 dBV, f = 1 kHz RL = 8 Ω, GAIN = +23dB to THD5th	—	0.07	0.5	%	
13	SP output noise voltage	VNSPO	Non-Signal using A curve filter GAIN = +23 Db	—	–78	–71	dBV	
14	SP maximum rating output	VMSPO	THD = 10%, f = 1 kHz RL = 8Ω, AGC = OFF	300	500	—	mW	
15	SP output level at power save	VSSPO	Vin = –31.0 dBV, f = 1 kHz RL = 8 Ω, GAIN = +23 dB using A curve filter	—	–114	–90	dBV	
16	SP AGC output level 1	VSPOA1	Vin = –17.0 dBV, f = 1 kHz RL = 8 Ω, GAIN = +23 dB AGC-Level = 4 dBV	3.0	4.0	5.0	dBV	
17	SP AGC output level 2	VSPOA2	Vin = –12.0 dBV, f = 1 kHz RL = 8 Ω, GAIN = +23 dB AGC-Level = 4 dBV	3.0	4.0	5.0	dBV	

■ Electrical Characteristics at VCC = 3.0 V , VCCD = 1.8 V , VCCSP = 3.0 V (continued)

Note) T_a = 25°C±2°C unless otherwise specified.

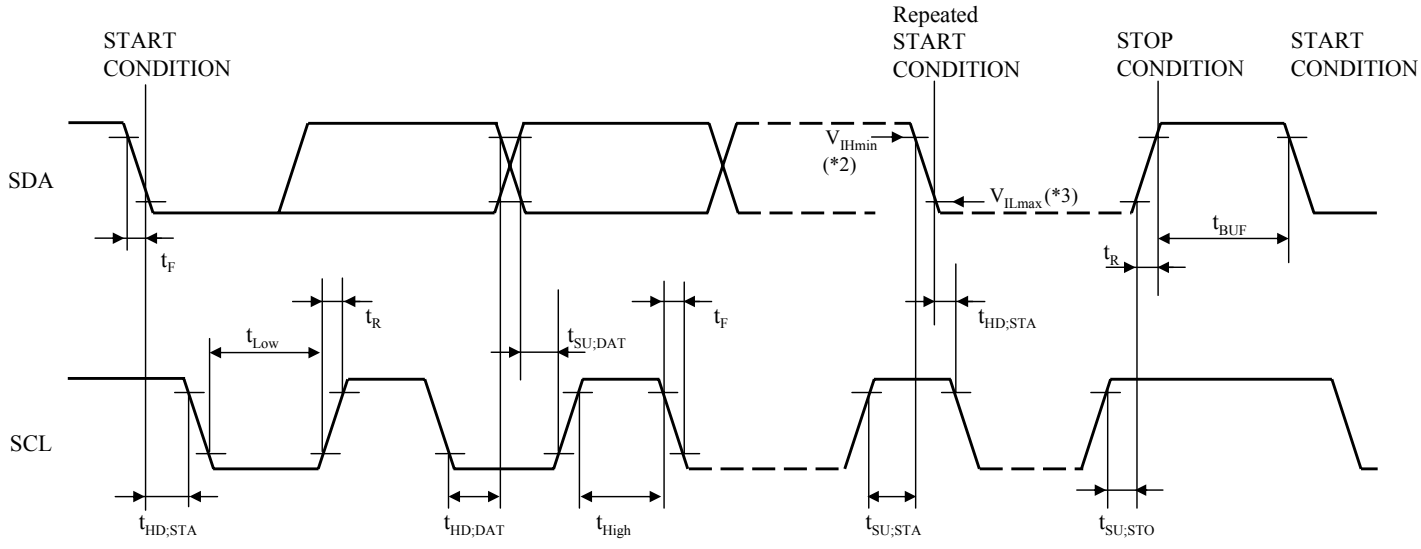
B No.	Parameter	Symbol	Conditions	Limits			Unit	Note
				Min	Typ	Max		
I²C interface								
43	SCL, SDA signal input Low Level	V_{IL}	—	− 0.5	—	0.3 × VCCD	V	
44	SCL, SDA signal input Low Level	V_{IH}	—	0.7 × VCCD	—	VCCD + 0.5	V	
45	SDA output signal Low Level	V_{OL}	Open corrector Sync current: 3 mA	0	—	0.2 × VCCD	V	
46	SCL,SDA Signal Input Current	I_i	Input voltage: 0.1 V to 1.7 V	–10	—	10	µA	
47	SCL maximum frequency of signal input	f_{SCL}	—	0	—	400	kHz	
The threshold voltage at 8-pin								
48	SD input Low Level	Vresetlth	—	—	—	0.1 × VCCD	V	
49	SD input High Level	Vreseththh	—	0.9 × VCCD	—	—	V	

■ Electrical Characteristics (Reference values for design) at VCC = 3.0 V , VCCD = 1.8 V , VCCSP = 3.0 V

Note) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Conditions	Limits			Unit	Note
				Min	Typ	Max		
I²C interface								
66	Bass free time between a condition of stop and a condition of start	t_{BUF}	—	1.3	—	—	µs	*1
67	Setup time of a condition of start	$t_{SU;STA}$	—	0.6	—	—	µs	*1
68	Hold time of a condition for start	$t_{HD;STA}$	—	0.6	—	—	µs	*1
69	"L" time of SCL clock	t_{Low}	—	1.3	—	—	µs	*1
70	"H" time of SCL clock	t_{High}	—	0.6	—	—	µs	*1
71	Rising time of SDA, SCL signal	t_R	—	—	—	0.3	µs	*1
72	Fall time of SDA,SCL signal	t_F	—	—	—	0.3	µs	*1
73	Data setup time	$t_{SU;DAT}$	—	0.1	—	—	µs	*1
74	Data hold time	$t_{HD;DAT}$	—	0	—	0.9	µs	*1
75	Rising up time of a condition of stop	$t_{SU;STO}$	—	0.6	—	—	µs	*1

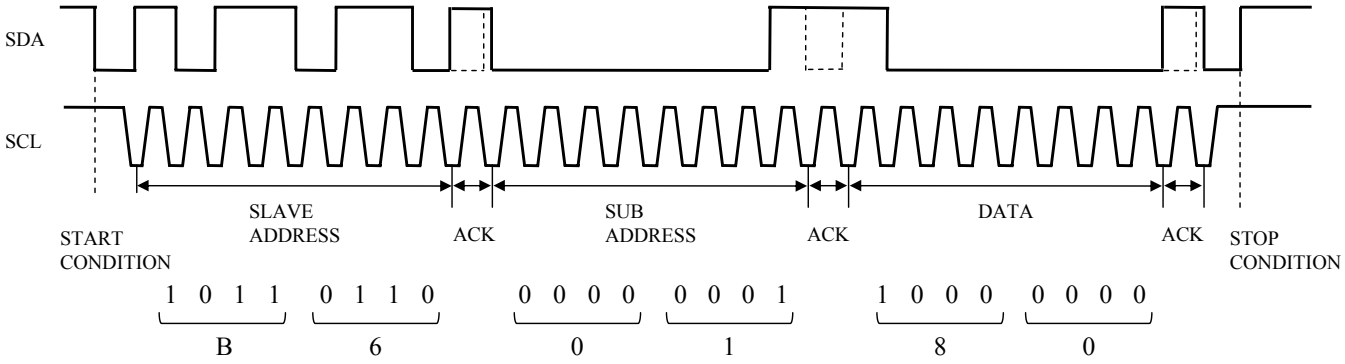
Note) *1: All values are V_{IHmin} (*2) and V_{ILmax} (*3) level standard.
*2: V_{IHmin} is the minimum limit of the signal input high level.
*3: V_{ILmax} is the maximum limit of the signal input low level.



■ Technical Data

- I^2C-bus Mode

1. Write Mode



Example of transmission messages

Two transmission messages (i.e., the SCL and SDA) are sent in synchronous serial transmission. The SCL is a clock with fixed frequency. The SDA indicates address data for the control of the reception side, and is sent in parallel in synchronization with the SCL. The data is transmitted in 8-bit, 3 octets (bytes) in principle, where every octet has an acknowledge bit. The following description provides information on the structure of the frame.

<Start Conditions>

When the level of the SDA changes to low from high while the level of the SCL is high, the data reception of the receiver will be enabled.

<Stop Conditions>

When the level of the SDA changes to high from low while the level of the SCL is high, the data reception of the receiver will be aborted.

<Slave Address>

The slave address is a specified one unique to each device. When the address of another device is sent, the reception will be aborted.

<Sub Address>

The sub address is a specified one unique to each function.

<Data>

Data is information under control.

<Acknowledge Bit>

The acknowledge bit is used to enable the master to acknowledge the reception of data for each octet. The master acknowledges the data reception of the receiver by transmitting a high-level signal to the receiver and receiving a low-level signal returned from the receiver as shown by the dotted lines in Fig.
The communication will be aborted if the low signal is not returned.

The SDA will not change when the level of the SCL is high except start or stop conditions are enabled.

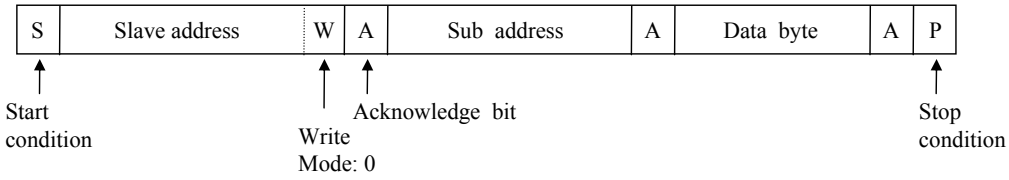
■ Technical Data (continued)

- I²C-bus Mode (continued)

1. Write Mode (continued)

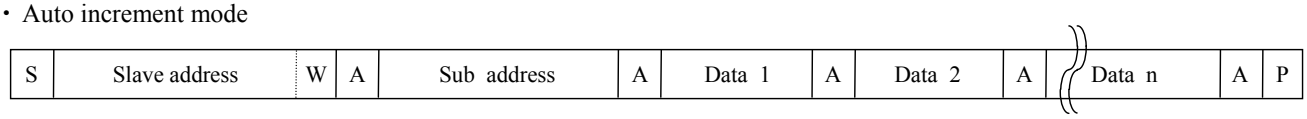
(a) I²C-bus PROTOCOL

- Slave address: 10110110 (B6Hex)
- Format (normal)



(b) Auto increment

- Sub-address 0*Hex: Auto increment mode
  (When the data is sent in sequence, the sub address will change one by one and the data will be input.)
- Auto increment mode



(c) Initial condition

The initial state of the device is not guaranteed. Therefore, the input of 00Hex resister-D0 (Note.1) will be absolutely 0, when the power is turned ON.

(d) Sub-address Byte and Data Byte Format

Sub-address	MSB Data byte LSB							
	D7	D6	D5	D4	D3	D2	D1	D0
*0Hex	GAIN 0 → +23dB 1 → +26dB	AGC-ON VCCSP dependence 0 → OFF 1 → ON	0 (Note.2)	0 (Note.2)	AGC 0 → OFF 1 → ON	SP Save 0 → ON 1 → OFF	Standby 0 → ON 1 → OFF	0 (Note.1)
*1Hex	AGC-ON data bit3	AGC-ON data bit2	AGC-ON data bit1	AGC-REC data bit3	AGC-REC data bit2	AGC-REC data bit1	AGC-ATT data bit2	AGC-ATT data bit1
*2Hex	0 (Note.2)	0 (Note.2)	0 (Note.2)	*	*	0 (Note.2)	0 (Note.2)	0 (Note.2)

<00Hex Register>
D0, D4, D5: Always set to 0
D1: Standby ON/OFF switch
D2: SP Save ON/OFF switch
D3: AGC ON/OFF switch
D6: AGC-ON VCCSP dependence ON/OFF selection
D7: GAIN +17 dB/+20 dB selection
<01Hex Register>
D0, D1 : AGC-attack-time selection
D2, D3,D4: AGC-recovery-time selection
D5,D6,D7: AGC-on-level selection
<02Hex Register>
D0 to D7: Always set to 0 (test & adjust mode)

0 (Note.2) ⬅ Please use these bit only Data = "0", because they are used by our company's final test and fine-tuning AGC-on level.

■ Technical Data (continued)

- I^2C-bus Mode (continued)

1. Write Mode (continued)

(e) AGC-attack-time selection

Write 01Hex Register		Attack time
D1	D0	
0	0	0.5 ms
0	1	1 ms
1	0	2 ms
1	1	4 ms

(f) AGC-recovery-time selection

Write 01Hex Register			Recovery time
D4	D3	D2	
0	0	0	1.0 s
0	0	1	1.5 s
0	1	0	2.0 s
0	1	1	3.0 s
1	0	0	4.0 s
1	0	1	6.0 s
1	1	0	8.0 s
1	1	1	12.0 s

(g) AGC-on-level selection (at VCC = 3.0 V, VCCSP = 3.0 V)

Write 01Hex Register			AGC On Level	Output Po (RL = 8W)	VCCSP (推奨値)
D7	D6	D5			
0	0	0	1 dBV	157 mW	—
0	0	1	2 dBV	198 mW	—
0	1	0	3 dBV	249 mW	—
0	1	1	4 dBV	314 mW	3.0 V ≤
1	0	0	5 dBV	395 mW	3.3 V ≤
1	0	1	6 dBV	498 mW	3.7 V ≤
1	1	0	7 dBV	626 mW	4.1 V ≤
1	1	1	8 dBV	789 mW	4.5 V

(h) AGC-on-level VCCSP dependence mode (at AGC On Level = 4 dBV)

AGC ON level increases by 0.75 dBV with each 0.3 V increase of VCCSP, and baseline of VCCSP is 3.0 V at AGC-on-level VCCSP dependence mode. When VCCSP is 3.0 V, AGC ON level is set according to table (g).

VCCSP	AGC On Level	Output Po (RL = 8 Ω)	VCCSP	AGC On Level	Output Po (RL = 8 Ω)
2.7 V	3.25 dBV	264 mW	3.9 V	6.25 dBV	527 mW
3.0 V	4 dBV	314 mW	4.2 V	7 dBV	626 mW
3.3 V	4.75 dBV	373 mW	4.5 V	7.75 dBV	745 mW
3.6 V	5.5 dBV	444 mW			

■ Technical Data (continued)

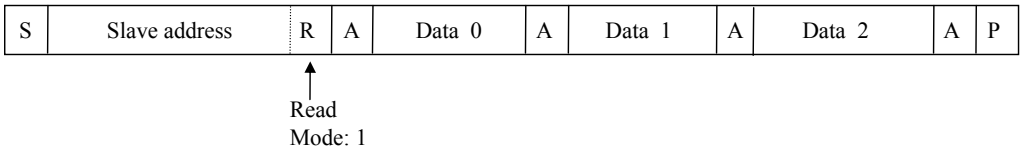
- I²C-bus Mode (continued)

2. Read Mode

(a) I²C-bus PROTOCOL

・Slave address 10110111(B7Hex)

・Format



Note) At the slave address input, it is sequentially output from data 0.
There is no necessity for inputting the sub-address.

(b) Sub-address Byte and Data Byte Format

	MSB Data byte LSB							
	D7	D6	D5	D4	D3	D2	D1	D0
Data 0	Sub address *0Hex Latch data [D7]	Sub address *0Hex Latch data [D6]	Sub address *0Hex Latch data [D5]	Sub address *0Hex Latch data [D4]	Sub address *0Hex Latch data [D3]	Sub address *0Hex Latch data [D2]	Sub address *0Hex Latch data [D1]	Sub address *0Hex Latch data [D0]
Data 1	Sub address *1Hex Latch data [D7]	Sub address *1Hex Latch data [D6]	Sub address *1Hex Latch data [D5]	Sub address *1Hex Latch data [D4]	Sub address *1Hex Latch data [D3]	Sub address *1Hex Latch data [D2]	Sub address *1Hex Latch data [D1]	Sub address *1Hex Latch data [D0]
Data 2	Sub address *2Hex Latch data [D7]	Sub address *2Hex Latch data [D6]	Sub address *2Hex Latch data [D5]	Sub address *2Hex Latch data [D4]	Sub address *2Hex Latch data [D3]	Sub address *2Hex Latch data [D2]	Sub address *2Hex Latch data [D1]	Sub address *2Hex Latch data [D0]

- Operating temperature guarantee of I²C-bus Control

The performance in the ambient temperature of operation is guaranteed theoretically in the design at normal temperature (25°C) by inspecting it at a speed of the clock that is about 50% earlier regarding the operating temperature guarantee of I²C-bus Control.

But the following characteristics are logical values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, Panasonic will respond in good faith to customer concerns.

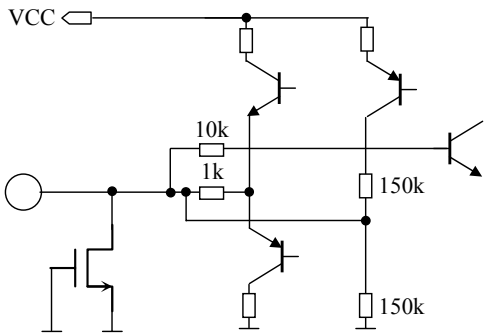
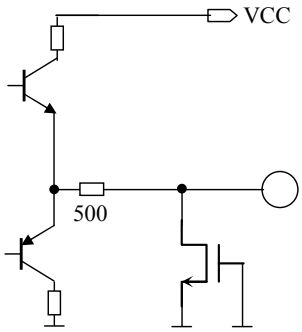
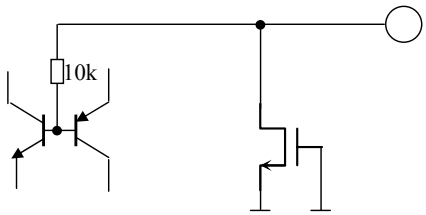
- Usage note of I²C bus

・The I²C bus of this product is designed to correspond to Standard mode (100 Kbps) and Fast mode (400 Kbps) in Philips Corporation I²C specification version 2.1. However, not correspond to High Speed mode (to 3.4 Mbps).
・This product operate as a slave device in I²C bus system.
・This product is not confirm to operate in multi-master bus system and mixing -speed bus system. And this product is not confirm connectivity to CBUS receiver. If using this product in these mode, please confirm availability to our company.
・Purchase of Panasonic I²C components conveys a license to use these components in an I²C systems under the Philips I²C patent right on condition that using condition conform to I²C standard specification approved by Philips Corporation.

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions

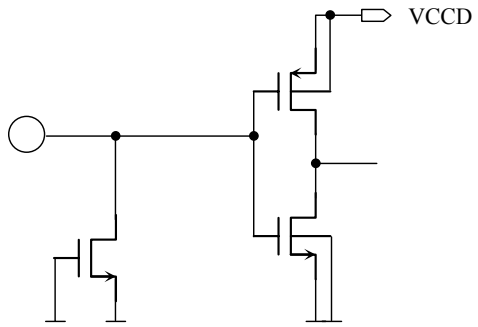
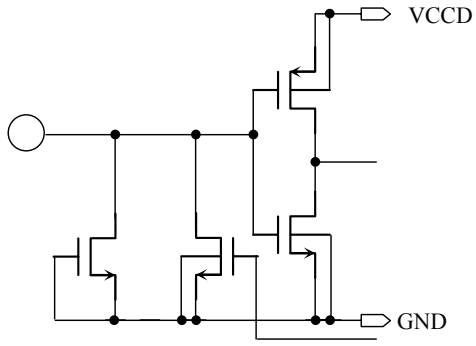
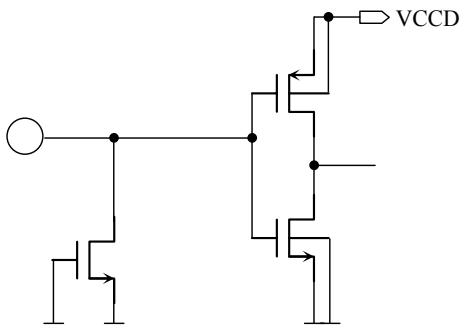
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Description
1	VREF DC 1.45 V		Reference Voltage Output
2	PREOUT DC 1.45 V		Pre-amplifier Output
3	FB DC 1.45 V		Pre-amplifier Negative Feedback Input
4	GND	—	Ground

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

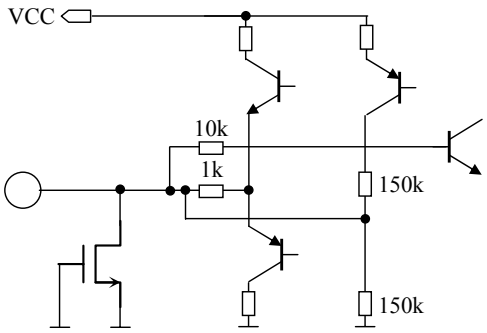
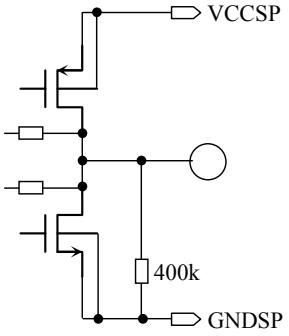
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Description
5	SCL Hi-Z		SCL Input on I^2C-Bus Control
6	SDA Hi-Z		SDA Input on I^2C-Bus Control
7	VCCD 1.8 V(typ.)	—	Power Supply for Logic Circuit
8	SD Connect VCCD to VCC 1.8 V to 3.0 V		Shutdown Control Shutdown mode is shorted to GND. (All data becomes 0.)

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

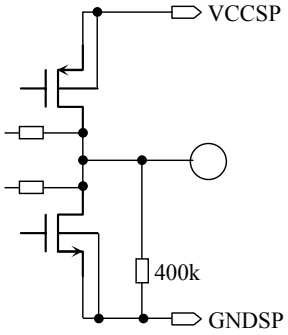
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Description
9	VCC 3.0 V(typ.)	—	Power Supply
10	VREFSP 3.0 V(typ.)		Reference Voltage Output for Speaker Amplifier
11	OUT_NEG DC 1.45 V		Speaker Output (Negative Phase)
12	GNDSP	—	Ground for Speaker Amplifier

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Description
13	OUT_POS DC 1.45 V		Speaker Output (Positive Phase)
14	VCCSP 3.0 V(typ.)	—	Power Supply for Speaker Amplifier
15	GND	—	Ground

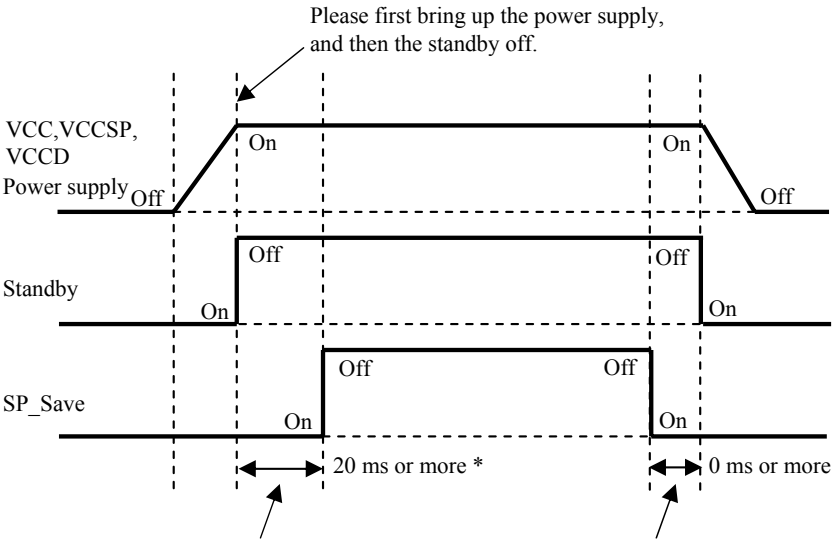
■ Technical Data (continued)

- Power supply and logic sequence

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

The timing control of power-ON/OFF and each logic according to the procedure below should be recommended for the best pop performance caused in switching.

1. The sequence of the power supply and each logic



The basic procedure at the power-on

1. The power OFF condition
   Both the standby and the SP_Save are in the ON condition.
2. Power ON
3. Standby Off
4. SP_Save Off

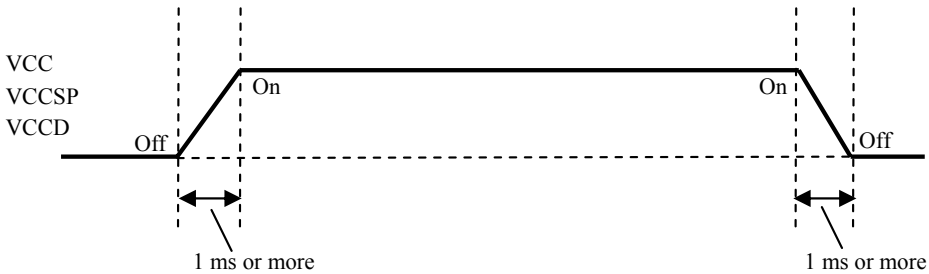
The basic procedure at the power-off

1. The power ON condition
   Both the standby and the SP_Save are in the OFF condition.
2. SP_Save On (= Standby On)
3. Standby On
4. Power Off

Note) *: This IC contains the pre-charge circuit. It is time until each bias is stabilized from Standby Off.
It depends for this time on the capacity value linked to a reference voltage terminal (VREF and VREFSP), and the capacity value and resistance linked to an input terminal (IN).
It is a recommendation value in a constant given in the example of ■ Application Circuit Example (Block Diagram).

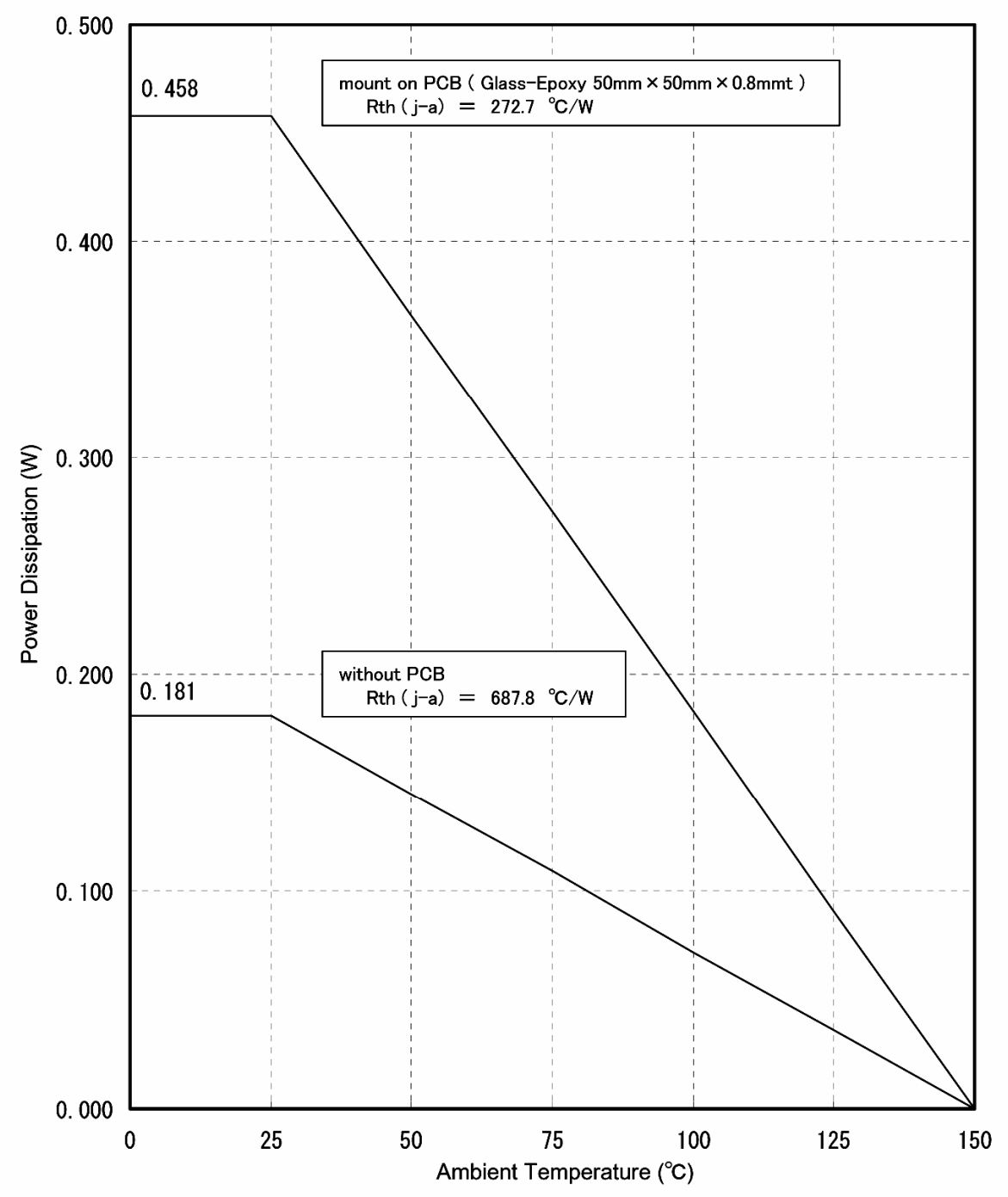
2. The sequence of VCC and VCCSP and VCCD

This IC have not a standup and falling order in VCC and VCCSP.
A standup and falling time of VCC and VCCSP recommend 1 or more ms.



■ Technical Data (continued)

• P_D — T_a diagram



■ Usage Notes

1. Please take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as SP output pin (Pin11, Pin13) – power supply pin short, SP output pin (Pin11, Pin13) – GND short, or SP output (Pin11, Pin13) -to-SP output-pin short (load short).

2. Please absolutely do not mount the IC in the reverse direction on to the printed-circuit-board.
   It damaged when the electricity is turned on.

3. Please do not make it open, because the open SD-pin (Pin8) is not fixed.

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