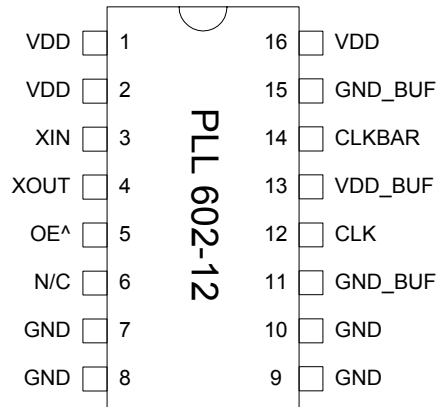


**FEATURES**

- Low phase noise output for the 96MHz to 200MHz range (-134 dBc at 10kHz offset).
- LVDS output.
- 12 to 25MHz crystal input.
- Integrated crystal load capacitor: no external load capacitor required.
- Output Enable selector.
- 3.3V operation.
- Available in 16 Pin TSSOP.

**PIN CONFIGURATION**



Note: <sup>^</sup> denotes internal pull up

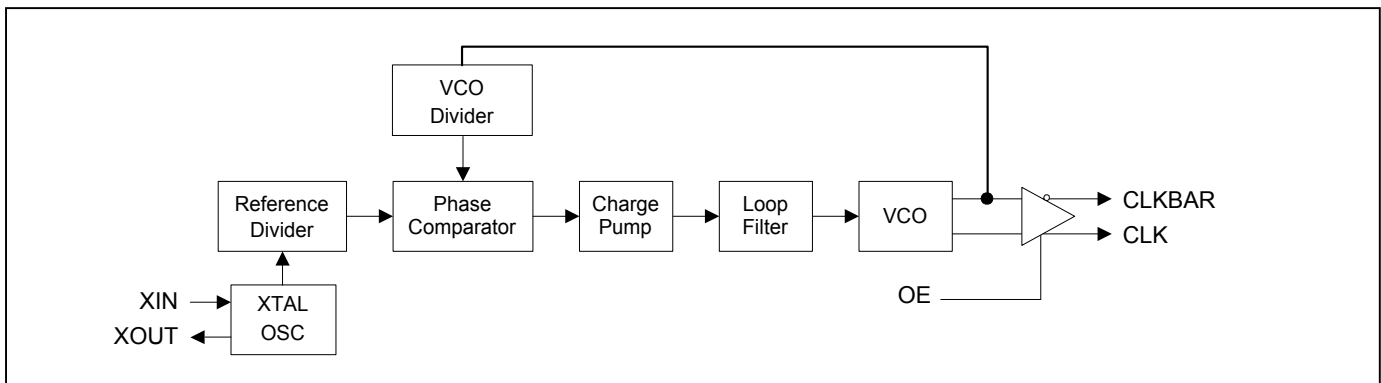
$$F_{OUT} = F_{XIN} \times 8$$

**DESCRIPTION**

The PLL602-12 is a monolithic low jitter and low phase noise (-134dBc/Hz @ 10kHz offset) XO IC with LVDS output, for 96MHz to 200MHz output range. It provides a low phase noise reference frequency using a low cost crystal. The chip delivers an output frequency of  $F_{XIN} \times 8$ . This makes the PLL602-12 ideal for a wide range of applications, including 155.52MHz for SONET.

OE (Pin 5)	Output State
0	Tri-state
1 (Default)	Output enabled

**BLOCK DIAGRAM**



## 96MHz – 192MHz Low Phase Noise LVDS XO (12 – 25MHz Crystal)

### PIN DESCRIPTIONS

Name	Number	Type	Description
VDD	1,2,16	P	Power supply.
XIN	3	I	Crystal input. See Crystal Specifications on page 2.
XOUT	4	I	Crystal output. See Crystal Specifications on page 2.
OE	5	I	Output enable input. Disables (tri-state) output when low. Internal pull-up enables output by default if pin is not connected to low.
N/C	6	-	Not connected.
GND	7,8,9,10	P	Ground.
GND_BUF	11,15	P	Ground for output buffers.
CLK	12	O	True clock output.
VDD_BUF	13	P	Power supply for output buffers.
CLKB	14	O	Complementary clock output.

### ELECTRICAL SPECIFICATIONS

#### 1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	$V_{DD}$		4.6	V
Input Voltage, dc	$V_I$	-0.5	$V_{DD}+0.5$	V
Output Voltage, dc	$V_O$	-0.5	$V_{DD}+0.5$	V
Storage Temperature	$T_S$	-65	150	°C
Ambient Operating Temperature*	$T_A$	-40	85	°C
Junction Temperature	$T_J$		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

\* Note: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

#### 2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	$F_{XIN}$	Parallel Fundamental Mode	12		25	MHz
Crystal Loading Rating	$C_L$ (xtal)			20		pF
Recommended ESR	$R_E$	AT cut			30	$\Omega$

## 96MHz – 192MHz Low Phase Noise LVDS XO (12 – 25MHz Crystal)

### 3. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic (with Loaded Outputs)	I <sub>DD</sub>	LVDS			60	mA
Operating Voltage	V <sub>DD</sub>		2.97		3.63	V
Output Clock Duty Cycle		@ 1.25V (LVDS)	45	50	55	%
Short Circuit Current				±50		mA

### 4. Jitter and Phase Noise Specification

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS	With capacitive decoupling between VDD and GND.		4		ps
Accumulated jitter RMS	With capacitive decoupling between VDD and GND. Over 10,000 cycles.		9		ps
Phase Noise relative to carrier	155MHz @100Hz offset		-95		dBc/Hz
Phase Noise relative to carrier	155MHz @1kHz offset		-120		dBc/Hz
Phase Noise relative to carrier	155MHz @10kHz offset		-125		dBc/Hz
Phase Noise relative to carrier	155MHz @100kHz offset		-121		dBc/Hz

**96MHz – 192MHz Low Phase Noise LVDS XO (12 – 25MHz Crystal)**

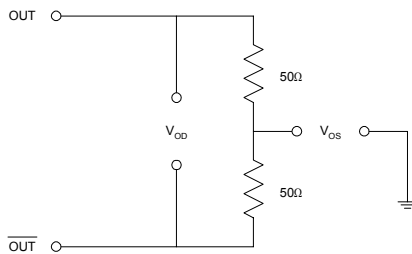
**5. LVDS Electrical Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	$V_{OD}$	$R_L = 100\ \Omega$ (see figure)	247	355	454	mV
$V_{DD}$ Magnitude Change	$\Delta V_{OD}$		-50		50	mV
Output High Voltage	$V_{OH}$			1.4	1.6	V
Output Low Voltage	$V_{OL}$		0.9	1.1		V
Offset Voltage	$V_{OS}$		1.125	1.2	1.375	V
Offset Magnitude Change	$\Delta V_{OS}$		0	3	25	mV
Power-off Leakage	$I_{OXD}$	$V_{out} = V_{DD}$ or GND $V_{DD} = 0V$		$\pm 1$	$\pm 10$	$\mu A$
Output Short Circuit Current	$I_{OSD}$			-5.7	-8	mA

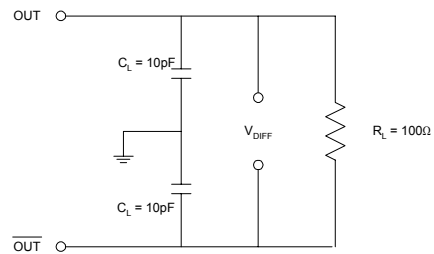
**6. LVDS Switching Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	$t_r$	$R_L = 100\ \Omega$ $C_L = 10\ pF$ (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	$t_f$		0.2	0.7	1.0	ns

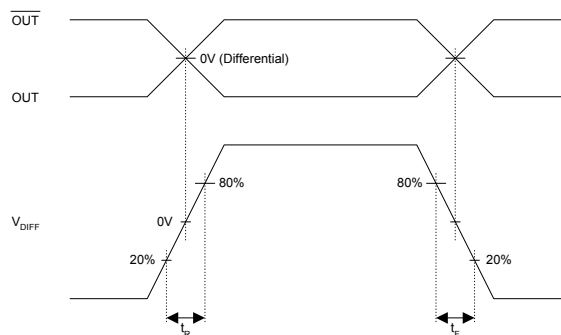
LVDS Levels Test Circuit



LVDS Switching Test Circuit



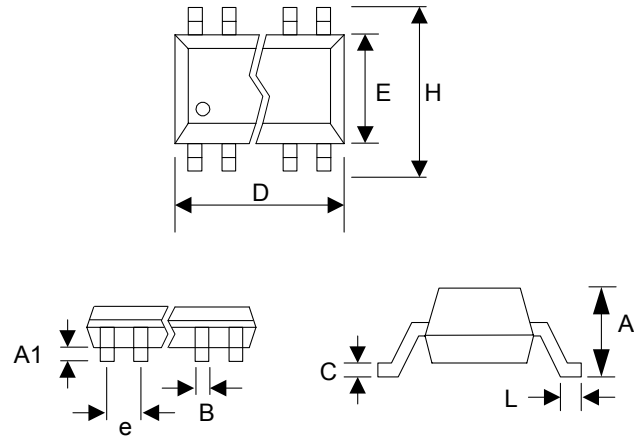
LVDS Transition Time Waveform



**96MHz – 192MHz Low Phase Noise LVDS XO (12 – 25MHz Crystal)**

**PACKAGE INFORMATION**

16 PIN TSSOP ( mm )		
Symbol	Min.	Max.
A	-	1.20
A1	0.05	0.15
B	0.19	0.30
C	0.09	0.20
D	4.90	5.10
E	4.30	4.50
H	6.40 BSC	
L	0.45	0.75
e	0.65 BSC	



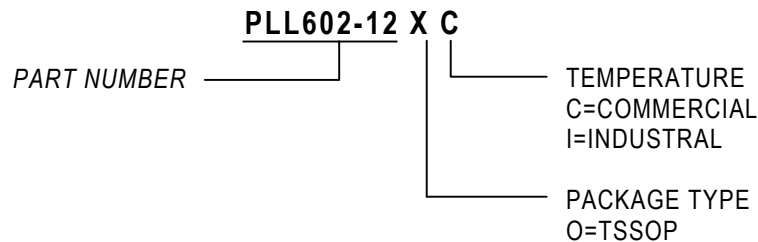
**ORDERING INFORMATION**

**For part ordering, please contact our Sales Department:**

47745 Fremont Blvd., Fremont, CA 94538, USA  
Tel: (510) 492-0990 Fax: (510) 492-0991

**PART NUMBER**

The order number for this device is a combination of the following:  
Device number, Package type and Operating temperature range



<u>Order Number</u>	<u>Marking</u>	<u>Package Option</u>
PLL602-12OC-R	P602-12OC	TSSOP - Tape and Reel
PLL602-12OC	P602-12OC	TSSOP – Tube

*PhaseLink Corporation, reserves the right to make changes in its products or specifications, or both at any time without notice. The information furnished by Phaselink is believed to be accurate and reliable. However, PhaseLink makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon this product.*

**LIFE SUPPORT POLICY:** PhaseLink's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of PhaseLink Corporation.