1.5V Drive Pch+Pch MOSFET

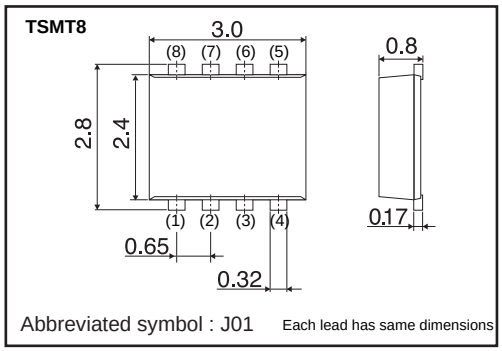
QS8J1

●Structure
Silicon P-channel MOSFET

●Features
1) Low On-resistance.
2) Low voltage drive. (1.5 V)
3) High power package.

●Applications
Switching

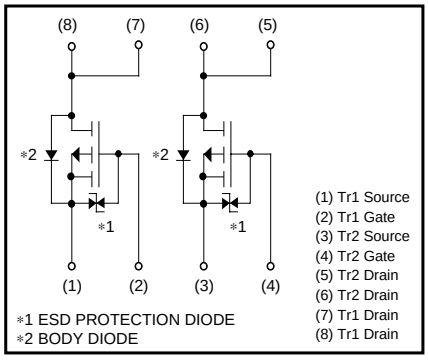
●Dimensions (Unit : mm)



●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
QS8J1		○

●Inner circuit



●Absolute maximum ratings (Ta=25°C)
<It is the same ratings for Tr1 and Tr2.>

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	−12	V
Gate-source voltage		V_{GSS}	±10	V
Drain current	Continuous	I_D	±4.5	A
	Pulsed	I_{DP} ∗1	±18	A
Source current (Body diode)	Continuous	I_S	−1	A
	Pulsed	I_{SP} ∗1	−18	A
Total power dissipation		P_D ∗2	1.5	W / TOTAL
			1.25	W / ELEMENT
Channel temperature		Tch	150	°C
Range of Storage temperature		Tstg	−55 to +150	°C

∗1 Pw≤10μs, Duty cycle≤1%
∗2 Mounted on a ceramic board

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	Rth(ch-a) ∗	83.3	°C/W / TOTAL
		100	°C/W / ELEMENT

∗ Mounted on a ceramic board.

●**Electrical characteristics** (Ta=25°C)

<It is the same characteristics for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	±10	μA	V_{GS}=±10V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	−12	–	–	V	I_D= −1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	−1	μA	V_{DS}= −12V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	−0.3	–	−1.0	V	V_{DS}= −6V, I_D= −1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$*	–	21	29	mΩ	I_D= −4.5A, V_{GS}= −4.5V
		–	27	38	mΩ	I_D= −2.2A, V_{GS}= −2.5V
		–	36	54	mΩ	I_D= −2.2A, V_{GS}= −1.8V
		–	49	98	mΩ	I_D= −0.9A, V_{GS}= −1.5V
Forward transfer admittance	$\|Y_{fs}\|$ *	6.5	–	–	S	V_{DS}= −6V, I_D= −4.5A
Input capacitance	C_{iss}	–	2450	–	pF	V_{DS}= −6V
Output capacitance	C_{oss}	–	320	–	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	–	290	–	pF	f=1MHz
Turn-on delay time	$t_{d\ (on)}$ *	–	12	–	ns	V_{DD} ≒ −6V
Rise time	t_r *	–	75	–	ns	V_{GS}= −4.5V
Turn-off delay time	$t_{d\ (off)}$ *	–	390	–	ns	I_D= −2.2A
Fall time	t_f *	–	215	–	ns	R_L ≒ 2.7Ω
						R_G=10Ω
Total gate charge	Q_g *	–	31	–	nC	V_{DD} ≒ −6V
Gate-source charge	Q_{gs} *	–	4.5	–	nC	V_{GS}= −4.5V
Gate-drain charge	Q_{gd} *	–	4.0	–	nC	I_D= −4.5A
						R_L ≒ 1.3Ω / R_G=10Ω

*Pulsed

●**Body diode characteristics** (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD}*	–	–	−1.2	V	I_S= −4.5A, V_{GS}=0V

* Pulsed

●**Electrical characteristic curves**

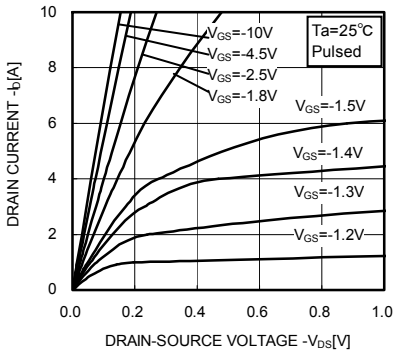


Fig.1 Typical Output Characteristics(Ⅰ)

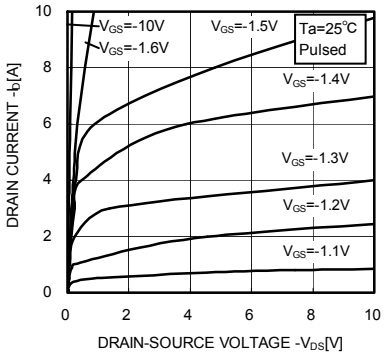


Fig.2 Typical Output Characteristics(Ⅱ)

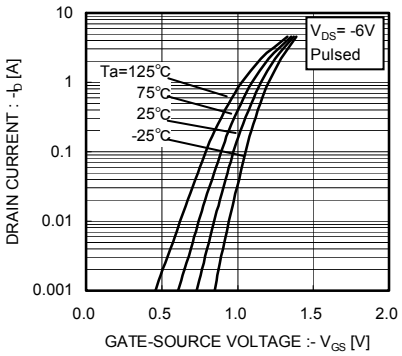


Fig.3 Typical Transfer Characteristics

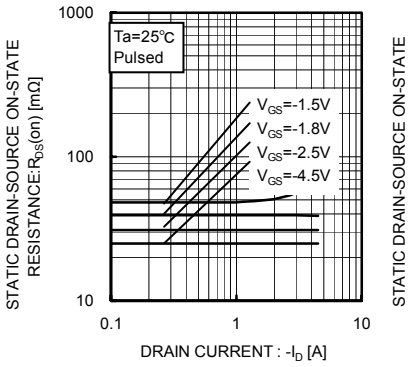


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(Ⅰ)

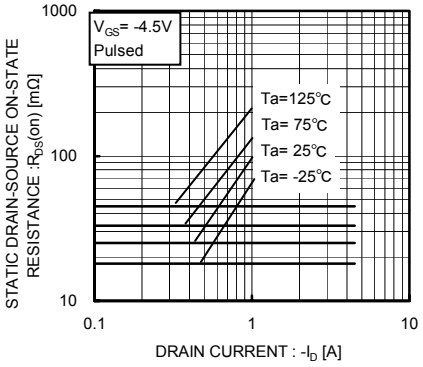


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(Ⅱ)

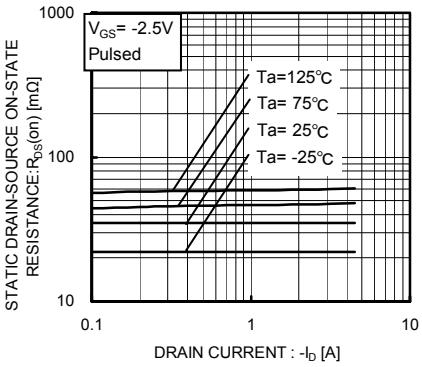


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(Ⅲ)

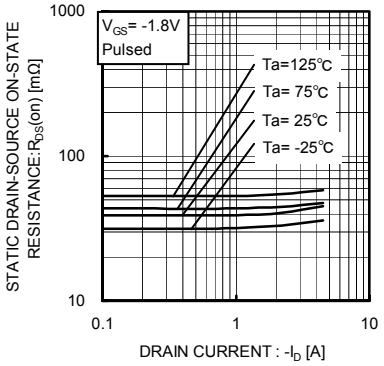


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(Ⅳ)

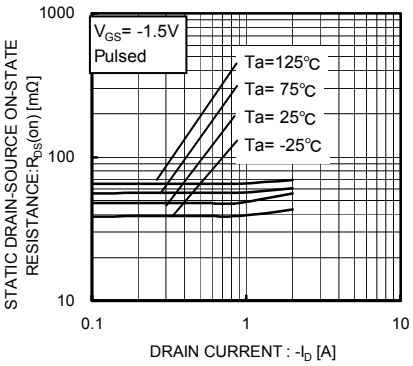


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(Ⅴ)

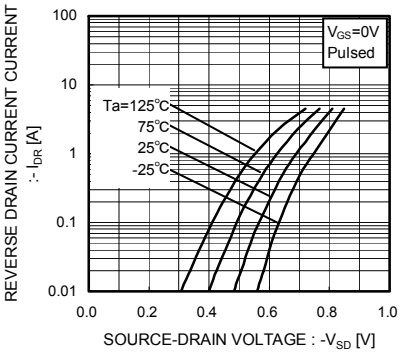


Fig.9 Reverse Drain Current vs. Sourse-Drain Voltage

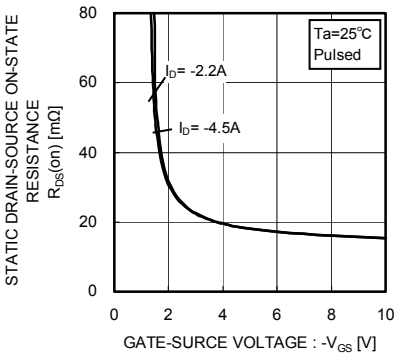


Fig.10 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

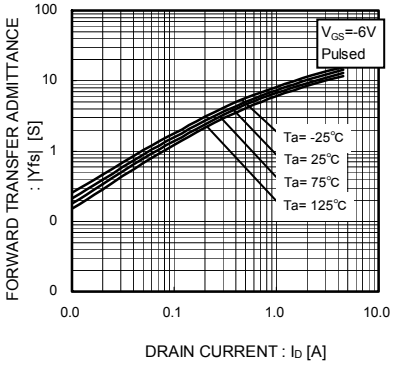


Fig.11 Forward Transfer Admittance vs. Drain Current

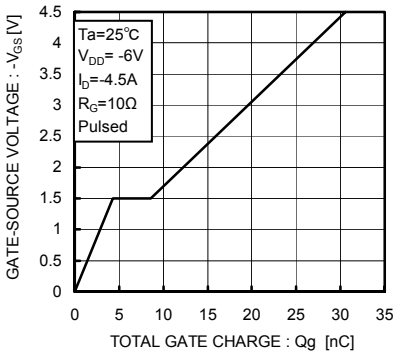


Fig.12 Dynamic Input Characteristics

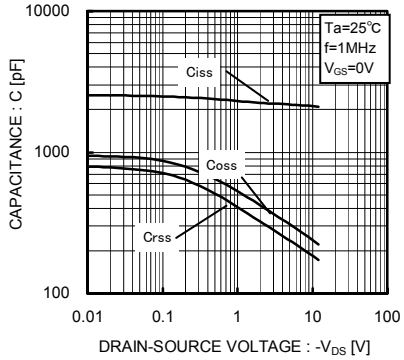


Fig.13 Typical Capacitance vs. Drain-Source Voltage

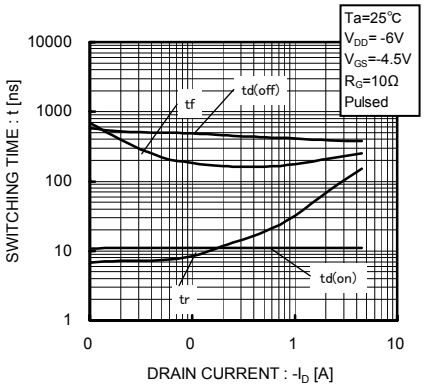


Fig.14 Switching Characteristics

●**Measurement circuits**

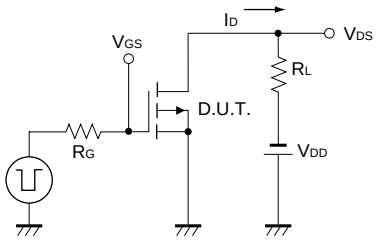


Fig.1-1 Switching Time Measurement Circuit

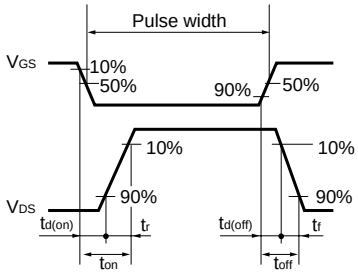


Fig.1-2 Switching Time Waveforms

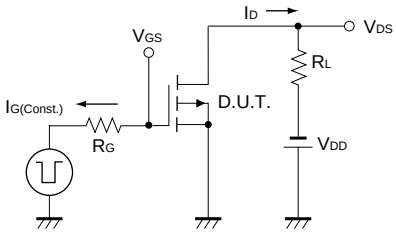


Fig.2-1 Gate Charge Measurement Circuit

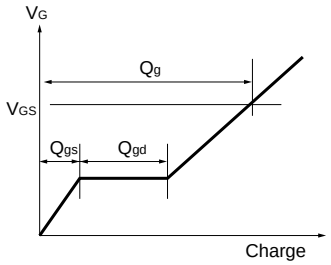


Fig.2-2 Gate Charge Waveform

●**Notice**

This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.

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