

General Description

The WST3415S is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent R_{DS(on)} and gate charge for most of the small power switching and load switch applications.

The WST3415S meet the RoHS and Green Product requirement with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent C_{dv/dt} effect decline
- Green Device Available

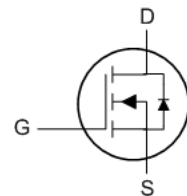
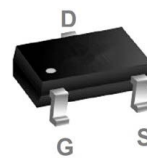
Product Summary

BVDSS	R _{DS(on)}	I _D
-20V	45 mΩ	-4.8A

Applications

- High Frequency Point-of-Load Synchronous Small power switching for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

SOT-23N Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	-20	V
V _{GS}	Gate-Source Voltage	±12	V
I _D @T _c =25°C	Continuous Drain Current, V _{GS} @ 4.5V ¹	-4.8	A
I _D @T _c =70°C	Continuous Drain Current, V _{GS} @ 4.5V ¹	-3.5	A
I _{DM}	Pulsed Drain Current ²	-12	A
P _D @T _A =25°C	Total Power Dissipation ³	0.83	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-ambient ¹	---	125	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	80	°C/W

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	-20	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.024	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-4.5V, I _D =-2.5A	---	45	70	mΩ
		V _{GS} =-2.5V, I _D =-2.3A	---	60	90	
		V _{GS} =-1.8V, I _D =-1A	---	75	110	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-0.5	-0.7	-1	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	-2.51	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-16V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =-16V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±8V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-3A	---	8.3	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	1.7	3.4	Ω
Q _g	Total Gate Charge (4.5V)	V _{DS} =-15V, V _{GS} =-4.5V, I _D =-2.5A	---	5	---	nC
Q _{gs}	Gate-Source Charge		---	0.5	---	
Q _{gd}	Gate-Drain Charge		---	7	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =-10V, V _{GS} =-4.5V, R _G =6Ω I _D =-1A, R _L =10Ω.	---	3.2	---	ns
T _r	Rise Time		---	11.5	---	
T _{d(off)}	Turn-Off Delay Time		---	25.5	---	
T _f	Fall Time		---	4	---	
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	300	---	pF
C _{oss}	Output Capacitance		---	53	---	
C _{rss}	Reverse Transfer Capacitance		---	47	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,4}	V _G =V _D =0V, Force Current	---	---	-1	A
I _{SM}	Pulsed Source Current ^{2,4}		---	---	-12	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1.2	V
t _{rr}	Reverse Recovery Time	I _F =-1A, dI/dt=100A/μs, T _J =25°C	---	10	---	nS
Q _{rr}	Reverse Recovery Charge		---	3.2	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper,t≤10sec.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The power dissipation is limited by 150°C junction temperature
- 4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

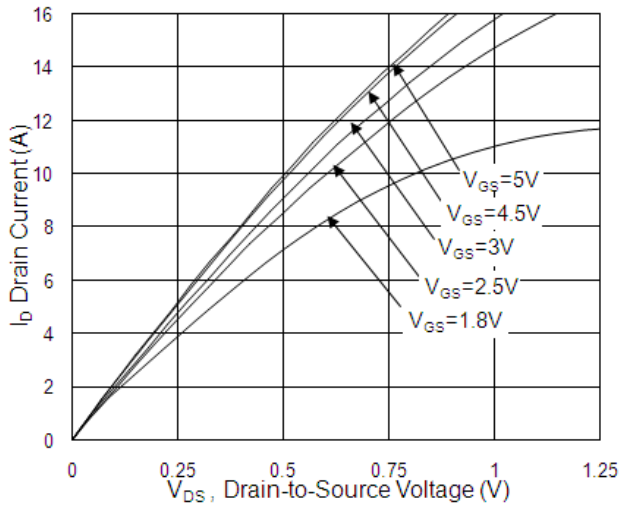


Fig.1 Typical Output Characteristics

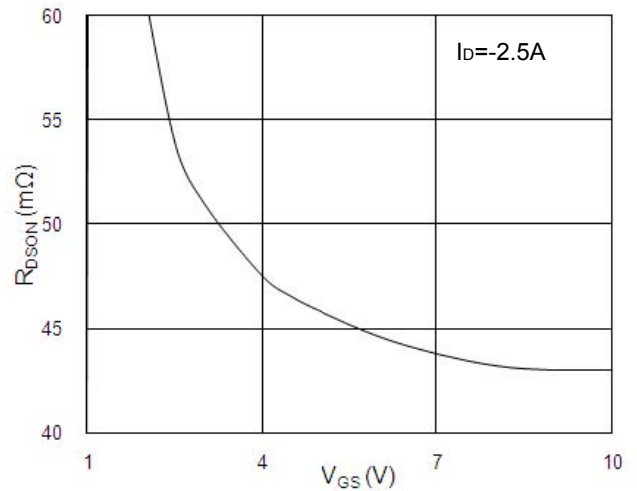


Fig.2 On-Resistance vs. Gate-Source

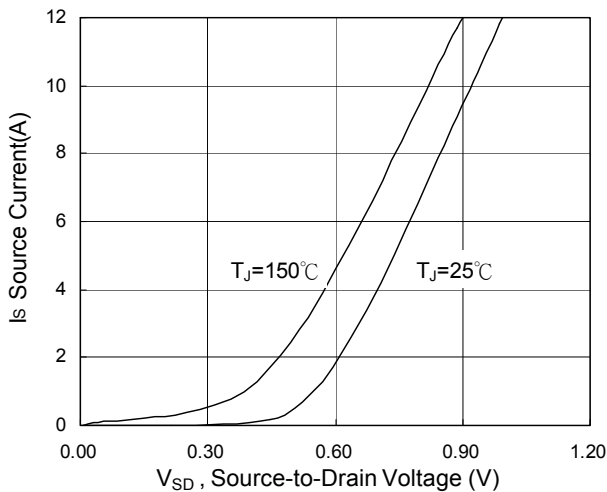


Fig.3 Forward Characteristics Of Reverse

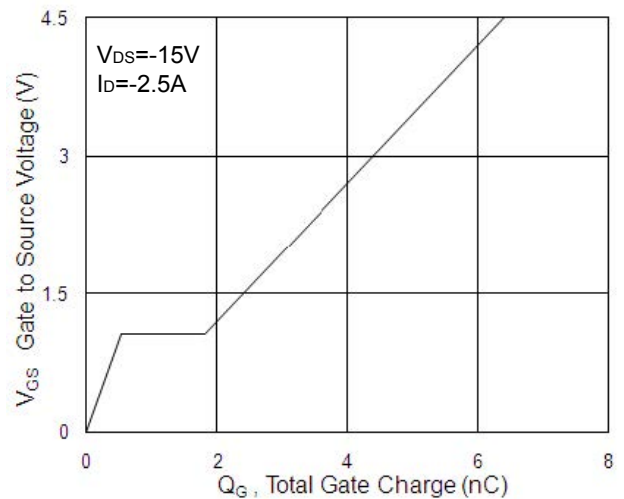


Fig.4 Gate-Charge Characteristics

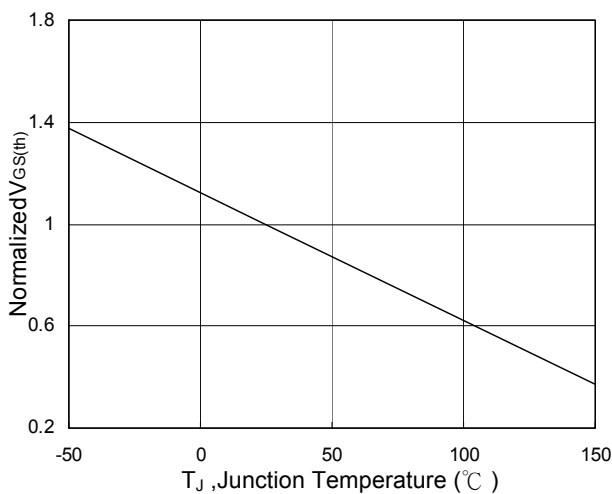


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

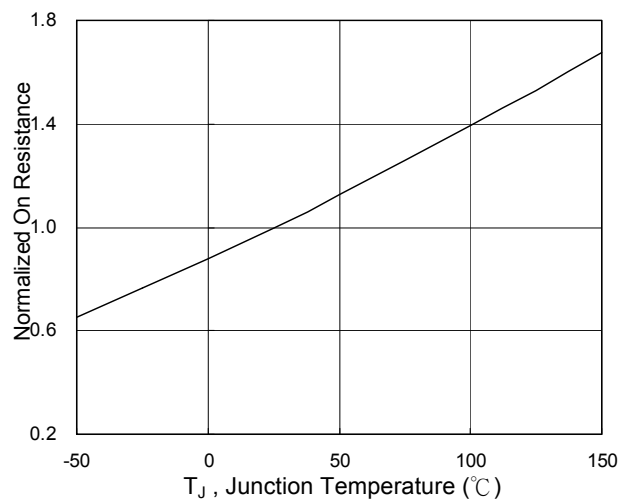


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

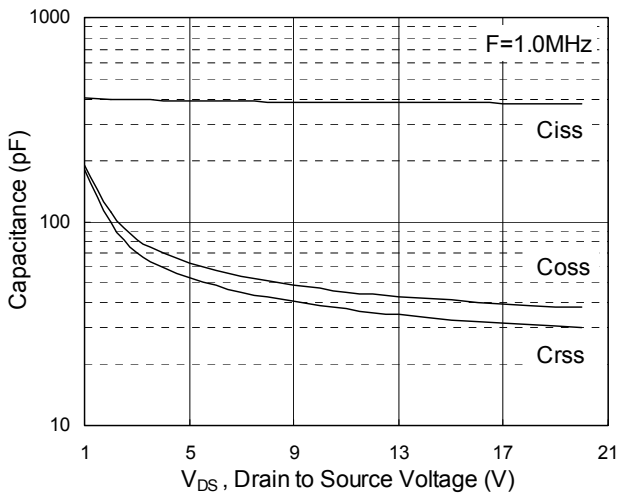


Fig.7 Capacitance

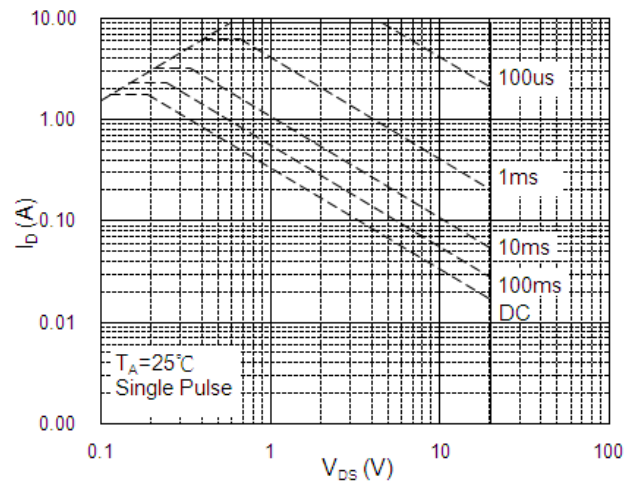


Fig.8 Safe Operating Area

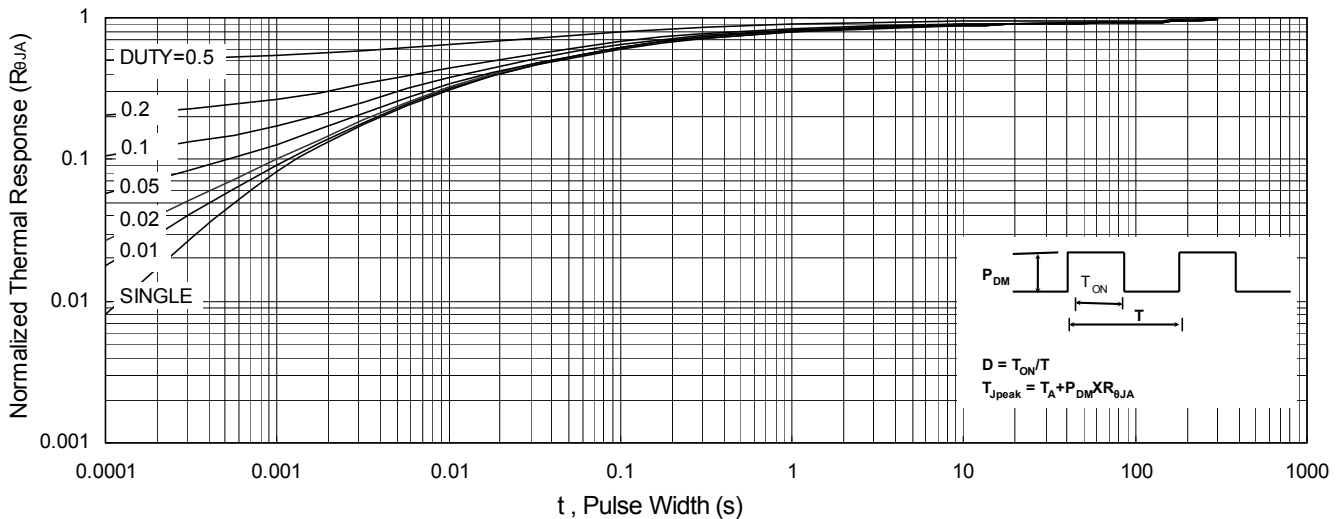


Fig.9 Normalized Maximum Transient Thermal Impedance

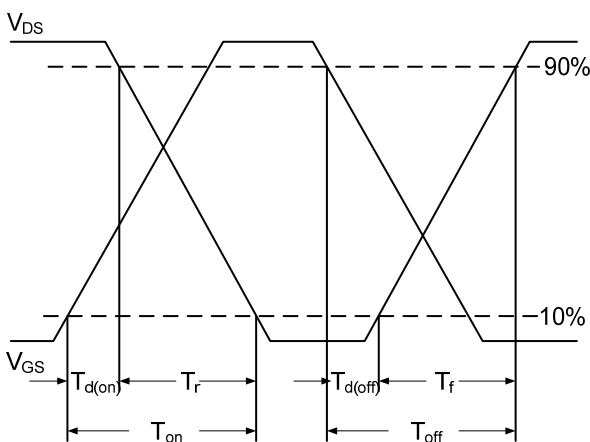


Fig.10 Switching Time Waveform

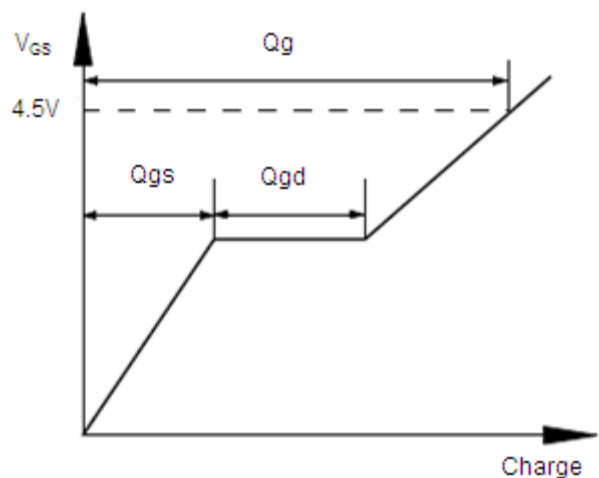


Fig.11 Gate Charge Waveform



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