OC-48/STM-16 Framer–POSIC2G™

Features

- **OC-48/STS-48/STM-16, OC-12/STS-12/STM-4, OC-3/STS3/STM-1 rates, concatenated and non-concatenated**
  - **— Complies with ITU-Standards G.707/Y.1322 and G.783**[1,2]
  - **— Complies with Bellcore GR253 rev.1, 1997**[3]
  - **— Channelized operation: supports 16xSTS-3c/VC4, 4xSTS-12c/VC4-4c, 2xSTS-24c/VC4-8c, and 1xSTS-48c/VC4-16c within OC-48 stream**
  - **— Supports TUG3 mapping in SDH mode**
- **Full duplex mapping of ATM cells over SONET/SDH**
  - **— Complies with ITU-Standards I.432.2**[4,5,6]
- **Full duplex mapping of packet-over-SONET/SDH: IETF RFC 1619/1662/2615 (HDLC/PPP)**[7,8,9]
- **Generic Protocol Encapsulator/Decapsulator delineates packets/frames with length-CRC frame construct**
  - **— Generic Framing Procedure (GFP) per ANSI T1X1.5**[10,11,12]
  - **— GFP 268r1**
  - **— Simple Data Link (SDL) - IETF RFC2823** [13]
  - **— Cypress Hybrid Data Transport (HDT)** [14]
- **User-programmable encapsulation**
- **User-programmable clear channel transport**
- **User-programmable SONET/SDH bypass**
- **Programmable frame tagging engine for packet preclassification enables such features as**
  - **— MPLS label lookup and tagging**
  - **— PPP: LCP and NCP tagging**
  - **— PPP control packets optionally sent to host CPU interface**
  - **— MAC/layer 3 address look up and tagging**
- **Programmable A1A2 processing bypass in Rx direction with frame sync input**
- **Complete section overhead (SOH), line overhead (LOH), and path overhead (POH) processing**
- **APS extraction, CPU interrupt generation, and programmable insertion of APS byte**
- **Line side APS port interface**
- **Provision for protection switching on SONET/SDH port**
- **Programmable PRBS generator and receiver**
- **Serial port to access line/section data communication channel (DCC) and voice communication channel (VCC)**
- **Full duplex UTOPIA/OIF-SPI (POS-PHY) level 3 interface** [15,16]
- **16-bit/32-bit host CPU interface bus**
- **JTAG and boundary scan**
- **Glue-less interface with Cypress CYS25G0101DX OC-48 PHY**
- **0.18-μm CMOS, 504-pin BGA package**
- **+1.8V for core, +3.3V for LVTTL I/O, +1.5V/+3.3V for HSTL/LVPECL I/O supply, and +0.75V/2.0V reference**

Applications

- Multiservice nodes
- ATM switches and routers
- Packet routers
- Multi-service routers
- SONET/SDH add-drop mux for packet/data applications
- SONET/SDH/ATM/POS test equipment

Notes:

1. ITU-T Recommendation G.707. “Network Node Interface for the Synchronous Digital Hierarchy.” 1996.
2. ITU-T Recommendation G.783. “Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks.” 2000.
3. Bellcore Publication GR-253-Core. “Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria.” 1997.
4. ITU-T Recommendation I.432.3. “B-ISDN User-Network Interface—Physical Layer Specification: 1544 kbit/s and 2048 kbit/s operation.” 1999.
5. American National Standards Institute. “Synchronous Optical Network (SONET)—Basic Description including Multiplex Structure, Rates and Formats.” ANSI T1.105–1995.
6. American National Standards Institute. “Synchronous Optical Network (SONET)—Payload Mappings.” ANSI T1.105.02–1998.
7. Simpson, W. “PPP Over SONET/SDH.” RFC 1619. May 1994.
8. Simpson, W., ed. “PPP in HDLC-like Framing.” RFC 1662. *Daydreamer.* July 1994.
9. Malis, A. and Simpson, W. “PPP Over SONET/SDH.” RFC 2615. June 1999.
10. Hernandez-Valencia, E. Lucent Technologies. “A Generic Frame Format for Data Over SONET (DoS).” March 2000.
11. Gorshe, C. and Steven. T1X1.5/99-204, T1 105.02. Draft Text for Mapping IEEE 802.3 Ethernet MAC Frames to SONET Payload. July 1999.
12. Hernandez-Valencia, E. Lucent Technologies. T1X1.5/2000-209. “Generic Framing Procedure (GFP) Specification.” October 9–13, 2000.
13. Carlson, J., P. Langner, E.J. Hernandez-Valencia, and J. Manchester. “PPP over Simple Data Link (SDL) using SONET/SDH with ATM-like Framing.” rfc2823.txt, May 2000.
14. Pankaj, K. “A Hybrid Data Transport Protocol for Optical Networks.” RFC draft-jha-optical-hdt-00.txt. November 2000.

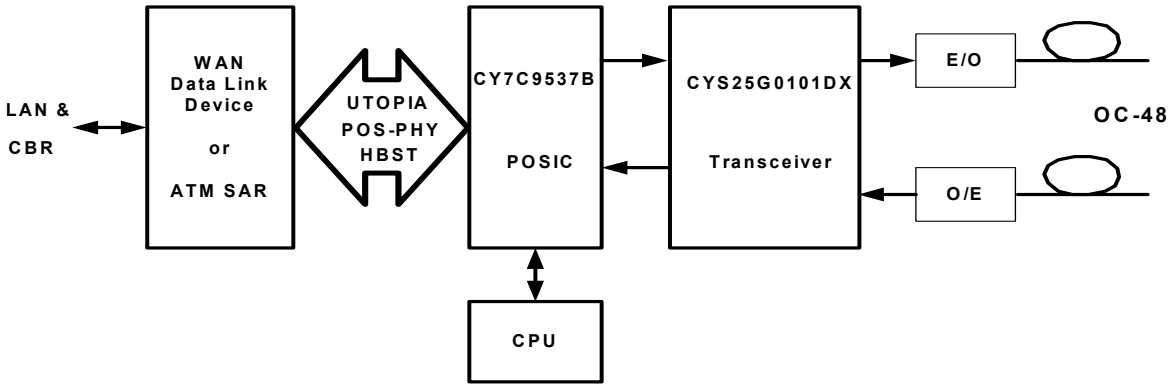
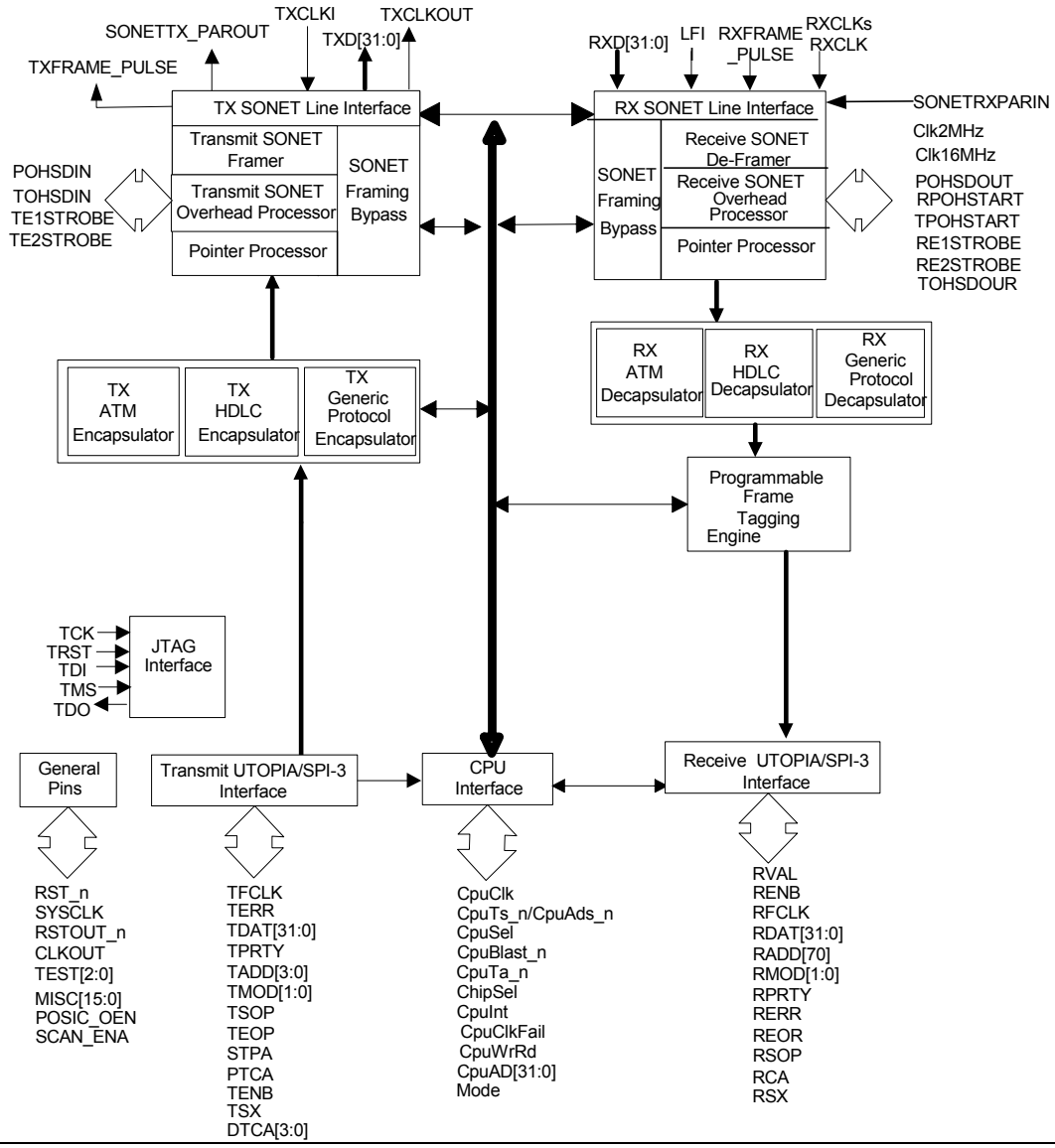


Figure 1. POSIC2G System Application Diagram

POSIC2G Logic Block Diagram



Overview

The CY7C9537B (POSIC2G) is a highly integrated SONET/SDH framer device for transport of ATM and IP packets over SONET/SDH links. It features special functions and architecture to support next-generation optical networking protocols for both SONET/SDH and direct data-over-fiber networks. UTOPIA level 3, OIF-SPI (POS-PHY) level 3 and high-bandwidth synchronous transfer (HBST) interfaces are provided on the system side.

POSIC2G performs complete SOH, LOH, and POH processing. Complete access to all overhead bytes is provided through register access via the host CPU interface. Access to selected overhead bytes is also available through the serial port. Optional frame sync input and Transport Overhead (TOH) bypass enables better interface with SPE/VC switched streams.

POSIC2G supports packet over SONET/SDH as PPP in HDLC-like frame as per IETF rfc 1619/1662/2615 (PPP). POSIC2G also supports full-duplex ATM over SONET/SDH transport in compliance with ITU I432.2.

The Generic Protocol Encapsulator/Decapsulator features wire rate framing, frame delineation and deframing with length-CRC pair header construct. Optional payload scrambling/descrambling and payload FCS are also provided. This enables POSIC2G to support many new-generation protocols like SDL, GFP, and HDT over SONET/SDH.

Clear channel mode enables transport of any raw byte streams on selected channels, while the rest of the channels are transporting data through any one of encapsulation/decapsulation engines.

The Programmable Frame Tagging Engine enables wire-rate tagging of packets/frames. For new-generation networking features such as MPLS, this engine can be programmed to tag based on existence/lack of specific label/field values, in the first 64 bytes of each packet. This way, packets are tagged for a variety of conditions, all programmable by the user, enabling sorting of packets in the incoming data stream and buffering packets accordingly. In a PPP application, control packets can optionally be sent over the host CPU interface directly.

SONET/SDH bypass mode allows use of this device for data transport in non-SONET/SDH point-to-point and mesh optical networks.

Transmit

In the transmit direction, packets are received from the system side, encapsulated/framed and mapped into the SONET/SDH payload. Finally the TOH is added and SONET/SDH frames are passed onto the fiber side/line side interface on a parallel bus.

The system side interface can be programmed either as UTOPIA level 3, or OIF-SPI level 3, or HBST modes. In the UTOPIA mode, ATM cells can be received either in 54- (8-bit interface) or 56- (8-bit and 32-bit interfaces) byte format. The sixth byte carries the channel number of the cell. In case of packets, the interface can be programmed as OIF-SPI level 3 or HBST operations. In these cases, the channel number is always carried in the first data transfer.

POSIC2G supports three basic types of encapsulation, namely (i) ATM, (ii) HDLC frame, and (iii) frames with length-CRC pair header construct based delineation. SDL, GFP and HDT frames are delineated based on length-CRC pair header construct and they are supported by POSIC2G. Clear channel or transparent mode (no encapsulation) is also supported. While in operation, only one type of encapsulation can be enabled for all channels. Some or all of the channels can be programmed as clear channels. For Clear Channels, the encapsulator engine will bypass the encapsulation and pass the packets without any processing to the next block.

Since POSIC2G does not have a packet storage memory on-chip, a channel bandwidth balanced packet flow is expected from the system side. To enable such a balanced transfer, POSIC2G has internal FIFO of 512 bytes per channel. The status of FIFO is provided through pins to the link layer.

Finally, the SONET/SDH framer inserts the packet/cells into the SONET/SDH frame. All overhead bytes are added. All alarm bits and status bits are inserted based on the status of incoming frames as well as programming done by the host CPU. The scrambler meets relevant standards and can optionally be disabled. Frames are finally sent out on the fiber side interface. If programmed to do so, the SONET/SDH framer can be bypassed and encapsulated packets/frames can be sent directly to the fiber-side interface.

Receive

In the receive direction, SONET/SDH frames are received from the fiber side. Data packets/frames are extracted from the payload and passed onto the selected decapsulator engine. If the SONET/SDH framer is bypassed, the incoming data stream is directly passed over to the decapsulator engine. Data packets/frames are then decapsulated and sent to the Programmable Frame Tagging Engine. They are then analyzed and tagged before being sent out to the system side via the UTOPIA, OIF-SPI level 3, or HBST interface. Tagging of frames is optional.

SONET/SDH frames entering from the fiber side are synchronized and the frame boundary is identified with A1A2 bytes. Frames can be optionally synchronized with Frame_Sync_Input to identify the boundary. Descrambling is performed to retrieve scrambled frames. Complete processing of all overhead bytes, Section, Line, and Path, is performed and all alarm bits are verified and alarms are raised as programmed. Full access to all overhead bytes is provided through register access. Access to selected overhead bytes is also provided through serial bus. The SONET/SDH deframing can be entirely bypassed.

The extracted payload is transferred to the decapsulator. The selected decapsulator engine delineates the payload stream, decapsulates and extracts packets/cells from the stream. Descrambling of packets/cells is optional. The packets/cells are then sent out to the programmable Frame Tagging Engine.

The Frame Tagging Engine optionally tags the packet/cell as programmed. The packet/cell is then transferred to the link layer device, through the System Interface (UTOPIA/OIF-SPI level 3, or HBST), with an additional eight bits of information. Four bits specify the channel and the other four bits specify the tag.

Protocol / Frame Types

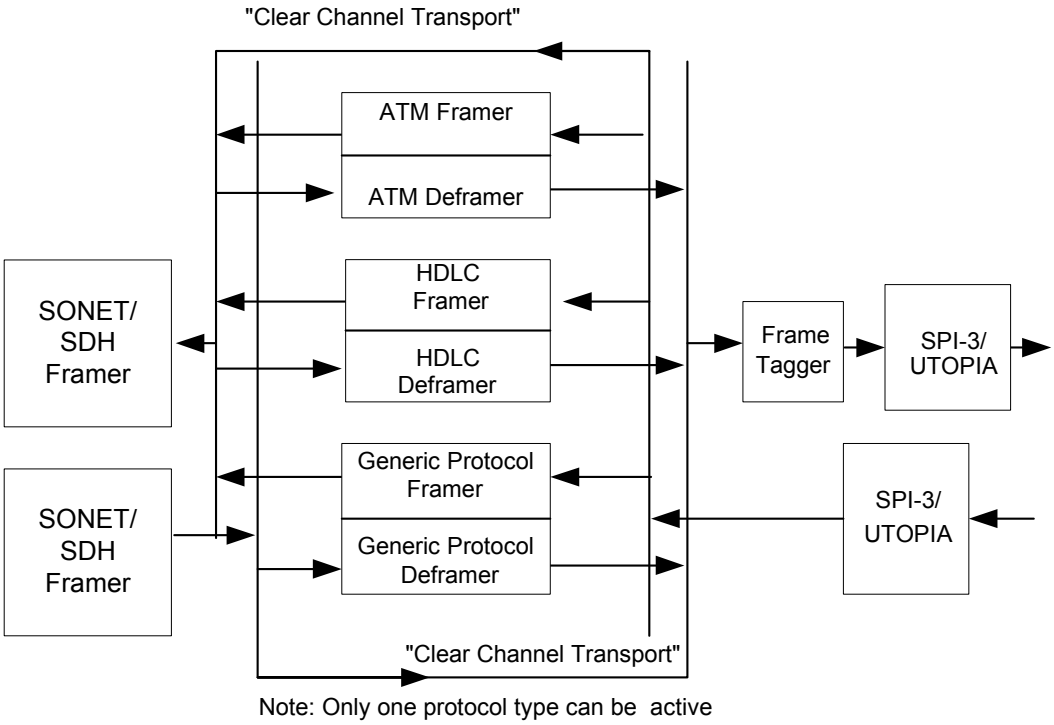


Figure 2. Protocol Framers

Generic Frame Encapsulation/Decapsulation

POSIC2G supports a variety of protocols/packets/frames to transport over a SONET/SDH link. For clarity of reference, in this document, framing of packets/cells into these protocols is called “encapsulation,” and the engine performing encapsulation is called an “encapsulator.” Similarly, deframing is called “decapsulation,” and the engine performing decapsulation is called a “decapsulator.”

Three different encapsulator and decapsulator engines are integrated into POSIC2G.

The ATM encapsulator computes and adds the HEC field, scrambles the cells and passes on to the SONET/SDH block. In case of underflow, ATM encapsulator also creates programmable idle cells.

The ATM decapsulator checks for HEC and integrity of the cell. It descrambles the cells, isolates and discards idle cells, and passes ATM cells to the Programmable Frame Tagging Engine.

The HDLC encapsulator performs Asynchronous Control Character Mapping (ACCM), stuffing, flag sequence insertion, and scrambling. Optionally, up to 16 bytes of header is inserted ahead of the packet while framing the packet. The host CPU can program this 16-byte header through register programming. Such programmable header insertion enables encapsulation of PPP, frame relay, or other protocol.

The HDLC decapsulator descrambles the incoming byte stream and searches the flag sequence. Upon finding the boundary, the decapsulator performs destuffing and ACCM demapping before passing the packets to the Programmable Frame Tagging Engine.

The Generic Protocol Encapsulator/Decapsulator supports all the protocols with delineation based on length-CRC pair header construct. In the transmit direction, it computes a 16-bit header CRC based on 2-byte length value received from the link layer device. The length and CRC fields are inserted as header of the frame ahead of the packet. Scrambling of the payload and 32-bit payload CRC computation and insertion are optional.

In the receive direction, frames are delineated based on the length-CRC construct pair header, integrity verified, payload extracted, optionally descrambled and sent to the Programmable Frame Tagging Engine.

The Generic Protocol Encapsulator/Decapsulator can support many protocols with length-CRC pair header construct as the frame delineation mechanism. For example, Simple Data Link (SDL), Generic Framing Procedure (GFP) in Data Over SONET (DOS) and Cypress Hybrid Data Transport (HDT) have frame structure supporting length-CRC construct based delineation.

Any selected channel can be programmed to become a clear channel. The encapsulator and decapsulator remain in transparent mode for the clear channel and data passes through without any modification. This feature can be used to transport any raw data streams on a portion of bandwidth while the rest of the bandwidth is utilized for protocol traffic.

Programmable Frame Tagging Engine

The Programmable Frame Tagging Engine provides preclassification of the packets/frames at the wire rate. This helps in utilizing the link layer device more efficiently.

The Programmable Frame Tagging Engine enables the user to perform preclassification of all the incoming packets into one of the 16 possible categories. Since each channel can have up to 16 different categories, and up to 16 concatenated channels are possible, this engine supports up to 256 different categories. For classification, two-pass comparison can be specified. For each comparison a field of up to six bytes can be selected within the first 64 bytes of the packet and compared with up to 16 programmed values. The comparison is on a bit by bit basis and any bit comparison can be masked with a user programmable mask register. A four-bit tag is attached to the cell/packet, based on the match. Host CPU can program these parameters through register programming.

The following functions can be achieved with the help of the Programmable Frame Tagging Engine:

- Incoming packet analysis to parse packets/frames/cells at wire speed.
- User-programmable routing of control packets to CPU for processing.
- Incoming frames tagged based on bits (such as congestion) in incoming packets.
- User-programmable offset to locate Ethernet and other frames within DOS and other proprietary M.AN networking protocols to allow MPLS processing.

SONET/SDH Bypass

POSIC2G supports the SONET/SDH framer/deframer bypass mode. Host CPU can program such bypass. In this mode, the data frames/packets, encapsulated by one of the encapsulators, will be transmitted transparently through SONET/SDH blocks to the fiber side and vice versa.

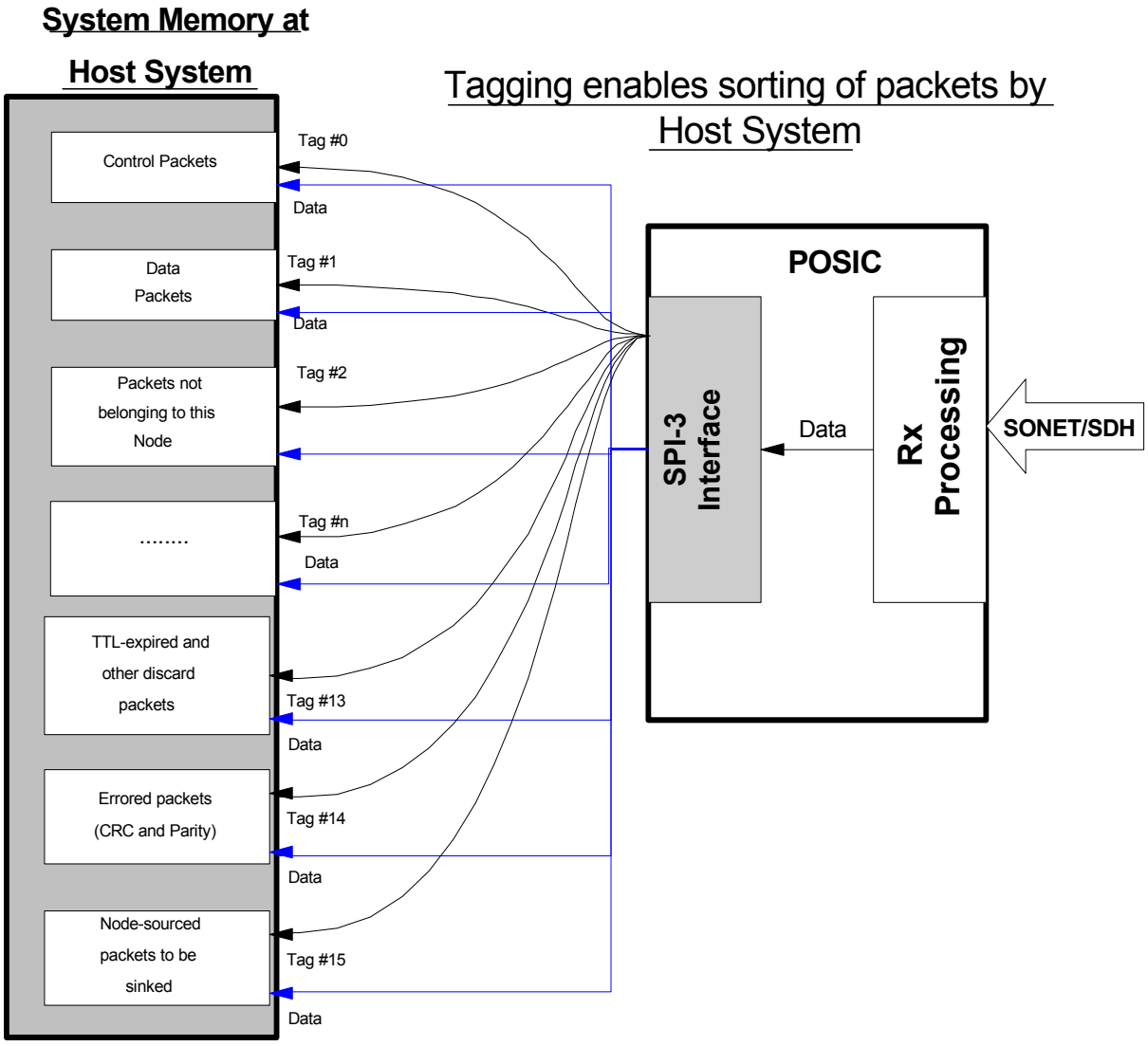


Figure 3. Frame Tagging Engine Data Sorting Diagram

System Interface

The system interface is programmable. For an application in an ATM system, the POSIC2G system interface can be programmed to be a PHY side interface as per UTOPIA level 3 specifications.

For variable length packets, the POSIC2G system interface can be programmed to be OIF-SPI level 3. ATM cells can also be transferred over a OIF-SPI level 3 bus.

The system interface can be programmed in HBST mode. In this case, a separate set of address pins are supported on the system side. This mode supports high-speed burst access.

CPU Interface

POSIC2G can interface with a 16-bit or 32-bit CPU. The CPU interface can be pin configured to be compatible with a Motorola or Intel bus interface. The CPU interface provides access to all registers of POSIC2G, collates all interrupt generated by various blocks and also supports control packet transfers.

Line Interface

The line interface/fiber side interface is configurable as 8-bit, 16-bit, or 32-bit, depending on the clock frequency and data rate. The options shown in *Table 1* are available.

Table 1. Configuration Options

Bus Width	Clock Frequency	Line Rate
8 bits	19.44 MHz	OC-3/STM-1
8 bits	77.76 MHz	OC-12/STM-4
16 bits	38.88 MHz	OC-12/STM-4
16 bits	155.52 MHz	OC-48/STM-16
32 bits	77.76 MHz	OC-48/STM-16

Clock Source

The transmit clock can be programmed to be one of the following sources:

- Received clock supplied by the PHY.
- External transmit clock source.

APS Port

POSIC2G provides a 16-bit APS port for 1+1 protection. The support of a main and standby PHY interface connectivity allows several different APS implementation options using POSIC2G.

Multi-Framer APS Implementation

Two POSIC2G devices can be connected to two different transceivers, optics and fibers. POSIC2G enables protection switching with only one device being main and connected to link layer. The standby POSIC2G device is connected to the main POSIC2G device and it is controlled by host CPU. POSIC2G provides APS byte information to the host CPU. The host CPU is expected to take a protection switching decision and provide necessary instructions to both POSIC2G devices.

In case of protection switching, in the transmit direction, the main POSIC2G will perform all other operations as programmed, except some of the line and section processing of SONET/SDH framing. The main POSIC2G device will then pass on the SPEs to the standby device through the APS port. The standby device will then perform the rest of the line and section processing and transport SONET/SDH frames over standby fiber.

Similarly, in case of protection switched mode, on the receive side, the standby device will process some of the line and section overhead and transfer the frames to main device through the APS port. The main device will perform the rest of the processing in the receive side.

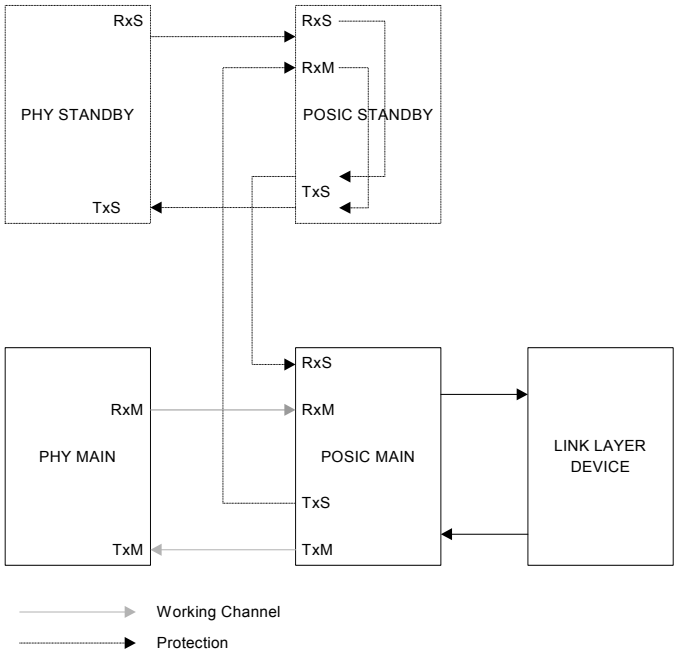


Figure 4. POSIC2G APS Implementation using Two POSIC Devices

Single Framer APS Implementation

A main and slave PHY device can be interfaced directly to the main and APS ports of a single POSIC2G device. In this case, the main PHY is connected to the main line interface and the standby PHY is connected to the APS port.

In the POSIC2G transmit path, SONET/SDH data is bridged across the main and APS ports (per linear 1+1 APS requirements). When protection switching, POSIC2G can be programmed to switch line inputs from the main receive port to the APS receive port, or vice versa.

This APS scheme provides solely optical/PHY link level protection.

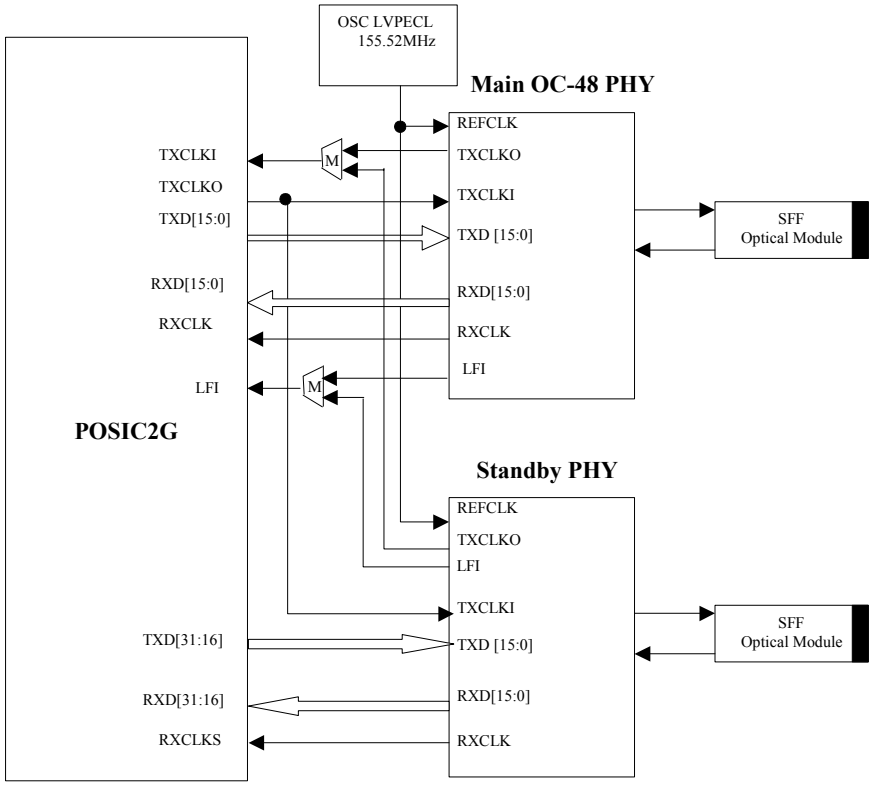
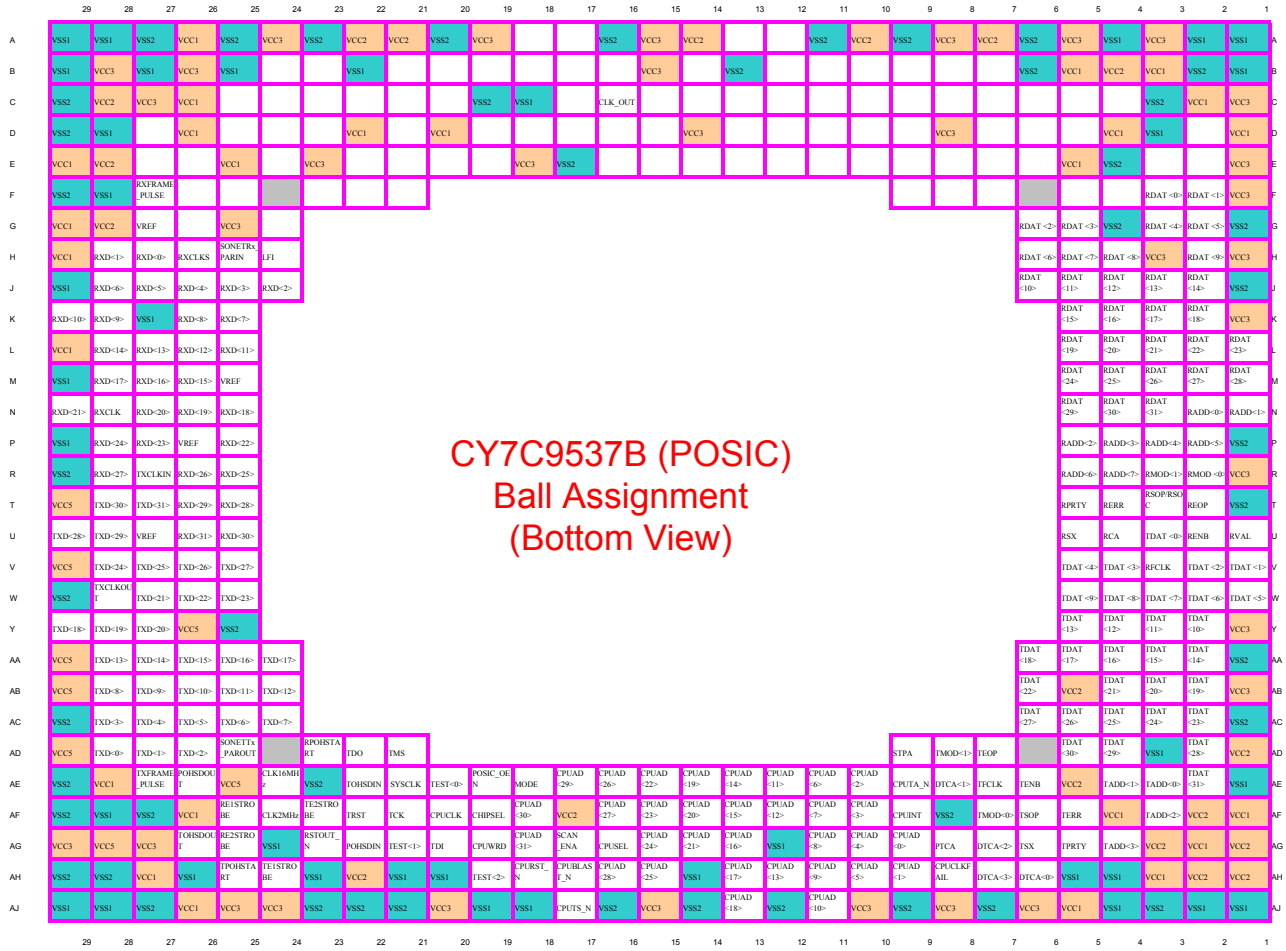


Figure 5. POSIC2G APS Implementation Using a Single POSIC Device

Pin Configuration



Pin Description

Signal Name	I/O	Pad Type	Pins	JTAG	Description
Line Interface Signals					
RXFRAME_PULSE	I	HSTL/LVTTL /LVPECL	1	N	**Optional Frame pulse input for line interface**. Active HIGH.
TXFRAME_PULSE	O	HSTL/LVTTL	1	N	**Frame pulse output for line interface**. Active HIGH.
RXD[31:0]	I	HSTL/LVTTL /LVPECL	32	N	**32-bit single ended receive data bus for SONET/SDH link**. This bus can be configured as two 16-bit buses in APS operation.
RXCLK	I	HSTL/LVTTL /LVPECL	1	N	**Receive clock input from the PHY device for line interface**.
RXCLKs	I	HSTL/LVTTL /LVPECL	1	N	**Receive clock input from the Slave PHY device for SONET/SDH link to support APS**.
TXCLKOUT	O	HSTL/LVTTL	1	N	**Transmit Clock to physical layer device for line interface**. This will be RXCLK or the TXCLKI based on the clock selection in the SONET Tx block register. During loopback this is same as the RXCLK.
TXCLKI	I	HSTL/LVTTL /LVPECL	1	N	**Input transmit clock from physical layer device for line interface**.
TXD[31:0]	O	HSTL/LVTTL	32	N	**32-bit single ended transmit data bus for line interface**. This bus can be configured as two 16-bit buses in APS operation.
SONETTX_PAROUT	O	HSTL/LVTTL	1	N	**SONET Tx Parity Output**. Can be ODD/EVEN parity, as programmed in the SONET/SDH Tx block register.
SONETRX_PARIN	I	HSTL/LVTTL /LVPECL	1	N	**SONET Rx Parity Input**. Can be ODD/EVEN parity, as programmed in the SONET/SDH Rx block register.
LFI_n	I	LVTTL	1	N	**Line fault indicator**. When LOW, this signal indicates that the PHY has detected Loss of Optical signal on the SONET link.
Overhead Bytes Access – Serial Ports					
Clk2MHz	O	LVTTL	1	N	**TOH Serial Port Clock Output**. TOHDout is clocked out on the rising edge of this clock and TOHDin is latched-in with the falling edge of this clock. The frequency is 2.048 MHz, derived from SysClk.
Clk16MHz	O	LVTTL	1	N	**POH Serial Port Clock Output**. POHDout is clocked out on rising edge of this clock and POHDin is latched-in with falling edge of this clock. The frequency is 16.625 MHz, derived from SysClk
TE1STROBE	O	LVTTL	1	N	**Transmit E1 Strobe**. Transmit TOH serial port data start indication. Active HIGH pulse generated once in every 125 ms. Indicates the first bit of E1 Byte.
TE2STROBE	O	LVTTL	1	N	**Transmit E2 Strobe**. Active HIGH pulse generated once in every 125 ms. Indicates the first bit of E2 Byte.
TPOHSTART	O	LVTTL	1	N	**Transmit POH Serial Port Data Start Indication**. Active HIGH pulse generated once in every 125 ms.
TOHSDIN	I	LVTTL	1	N	**Transport over head serial port data input**.
POHSDIN	I	LVTTL	1	N	**Path over head serial port data input**.
RE1STROBE	O	LVTTL	1	N	**Receive E1 Strobe**. Receive TOH serial port data start indication. Active HIGH pulse generated once in every 125 ms. Indicates that the POSIC2G expects the first bit of the first byte of E1 should accompany the next clock edge. MSB is transmitted first.
RE2STROBE	O	LVTTL	1	N	**Receive E2 Strobe**. Active HIGH pulse generated once in every 125 ms. Indicates that the POSIC2G expects the first bit of the first byte of E2 should accompany the next clock edge. MSB is transmitted first.
RPOHSTART	O	LVTTL	1	N	**Receive POH Serial Port Data Start Indication**. Active HIGH pulse generated once in every 125 ms. Indicates that the POSIC2G expects the first bit of the first byte of RPOH should accompany the next clock edge.
TOHSDOUT	O	LVTTL	1	N	**Transport over head serial port data output**.
POHSDOUT	O	LVTTL	1	N	**Path over head serial port data output**.

Pin Description (continued)

Signal Name	I/O	Pad Type	Pins	JTAG	Description
System Interface (OIF-SPI level 3/UTOPIA level 3/HBST) signals (in this section, POS = OIF-SPI Level 3, ATM = Utopia level 3 mode)					
RVAL	O	LVTTL	1	N	**POS:** **Receive Data Valid (RVAL) signal.** RVAL indicates the validity of receive data signals. RVAL will transition LOW when receive FIFO is empty or at the end of a packet. When RVAL is HIGH, the RDAT[31:0], RPRTY, RMOD[1:0], RSOP, REOP, and RERR signals are valid. When RVAL is LOW, the RDAT[31:0], RPRTY, RMOD[1:0], RSOP, REOP, and RERR signals are invalid and must be disregarded. **HBST:** **Receive Data Valid (RDVAL) signal.** The RDATA, RBVAL, RSOP, REOP, RERR, and RADDR are valid when this signal is active.
RENB	I	LVTTL	1	N	**POS:** **Receive Read Enable (RENB) signal.** The RENB signal is used to control the flow of data from the receive FIFOs. During data transfer, RVAL must be monitored as it will indicate if the RDAT[31:0], RPRTY, MOD[1:0], RSOP, REOP, RERR and RSX are valid. The system may deassert RENB at anytime if it is unable to accept data from POSIC2G. When RENB is sampled LOW by POSIC2G, a read is performed from the receive FIFO and the RDAT[31:0], RPRTY, RMOD[1:0], RSOP, REOP, RERR, RSX and RVAL signals are updated on the following rising edge of RFCLK. When RENB is sampled HIGH by POSIC2G, a read is not performed and the RDAT[31:0], RPRTY, RMOD[1:0], RSOP, REOP, RERR, RSX and RVAL signals will not be updated. **ATM:** **Enable Data Transfers (RxENb*) signal** Enables port selection. **HBST:** **Receive Data Ready (RREADY_n) signal** Active LOW signal, indicates ready to accept data. The device will send valid data 2 clocks after the assertion of this signal.
RFCLK	I	LVTTL	1	N	**POS:** **Receive FIFO Write Clock (RFCLK).** RFCLK is used to synchronize data transfer transactions between the LINK Layer device and the POSIC2G. RFCLK may cycle at a rate up to 100 MHz. **ATM:** **Transfer/interface clock (RxClk)** **HBST:** **Receive Clock (RCLK).** Max 104-MHz Receive Clock for level-3 operation. All signals are latched out on the rising edge of this clock.

Pin Description (continued)

Signal Name	I/O	Pad Type	Pins	JTAG	Description
RDAT[31:0]	O	LVTTL	32	N	**POS:** **Receive Packet Data Bus (RDAT[31:0])** The RDAT[31:0] bus carries the packet octets that are read from the receive FIFO and the in-band port address of the selected receive FIFO. RDAT[31:0] is considered valid only when RVAL is asserted. Given the defined data structure, bit 31 is received first and bit 0 is received last. **ATM:** **Receive Cell Data Bus (RxData[31:0])** The RDAT[31:0] bus carries the cell octets that are read from the receive FIFO. RDAT[31:0] is considered valid only when RENB is asserted. Given the defined data structure, bit 31 is received first and bit 0 is received last RDAT[31:0] is updated on the rising edge of RCLK. This bus is big-endian in format. **HBST:** **Receive Data Bus (RDATA[31:0])** 32-bit Data Bus, the data is valid when RDVAL signal is active.
RADD[7:0]	O	LVTTL	8	N	**HBST:** **Receive Port Address (RADDR[7:0]).** When RDVAL signal is active, this address on this bus indicates port address in RADDR[3:0] and tag value in RADDR[7:4]. In single-channel mode all 8 bits will contain the tag value. RADDR is considered valid only when RDVAL is asserted
RMOD[1:0]	O	LVTTL	2	N	**POS:** **Receive Word Modulo (RMOD[1:0]) signal.** RMOD[1:0] indicates the number of valid bytes of data in RDAT[31:0]. The RMOD bus should always be all zero, except during the last double-word transfer of a packet on RDAT[31:0]. When REOP is asserted, the number of valid packet data bytes on RDAT[31:0] is specified by RMOD[1:0] RMOD[1:0] = “00” RDAT[31:0] valid RMOD[1:0] = “01” RDAT[31:8] valid RMOD[1:0] = “10” RDAT[31:16] valid RMOD[1:0] = “11” RDAT[31:24] valid RMOD[1:0] is considered valid only when RVAL is asserted. **HBST:** **Receive Data Byte Valid (RBVAL[1:0]) signals.** This indicates the number of bytes data bytes valid on the RDATA bus, 00 = 4 bytes valid, 11 = 1 byte valid.
RPRTY	O	LVTTL	1	N	**POS:** **Receive Parity (RPRTY) signal.** The receive parity (RPRTY) signal indicates the parity calculated over the RDAT bus. RPRTY supports both odd and even parity. **ATM:** **Receive Parity (RxPrty) signal.** Data bus odd parity. **HBST:** **Receive Bus Parity (RPARITY) signal.** Receive bus parity, Even/Odd parity calculated on the data bus alone or on all the bus signals (RDATA, RADDR, RDVAL, RBVAL, RSOP, REOP, RERR).

Pin Description (continued)

Signal Name	I/O	Pad Type	Pins	JTAG	Description
RERR	O	LVTTL	1	N	**POS:** **Receive Error Indicator (RERR) signal.** RERR is used to indicate that the current packet is aborted and should be discarded. RERR shall only be asserted when REOP is asserted. Conditions that can cause RERR to be set may be, but are not limited to, FIFO overflow, abort sequence detection, and FCS error. RERR is considered valid only when RVAL is asserted. **HBST:** **Receive Error Indicator (RERR) signal.** A HIGH indicates the current packet or cell has error.
REOP	O	LVTTL	1	N	**POS:** **Receive End Of Packet (REOP) signal.** REOP is used to delineate the packet boundaries on the RDAT bus. When REOP is HIGH, the end of the packet is present on the RDAT bus. REOP is required to be present at the end of every packet and is considered valid only when RVAL is asserted. **HBST:** **End of Packet/Cell (REOP) signal.** A HIGH indicates the end of packet or cell.
RSOP/RSOC	O	LVTTL	1	N	**POS:** **Receive Start of Packet (RSOP) signal.** RSOP is used to delineate the packet boundaries on the RDAT bus. When RSOP is HIGH, the start of the packet is present on the RDAT bus. RSOP is required to be present at the start of every packet and is considered valid when RVAL is asserted. **ATM:** **Receive Start of Cell (RxSOC).** This signal marks the start of a cell structure on the RxData bus. The first word of the cell structure is present on the RxData[31:0] bus when RxSOC is HIGH. RxSOC is updated on the rising edge of RxClk. **HBST:** **Receive Start of Packet/Cell (RSOP) signal.** A HIGH indicates start of packet or start of cell.
RCA	O	LVTTL	1	N	**ATM:** **UTOPIA Receive Cell Available (RxClav).** RxClav will be asserted, whenever a minimum of 1 cell of data is available in the Receive FIFO. **HBST:** **Receive FIFO Available (RSTFA) signal.** RSTFA indicates when data is available in the receive FIFO. RSTFA will be asserted, whenever receive FIFO has at least predefined number of bytes to be read (the number of bytes is user programmable). RSTFA is updated on the rising edge of RCLK.
RSX	O	LVTTL	1	N	**POS:** **Receive Start of Transfer signal.** RSX indicates when the in-band port address is present on the RDAT bus. When RSX is HIGH and RVAL is LOW, the value of RDAT[7:0] is the address of the receive FIFO to be selected by POSIC2G. Subsequent data transfers on the RDAT bus will be from the port as specified by the in-band address.

Pin Description (continued)

Signal Name	I/O	Pad Type	Pins	JTAG	Description
TFCLK	I	LVTTL	1	N	**POS:** **Transmit FIFO Write Clock (TFCLK).** TFCLK is used to synchronize data transfer transactions between the LINK Layer device and POSIC2G. TFCLK may cycle at a rate up to 100 MHz. **ATM:** **Transfer/Interface Clock (TxClk).** **HBST:** **Transmit Clock (TCLK).** Max. 104-MHz Transmit Clock for level-3 operation. All transmit signals are sampled on rising edge of the clock.
TERR	I	LVTTL	1	N	**POS:** **Transmit Error Indicator (TERR) signal.** TERR is used to indicate that the current packet should be aborted. When TERR is set HIGH, the current packet is aborted. TERR should only be asserted when TEOP is asserted. **HBST:** **Transmit Error Indicator (TERR) signal.** A HIGH indicates the current packet or cell has error.
TENB	I	LVTTL	1	N	**POS:** **Transmit Write Enable (TENB) signal.** The TENB signal is used to control the flow of data to the transmit FIFOs. When TENB is HIGH, the TDAT, TMOD, TSOP, TEOP, and TERR signals are invalid and are ignored by POSIC2G. The TSX signal is valid and is processed by POSIC2G when TENB is HIGH. When TENB is LOW, the TDAT, TMOD, TSOP, TEOP and TERR signals are valid and are processed by POSIC2G. Also, the TSX signal is ignored by POSIC2G when TENB is LOW. **ATM:** **Transmit Write Enable (TxEnb*).** This signal is an active LOW input which is used to initiate writes to the transmit FIFOs. When TxEnb* is sampled HIGH, the information sampled on the TxData, TxPrty, and TxSOC signals are invalid. When TxEnb* is sampled LOW, the information sampled on the TxData, TxPrty, and TxSOC signals are valid and are written into the transmit FIFO. TxEnb* is sampled on the rising edge of TxClk. **HBST:** **Transmit Data Valid (TDVAL_n) signal.** The TDVAL_n signal is used to control the flow of data to the transmit FIFOs. When TDVAL_n is HIGH, the TDATA, TBVAL, TSOP, TADDR, TSOP, TEOP, and TERR signals are valid and are processed by POSIC2G.

Pin Description (continued)

Signal Name	I/O	Pad Type	Pins	JTAG	Description
TDAT[31:0]	I		32	N	**POS:** **Transmit Packet Data Bus (TDAT) bus.** This bus carries the packet octets that are written to the selected transmit FIFO and the in-band port address to select the desired transmit FIFO. The TDAT bus is considered valid only when TENB is simultaneously asserted. Data is transmitted in big endian order on TDAT[31:0]. Given the defined data structure, bit 31 is transmitted first and bit 0 is transmitted last. **ATM:** **Transmit Data Bus (TxData) bus.** This data bus carries the ATM cell. Data on this bus is valid only if TxEnb* is HIGH. TxData[31:0] is three-stated if TxEnb* is LOW. TxData[31:0] is updated on the rising edge of TxClk. **HBST:** **Transmit Data Bus (TDATA) bus.** 32-bit Data bus. The data is valid when TDVAL_n signal is active.
TPRTY	I	LVTTL	1	N	**POS:** **Transmit Bus Parity (TPRTY) signal.** The transmit parity (TPRTY) signal indicates the parity calculated over the TDAT bus. TPRTY is considered valid only when TENB is asserted. TPRTY is supported for both even and odd parity. **ATM:** **Transmit Bus Parity (TxPrty).** This signal indicates the parity on the TxData bus. A parity error is indicated by a status bit and a maskable interrupt. TxPrty is considered valid only when TxEnb* is simultaneously asserted. TxPrty is sampled on the rising edge of TxClk. **HBST:** **Transmit Bus Parity (TPARITY) signal.** Even/Odd parity calculated on the data bus alone or on all the bus signals (TDATA, TADDR, TDVAL_n, TBVAL, TSOP, TEOP, and TERR).
TADD[3:0]	I	LVTTL	4	N	**POS:** **Transmit Address Bus (PTADR) bus.** Address driven by Link layer to poll and select the appropriate POSIC2G channel (port). The value for the Transmit and Receive portions of a channel should be identical. Address 31 indicates a null port. **ATM:** **Transmit Address Bus (TxAddr) bus.** Address of POSIC2G channel being selected. **HBST:** **Port Address (TADDR) bus.** Address driven by the Link Layer to indicate the port address of current data transfer.

Pin Description (continued)

Signal Name	I/O	Pad Type	Pins	JTAG	Description
TMOD[1:0]	I	LVTTL	2	N	**POS:** **Transmit Word Modulo (TMOD[1:0]) signal.** TMOD[1:0] indicates the number of valid bytes of data in TDAT[31:0]. The TMOD bus should always be all zero, except during the last double-word transfer of a packet on TDAT[31:0]. When TEOP is asserted, the number of valid packet data bytes on TDAT[31:0] is specified by TMOD[1:0]. TMOD[1:0] = “00” TDAT[31:0] valid TMOD[1:0] = “01” TDAT[31:8] valid TMOD[1:0] = “10” TDAT[31:16] valid TMOD[1:0] = “11” TDAT[31:24] valid In 16-bit mode, only TMOD[0] is valid. TMOD[0] = “1” TDAT[15:8] valid (16-bit mode) TMOD[0] = “0” TDAT[15:0] valid (16-bit mode) **HBST:** **Transmit Byte Valid (TBVAL[1:0]) signals.** This indicates the number of bytes data bytes on the TDATA bus, 00 = 4 bytes valid, 11 = 1 byte valid.
TSOP	I	LVTTL	1	N	**POS:** **Transmit Start of Packet (TSOP) signal.** TSOP is used to delineate the packet boundaries on the TDAT bus. When TSOP is HIGH, the start of the packet is present on the TDAT bus. TSOP is required to be present at the beginning of every packet and is considered valid only when TENB is asserted. **ATM:** **Transmit Start of Cell (TxSOC) signal.** This signal marks the start of a cell structure on the TxData bus. TxSOC must be present for each cell. TxSOC is considered valid only when TxEnb* is simultaneously asserted. TxSOC is sampled on the rising edge of TxClk. **HBST:** **Transmit Start of Packet (TSOP) signal.** A high indicates the start of packet or start of cell.
TEOP	I	LVTTL	1	N	**POS:** **Transmit End of Packet (TEOP) signal.** TEOP is used to delineate the packet boundaries on the TDAT bus. When TEOP is HIGH, the end of the packet is present on the TDAT bus. TEOP is required to be present at the end of every packet and is considered valid only when TENB is asserted. **HBST:** **Transmit End of Packet (TEOP) signal.** A HIGH indicates the end of packet or end of cell.
DTCA[3:0]	O	LVTTL	4	N	**POS:** **Transmit Packet Available (DTPA) bus.** This signal provides direct status indication of the fill status of the transmit FIFO. Note that, regardless of what fill level TPA is set to indicate “full” at, the transmit packet processor can store 256 bytes of data. When DTPA transitions HIGH, it indicates that the transmit FIFO has enough room to store a configurable number of data bytes. This transition level is selected in the CPU programmable registers. When TPA transitions LOW, it indicates that the transmit FIFO is either full or near full as specified by the CPU programmable registers. DTPA is updated on the rising edge of TFCLK. **HBST:** **Polled FIFO Available Status (TFAST) bus.** When the signal TSOFST is active, the status of channels 0,4,8,12 is given first followed by 1,5,9,13 and 2,6,10,14 and the last 3,7,11,15.

Pin Description (continued)

Signal Name	I/O	Pad Type	Pins	JTAG	Description
STPA	O	LVTTL	1	N	**POS:** **Selected Channel Transmit Packet Available (STPA) signal.** STPA transitions HIGH when a predefined minimum number of bytes are available in the selected transmit FIFO. Once HIGH, STPA indicates that transmit FIFO is not full. When STPA transitions LOW, it optionally indicates that transmit FIFO is full or near full (user programmable). STPA always provides status indication for the selected channel in order to avoid FIFO overflows while polling is performed. STPA is three-stated when TENB is deasserted in the previous cycle. STPA is also deasserted when either the null-port address (0x1F) or an address not matching the POSIC2G address is presented on the TADR[3:0] signals when TENB is sampled HIGH (has been deasserted during the previous clock cycle). STPA is mandatory only if packet-level transfer mode is supported. It is not be driven in byte-level mode. **ATM:** There is no corresponding pin definition in ATM mode, however, this pin will output the same signal as STPA in POS mode **HBST:** **FIFO Available Status (TSTFA) signal.** FIFO available status of the selected port is reflected on this pin two clocks after detecting the port address when the TDVAL signal is active.
PTCA	O	LVTTL	1	N	**POS:** **Polled-Port Transmit Packet Available (PTPA) signal.** PTPA transitions HIGH when a predefined (user-programmable) minimum number of bytes are available in the polled transmit FIFO. Once HIGH, PTPA indicates that the transmit FIFO is not full. When PTPA transitions LOW, it optionally indicates that transmit FIFO is full or near full (user-programmable). PTPA allows polling the POSIC2G channel selected by TADR[3:0] when TENB is asserted. PTPA is driven by a POSIC2G when its address is polled by TADR[3:0]. POSIC2G will three-state PTPA when either the null-port address (0x1F) or an address not matching POSIC2G is provided on TADR[3:0]. PTPA is mandatory only if in packet-level transfer mode. It will not be driven in byte-level mode. **ATM:** **UTOPIA Transmit Cell Available (TxClav)** The TxClav signal indicates when a cell is available in the transmit FIFO for the port polled by TxAddr[3:0] when TxEnb* is asserted. When HIGH, TxClav indicates that the corresponding transmit FIFO is not full and a complete cell may be written. When TxClav goes LOW, it can be configured to indicate either that the corresponding transmit FIFO is near full or that the corresponding transmit FIFO is full. TxClav is three-stated when either the null-Port address (0x1F) or an address not matching the address space set is latched from the TxAddr[4:0] inputs when TxEnb* is HIGH. TxClav is updated on the rising edge of TxClk. **HBST:** **FIFO Available status on TFAST bus (TSOFST) signal.** Active HIGH pulse indicates the start of FIFO available status on TFAST bus. This signal is repeated once in every four clocks.
TSX	I	LVTTL	1	N	**POS:** **Transmit Start of Transfer (TSX) signal.** TSX indicates inband port address on the TDAT bus. When TENB is HIGH and TSX is asserted (HIGH), the value of TADR[3:0] is the address of transmit FIFO selected. TSX is valid only when TENB is deasserted.

Pin Description (continued)

Signal Name	I/O	Pad Type	Pins	JTAG	Description
CPU Interface Signals					
CpuClk	I	LVTTL	1	N	**CPU Clock**.
CpuSel	I	LVTTL	1	Y	**Used to select between Intel and Motorola CPU**. '0' = Motorola, '1' = Intel.
CpuTs_n/CpuAds_n	I	LVTTL	1	Y	**Transfer Start**. Active LOW.
CpuWrRd	I	LVTTL	1	Y	**Write/Read Signal**. In Intel mode, this signal is active HIGH during write operation. In Motorola mode, this signal is active LOW during write operation.
CpuTa_n	O	LVTTL	1	Y	**Transfer Acknowledge/Data Ready**. Active LOW. Open Drain Output
CpuBlast_n/ CpuBdip_n	I	LVTTL	1	Y	**Used with Burst Transaction**. Active LOW.
CpuInt/	O	LVTTL	1	Y	**Interrupt to CPU**. Active LOW.
CpuClkFail	O	LVTTL	1	Y	**CPU Clock fail signal**. When LOW indicates failure of CPU clock.
CpuAD[31:0]	I/O	LVTTL	32	Y	**Address/Data Bus**.
ChipSel	I	LVTTL	1	Y	**The chip select signal for POSIC2G**. Active Low
Mode	I	LVTTL	1	Y	**32/16 bit mode select**. '0' = 32-bit mode, '1' otherwise
JTAG Interface Signals					
TCK	I	LVTTL	1		JTAG Mode: Test clock
TRST	I	LVTTL	1		JTAG Mode: Test reset
TDI	I	LVTTL	1		JTAG Mode: Test input
TMS	I	LVTTL	1		JTAG Mode: Test mode Select. Pull-down to GND during POSIC2G normal operation.
TDO	O	LVTTL	1		JTAG Mode: Test Output
Miscellaneous Signals					
VREF	I	VREF	4	N	**Reference Voltage for HSTL and LVPECL inputs**. Set to GND during LVTTL mode of operation.
RST_n	I	LVTTL	1	N	**Active LOW asynchronous reset input**.
SYSCLK	I	LVTTL	1	N	**133-MHz System Clock**.
CLKOUT	O	LVTTL	1	N	**SYSCLK Out**.
RSTOUT	O	LVTTL	1	Y	**Reset Out**. This pin will go LOW when writing a "1" to the Device Reset Register (Block Addr = 0x00, Reg Addr = 0xb) to deactivate the chip from the reset condition.
TEST[2:0]	I	LVTTL	3	Y	**Test Mode selection signals**. Pull-up to '1' during POSIC2G normal operation.
SCAN_ENA	I	LVTTL	1	Y	**SCAN ENABLE pin**. Active HIGH. During POSIC2G normal operation this signal should be LOW.
POSIC_OEN	I	LVTTL	1	N	**The POSIC2G Output Enable (POSIC_OEN) signal**. When set to logic one, all POSIC2G outputs (except CpuTa_n) are held three-state. When POSIC_OEN is set to logic zero, all interfaces are enabled. Pull-down to '0' for normal operation.
Total IO Pins			**336**		
Power: VCC Pad+Core	P		85		
Power: GND Pad+Core	P		83		
TOTAL			504		I/Os: 336; Power: 168

Pin Assignment

Pin assignment is tentative. Please check with Cypress for final information.

Pin Assignment Table

Signal	Ball	Pin Type
RDAT<0>	F3	LVTTL_OUT
RDAT<1>	F2	LVTTL_OUT
RDAT<10>	J6	LVTTL_OUT
RDAT<11>	J5	LVTTL_OUT
RDAT<12>	J4	LVTTL_OUT
RDAT<13>	J3	LVTTL_OUT
RDAT<14>	J2	LVTTL_OUT
RDAT<15>	K5	LVTTL_OUT
RDAT<16>	K4	LVTTL_OUT
RDAT<17>	K3	LVTTL_OUT
RDAT<18>	K2	LVTTL_OUT
RDAT<19>	L5	LVTTL_OUT
RDAT<2>	G6	LVTTL_OUT
RDAT<20>	L4	LVTTL_OUT
RDAT<21>	L3	LVTTL_OUT
RDAT<22>	L2	LVTTL_OUT
RDAT<23>	L1	LVTTL_OUT
RDAT<24>	M5	LVTTL_OUT
RDAT<25>	M4	LVTTL_OUT
RDAT<26>	M3	LVTTL_OUT
RDAT<27>	M2	LVTTL_OUT
RDAT<28>	M1	LVTTL_OUT
RDAT<29>	N5	LVTTL_OUT
RDAT<3>	G5	LVTTL_OUT
RDAT<30>	N4	LVTTL_OUT
RDAT<31>	N3	LVTTL_OUT
RDAT<4>	G3	LVTTL_OUT
RDAT<5>	G2	LVTTL_OUT
RDAT<6>	H6	LVTTL_OUT
RDAT<7>	H5	LVTTL_OUT
RDAT<8>	H4	LVTTL_OUT
RDAT<9>	H2	LVTTL_OUT
RADD<0>	N2	LVTTL_OUT
RADD<1>	N1	LVTTL_OUT
RADD<2>	P5	LVTTL_OUT
RADD<3>	P4	LVTTL_OUT
RADD<4>	P3	LVTTL_OUT
RADD<5>	P2	LVTTL_OUT
RADD<6>	R5	LVTTL_OUT
RADD<7>	R4	LVTTL_OUT
RERR	T4	LVTTL_OUT

Pin Assignment Table (continued)

Signal	Ball	Pin Type
RMOD<0>	R2	LVTTL_OUT
RMOD<1>	R3	LVTTL_OUT
RPRTY	T5	LVTTL_OUT
REOP	T2	LVTTL_OUT
RCA	U4	LVTTL_OUT
RSOP/RSOC	T3	LVTTL_OUT
RSX	U5	LVTTL_OUT
RVAL	U1	LVTTL_OUT
RFCLK	V3	LVTTL_IN
RENB	U2	LVTTL_IN
TADD<0>	AE3	LVTTL_IN
TADD<1>	AE4	LVTTL_IN
TADD<2>	AF3	LVTTL_IN
TADD<3>	AG4	LVTTL_IN
TDAT<0>	U3	LVTTL_IN
TDAT<1>	V1	LVTTL_IN
TDAT<10>	Y2	LVTTL_IN
TDAT<11>	Y3	LVTTL_IN
TDAT<12>	Y4	LVTTL_IN
TDAT<13>	Y5	LVTTL_IN
TDAT<14>	AA2	LVTTL_IN
TDAT<15>	AA3	LVTTL_IN
TDAT<16>	AA4	LVTTL_IN
TDAT<17>	AA5	LVTTL_IN
TDAT<18>	AA6	LVTTL_IN
TDAT<19>	AB2	LVTTL_IN
TDAT<2>	V2	LVTTL_IN
TDAT<20>	AB3	LVTTL_IN
TDAT<21>	AB4	LVTTL_IN
TDAT<22>	AB6	LVTTL_IN
TDAT<23>	AC2	LVTTL_IN
TDAT<24>	AC3	LVTTL_IN
TDAT<25>	AC4	LVTTL_IN
TDAT<26>	AC5	LVTTL_IN
TDAT<27>	AC6	LVTTL_IN
TDAT<28>	AD2	LVTTL_IN
TDAT<29>	AD4	LVTTL_IN
TDAT<3>	V4	LVTTL_IN
TDAT<30>	AD5	LVTTL_IN
TDAT<31>	AE2	LVTTL_IN
TDAT<4>	V5	LVTTL_IN
TDAT<5>	W1	LVTTL_IN
TDAT<6>	W2	LVTTL_IN
TDAT<7>	W3	LVTTL_IN

Pin Assignment Table (continued)

Signal	Ball	Pin Type
TDAT<8>	W4	LVTTL_IN
TDAT<9>	W5	LVTTL_IN
TERR	AF5	LVTTL_IN
TENB	AE6	LVTTL_IN
TPRTY	AG5	LVTTL_IN
TSOP	AF6	LVTTL_IN
TEOP	AD7	LVTTL_IN
TSX	AG6	LVTTL_IN
TFCLK	AE7	LVTTL_IN
TMOD<0>	AF7	LVTTL_IN
TMOD<1>	AD8	LVTTL_IN
DTCA<0>	AH6	LVTTL_OUT
DTCA<1>	AE8	LVTTL_OUT
DTCA<2>	AG7	LVTTL_OUT
DTCA<3>	AH7	LVTTL_OUT
STPA	AD9	LVTTL_OUT
PTCA	AG8	LVTTL_OUT
CPUTA_N	AE9	Open Drain Output
CPUCLKFAIL	AH8	LVTTL_OUT
CPUINT	AF9	LVTTL_OUT
CPUAD<0>	AG9	LVTTL_IO
CPUAD<1>	AH9	LVTTL_IO
CPUAD<10>	AJ11	LVTTL_IO
CPUAD<11>	AE12	LVTTL_IO
CPUAD<12>	AF12	LVTTL_IO
CPUAD<13>	AH12	LVTTL_IO
CPUAD<14>	AE13	LVTTL_IO
CPUAD<15>	AF13	LVTTL_IO
CPUAD<16>	AG13	LVTTL_IO
CPUAD<17>	AH13	LVTTL_IO
CPUAD<18>	AJ13	LVTTL_IO
CPUAD<19>	AE14	LVTTL_IO
CPUAD<2>	AE10	LVTTL_IO
CPUAD<20>	AF14	LVTTL_IO
CPUAD<21>	AG14	LVTTL_IO
CPUAD<22>	AE15	LVTTL_IO
CPUAD<23>	AF15	LVTTL_IO
CPUAD<24>	AG15	LVTTL_IO
CPUAD<25>	AH15	LVTTL_IO
CPUAD<26>	AE16	LVTTL_IO
CPUAD<27>	AF16	LVTTL_IO
CPUAD<28>	AH16	LVTTL_IO
CPUAD<29>	AE17	LVTTL_IO
CPUAD<3>	AF10	LVTTL_IO

Pin Assignment Table (continued)

Signal	Ball	Pin Type
CPUAD<30>	AF18	LVTTL_IO
CPUAD<31>	AG18	LVTTL_IO
CPUAD<4>	AG10	LVTTL_IO
CPUAD<5>	AH10	LVTTL_IO
CPUAD<6>	AE11	LVTTL_IO
CPUAD<7>	AF11	LVTTL_IO
CPUAD<8>	AG11	LVTTL_IO
CPUAD<9>	AH11	LVTTL_IO
CPUSEL	AG16	LVTTL_IN
MODE	AE18	LVTTL_IN
CPUTS_N	AJ17	LVTTL_IN
CPUWRD	AG19	LVTTL_IN
CPUBLAST_N	AH17	LVTTL_IN
CHIPSEL	AF19	LVTTL_IN
SCAN_ENA	AG17	LVTTL_IN
POSIC_OEN	AE19	LVTTL_IN
CPUCLK	AF20	LVTTL_IN
RST_N	AH18	LVTTL_IN
TEST<0>	AE20	LVTTL_IN
TEST<1>	AG21	LVTTL_IN
TEST<2>	AH19	LVTTL_IN
TCK	AF21	LVTTL_IN
SYSCLK	AE21	LVTTL_IN
TDI	AG20	LVTTL_IN
TMS	AD21	LVTTL_IN
TRST	AF22	LVTTL_IN
TDO	AD22	LVTTL_OUT
RSTOUT	AG23	LVTTL_OUT
CLKOUT	C16	LVTTL_OUT
TOHSDIN	AE22	LVTTL_IN
POHSDIN	AG22	LVTTL_IN
TE1STROBE	AH24	LVTTL_OUT
TE2STROBE	AF23	LVTTL_OUT
TPOHSTART	AH25	LVTTL_OUT
RPOHSTART	AD23	LVTTL_OUT
CLK2MHz	AF24	LVTTL_OUT
CLK16MHz	AE24	LVTTL_OUT
RE1STROBE	AF25	LVTTL_OUT
RE2STROBE	AG25	LVTTL_OUT
POHSDOUT	AE26	LVTTL_OUT
TOHSDOUT	AG26	LVTTL_OUT
TXFRAME_PULSE	AE27	HSTL/LVTTL_OUT
SONETTx_PAROUT	AD25	HSTL/LVTTL_OUT
TXD<0>	AD28	HSTL/LVTTL_OUT

Pin Assignment Table (continued)

Signal	Ball	Pin Type
TXD<1>	AD27	HSTL/LVTTL_OUT
TXD<10>	AB26	HSTL/LVTTL_OUT
TXD<11>	AB25	HSTL/LVTTL_OUT
TXD<12>	AB24	HSTL/LVTTL_OUT
TXD<13>	AA28	HSTL/LVTTL_OUT
TXD<14>	AA27	HSTL/LVTTL_OUT
TXD<15>	AA26	HSTL/LVTTL_OUT
TXD<16>	AA25	HSTL/LVTTL_OUT
TXD<17>	AA24	HSTL/LVTTL_OUT
TXD<18>	Y29	HSTL/LVTTL_OUT
TXD<19>	Y28	HSTL/LVTTL_OUT
TXD<2>	AD26	HSTL/LVTTL_OUT
TXD<20>	Y27	HSTL/LVTTL_OUT
TXD<21>	W27	HSTL/LVTTL_OUT
TXD<22>	W26	HSTL/LVTTL_OUT
TXD<23>	W25	HSTL/LVTTL_OUT
TXD<24>	V28	HSTL/LVTTL_OUT
TXD<25>	V27	HSTL/LVTTL_OUT
TXD<26>	V26	HSTL/LVTTL_OUT
TXD<27>	V25	HSTL/LVTTL_OUT
TXD<28>	U29	HSTL/LVTTL_OUT
TXD<29>	U28	HSTL/LVTTL_OUT
TXD<3>	AC28	HSTL/LVTTL_OUT
TXD<30>	T28	HSTL/LVTTL_OUT
TXD<31>	T27	HSTL/LVTTL_OUT
TXD<4>	AC27	HSTL/LVTTL_OUT
TXD<5>	AC26	HSTL/LVTTL_OUT
TXD<6>	AC25	HSTL/LVTTL_OUT
TXD<7>	AC24	HSTL/LVTTL_OUT
TXD<8>	AB28	HSTL/LVTTL_OUT
TXD<9>	AB27	HSTL/LVTTL_OUT
TXCLKOUT	W28	HSTL/LVTTL_OUT
TXCLKI	R27	HSTL/LVTTLLVPECL_IN
VREF	U27	0.75V/2.0V INPUT
VREF	P26	0.75V/2.0V INPUT
VREF	M25	0.75V/2.0V INPUT
VREF	G27	0.75V/2.0V INPUT
RXCLK	N28	HSTL/LVTT/LLVPECL_IN
RXCLKS	H26	HSTL/LVTTL/LVPECL_IN
RXD<0>	H27	HSTL/LVTTL/LVPECL_IN
RXD<1>	H28	HSTL/LVTTL/LVPECL_IN
RXD<10>	K29	HSTL/LVTTL/LVPECL_IN
RXD<11>	L25	HSTL/LVTTL/LVPECL_IN
RXD<12>	L26	HSTL/LVTTL/LVPECL_IN

Pin Assignment Table (continued)

Signal	Ball	Pin Type
RXD<13>	L27	HSTL/LVTTL/LVPECL_IN
RXD<14>	L28	HSTL/LVTTL/LVPECL_IN
RXD<15>	M26	HSTL/LVTTL/LVPECL_IN
RXD<16>	M27	HSTL/LVTTL/LVPECL_IN
RXD<17>	M28	HSTL/LVTTL/LVPECL_IN
RXD<18>	N25	HSTL/LVTTL/LVPECL_IN
RXD<19>	N26	HSTL/LVTTL/LVPECL_IN
RXD<2>	J24	HSTL/LVTTL/LVPECL_IN
RXD<20>	N27	HSTL/LVTTL/LVPECL_IN
RXD<21>	N29	HSTL/LVTTL/LVPECL_IN
RXD<22>	P25	HSTL/LVTTL/LVPECL_IN
RXD<23>	P27	HSTL/LVTTL/LVPECL_IN
RXD<24>	P28	HSTL/LVTTL/LVPECL_IN
RXD<25>	R25	HSTL/LVTTL/LVPECL_IN
RXD<26>	R26	HSTL/LVTTL/LVPECL_IN
RXD<27>	R28	HSTL/LVTTL/LVPECL_IN
RXD<28>	T25	HSTL/LVTTL/LVPECL_IN
RXD<29>	T26	HSTL/LVTTL/LVPECL_IN
RXD<3>	J25	HSTL/LVTTL/LVPECL_IN
RXD<30>	U25	HSTL/LVTTL/LVPECL_IN
RXD<31>	U26	HSTL/LVTTL/LVPECL_IN
RXD<4>	J26	HSTL/LVTTL/LVPECL_IN
RXD<5>	J27	HSTL/LVTTL/LVPECL_IN
RXD<6>	J28	HSTL/LVTTL/LVPECL_IN
RXD<7>	K25	HSTL/LVTTL/LVPECL_IN
RXD<8>	K26	HSTL/LVTTL/LVPECL_IN
RXD<9>	K28	HSTL/LVTTL/LVPECL_IN
SONETRx_PARIN	H25	HSTL/LVTTL/LVPECL_IN
LFI_n	H24	LVTTL_IN
RXFRAME_PULSE	F27	HSTL/LVTTL/LVPECL_IN
NC	E27	Do not use
NC	D27	Do not use
NC	D24	Do not use
NC	C24	Do not use
NC	B24	Do not use
NC	F23	Do not use
NC	D23	Do not use
NC	C23	Do not use
NC	B23	Do not use
NC	F22	Do not use
NC	E22	Do not use
NC	C22	Do not use
NC	G26	Do not use
NC	F21	Do not use

Pin Assignment Table (continued)

Signal	Ball	Pin Type
NC	E21	Do not use
NC	D21	Do not use
NC	C21	Do not use
NC	B21	Do not use
NC	E20	Do not use
NC	C20	Do not use
NC	B20	Do not use
NC	E19	Do not use
NC	B19	Do not use
NC	F26	Do not use
NC	B18	Do not use
NC	A18	Do not use
NC	E26	Do not use
NC	F25	Do not use
NC	D25	Do not use
NC	C25	Do not use
NC	G24	Do not use
NC	E24	Do not use
NC	B17	Do not use
NC	D19	Do not use
NC	A17	Do not use
NC	B16	Do not use
NC	D18	Do not use
NC	C15	Do not use
NC	D17	Do not use
NC	C17	Do not use
NC	D13	Do not use
NC	C13	Do not use
NC	A13	Do not use
NC	D12	Do not use
NC	C12	Do not use
NC	B12	Do not use
NC	A12	Do not use
NC	C11	Do not use
NC	B11	Do not use
NC	E16	Do not use
NC	D16	Do not use
NC	E15	Do not use
NC	D15	Do not use
NC	E14	Do not use
NC	C14	Do not use
NC	B14	Do not use
NC	E13	Do not use
NC	E12	Do not use

Pin Assignment Table (continued)

Signal	Ball	Pin Type
NC	E11	Do not use
NC	C9	Do not use
NC	B9	Do not use
NC	F8	Do not use
NC	E8	Do not use
NC	C8	Do not use
NC	B8	Do not use
NC	F7	Do not use
NC	E7	Do not use
NC	D7	Do not use
NC	C7	Do not use
NC	D11	Do not use
NC	B7	Do not use
NC	E6	Do not use
NC	D6	Do not use
NC	C6	Do not use
NC	F5	Do not use
NC	D5	Do not use
NC	C5	Do not use
NC	F4	Do not use
NC	C4	Do not use
NC	E3	Do not use
NC	E10	Do not use
NC	E2	Do not use
NC	D2	Do not use
NC	D10	Do not use
NC	C10	Do not use
NC	B10	Do not use
NC	F9	Do not use
NC	E9	Do not use
NC	D9	Do not use
VSS1	A1, B1, AE1, AJ1, AJ2, AG12, A2, D3, AD3, AH4, AJ4, A4, AH5, AH14, C18, AJ18, AJ19, AH20, AH21, B22, AH23, AG24, B25, AH26, B27, K27, AJ28, AF28, A28, D28, F28, A29, B29, J29, M29, P29, AJ29	Core + Input Pin GND
VSS2	G1, J1, P1, T1, AA1, AC1, B2, C3, AJ3, E4, G4, A6, B6, AJ7, AF8, A9, AJ9, A11, AJ12, B13, AJ14, A16, AJ16, E17, C19, A20, AJ21, AJ22, A23, AE23, AJ23, A25, A27, AF27, AJ27, AH28, C29, D29, F29, R29, W29, AC29, AE29, AF29, AH29, Y25	Output Pin GND
V_{CC1}	D1, AF1, AG2, C2, B3, AH3, D4, AF4, B5, E5, AJ5, D20, D22, E25, A26, C26, D26, AF26, AJ26, AH27, AE28, E29, G29, H29, L29	Core Voltage, 1.8V
V_{CC2}	AD1, AG1, AH1, AF2, AH2, AG3, B4, AB5, AE5, A7, A10, A14, AF17, A21, A22, AH22, C28, E28, G28	LVTTL Input Pin Power Supply, 3.3V

Pin Assignment Table (continued)

Signal	Ball	Pin Type
V_{CC3}	C1, E1, F1, H1, K1, R1, Y1, AB1, A3, H3, A5, AJ6, A8, D8, AJ8, AJ10, D14, A15, B15, AJ15, E18, A19, AJ20, E23, A24, AJ24, G25, AJ25, B26, C27, AG27, B28, AG29	LVTTL Output Pin Power Supply, 3.3V
V_{CC5}	AE25, AG28, T29, V29, AA29, AB29, AD29, Y26	HSTL Output Pin Power Supply, 1.5V/3.3V

Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)

Operating range specifies temperature and voltage boundary conditions for safe operation of the device. Operation outside these boundary may affect the performance and life of the device.

Table 2. Absolute Maximum Ratings

Parameter	Value	Unit
Case Temperature	–40 to 85	°C
Storage Temperature	150	°C
Absolute Maximum Junction Temperature	125	°C
Lead Temperature	220	°C
Supply Voltage V_{CC1} for Core	2.43	V
Supply Voltage V_{CC2} for LVTTL Inputs	4.785	V
Supply Voltage V_{CC3} for LVTTL Outputs	4.785	V
Supply Voltage V_{CC5} for HSTL/LVTTL Outputs	4.785	V
V_{REF}	V_{CC} + 0.3	V
All Inputs Values	V_{CC} + 0.3	V
Static Discharge Voltage (ESD)	>2000	V
Latch-up Current	>200	mA
Maximum output short circuit current for all I/O configurations (V_{OUT} = 0V)[17]	–100	mA

Operating Range

Table 3. Operating Range

Range	Ambient Temperature	V_{CC1}	V_{CC5}(HSTL)	V_{CC2}, V_{CC3}, V_{CC5}
Commercial	0°C to +70°C	1.71V to 1.89V	1.425V to 1.575V	3.135V to 3.465V
Industrial	–40°C to +85°C	1.71V to 1.89V	1.425V to 1.575V	3.135V to 3.465V

DC Specifications

Table 4. DC Specifications

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{CC1}	Power Supply for Core		1.71	1.89	V
V_{CC2}	Power Supply for LVTTL Inputs		3.135	3.465	V
V_{CC3}	Power Supply for LVTTL Outputs		3.135	3.465	V
V_{CC5}	Power Supply for HSTL/LVTTL Outputs		1.425/3.135	1.575/3.465	V
$V_{REF(HSTL)}$	Reference Voltage for HSTL Inputs		0.68	0.9	V
$V_{REF(LVPECL)}$	Reference Voltage for LVPECL Inputs		V_{CC2} – 1.4	V_{CC2} – 1.2	V
I_{CC1}	V_{CC1} Supply Current		–	1	A
I_{CC2}	V_{CC2} Supply Current		–	0.1	A
I_{CC3}	V_{CC3} Supply Current	20-pF capacitive load	–	0.75	A
I_{CC5}	V_{CC5} Supply Current	20-pF capacitive load	–	0.28	A
PW	Total Chip Power	20 pF capacitive load	–	4.57	Watt
I_{OS}[17]	Output Short Circuit Current for all I/O configurations	V_{OUT} = 0V	–20	–100	mA

Note:
17. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. Tested initially and after any design or process changes that may affect these parameters.

Table 4. DC Specifications (continued)

Parameter	Description	Test Conditions	Min.	Max.	Unit
LVTTL I/Os					
V_{OHT}	Output HIGH Voltage	All V_{CC} = Min. I_{OH} = –8.0 mA	2.4	–	V
V_{OLT}	Output LOW Voltage	All V_{CC} = Min. I_{OL} = 8.0 mA	–	0.4	V
V_{IHT}	Input HIGH Voltage		2.0	V_{CC2} + 0.3	V
V_{ILT}	Input LOW Voltage		–0.3	0.8	V
I_{IHT}	Input HIGH Current	All V_{CC} = Max., V_{IN} = V_{CC2}	–	10	µA
I_{ILT}	Input LOW Current	All V_{CC} = Max., V_{IN} = 0V	–	–10	µA
HSTL I/Os					
V_{REF}	Reference Voltage		0.68	0.9	
$V_{OH(DC)}$	Output HIGH Voltage	All V_{CC} = Min. I_{OH} = –8.0 mA	V_{CC5} – 0.4	–	V
$V_{OL(DC)}$	Output LOW Voltage	All V_{CC} = Min. I_{OL} = 8.0 mA	–	0.4	V
$V_{OH(AC)}$	Output HIGH Voltage		V_{CC5} – 0.5		V
$V_{OL(AC)}$	Output LOW Voltage		–	0.5	V
$V_{IH(DC)}$	Input HIGH Voltage		V_{REF} + 0.1	–	V
$V_{IL(DC)}$	Input LOW Voltage		–	V_{REF} – 0.1	V
$V_{IH(AC)}$	Input HIGH Voltage	V_{CC1} = 1.71V	V_{REF} + 0.2		V
$V_{IL(AC)}$	Input LOW Voltage	V_{CC1} = 1.89V	–	V_{REF} – 0.2	V
I_{IHH}	Input HIGH Current	All V_{CC}= Max. V_{IN} = V_{CC1}	–	10	µA
I_{ILH}	Input LOW Current	All V_{CC}= Max. V_{IN} = 0V	–	–10	µA
LVPECL Inputs					
V_{REF}	Reference Voltage		V_{CC2} – 1.4	V_{CC2} – 1.2	V
$V_{IH(DC)}$	Input HIGH Voltage		V_{CC2} – 1.1	–	V
$V_{IL(DC)}$	Input LOW Voltage		–	V_{CC2} – 1.5	V
$V_{IH(AC)}$	Input HIGH Voltage		V_{CC2} – 1.0		V
$V_{IL(AC)}$	Input LOW Voltage		–	V_{CC2} – 1.6	V
I_{IHH}	Input HIGH Current	All V_{CC}= Max. V_{IN} = V_{CC2}	–	10	µA
I_{ILH}	Input LOW Current	All V_{CC}= Max. V_{IN} = 0V	–	–10	µA

Reset Requirements

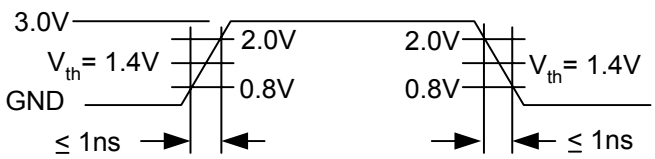
Asserting the RST_n signal will asynchronously reset all sequential elements of POSIC2G. Even though the reset is treated as asynchronous signal, it is recommended that a minimum of 1-ms-wide active LOW RST_n is applied after all power supplies have stabilized.

Power-up Requirements

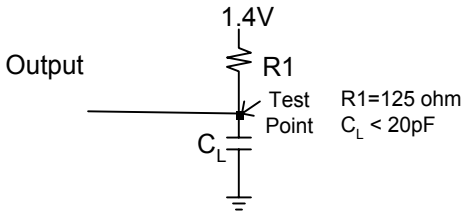
When HSTL I/O is used, V_{CC1}, V_{CC2}, and V_{CC3} need to be powered up first at least 300 ms before V_{CC5} supply. There is no particular power-up sequence requirements among V_{CC1}, V_{CC2}, and V_{CC3} in this case.

There is no particular power-up sequence requirements among V_{CC1}, V_{CC2}, V_{CC3}, and V_{CC5} if HSTL I/O is not used. RST_n needs to be activated until all the power supplies have stabilized.

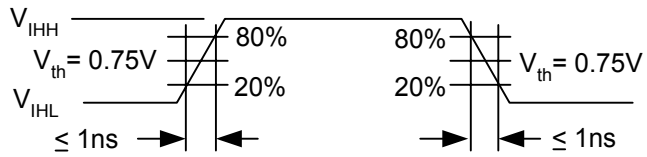
AC Test Loads and Waveform



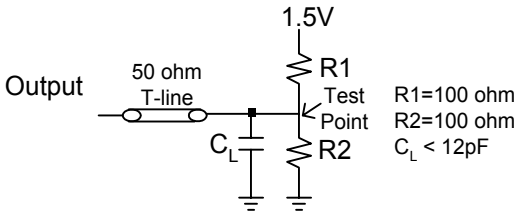
(a) LvTTL Input Test Waveform



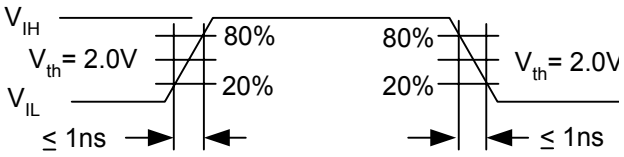
(a) LVTTL AC Test Load



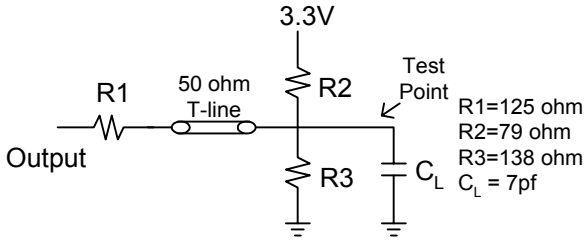
(b) HSTL Input Test Waveform



(b) HSTL AC Test Load



(c) LVPECL Input Test Waveform



(c) LVPECL-compliant Termination

AC and Timing Specifications

The POSIC2G device interfaces to industry standard peripheral devices or buses. Hence the POSIC2G pin timing parameters are governed by the interface requirements of the peripherals or the relevant standards. *Table 5* details the timing requirements.

Table 5. POSIC2G Pin Timing Requirements

POSIC2G Pin Group	Peripheral Device/ Bus Standard	Compatible/ Suggested Part Number	Reference/Remarks
Line Interface	16 bits/8 bits HSTL/Single-ended LVPECL interface	CYS25G0101DX	Refer to PHY data sheet
Overhead Bytes Access – Serial Ports	LVTTL	–	Described in this document
System Interface	UTOPIA Level 3 / OIF-SPI Level3 HBST	–	ATM Forum: BTD-PHY-UL3-01.05 Saturn Group: PMC-980495 Issue Described in this document
Host CPU Interface	16-/32-bit CPU Interface LVTTL	Compatible to Intel/Motorola CPUs	

AC Specifications

Table 6. Line Interface Timing Parameter Values

Parameter	Description	Min.	Max.	Unit
f_{TS}[18]	TXCLKOUT, TXCLKI Frequency (must be frequency coherent to RXCLK when used as the transmit PLL clock source). f_{TS} nominal (f_{TSN}) can be 155.52 MHz, 77.76 MHz, 38.88 MHz, 19.44 MHz—depends on the Bus Width and Line Rate used.	f_{TSN} * (1 – 0.65%)	f_{TSN} * (1 + 0.65%)	MHz
$t_{TXCLKIP}$[18]	TXCLKI Period	1/(f_{TS} max.)	1/(f_{TS} min.)	ns
$t_{TXCLKID}$	TXCLKI Duty Cycle	43	57	%
t_{TXCLKP}[18]	TXCLKOUT Period	1/(f_{TS} max.)	1/(f_{TS} min.)	ns
t_{TXCLKD}[18]	TXCLKOUT Duty Cycle	40	60	%
t_{TXCLKR}[19]	TXCLKOUT Rise Time	0.3	1.5	ns
t_{TXCLKF}[19]	TXCLKOUT Fall Time	0.3	1.5	ns
t_{TXDO}	TXD Output Delay after ↑ of TXCLKOUT	0.5	4.5	ns
t_{TXFPO}	TXFRAME_PULSE Output Delay after ↑ of TXCLKOUT	0.5	4.5	ns
$t_{PAROUTO}$	SONETTX_PAROUT Output Delay after ↑ of TXCLKOUT	0.5	4.5	ns
t_{TXFPPW}	TXFRAME_PULSE Width	6	55	ns
f_{RS}[18]	RXCLK Frequency. f_{RS} nominal (f_{RS}N) can be 155.52 MHz, 77.76 MHz, 38.88 MHz, 19.44 MHz depends on the Bus Width and Line Rate used	f_{RSN} * (1 – 0.65%)	f_{RSN} * (1 + 0.65%)	MHz
t_{RXCLKP}[18]	RXCLK Period	1/(f_{RS} max.)	1/(f_{RS} min.)	ns
$t_{RXCLKOD}$[18]	RXCLK Duty Cycle	43	57	%
t_{RXCLKR}[19]	RXCLK Rise Time	–	1.5	ns
t_{RXCLKF}[19]	RXCLK Fall Time	–	1.5	ns
t_{RXDS}	Recovered Data Set-up to ↑ of RXCLK	1.5	–	ns
t_{RXDH}	Recovered Data Hold from ↑ of RXCLK	1.25	–	ns
t_{RXFPS}	RXFRAME_PULSE Set-up to ↑ of RXCLK	1.5	–	ns
t_{RXFPH}	RXFRAME_PULSE Hold from ↑ of RXCLK	1.25	–	ns
t_{PARINS}	SONETRX_PARIN Set-up to ↑ of RXCLK	1.5	–	ns
t_{PARINH}	SONETRX_PARIN Hold from ↑ of RXCLK	1.25	–	ns

Table 7. OIF-SPI Level 3 Transmit System Interface Timing Parameter Values

Parameter	Description	Min.	Max.	Unit
f_{TFCLK}[18]	TFCLK Frequency	-	104	MHz
t_{TFCLKD}[18]	TFCLK Duty Cycle	40	60	%
t_{TENBS}	TENB Set-up time to TFCLK[20]	2	–	ns
t_{TENBH}	TENB Hold time to TFCLK[21]	0.5	–	ns
t_{TDATS}	TDAT[31:0] Set-up time to TFCLK[20]	2	–	ns
t_{TDATH}	TDAT[31:0] Hold time to TFCLK[21]	0.5	–	ns
t_{TPRTYS}	TPRTY Set-up time to TFCLK[20]	2	–	ns
t_{TPRTYH}	TPRTY Hold time to TFCLK[21]	0.5	–	ns
t_{TSOPS}	TSOP Set-up time to TFCLK[20]	2	–	ns
t_{TSOPH}	TSOP Hold time to TFCLK[21]	0.5	–	ns

Notes:
18. The parameter is guaranteed by design and is not tested during production.
19. The parameter is guaranteed by characterization and is not tested during production.
20. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4V point of the input to the 1.4V point of the clock.
21. When a hold time is specified between an input and a clock, the hold time is the time in the nanoseconds from the 1.4V point of the clock to the 1.4V point of the input.

Table 7. OIF-SPI Level 3 Transmit System Interface Timing Parameter Values (continued)

Parameter	Description	Min.	Max.	Unit
t_{TEOPS}	TEOP Set-up time to TFCLK[20]	2	–	ns
t_{TEOPH}	TEOP Hold time to TFCLK[21]	0.5	–	ns
t_{TERRS}	TERR Set-up time to TFCLK[20]	2	–	ns
t_{TERRH}	TERR Hold time to TFCLK[21]	0.5	–	ns
t_{TSXS}	TSX Set-up time to TFCLK[20]	2	–	ns
t_{TSXH}	TSX Hold time to TFCLK[21]	0.5	–	ns
t_{TMODS}	TMOD Set-up time to TFCLK[20]	2	–	ns
t_{TMODH}	TMOD Hold time to TFCLK[21]	0.5	–	ns
t_{PTADRS}	PTADR Set-up time to TFCLK[20]	2	–	ns
t_{PTADRH}	PTADR Hold time to TFCLK[21]	0.5	–	ns
t_{DTPAO}	TFCLK HIGH to DTPA Valid[22, 23]	1.5	6	ns
t_{STPAO}	TFCLK HIGH to STPA Valid[22, 23]	1.5	6	ns
t_{PTCAO}	TFCLK HIGH to PTCA Valid[22, 23]	1.5	6	ns

Table 8. OIF-SPI Level 3 Receive System Interface Timing Parameter Values

Parameter	Description	Min.	Max.	Unit
f_{RFCLK}[18]	RFCLK Frequency	–	104	MHz
t_{RFCLKD}[18]	RFCLK Duty Cycle	40	60	%
t_{RENBS}	RENB Set-up time to RFCLK[20]	2	–	ns
t_{RENBH}	RENB Hold time to RFCLK [21]	0.5	–	ns
t_{RDATD}	RFCLK HIGH to RDAT[31:0] Valid [22, 23]	1.5	6	ns
t_{RPRTYD}	RFCLK HIGH to RPRTY Valid[22, 23]	1.5	6	ns
t_{RSOPD}	RFCLK HIGH to RSOP Valid[22, 23]	1.5	6	ns
t_{REOPD}	RFCLK HIGH to REOP Valid[22, 23]	1.5	6	ns
t_{RERRD}	RFCLK HIGH to RERR Valid[22, 23]	1.2	6	ns
t_{RMODD}	RFCLK HIGH to RMOD[1:0] Valid[22, 23]	1.5	6	ns
t_{RSXD}	RFCLK HIGH to RSX Valid[22, 23]	1.5	6	ns

Table 9. UTOPIA Level 3 Receive System Interface Timing Parameter Values

Parameter	Description	Min.	Max.	Unit
f_{RxClk}[18]	RxClk Frequency	–	104	MHz
t_{RxClkD}[18]	RxClk Duty Cycle	40	60	%
t_{RxEnbS}	RxEnb Set-up Time to RxClk	2	–	ns
t_{RxEnbH}	RxEnb Hold Time to RxClk	0.5	–	ns
$t_{RxDataO}$	RxClk HIGH to RxData [31:0] Valid	–	6	ns
t_{RxSocO}	RxClk HIGH to RxSoc Valid	–	6	ns
$t_{RxPrtyO}$	RxClk HIGH to RxPrty Valid	–	6	ns
$t_{PxClavO}$	RxClk HIGH to RxClav Valid	–	6	ns

Notes:
22. Output propagation delay time is in nanoseconds from the 1.4V point of the reference signal to the 1.4V point of the output.
23. Maximum output propagation delays are measured with 30-pF load on the inputs.

Table 10.UTOPIA Level 3 Transmit System Interface Timing Parameter Values

Parameter	Description	Min.	Max.	Unit
f_{TxClk}[18]	TxClk Frequency	–	104	MHz
t_{TxClkD}[18]	TxClk Duty Cycle	40	60	%
t_{TxEnbS}	TxEnb Set-up Time to TxClk	2	–	ns
t_{TxEnbH}	TxEnb Hold Time to TxClk	0.5	–	ns
$t_{TxAddrS}$	TxAddr Set-up Time to TxClk	2	–	ns
$t_{TxxAddrH}$	TxAddr Hold Time to TxClk	0.5	–	ns
$t_{TxDataS}$	TxData [31:0] Set-up Time to TfClk	2	–	ns
$t_{TxDataH}$	TxData [31:0] Hold Time to TfClk	0.5	–	ns
$t_{TxPrtyS}$	TxPrty Set-up Time to TfClk	2	–	ns
$t_{TxPrtyH}$	TxPrty Hold Time to TfClk	0.5	–	ns
t_{TxSocS}	TxSoc Set-up Time to TfClk	2	–	ns
t_{TxSocH}	TxSoc Hold Time to TfClk	0.5	–	ns
t_{PTCAO}	TfClk HIGH to PTCA Valid	–	6	ns

Table 11.HBST Transmit System Interface Timing Parameter Values

Parameter	Description	Min.	Max.	Unit
f_{TCLK}[18]	TCLK Frequency		104	MHz
t_{TCLKD}[18]	TCLK Duty Cycle	40	60	%
t_{TADDRS}	TADDR[3:0] Set-up Time to TCLK	2	–	ns
t_{TADDRH}	TADDR[3:0] Hold Time to TCLK	0.5	–	ns
t_{TDATAS}	TDATA [31:0] Set-up Time to TCLK	2	–	ns
t_{TDATAH}	TDATA [31:0] Hold Time to TCLK	0.5	–	ns
$t_{TPARITYS}$	TPARITY Set-up Time to TCLK	2	–	ns
$t_{TPARITYH}$	TPARITY Hold Time to TCLK	0.5	–	ns
t_{TBVALS}	TBVAL[2:0] Set-up Time to TCLK	2	–	ns
t_{TBVALH}	TBVAL[2:0] Hold Time to TCLK	0.5	–	ns
t_{TDVALS}	TDVAL_n Set-up Time to TCLK	2	–	ns
t_{TDVALH}	TDVAL_n Hold Time to TCLK	0.5	–	ns
t_{TSOPS}	TSOP Set-up Time to TCLK	2	–	ns
t_{TSOPH}	TSOP Hold Time to TCLK	0.5	–	ns
t_{TEOPS}	TEOP Set-up Time to TCLK	2	–	ns
t_{TEOPH}	TEOP Hold Time to TCLK	0.5	–	ns
t_{TERRS}	TERR Set-up Time to TCLK	2	–	ns
t_{TERRH}	TERR Hold Time to TCLK	0.5	–	ns
t_{TSTFAO}	TCLK HIGH to TSTFA Valid	1.5	6	ns
$t_{TSOFSTO}$	TCLK HIGH to TSOFST Valid	1.5	6	ns
t_{TFASTO}	TCLK HIGH to TFAST[3:0] Valid	1.5	6	ns

Table 12.HBST Receive System Interface Timing Parameter Values

Parameter	Description	Min.	Max.	Unit
f_{RCLK}[18]	RCLK Frequency	–	104	MHz
t_{RCLKD}[18]	RCLK Duty Cycle	40	60	%
$t_{RREADYS}$	RREADY_n Set-up Time to RCLK	2	–	ns
$t_{RREADYD}$	RREADY_n Hold Time to RCLK	0.5	–	ns
t_{RDATAO}	RCLK HIGH to RDATA[31:0] Valid	1.5	6	ns
t_{RADDRO}	RCLK HIGH to RADDR[7:0] Valid	1.5	6	ns
$t_{RPARITYO}$	RCLK HIGH to RPARITY Valid	1.5	6	ns
t_{RSOPO}	RCLK HIGH to RSOP Valid	1.5	6	ns
t_{REOPO}	RCLK HIGH to REOP Valid	1.5	6	ns
t_{RERRO}	RCLK HIGH to RERR Valid	1.2	6	ns
t_{RBVALO}	RCLK HIGH to RBVAL[2:0] Valid	1.5	6	ns
t_{RDVALO}	RCLK HIGH to RDVAL Valid	1.5	6	ns
t_{RSTFAO}	RCLK HIGH to RSTFA Valid	1.5	6	ns

Table 13.CPU System Interface Timing Parameter Values

Parameter	Description	Min.	Max.	Unit
f_{SYSCLK}[18]	SYSCLK Frequency	133	133.33	MHz
$t_{SYSCLKD}$[18]	SYSCLK Duty Cycle	45	55	%
f_{CpuClk}[18]	CpuClk Freq.	–	66	MHz
$t_{CpuAdsS}$	CpuAds_n Set-up Time to CpuClk	7	–	ns
$t_{CpuAdsH}$	CpuAds_n Hold Time to CpuClk	2	–	ns
t_{CpuADS}	CpuAD Set-up Time to CpuClk	7	–	ns
t_{CpuADH}	CpuAD Hold Time to CpuClk	2	–	ns
t_{CpuADZ}[18]	CpuAD Float	-	14	ns
t_{CpuADO}	CpuAD Output Delay after CpuClk Rise	-	10.1	ns
$t_{CpuWrRdS}$	CpuWrRd Set-up Time to CpuClk	7	–	ns
$t_{CpuWrRdH}$	CpuWrRd Hold Time to CpuClk	2	–	ns
t_{CpuTaO}	CpuTa_n Valid Delay	–	10.1	ns
$t_{CpuBlastS}$	CpuBlast_n Set-up to CpuClk	7	–	ns
$t_{CpuBlastH}$	CpuBlast_n Hold to CpuClk	2	–	ns
$t_{CpuSelS}$	CpuSel Set-up to CpuClk	7	–	ns
$t_{CpuSelH}$	CpuSel Hold to CpuClk	2	–	ns
$t_{CpuIntO}$	CpuInt Valid Delay	–	10.1	ns

Table 14.TOH Serial Interface Receive Timing Parameter Values

Parameter	Description	Min.	Max.	Unit
$t_{Clk2MHzH}$[18]	Clk2MHz High Period	31	34	SYSCLK cycles
$t_{Clk2MHzL}$[18]	Clk2MHz Low Period	31	34	SYSCLK cycles
$t_{Clk2MHzR}$[19]	Clk2MHz Rise Time	–	6	ns
$t_{Clk2MHzF}$[19]	Clk2MHz Fall Time	–	6	ns
t_{REPW}	RE1STROBE or RE2STROBE Pulse Width	62	67	SYSCLK cycles
t_{REO}	RE1STROBE or RE2STROBE Output Delay after Clk2MHZ Rising Edge	–	8	ns
$t_{TOHSDOUTO}$	TOHSDOUT Output Delay after Clk2MHZ Rising Edge	–	8	ns

Table 15.POH Serial Interface Receive Timing Parameter Values

Parameter	Description	Min.	Max.	Unit
$t_{Clk16MHzH}$[18]	Clk16MHz High Period	3	5	SYSCLK cycles
$t_{Clk16MHzL}$[18]	Clk16MHz Low Period	3	5	SYSCLK cycles
$t_{Clk16MHzR}$[19]	Clk16MHz Rise Time	–	6	ns
$t_{Clk16MHzF}$[19]	Clk16MHz Fall Time	–	6	ns
t_{RPOHPW}[19]	RPOHSTART Pulse Width	7	9	SYSCLK cycles
t_{RPOHO}	RPOHSTART Output Delay after Clk16MHZ Rising Edge	–	8	ns
$t_{POHSDOUTO}$	POHSDOUT Output Delay after Clk16MHZ Rising Edge	–	8	ns

Table 16.TOH Serial Interface Transmit Timing Parameter Values

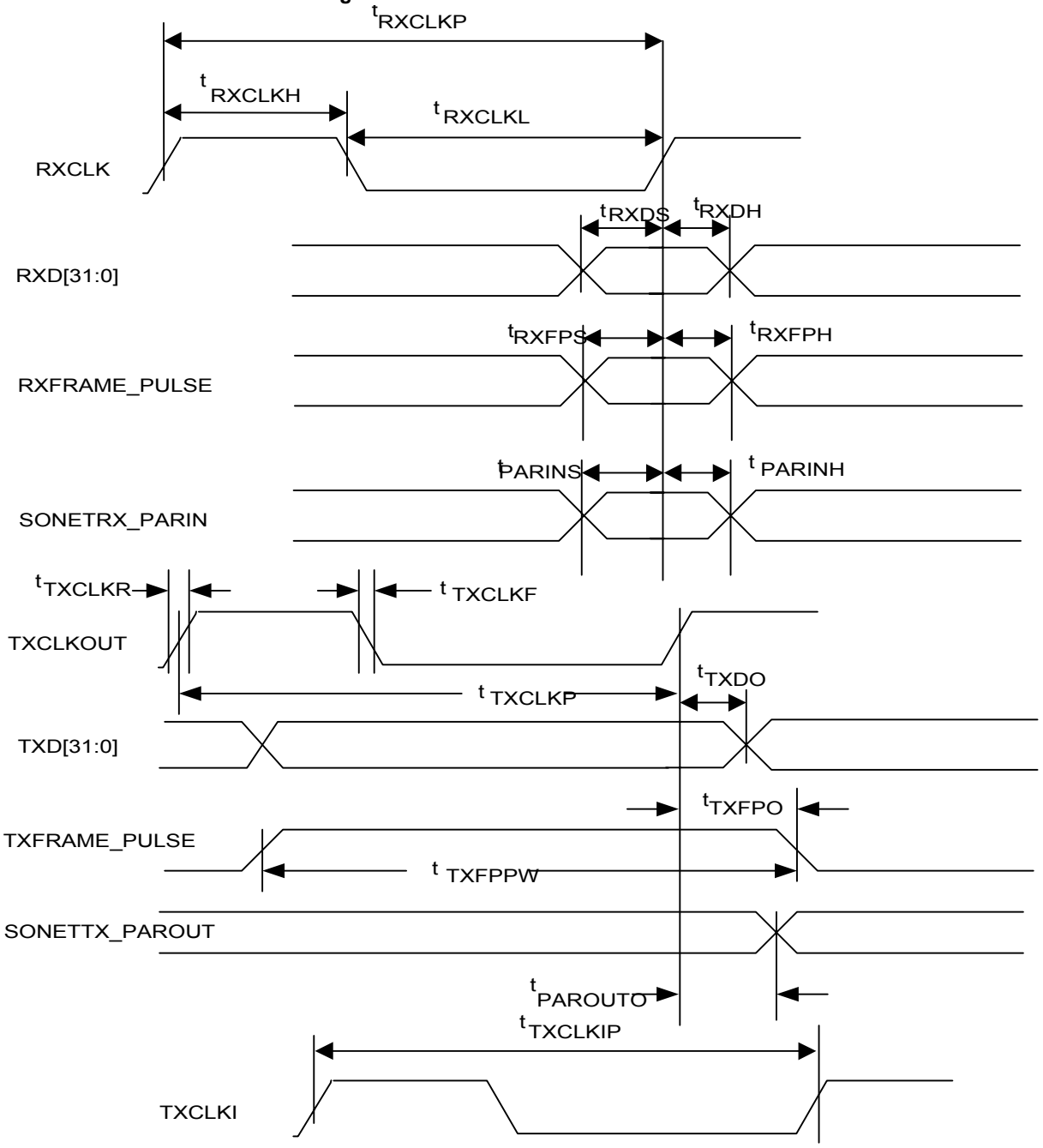
Parameter	Description	Min.	Max.	Unit
$t_{Clk2MHzH}$[18]	Clk2MHz High Period	31	34	SYSCLK cycles
$t_{Clk2MHzL}$[18]	Clk2MHz Low Period	31	34	SYSCLK cycles
$t_{Clk2MHzR}$[19]	Clk2MHz Rise Time	–	6	ns
$t_{Clk2MHzF}$[19]	Clk2MHz Fall Time	–	6	ns
t_{TEPW}[19]	TE1STROBE or TE2STROBE Pulse Width	62	67	SYSCLK cycles
t_{TEO}	TE1STROBE or TE2STROBE Output Delay after Clk2MHz Rising Edge	–	8	ns
$t_{TOHSDINS}$	Set-up Time of TOHSDIN before the Falling Edge of Clk2 MHz	50	–	ns
$t_{TOHSDINH}$	Hold Time of TOHSDIN after the Falling Edge of Clk2 MHz	50	–	ns

Table 17.POH Serial Interface Transmit Timing

Parameter	Description	Min.	Max.	Unit
$t_{Clk16MHzH}$[18]	Clk16MHz High Period	3	5	SYSCLK cycles
$t_{Clk16MHzL}$[18]	Clk16MHz Low Period	3	5	SYSCLK cycles
$t_{Clk16MHzR}$[19]	Clk16MHz Rise Time	–	6	ns
$t_{Clk16MHzF}$[19]	Clk16MHz Fall Time	–	6	ns
t_{TPOHPW}[19]	TPOHSTART Pulse Width	7	9	SYSCLK cycles
t_{TPOHO}	TPOHSTART Output Delay after Rising Edge of Clk16MHz	–	8	ns
$t_{POHSDINS}$	Set-up Time of POHSDIN before Falling Edge of Clk16MHz	20	–	ns
$t_{POHSDINH}$	Hold Time of POHSDIN after Falling Edge of Clk16MHz	20	–	ns

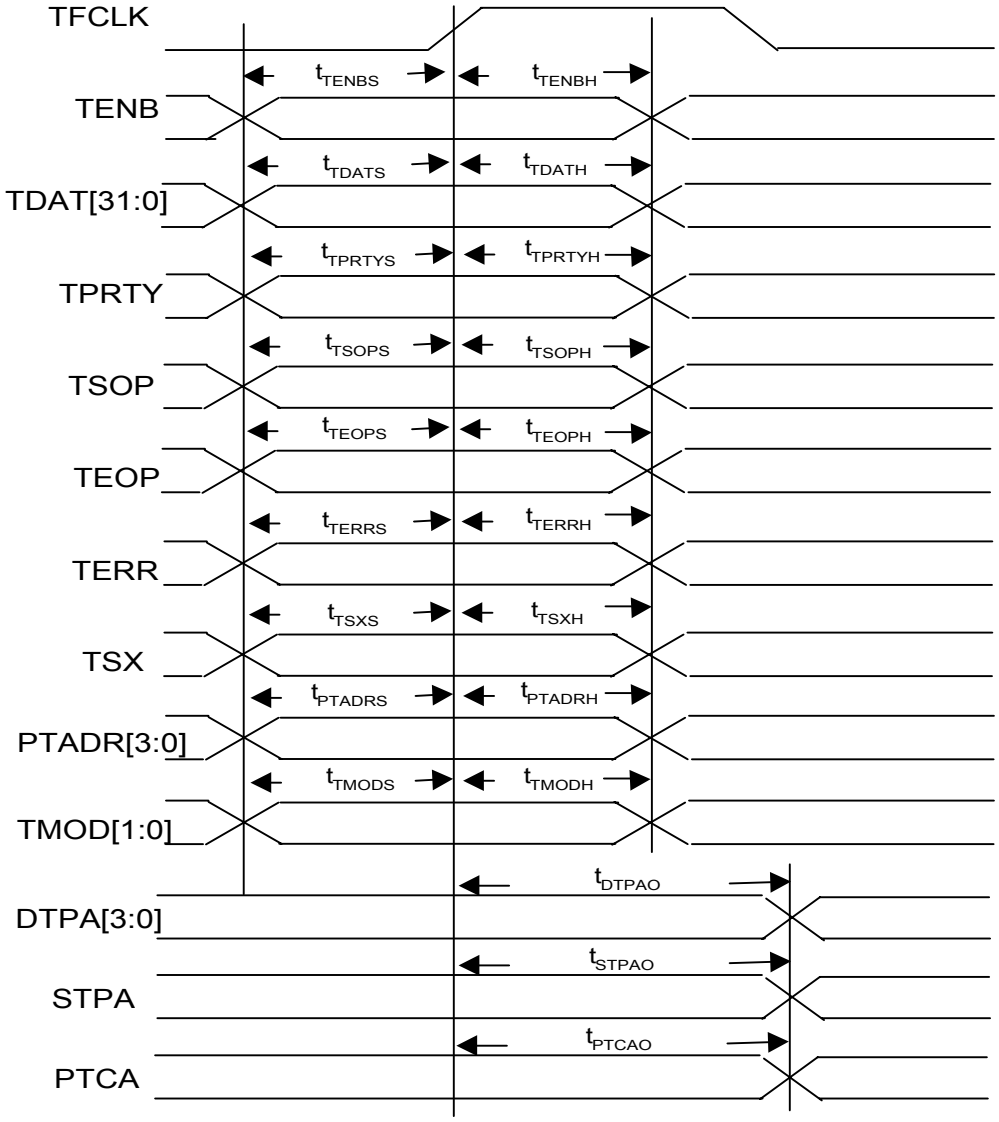
Switching Waveforms

Line Transmit and Receive Interface Timing



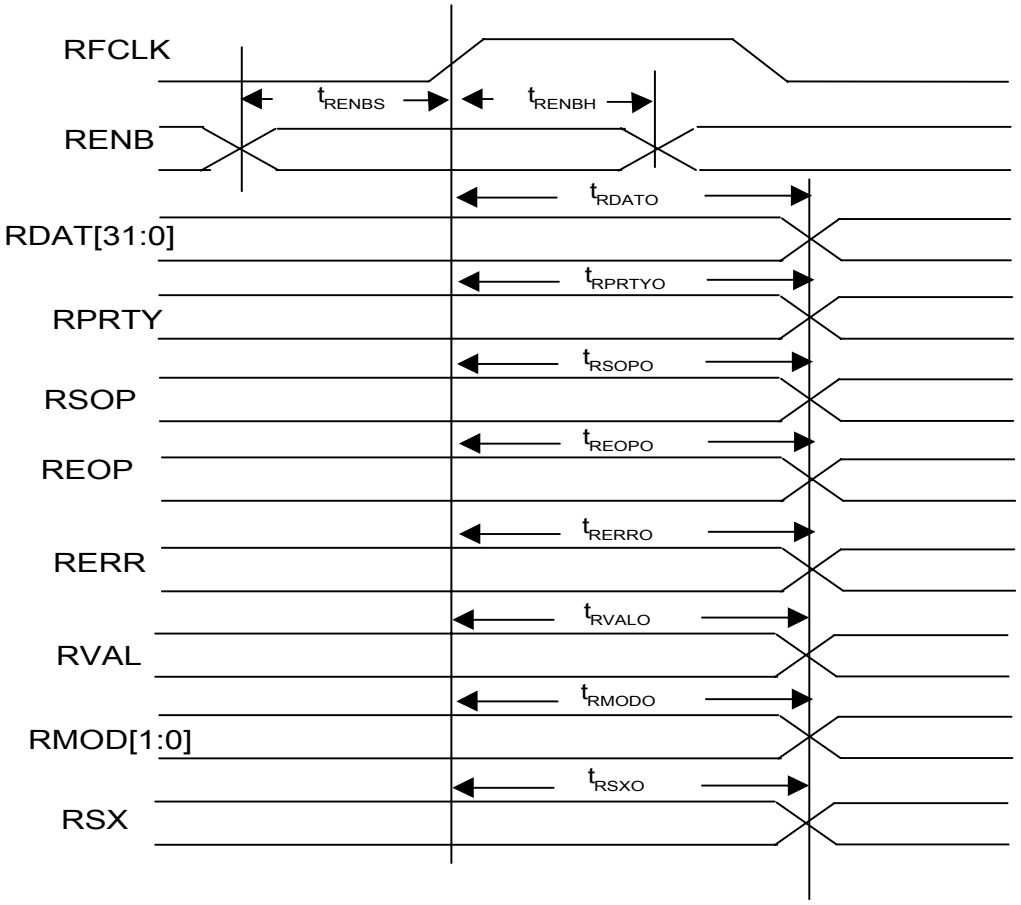
Switching Waveforms (continued)

Transmit OIF-SPI Level 3 System Interface Timing

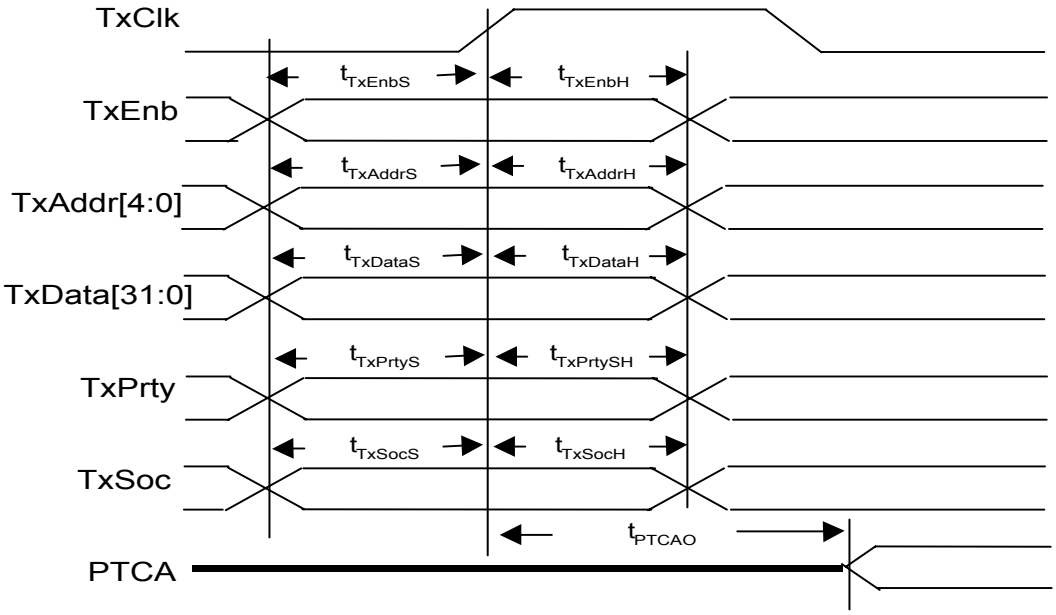


Switching Waveforms (continued)

Receive OIF-SPI Level 3 System Interface Timing

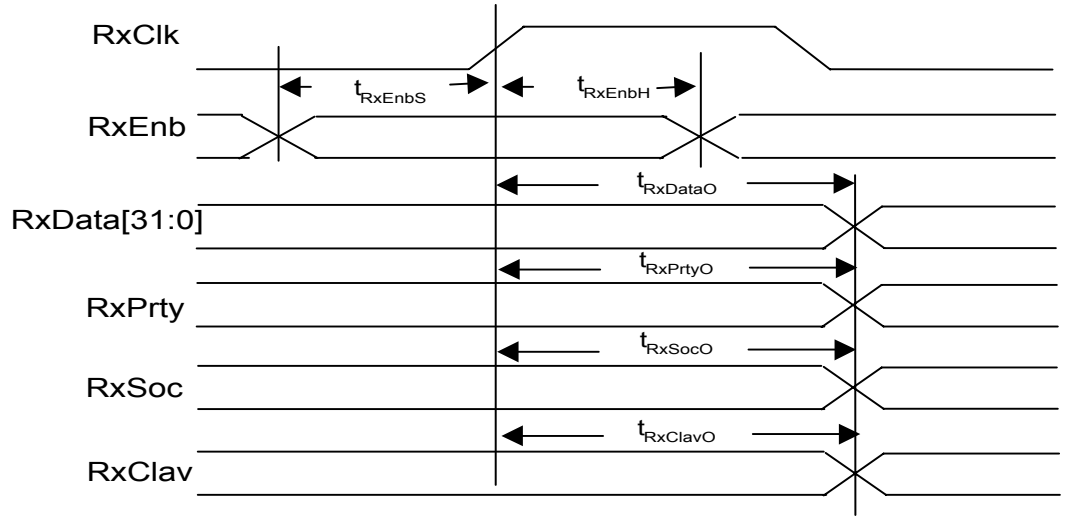


Transmit UTOPIA Level 3 System Interface Timing

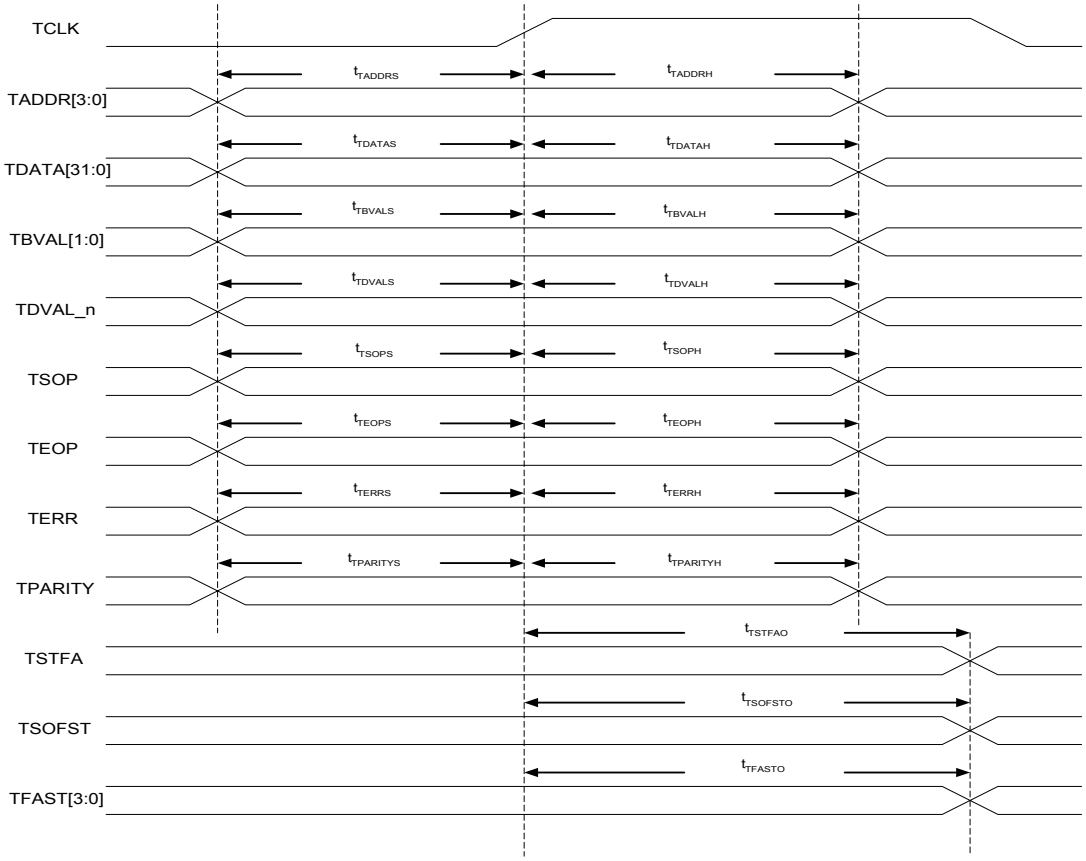


Switching Waveforms (continued)

Receive UTOPIA Level 3 System Interface Timing

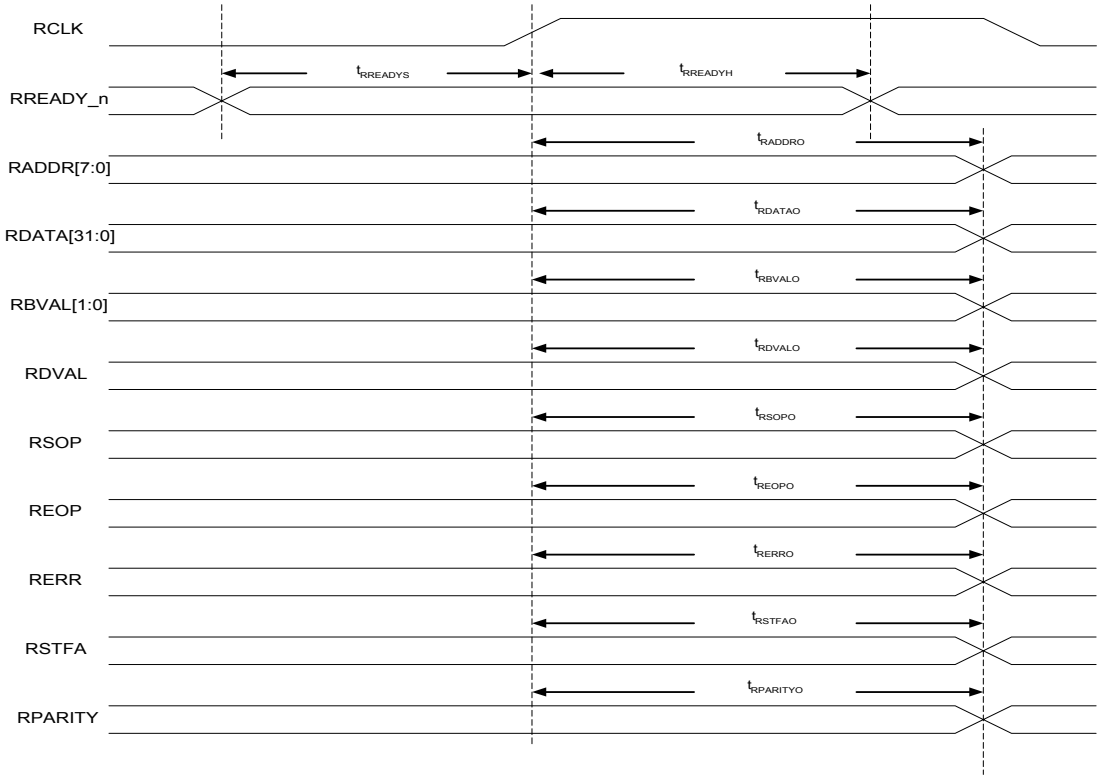


Transmit HBST System Interface Timing



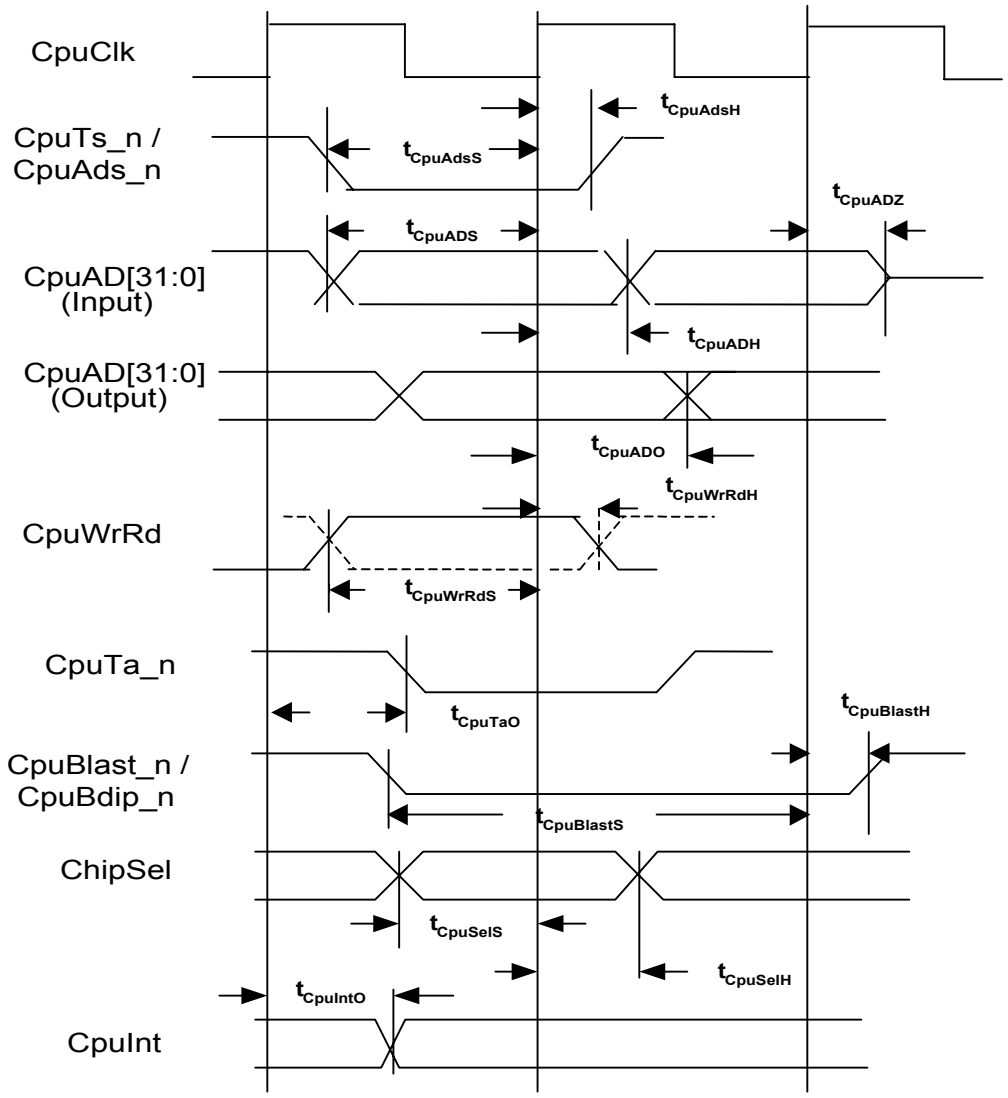
Switching Waveforms (continued)

Receive HBST System Interface Timing



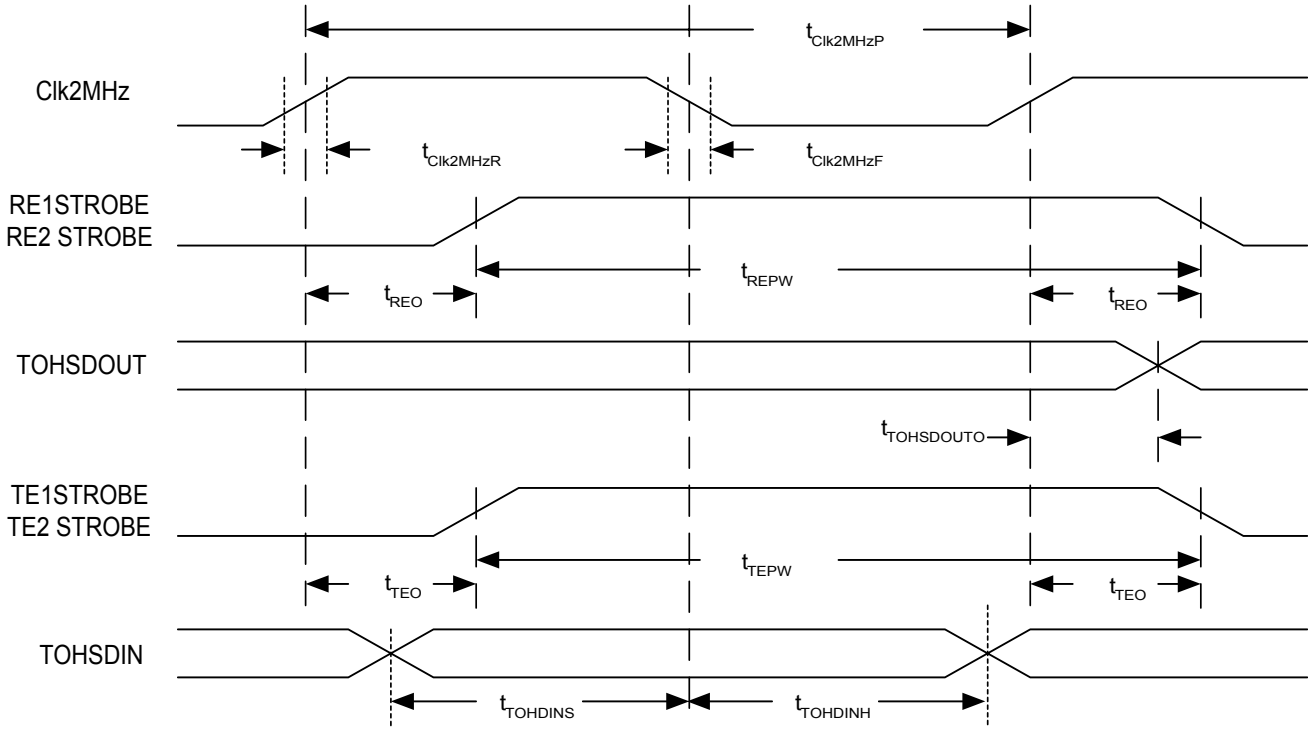
Switching Waveforms (continued)

CPU System Interface Timing

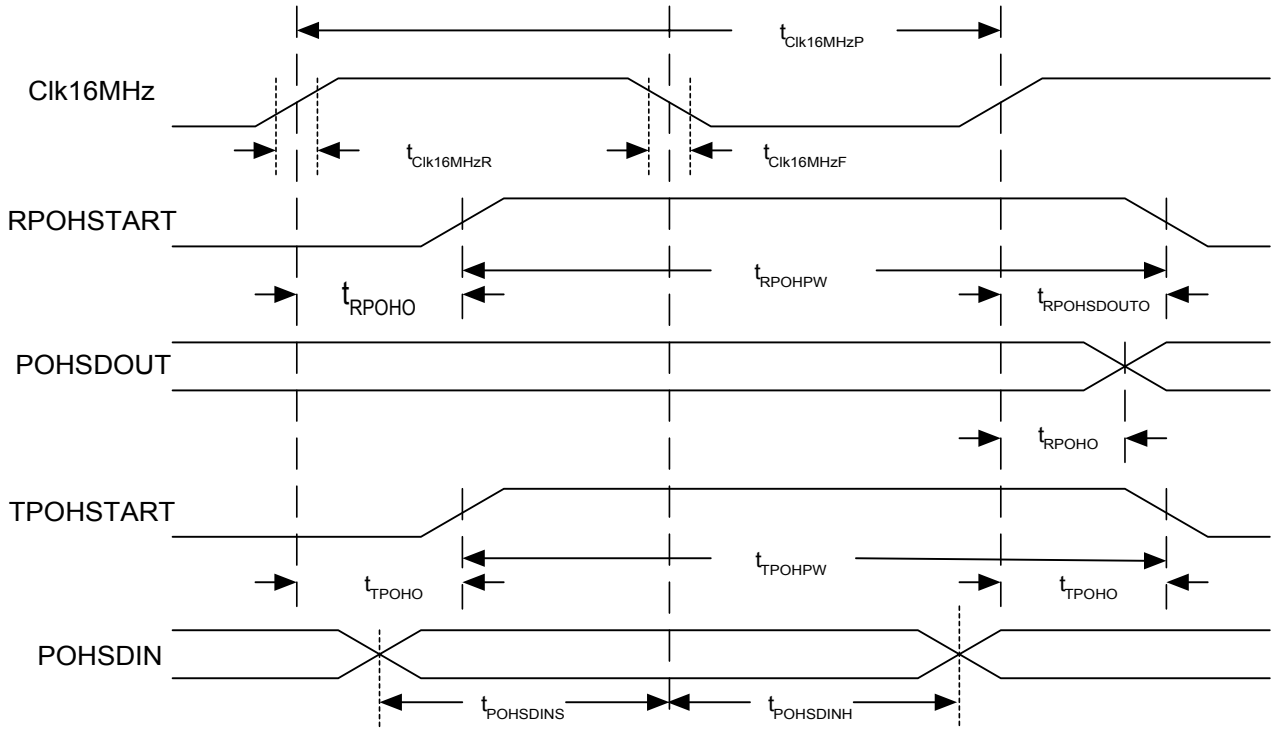


Switching Waveforms (continued)

TOH Serial Interface Timing



POH Serial Interface Timing

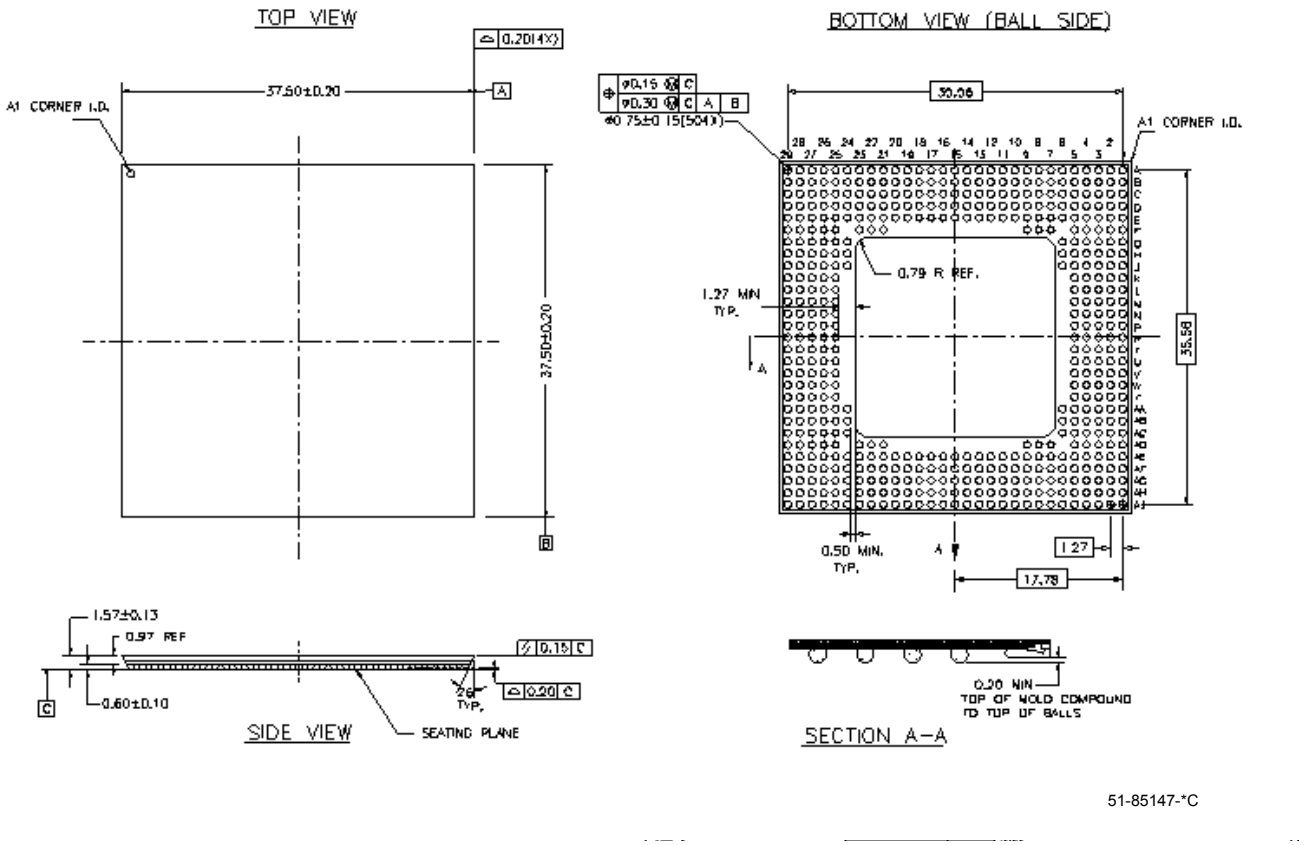


Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
Standard	CY7C9537B-BLC	BL504	504-pin BGA	Commercial
Standard	CY7C9537B-BLI	BL504	504-pin BGA	Industrial

Package Diagram

504-Lead L2 Ball Grid Array (37.50 x 37.50 x 1.57 mm) BL504



Please see Device Manual and errata document for further details on functional description.

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Document History Page

Document Title: OC-48/STM-16 Framer–POSIC2G™ Document Number: 38-02079				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	127208	07/03/03	QJL	New Data Sheet
*A	129315	10/17/03	CFK	Added specification references section Added Single POSIC2G APS implementation scheme description Removed statement that pin assignment is tentative Improved readability of pin diagram Added 16-bit mode operation pin description for TMOD and RMOD Clarified that POSIC_OEn signal three-states all POSIC2G outputs Changed CLK_OUT to CLKOUT in pin assignment table Corrected notes for parameters guaranteed by design/char Changed tRERRD/tRERRO parameter minimum from 1.5 ns to 1.2 ns Changed fSYSCLK to max 133.33 MHz Removed errata section (reference separate errata document) Changed POSIC2GB to POSIC2G
*B	131096	12/04/03	CFK	Clarified supported channelized operation modes in Features section Changed from Preliminary to Final data sheet
*C	132896	01/26/04	CFK	Minor Change: MPN uploaded to CAS.
*D	215296	See ECN	PIR	No content change. Post to web under NDA.
*E	317619	See ECN	QJL	Updated Icc3 to 0.75A. Updated Icc5 to 0.28A. Updated max Ios from TBD to -100mA. Updated Icc1 to 1A. Post to web under NDA.
*F	359676	See ECN	QJL	Note that NC pins are “do not use.”