Product Specification

PE42542

UltraCMOS® SP4T RF Switch
9 kHz–18 GHz

Features

- HaRP technology enhanced
  - Fast settling time
  - No gate and phase lag
  - No drift in insertion loss and phase
- Low insertion loss
  - 1.10 dB @ 3 GHz
  - 2.10 dB @ 13.5 GHz
  - 2.50 dB @ 16 GHz
  - 3.10 dB @ 18 GHz
- High isolation
  - 55 dB @ 3 GHz
  - 33 dB @ 13.5 GHz
  - 29 dB @ 16 GHz
  - 26 dB @ 18 GHz
- ESD performance
  - 3500V HBM on all pins
  - 150V MM on all pins
  - 500V CDM on all pins

Product Description

The PE42542 is a HaRP™ technology-enhanced absorptive SP4T RF switch designed for use in Test/ ATE, microwave and other wireless applications. This broadband general purpose switch maintains excellent RF performance and linearity from 9 kHz through 18 GHz. The PE42542 exhibits low insertion loss, high isolation performance and has fast settling time. No blocking capacitors are required if DC voltage is not present on the RF ports.

The PE42542 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

Peregrine's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

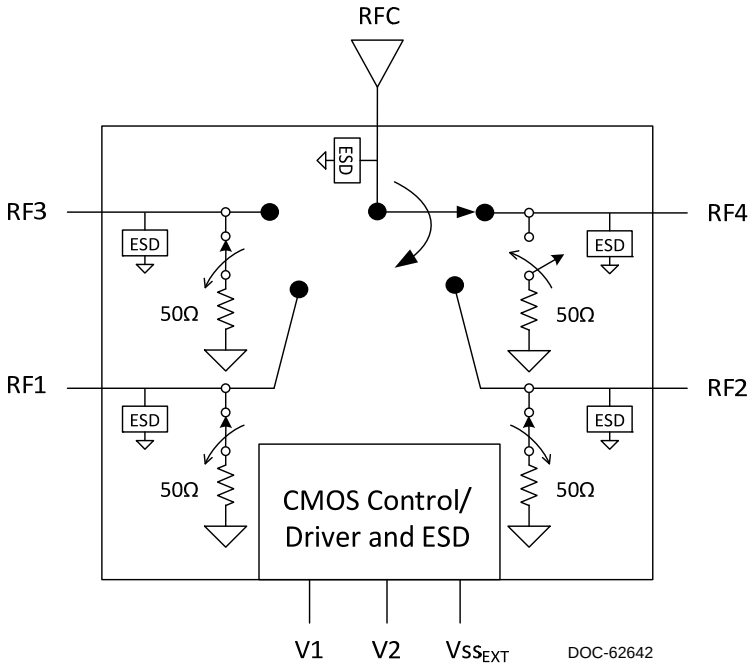
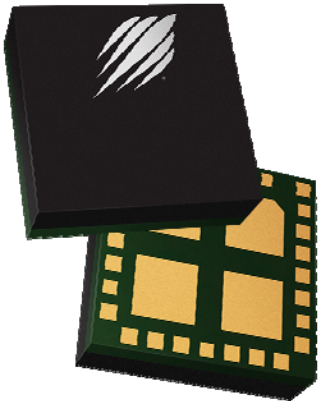


Figure 2. Package Type
29-lead 4 × 4 mm LGA



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Table 1. Electrical Specifications @ 25°C ($Z_S = Z_L = 50\Omega$), unless otherwise noted
Normal Mode[1]: V_{DD} = 3.3V, V_{SS_EXT} = 0V or Bypass Mode[2]: V_{DD} = 3.4V, V_{SS_EXT} = −3.4V

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency			9 k		18 G	Hz
Insertion loss	RFC–RFX	9 kHz–10 MHz		0.70	0.90	dB
		10–3000 MHz		1.10	1.40	dB
		3000–7500 MHz		1.50	1.95	dB
		7500–10000 MHz		1.75	2.20	dB
		10000–13500 MHz		2.10	2.40	dB
		13500–16000 MHz		2.50	2.80	dB
		16000–18000 MHz		3.10	4.10	dB
Isolation	RFX–RFX	9 kHz–10 MHz	80	90		dB
		10–3000 MHz	53	55		dB
		3000–7500 MHz	46	48		dB
		7500–10000 MHz	42	44		dB
		10000–13500 MHz	35	37		dB
		13500–16000 MHz	30	31		dB
		16000–18000 MHz	26	27		dB
Isolation	RFC–RFX	9 kHz–10 MHz	80	90		dB
		10–3000 MHz	54	55		dB
		3000–7500 MHz	41	42		dB
		7500–10000 MHz	36	38		dB
		10000–13500 MHz	31	33		dB
		13500–16000 MHz	27	29		dB
		16000–18000 MHz	24	26		dB
Return loss (active and common port)	RFC–RFX	9 kHz–10 MHz		25		dB
		10–3000 MHz		15		dB
		3000–18000 MHz		13		dB
Return loss (terminated port)	RFX	9 kHz–18000 MHz		16		dB
Input 0.1dB compression point[3]	RFC–RFX			*Fig. 4*		dBm
Input IP2	RFC–RFX	10–18000 MHz		118		dBm
Input IP3	RFC–RFX	10–18000 MHz		58		dBm
Settling time		50% CTRL to 0.05 dB final value		7	10	µs
Switching time		50% CTRL to 90% or 10% of final value		3	4.5	µs

Notes: 1. Normal mode: connect V_{SS_EXT} (pin 29) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.
2. Bypass mode: use V_{SS_EXT} (pin 29) to bypass and disable internal negative voltage generator.
3. The input 0.1dB compression point is a linearity figure of merit. Refer to *Table 3* for the RF input power P_{MAX} (50Ω).

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Figure 3. Pin Configuration (Top View)

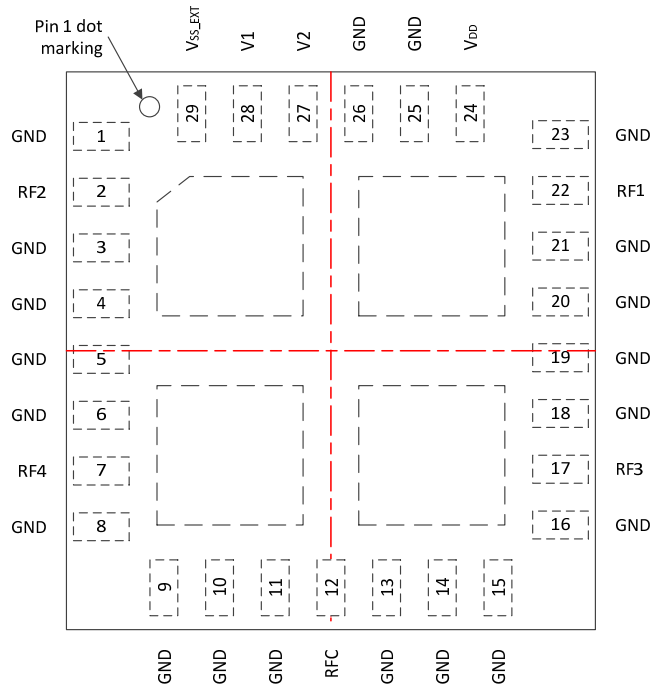


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1, 3–6, 8–11, 13–16, 18–21, 23, 25, 26	GND	Ground
2	RF2[1]	RF port 2
7	RF4[1]	RF port 4
12	RFC[1]	RF common
17	RF3[1]	RF port 3
22	RF1[1]	RF port 1
24	V_{DD}	Supply voltage (nominal 3.3V)
27	V2	Digital control logic input 2
28	V1	Digital control logic input 1
29	V_{SS_EXT} [2]	External V_{SS} negative voltage control
Pad	GND	Exposed pad: Ground for proper operation

Notes: 1. RF pins 2, 7, 12, 17, and 22 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2. Use V_{SS_EXT} (pin 29) to bypass and disable internal negative voltage generator. Connect V_{SS_EXT} (pin 29) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.

Table 3. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Unit
Normal mode[1] (V_{SS_EXT} = 0V)					
Supply voltage	V_{DD}	2.3		5.5	V
Supply current	I_{DD}		120	200	uA
Bypass mode[2] (V_{SS_EXT} = –3.4V)					
Supply voltage (V_{DD} ≥ 3.4V for *Table 1* full spec. compliance)	V_{DD}	2.7	3.4	5.5	V
Supply current	I_{DD}		50	80	uA
Negative supply voltage	V_{SS_EXT}	–3.6		–3.2	V
Negative supply current	I_{SS}	–40	–16		uA
Normal or Bypass mode					
Digital input high (V1, V2)	V_{IH}	1.17		3.6	V
Digital input low (V1, V2)	V_{IL}	–0.3		0.6	V
RF input power, CW (RFC–RFX)[3] 9 kHz–2.9 MHz ≥ 2.9 MHz–18 GHz	$P_{MAX,CW}$			*Fig. 4* 30	dBm dBm
RF input power, pulsed (RFC–RFX)[4] 9 kHz–2.9 MHz ≥ 2.9 MHz–18 GHz	$P_{MAX,PULSED}$			*Fig. 4* 32	dBm dBm
RF input power into terminated ports, CW (RFX)[3] 9 kHz–1.4 MHz ≥ 1.4 MHz–18 GHz	$P_{MAX,TERM}$			*Fig. 4* 20	dBm dBm
Operating temperature range	T_{OP}	–40	+25	+85	°C

Notes: 1. Normal mode: connect V_{SS_EXT} (pin 29) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator
2. Bypass mode: use V_{SS_EXT} (pin 29) to bypass and disable internal negative voltage generator
3. 100% duty cycle, all bands, 50Ω
4. Pulsed, 5% duty cycle of 4620 µs period, 50Ω

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Table 4. Absolute Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	–0.3	5.5	V
Digital input voltage (V1, V2)	V_{CTRL}	–0.3	3.6	V
RF input power, CW (RFC-RFX)[1] 9 kHz–2.9 MHz ≥ 2.9 MHz–18 GHz	$P_{MAX,CW}$		Fig. 4 33	dBm dBm
RF input power, pulsed (RFC-RFX)[2] 9 kHz–2.9 MHz ≥ 2.9 MHz–18 GHz	$P_{MAX,PULSED}$		Fig. 4 34	dBm dBm
RF input power into terminated ports, CW (RFX)[1] 9 kHz–1.4 MHz ≥ 1.4 MHz–18 GHz	$P_{MAX,TERM}$		Fig. 4 22	dBm dBm
Storage temperature range	T_{ST}	–65	+150	°C
ESD voltage HBM,[3] all pins	$V_{ESD,HBM}$		3500	V
ESD voltage MM[4], all pins	$V_{ESD,MM}$		150	V
ESD voltage CDM[5], all pins	$V_{ESD,CDM}$		500	V

Notes: 1. 100% duty cycle, all bands, 50Ω
2. Pulsed, 5% duty cycle of 4620 µs period, 50Ω
3. Human Body Model (MIL_STD 883 Method 3015)
4. Machine Model (JEDEC JESD22-A115)
5. Charged Device Model (JEDEC JESD22-C101)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Switching Frequency

The PE42542 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 29 = GND). Switching frequency describes the time duration between switching events. Switching time is the duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

Optional External V_{SS} Control (V_{SS_EXT})

For proper operation, the V_{SS_EXT} control pin must be grounded or tied to the V_{SS} voltage specified in *Table 3*. When the V_{SS_EXT} control pin is grounded, FETs in the switch are biased with an internal negative voltage generator. For applications that require the lowest possible spur performance, V_{SS_EXT} can be applied externally to bypass the internal negative voltage generator.

Spurious Performance

The typical spurious performance of the PE42542 is –150 dBm when V_{SS_EXT} = 0V (pin 29 = GND). If further improvement is desired, the internal negative voltage generator can be disabled by setting V_{SS_EXT} = –3.4V.

Table 5. Truth Table

State	V1	V2
RF1 on	0	0
RF2 on	1	0
RF3 on	0	1
RF4 on	1	1

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE42542 in the 29-lead 4 × 4 mm LGA package is MSL3.

Hot Switching

The maximum hot switching capability of the PE42542 is 20 dBm from 1.4 MHz to 18 GHz. The maximum hot switching capability below 1.4 MHz does not exceed the maximum RF CW terminated power, see *Figure 4*. Hot switching occurs when RF power is applied while switching between RF ports.

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Figure 4a. Power De-rating Curve for 9 kHz–18 GHz @ 25°C Ambient (50Ω)

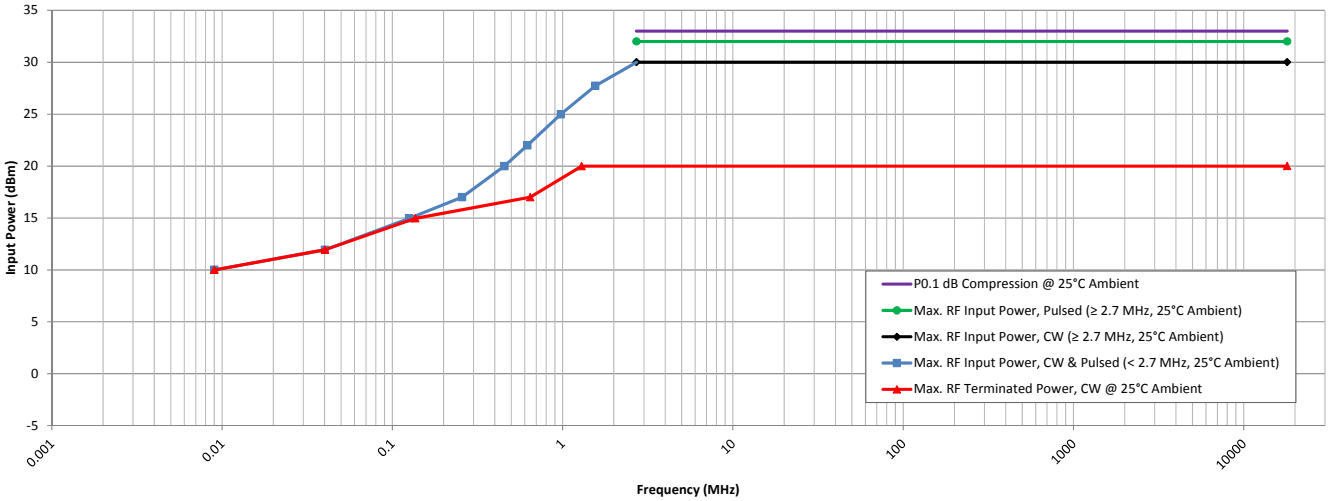
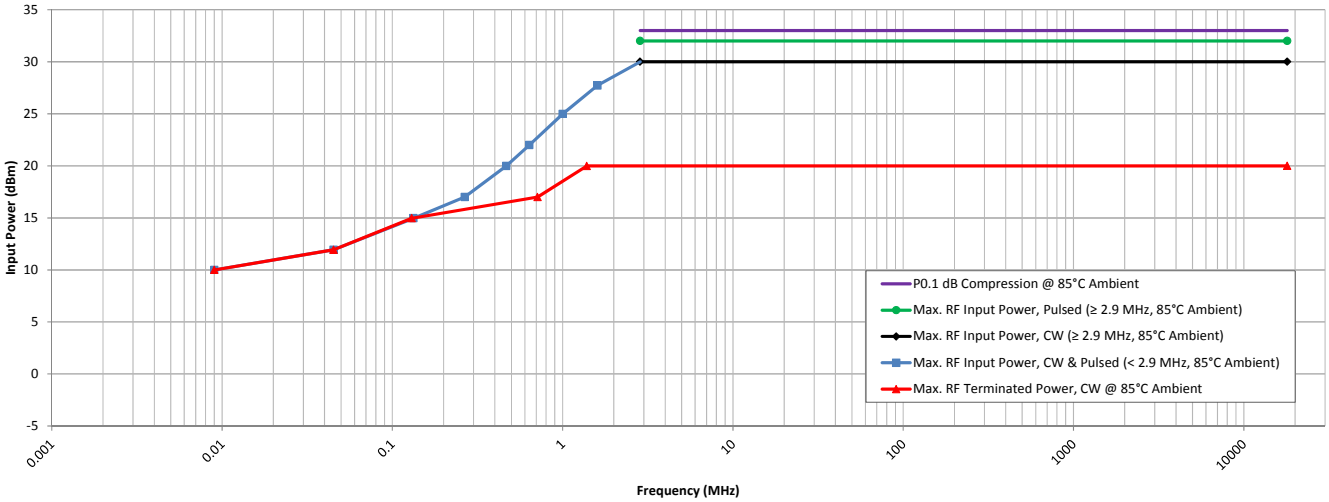


Figure 4b. Power De-rating Curve for 9 kHz–18 GHz @ 85°C Ambient (50Ω)



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Typical Performance Data @ 25°C and V_{DD} = 3.3V (Z_S = Z_L = 50Ω), unless otherwise noted

Figure 5. Insertion Loss (RFC–RFX)

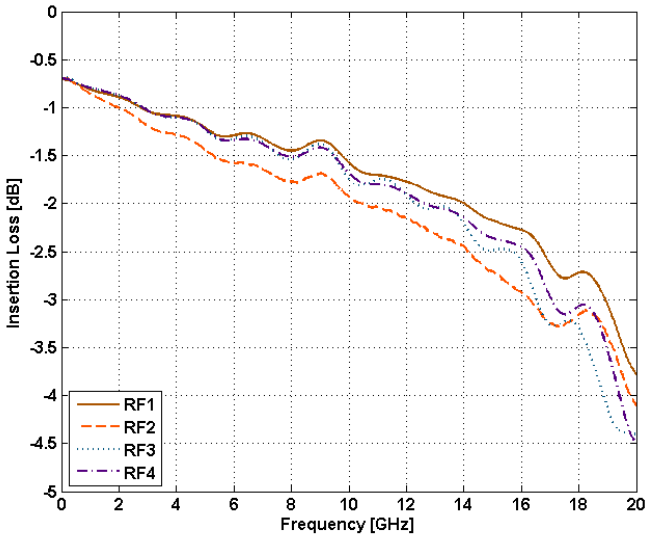


Figure 6. Insertion Loss vs. Temp (RFC–RFX)

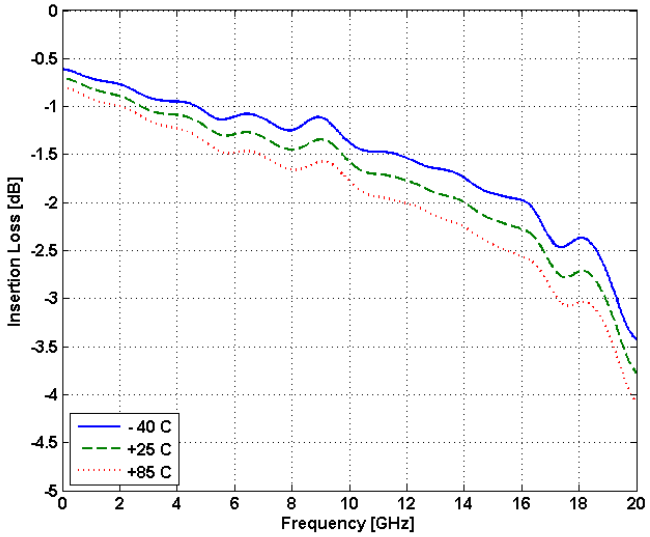
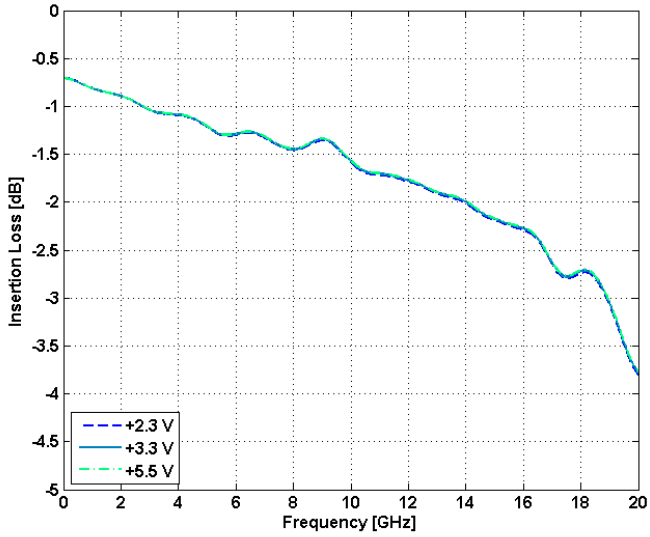


Figure 7. Insertion Loss vs. V_{DD} (RFC–RFX)



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Typical Performance Data @ 25°C and V_{DD} = 3.3V (Z_S = Z_L = 50Ω), unless otherwise noted

Figure 8. RFC Port Return Loss vs. Temp

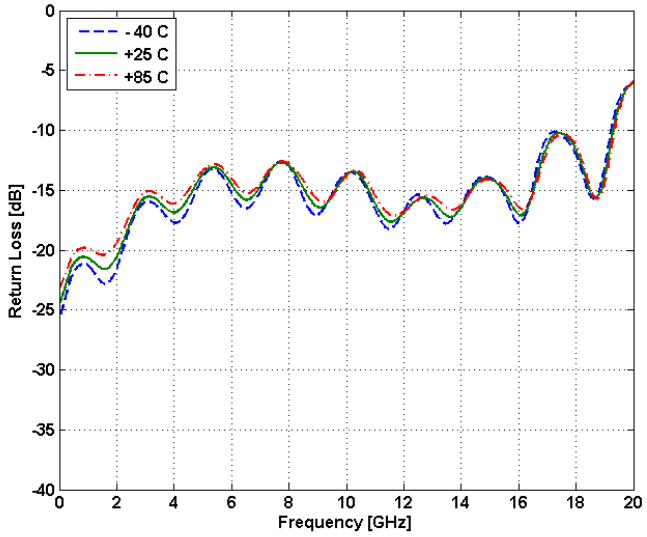


Figure 9. RFC Port Return Loss vs. V_{DD}

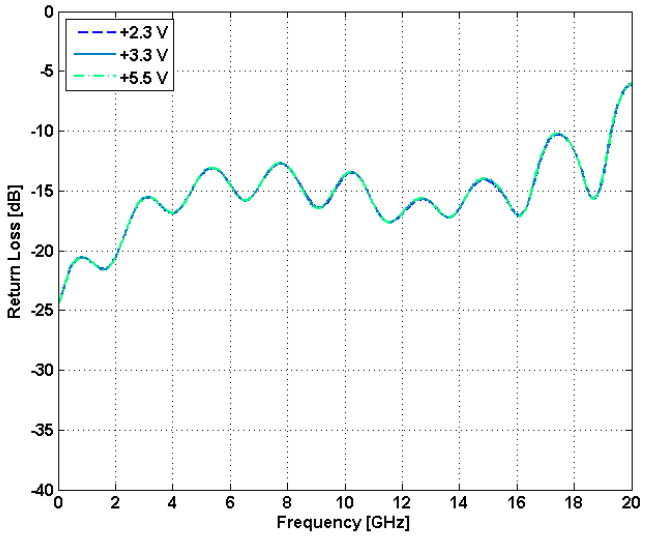


Figure 10. Active Port Return Loss vs. Temp

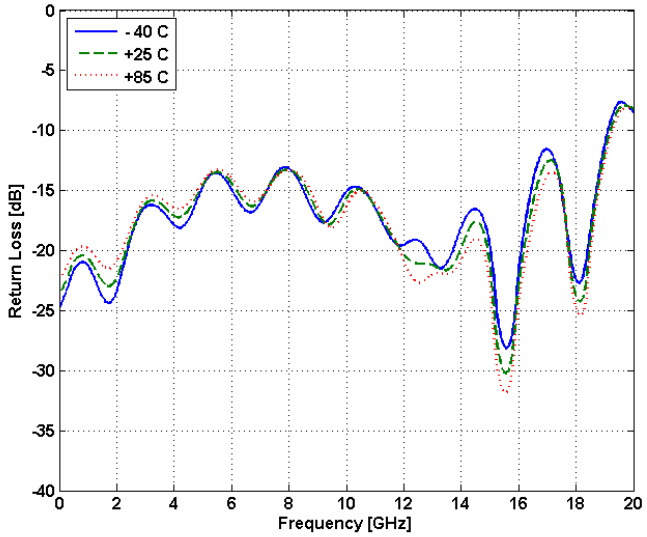
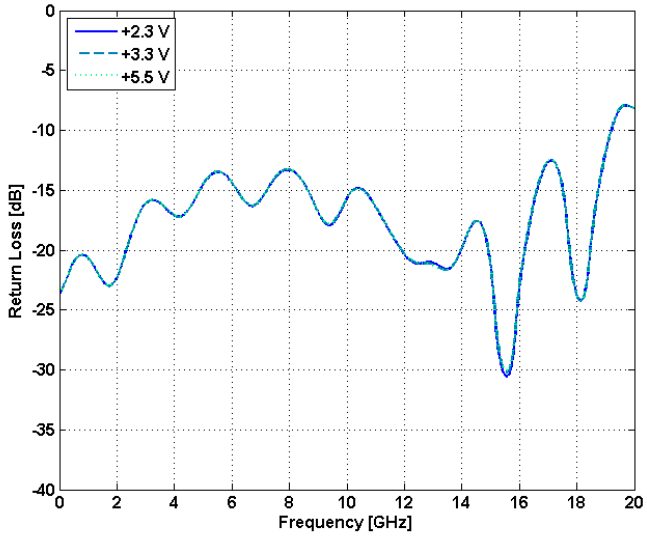


Figure 11. Active Port Return Loss vs. V_{DD}



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Typical Performance Data @ 25°C and V_{DD} = 3.3V (Z_S = Z_L = 50Ω), unless otherwise noted

Figure 12. Terminated Port Return Loss vs. Temp

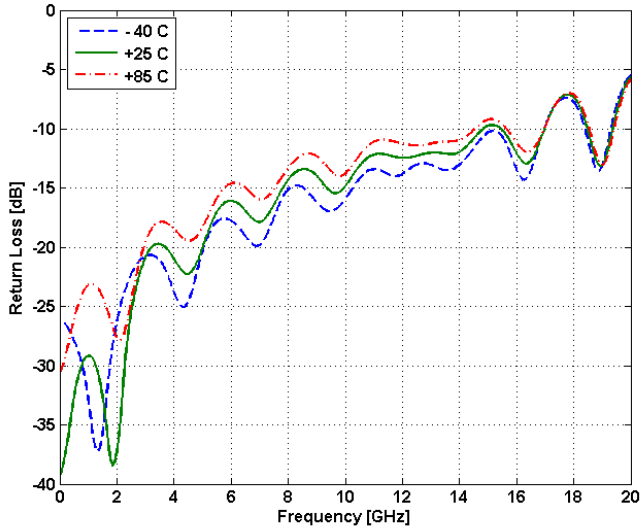
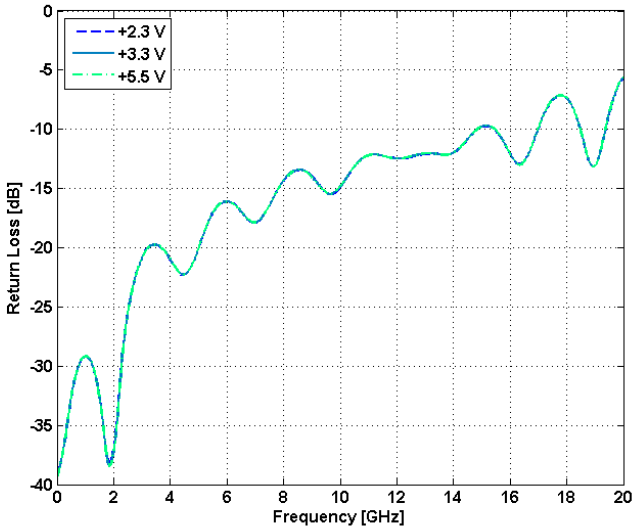


Figure 13. Terminated Port Return Loss vs. V_{DD}



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Typical Performance Data @ 25°C and V_{DD} = 3.3V (Z_S = Z_L = 50Ω), unless otherwise noted

Figure 14. Isolation vs. Temp (RFX–RFX)*

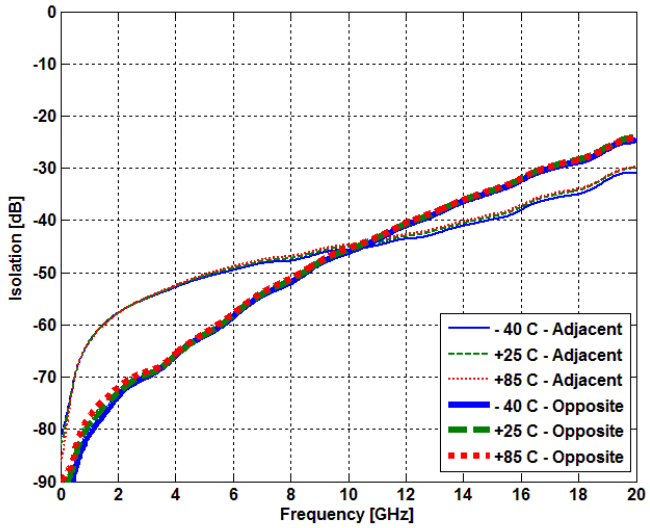
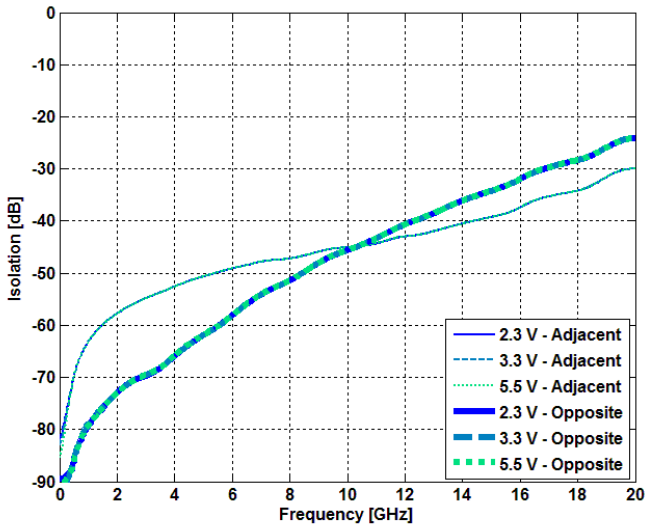


Figure 15. Isolation vs. V_{DD} (RFX–RFX)*



Note: * RF1 adjacent to RF3
RF2 adjacent to RF4
RF1 and RF3 opposite to RF2 and RF4

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Typical Performance Data @ 25°C and V_{DD} = 3.3V (Z_S = Z_L = 50Ω), unless otherwise noted

Figure 16. Isolation vs. Temp (RFC–RFX, RF1 or RF2 Active)*

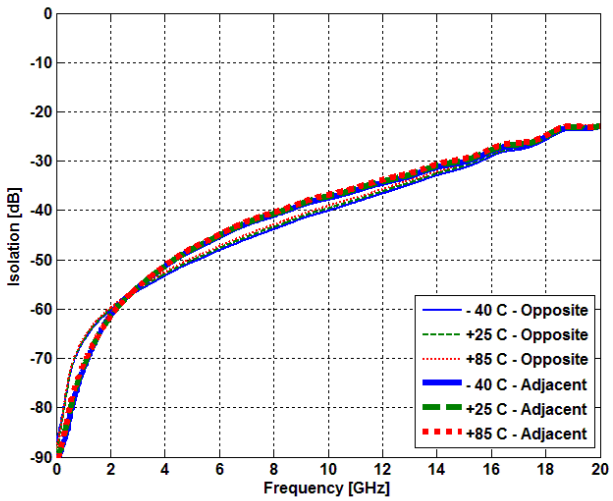


Figure 17. Isolation vs. V_{DD} (RFC–RFX, RF1 or RF2 Active)*

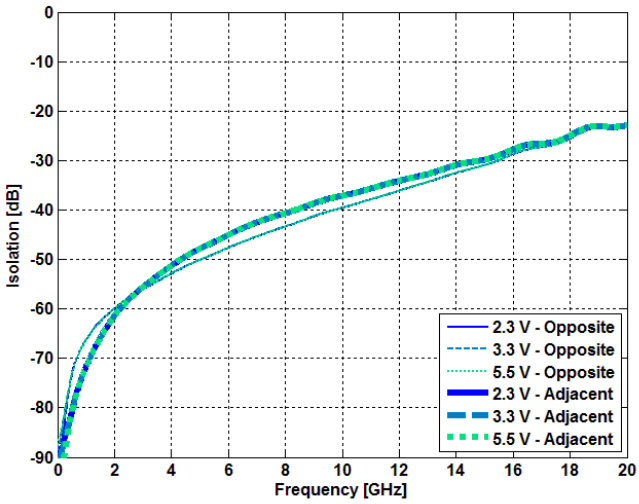


Figure 18. Isolation vs. Temp (RFC–RFX, RF3 or RF4 Active)*

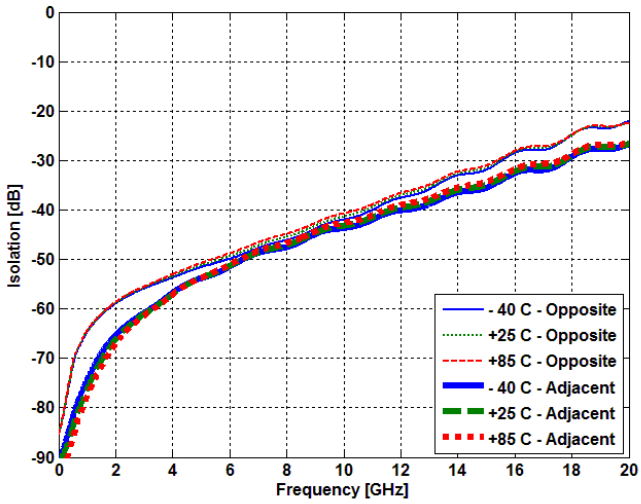
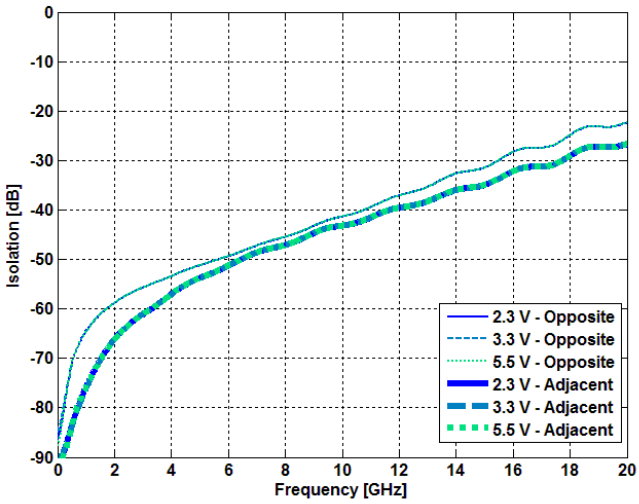


Figure 19. Isolation vs. V_{DD} (RFC–RFX, RF3 or RF4 Active)*



Note: * RF1 adjacent to RF3
RF2 adjacent to RF4
RF1 and RF3 opposite to RF2 and RF4

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Evaluation Kit

The SP4T switch evaluation board was designed to ease customer evaluation of Peregrine's PE42542. The RF common port is connected through a 50Ω transmission line via the SMA connector, J1. RF1, RF2, RF3 and RF4 ports are connected through 50Ω transmission lines via SMA connectors J4, J3, J2 and J5, respectively. A 50Ω through transmission line is available via SMA connectors J6 and J7, which can be used to de-embed the loss of the PCB. J13 provides DC and digital inputs to the device.

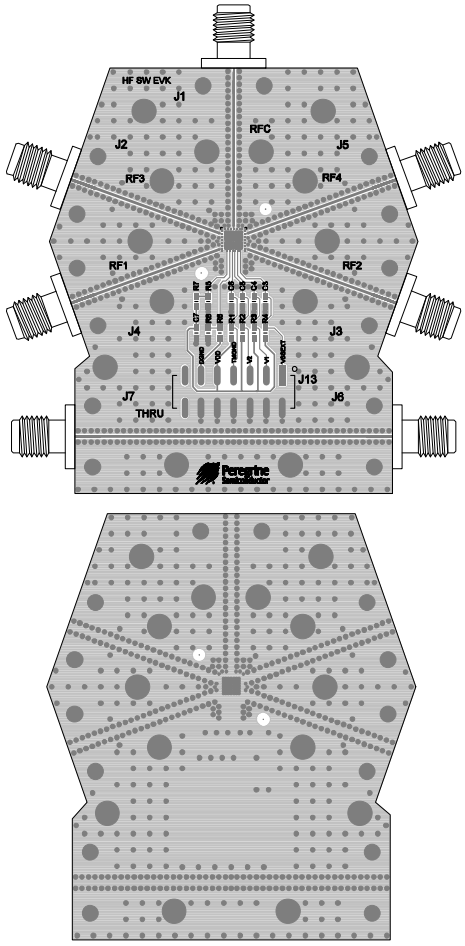
The board is constructed of a four metal layer material with a total thickness of 62 mils. The top RF layer is Rogers 4360 material with a thickness of 32 mils and the ε_r = 6.4. The middle layers provide ground for the transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 18 mils, trace gaps of 7 mils and metal thickness of 2.1 mils.

For the true performance of the PE42542 to be realized, the PCB should be designed in such a way that RF transmission lines and sensitive DC I/O traces are heavily isolated from one another.

High frequency insertion loss and return loss can be further improved by external series inductive tuning traces in the customer application board layout. For example, to improve 12–18 GHz performance, use ~180 pH for RFX ports and ~50 pH for RFC port.

Vector de-embed is recommended to more accurately calculate the performance of the DUT. Refer to Application Note 39 "*Vector De-embedding of the PE42542 and PE42543 SP4T RF Switches"* for additional information. The half thru line data file can be downloaded from Peregrine's website to facilitate the vector de-embedding.

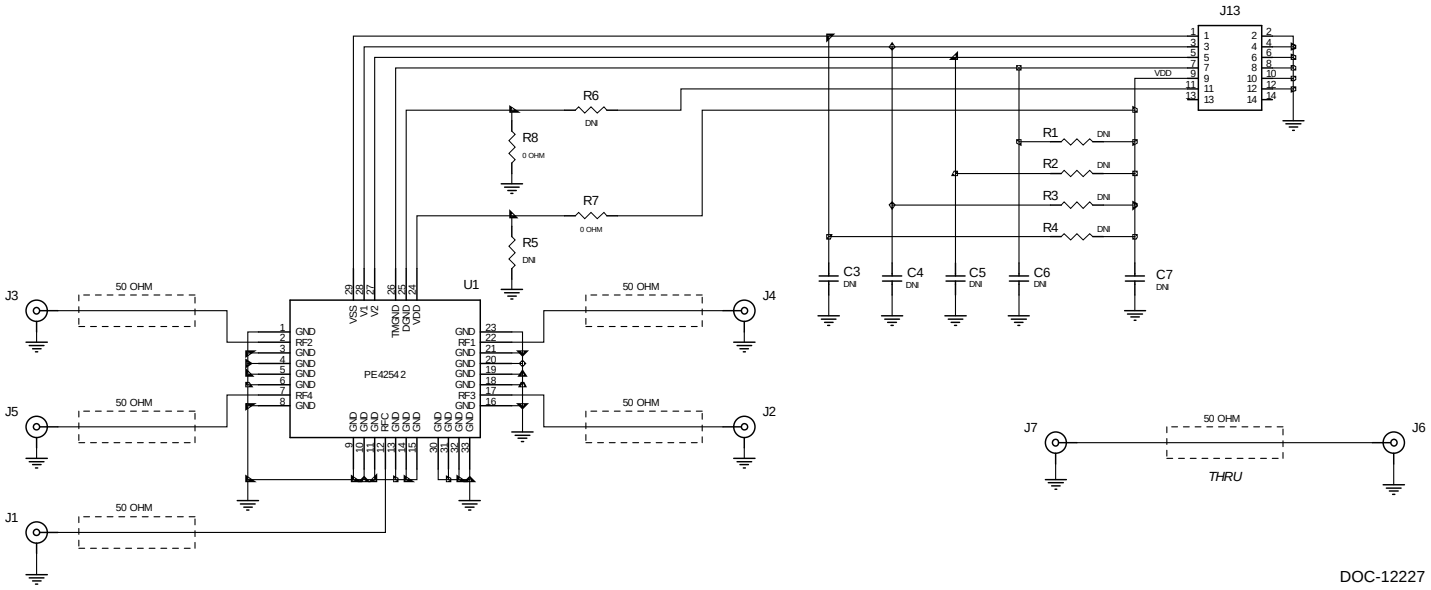
Figure 20. Evaluation Board Layout



PRT-09205

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Figure 21. Evaluation Board Schematic



CAUTION: Contains parts and assemblies susceptible to damage by electrostatic discharge (ESD).

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Figure 22. Package Drawing

29-lead 4 × 4 mm LGA

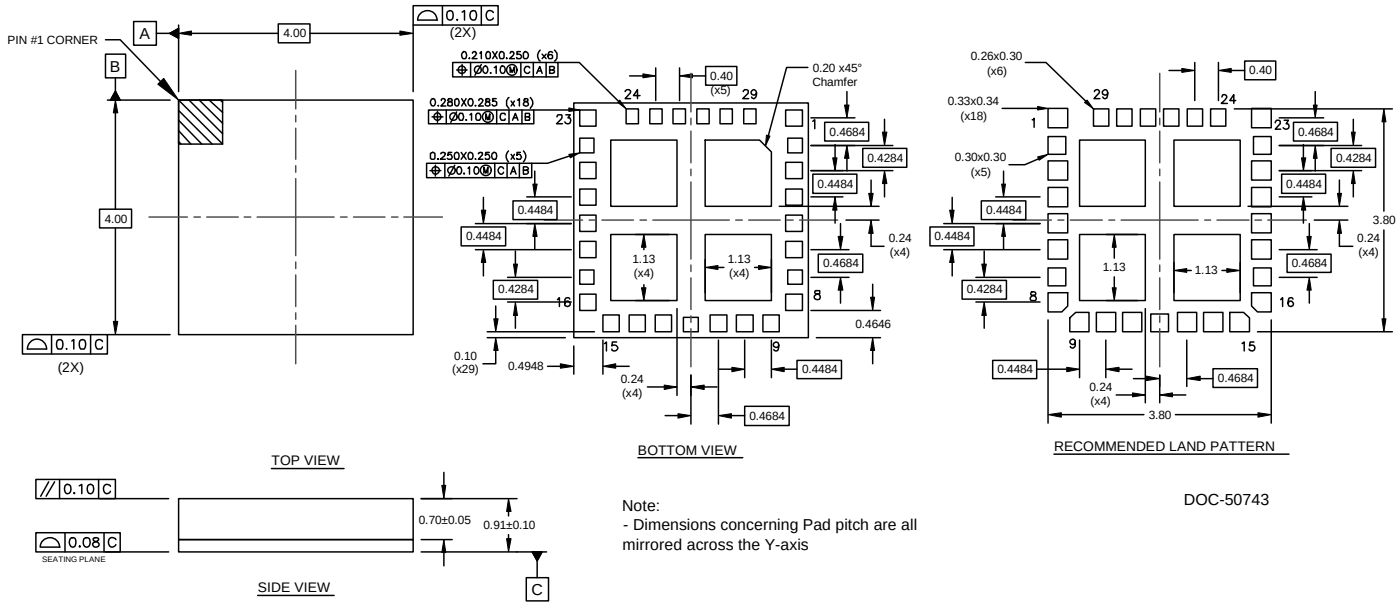
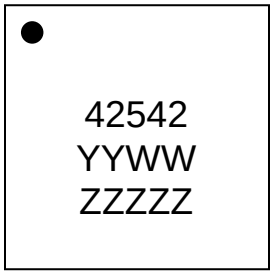


Figure 23. Top Marking Specification



DOC-51207-2

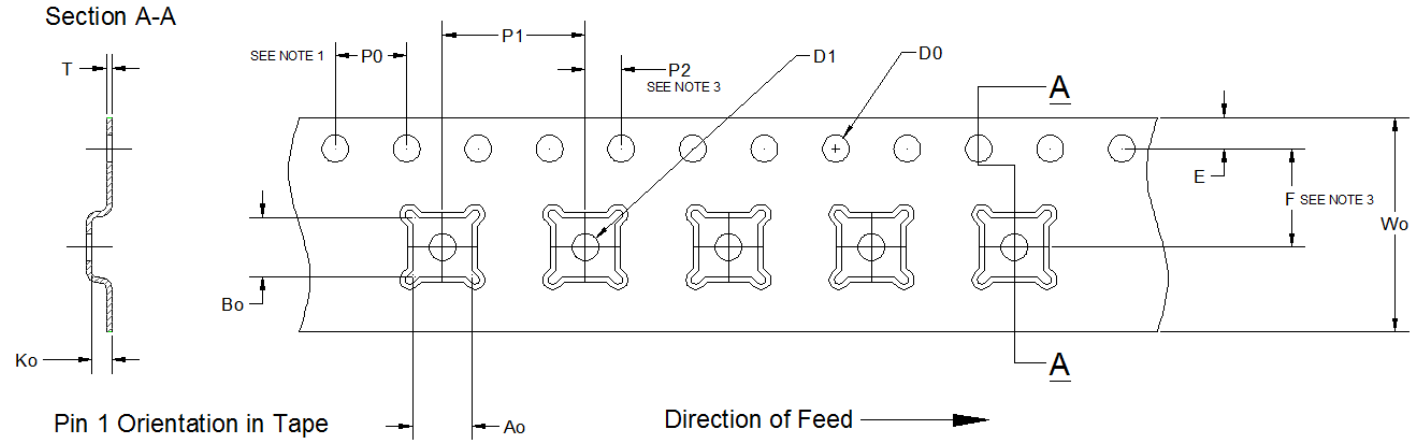
● = Pin 1 designator

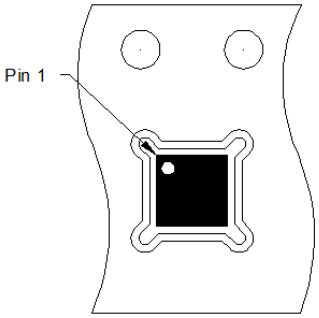
YYWW = Date code, last two digits of assembly year and work week

ZZZZZ = Last five characters of the assembly lot code

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Figure 24. Tape and Reel Drawing





NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

Ao	4.35
Bo	4.35
Ko	1.10
Do	1.50 + 0.10/ - 0.00
D1	1.50 Min
E	1.75 +/- 0.10
F	5.50 +/- 0.05
Po	4.00
P1	8.00
P2	2.00 +/- 0.05
T	0.30 +/- 0.05
Wo	12.00 +/- 0.30

Table 6. Ordering Information

Order Code	Description	Package	Shipping Method
PE42542A-X	PE42542 SP4T RF switch	29-lead 4 × 4 mm LGA	500 units / T&R
EK42542-02	PE42542 Evaluation kit	Evaluation kit	1 / Box

Sales Contact and Information

For sales and contact information please visit www.psemi.com.

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