RX610 Group Datasheet
RENESAS 32-Bit MCU

R01DS0097EJ0120
Rev.1.20
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1. Overview

1.1 Features

The RX610 Group is an MCU with the high-speed, high-performance RX CPU as its core.

One basic instruction is executable in one cycle of the system clock. Calculation functionality is further enhanced, with the inclusion of a single-precision floating-point calculation unit as well as a 32-bit multiplier and divider. Additionally, code efficiency is improved by instructions with lengths that are variable in byte units and by an enhanced range of addressing modes.

Timers, serial communication interfaces, I^2C bus interfaces, an A/D converter, and a D/A converter are incorporated as peripheral functions which are essential to embedded devices.

Facilities for connecting external memory are also included, enabling direct connection to memory and peripheral LSI circuits. The on-chip memory is flash memory capable of large-capacity, high-speed operation, and this significantly reduces the cost of configuring systems.

1.1.1 Applications

Office automation equipment and digital industrial equipment

1.1.2 Outline of Specifications

Table 1.1 lists the specifications of the RX610 Group in outline.

Table 1.1 Outline of Specifications

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 100 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction in one state (in one system clock cycle) • Address space: 4-Gbyte linear address • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Nine 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point operation instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 x 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions conforming to the IEEE754 standard
Memory	Flash	• Flash capacity: 2 Mbytes (max.) • Three types of on-board programming modes SCI boot mode, user program mode, and user boot mode
	RAM	RAM capacity: 128 Kbytes
	Data flash	Data flash capacity: 32 Kbytes
MCU operating modes		Single-chip mode, on-chip ROM enabled extended mode, and on-chip ROM disabled extended mode
Clock	Clock generation circuit	• One main clock oscillation circuit • Includes a PLL circuit and frequency divider, so the operating frequency is selectable • System clock, peripheral module clock, and external bus clock are independently specifiable. The CPU, DMAC, DTC, ROM, and RAM run in synchronization with the system clock (ICLK): 8 to 100 MHz Peripheral modules run in synchronization with the peripheral module clock (PCLK): 8 to 50 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): 8 to 25 MHz
Power down	Power-down function	• Module stop function • Four power-down modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode

Classification	Module/Function	Description
Interrupt	Interrupt control unit	• Peripheral function interrupts: 116 • External interrupts: 16 (pins IRQ15 to IRQ0) • Non-maskable interrupt: 1 (the NMI pin) • Eight priority orders specifiable
External bus extension		• The external address space can be divided into eight areas (CS0 to CS7), each of which is independently controllable. Capacity of each area: 16 Mbytes Chip-select signals (CS0# to CS7#) can be output for each area. 8-bit or 16-bit bus space can be specified for each area. The data arrangement is selectable as little endian or big endian for each area. (only for data) • Separate bus system • Wait control • Write buffer programming
DMA	DMA controller	• 4-channel DMA transfer available • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activated by interrupt requests (chain transfer enabled)
I/O ports	Programmable I/O ports	• I/O pins: 117 (144-pin LQFP), 140 (176-pin LFBGA) • Pull-up resistors: 40 • Open-drain outputs: 16 • 5-V tolerance: 10
Timer	16-bit timer pulse unit	• (16 bits x 6 channels) x 2 units • Up to 16 pulse inputs and outputs • Select from among 7 or 8 counter-input clocks for each channel • Input capture/output compare function • Maximum of 15-phase PWM output possible in PWM mode • Buffered operation, phase counting mode (two-phase encoder input), and cascaded operation (32 bits x 2 channels) settable for each channel • PPG output trigger can be generated • Conversion start trigger for the A/D converter can be generated
	Programmable pulse generator	• (4 bits x 4 groups) x 2 units • Provides pulse outputs by using the TPU output as a trigger • Maximum of 32-bit pulse output possible
	8-bit timer	• (8 bits x 2 channels) x 2 units • Select from among 8 clock sources (7 internal clocks and 1 external clock) • Allows the output of pulse trains with a desired duty cycle or PWM signals • Cascading of 2 channels enables it to be used as a 16-bit timer • Generation of trigger to start A/D converter conversion • Capable of generating baud rate clock for SCI5 and SCI6
	Compare match timer	• (16 bits x 2 channels) x 2 units • Select from among 4 counter-input clocks

Watchdog timer		• 8 bits x 1 channel • Select from among 8 counter-input clocks • Switchable between watchdog timer mode and interval timer mode
Communication function	Serial communication interface	• 7 channels • Serial communication mode: Asynchronous, clock synchronous, and smart card interface • On-chip baud rate generator allows any bit rate to be selected • Choice of LSB-first or MSB-first transfer • Enables average transfer rate clock input from TMR (SCI5, SCI6)
	I^2C bus interface	• 2 channels • Communication format I^2C bus format/SMBus format Master/slave selectable (For multi-master operation) • Maximum transfer rate: 1 Mbps
A/D converter		• 4 units (1 unit x 4 channels) • 10-bit resolution • Conversion time: 1.0 μs per channel (at 50-MHz (PCLK) operation) • Two kinds of operating modes Single mode and scan mode (single scan mode or continuous scan mode) • Sample-and-hold function • Three types of A/D conversion start Conversion can be started by software, a conversion start trigger by the timer (TPU or TMR), or an external trigger signal.
D/A converter		• 2 channels • 10-bit resolution • Output voltage: 0 V to VREFH
CRC calculator		• CRC code generation for arbitrary data lengths in 8-bit units • One of three generating polynomials selectable $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$ • CRC code generation for LSB-first or MSB-first communication selectable
Operating frequency		8 to 100 MHz
Power supply voltage		V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6V, VREFH = 3.0 to AV_{CC}
Supply current		50 mA (typ.) (regular specifications)
Operating temperature		−20 to +85°C (regular specifications), −40 to +85°C (wide-range specifications)
Package		176-pin LFBGA (PLBG0176GA-A) 144-pin LQFP (PLQP0144KA-A)

1.2 List of Products

Table 1.2 is the list of products, and figure 1.1 shows how to read the product part no.

Table 1.2 List of Products

Part No.	Package	ROM Capacity	RAM Capacity	Data Flash	Operating Frequency (Max.)
R5F56108VNFP	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56108VDFP	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56108WNBG	PLBG0176GA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56108WDBG	PLBG0176GA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56107VNFP	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56107VDFP	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56107WNBG	PLBG0176GA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56107WDBG	PLBG0176GA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56106VNFP	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz
R5F56106VDFP	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz
R5F56106WNBG	PLBG0176GA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz
R5F56106WDBG	PLBG0176GA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz
R5F56104VNFP	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56104VDFP	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56104WNBG	PLBG0176GA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz
R5F56104WDBG	PLBG0176GA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz

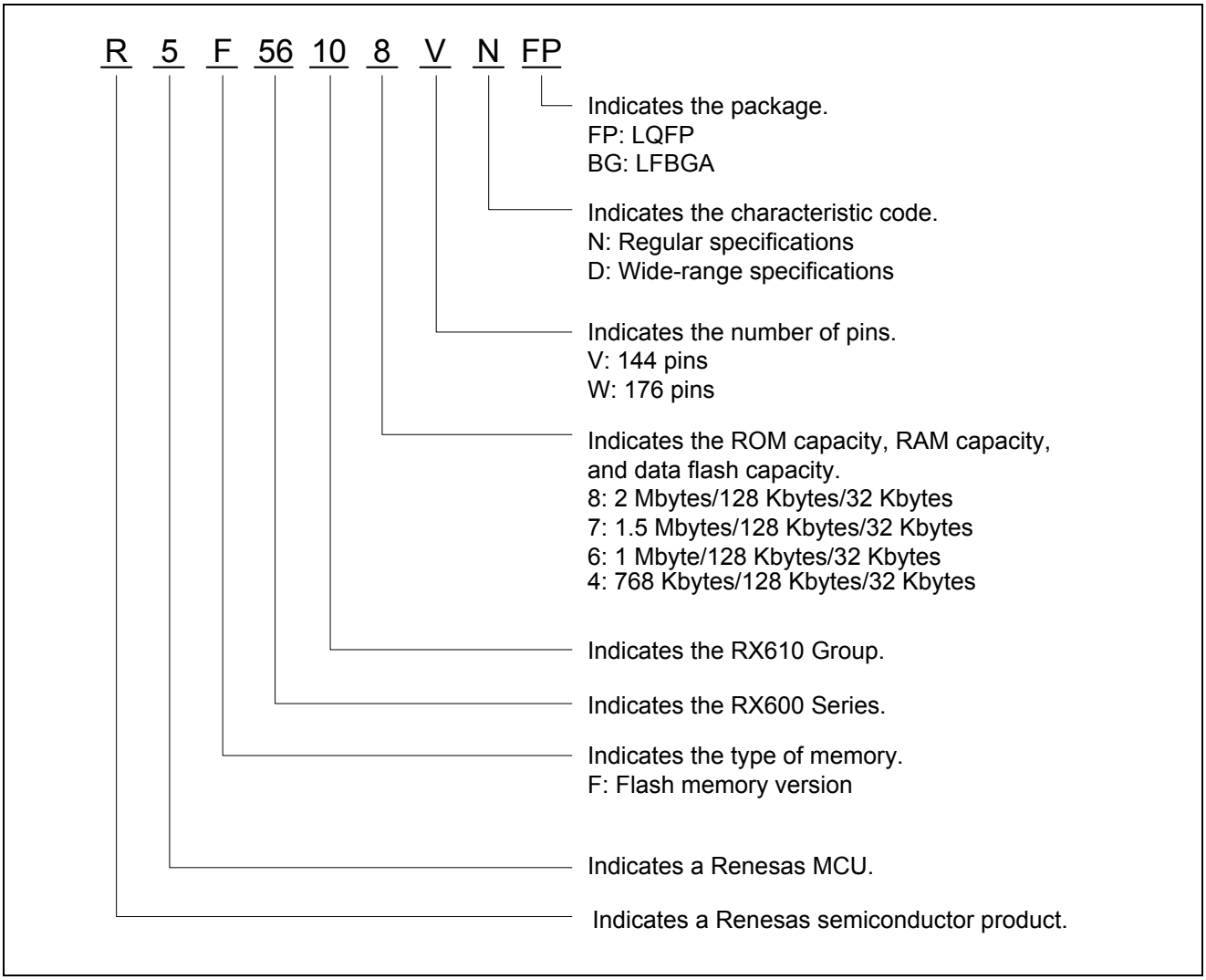
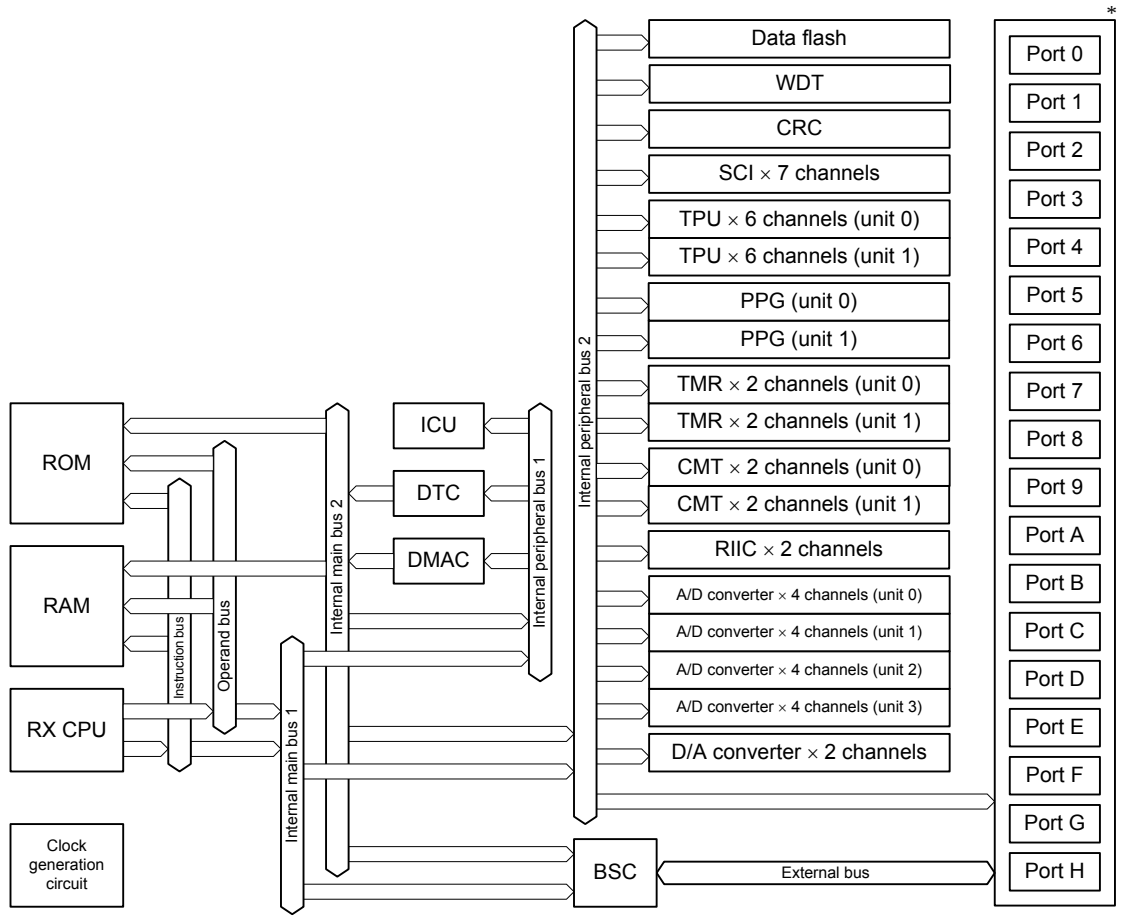


Figure 1.1 How to Read the Product Part No.

1.3 Block Diagram

Figure 1.2 shows a block diagram of the RX610 Group.



[Legend]

ICU:	Interrupt control unit	SCI:	Serial communications interfaces
DTC:	Data transfer controller	TPU:	16-bit timer pulse unit
DMAC:	DMA controller	PPG:	Programmable pulse generator
BSC:	Bus controller	TMR:	8-bit timer
WDT:	Watchdog timer	CMT:	Compare match timer
CRC:	CRC (Cyclic Redundancy Check) calculator	RIIC:	I^2C bus interface

Note: * Ports F and H are not included in the 144-pin LQFP package.

Figure 1.2 Block Diagram

1.4 Pin Assignments

Figures 1.3 and 1.4 show the pin assignments of the 176-pin LFBGA and the 144-pin LQFP, respectively. Figure 1.5 (assistance diagram) shows the pin assignment the 144-pin LQFP. Tables 1.3 and 1.4 show the lists of pins and pin functions of the 176-pin LFBGA and the 144-pin LQFP, respectively.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	PE0	PE2	PE5	PG5	VSS	PA1	PA5	PH1	P70	P74	PB3	PB6	PC1	VCC	PC3	15
14	PD6	PE1	PE3	PE7	PG6	PA0	PA4	PH0	VCC	P73	PB4	PC0	PC2	PC4	PC5	14
13	PD4	PD5	PD7	PE6	PG7	PA2	PA6	VSS	P71	PB1	PB5	VSS	PH2	PC6	P75	13
12	P63	VCC	VSS	PE4	VCC	PA3	PA7	PB0	P72	PB2	PB7	PC7	P76	P77	PH3	12
11	P60	P61	P62	P64								PH4	VSS	VCC	PH5	11
10	PD1	PD0	PD2	PD3								P51	P50	PH6	PH7	10
9	PG2	PG1	PG3	PG4								P81	P80	P52	P53	9
8	P97	P96	BSCANP	PG0								P83	VSS	VCC	P82	8
7	P93	P92	P94	P95								P57	P56	P54	P55	7
6	P90	VCC	VSS	P91								P37	P36	P84	P35	6
5	P46	P45	P47	P44								P14	P12	P11	P10	5
4	P43	P42	P41	P40	P00	MDE	P86	VSS	P34	P33	PF0	VSS	P16	P15	P13	4
3	VREFL	VREFH	P03	AVSS	EMLE	VCL	P85	EXTAL	PF6	P32	PF3	VCC	P20	PLLVCC	PLLVSS	3
2	AVCC	P05	P66	P01	WDTOVF#	MD0	XTAL	NMI	PF4	P30	PF1	P26	P24	P22	P17	2
1	P04	P67	P02	P65	VSS	MD1	RES#	VCC	PF5	P31	PF2	P27	P25	P23	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

RX610Group
PLBG0176GA-A
(176-pin LFBGA)
(Upper perspective view)

Figure 1.3 Pin Assignment of the 176-pin LFBGA

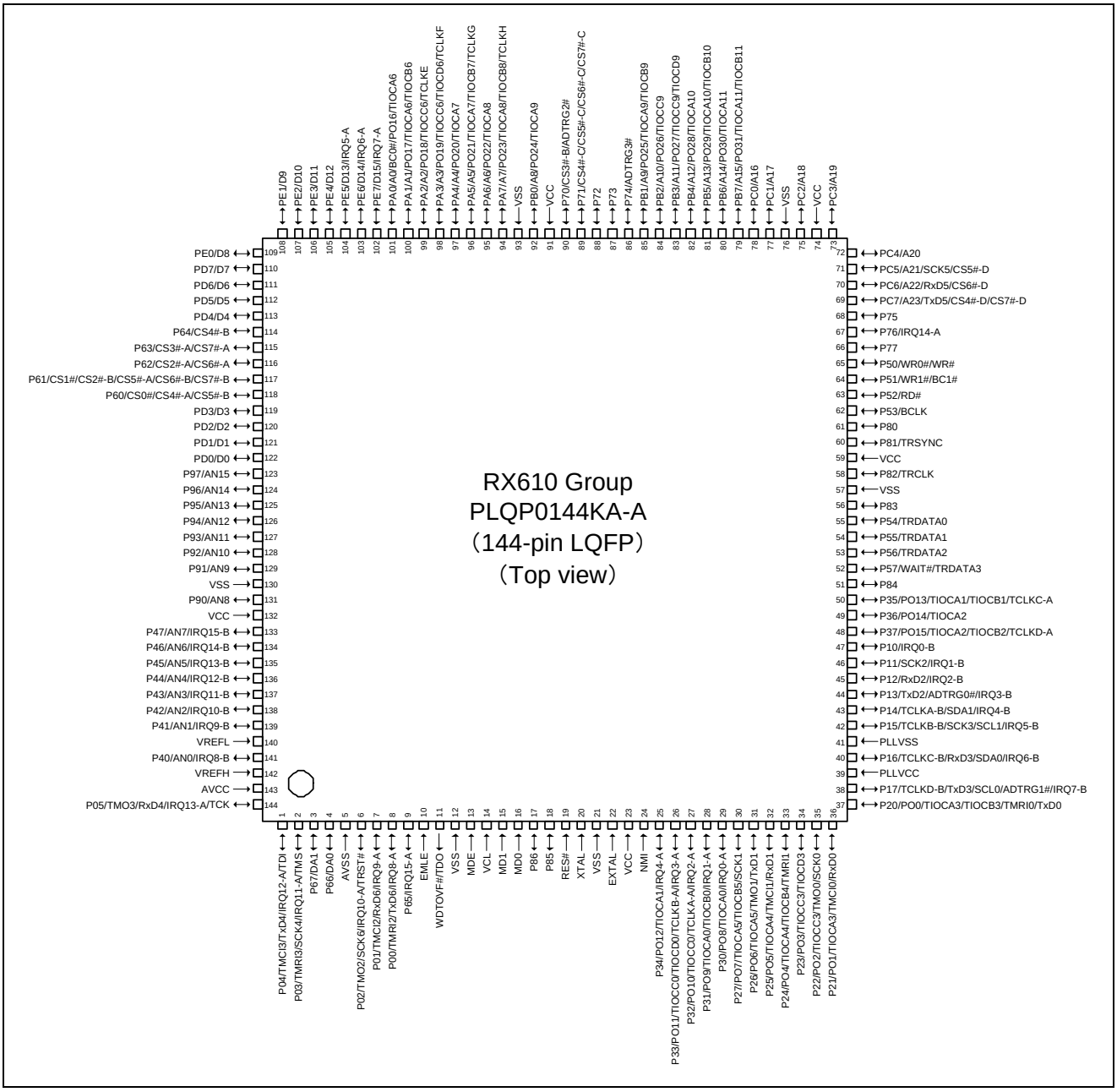


Figure 1.4 Pin Assignment of the 144-Pin LQFP

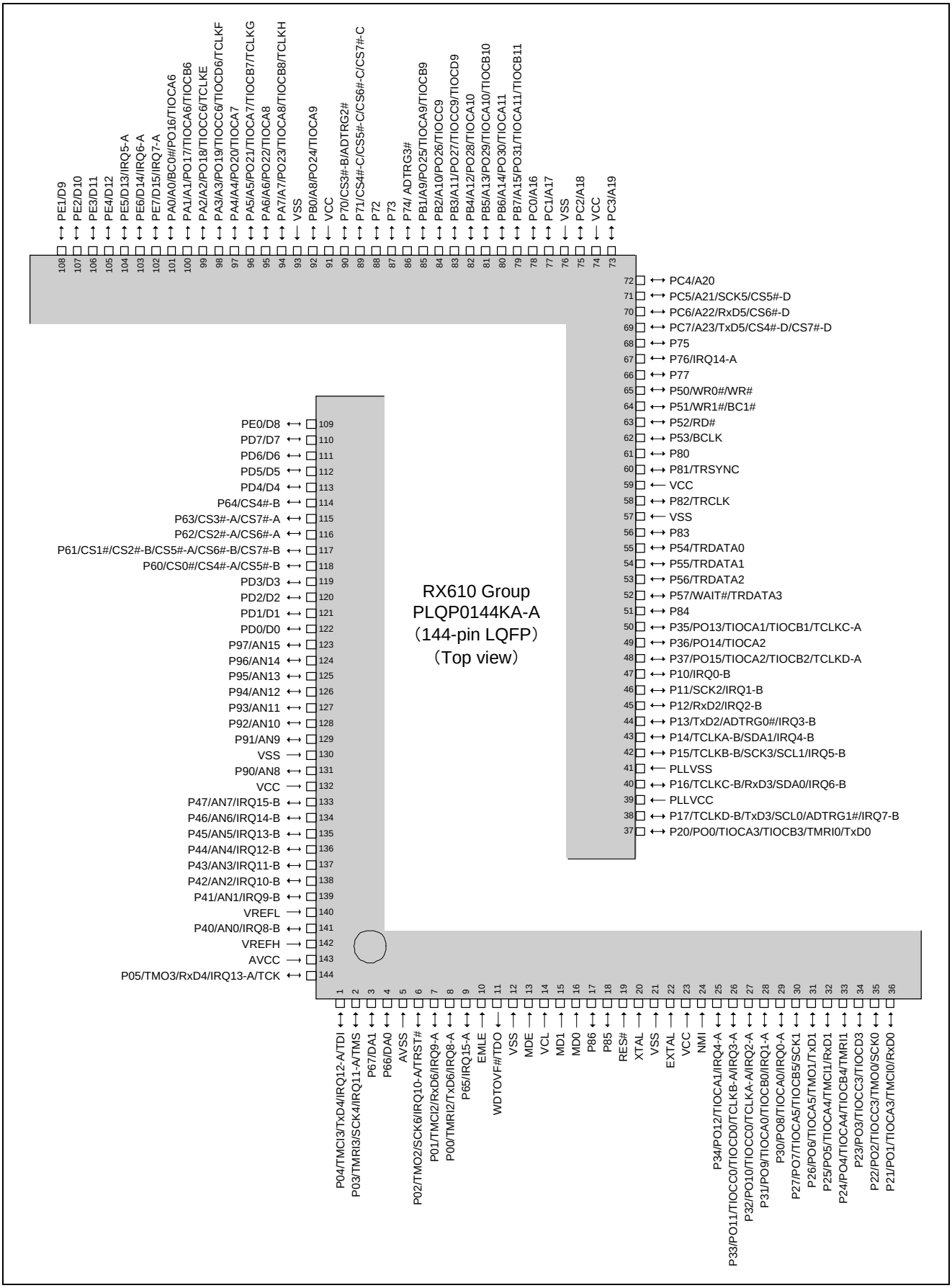


Figure 1.5 Pin Assignment (Assistance Diagram) of the 144-Pin LQFP

Table 1.3 List of Pins and Pin Functions (176-Pin LFBGA)

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
A1		P04	IRQ12-A		TMCI3	TxD4		TDI
A2	AVCC							
A3	VREFL							
A4		P43	IRQ11-B				AN3	
A5		P46	IRQ14-B				AN6	
A6		P90					AN8	
A7		P93					AN11	
A8		P97					AN15	
A9		PG2						
A10		PD1		D1				
A11		P60		CS0#/ CS4#-A/ CS5#-B				
A12		P63		CS3#-A/ CS7#-A				
A13		PD4		D4				
A14		PD6		D6				
A15		PE0		D8				
B1		P67					DA1	
B2		P05	IRQ13-A		TMO3	RxD4		TCK
B3	VREFH							
B4		P42	IRQ10-B				AN2	
B5		P45	IRQ13-B				AN5	
B6	VCC							
B7		P92					AN10	
B8		P96					AN14	
B9		PG1						
B10		PD0		D0				
B11		P61		CS1#/ CS2#-B/ CS5#-A/ CS6#-B/ CS7#-B				
B12	VCC							
B13		PD5		D5				
B14		PE1		D9				
B15		PE2		D10				
C1		P02	IRQ10-A		TMO2	SCK6		TRST#
C2		P66					DA0	
C3		P03	IRQ11-A		TMRI3	SCK4		TMS
C4		P41	IRQ9-B				AN1	
C5		P47	IRQ15-B				AN7	

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
C6	VSS							
C7		P94					AN12	
C8	BSCANP							
C9		PG3						
C10		PD2		D2				
C11		P62		CS2#-A/ CS6#-A				
C12	VSS							
C13		PD7		D7				
C14		PE3		D11				
C15		PE5	IRQ5-A	D13				
D1		P65	IRQ15-A					
D2		P01	IRQ9-A		TMCI2	RxD6		
D3	AVSS							
D4		P40	IRQ8-B				AN0	
D5		P44	IRQ12-B				AN4	
D6		P91					AN9	
D7		P95					AN13	
D8		PG0						
D9		PG4						
D10		PD3		D3				
D11		P64		CS4#-B				
D12		PE4		D12				
D13		PE6	IRQ6-A	D14				
D14		PE7	IRQ7-A	D15				
D15		PG5						
E1	VSS							
E2	WDTOVF#							TDO
E3	EMLE							
E4		P00	IRQ8-A		TMRI2	TxD6		
E12	VCC							
E13		PG7						
E14		PG6						
E15	VSS							
F1	MD1							
F2	MD0							
F3	VCL							
F4	MDE							
F12		PA3		A3	PO19/ TIOCC6/ TIOCD6/ TCLKF			

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
F13		PA2		A2	PO18/ TIOCC6/ TCLKE			
F14		PA0		A0/BC0#	PO16/ TIOCA6			
F15		PA1		A1	PO17/ TIOCA6/ TIOCB6			
G1	RES#							
G2	XTAL							
G3		P85						
G4		P86						
G12		PA7		A7	PO23/ TIOCA8/ TIOCB8/ TCLKH			
G13		PA6		A6	PO22/ TIOCA8			
G14		PA4		A4	PO20/ TIOCA7			
G15		PA5		A5	PO21/ TIOCA7/ TIOCB7/ TCLKG			
H1	VCC							
H2			NMI					
H3	EXTAL							
H4	VSS							
H12		PB0		A8	PO24/ TIOCA9			
H13	VSS							
H14		PH0						
H15		PH1						
J1		PF5						
J2		PF4						
J3		PF6						
J4		P34	IRQ4-A		PO12/ TIOCA1			
J12		P72						
J13		P71		CS4#-C/ CS5#-C/ CS6#-C/ CS7#-C				
J14	VCC							

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
J15		P70		CS3#-B			ADTRG2#	
K1		P31	IRQ1-A		PO9/ TIOCA0/ TIOCB0			
K2		P30	IRQ0-A		PO8/ TIOCA0			
K3		P32	IRQ2-A		PO10/ TIOCC0/ TCLKA-A			
K4		P33	IRQ3-A		PO11/ TIOCC0/ TIOCD0/ TCLKB-A			
K12		PB2		A10	PO26/ TIOCC9			
K13		PB1		A9	PO25/ TIOCA9/ TIOCB9			
K14		P73						
K15		P74					ADTRG3#	
L1		PF2						
L2		PF1						
L3		PF3						
L4		PF0						
L12		PB7		A15	PO31/ TIOCA11/ TIOCB11			
L13		PB5		A13	PO29/ TIOCA10/ TIOCB10			
L14		PB4		A12	PO28/ TIOCA10			
L15		PB3		A11	PO27/ TIOCC9/ TIOCD9			
M1		P27			PO7/ TIOCA5/ TIOCB5	SCK1		
M2		P26			PO6/ TIOCA5/ TMO1	TxD1		
M3	VCC							
M4	VSS							
M5		P14	IRQ4-B		TCLKA-B	SDA1		

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
M6		P37			PO15/ TIOCA2/ TIOCB2/ TCLKD-A			
M7		P57		WAIT#				TRDATA3
M8		P83						
M9		P81						TRSYNC
M10		P51		WR1#/BC1#				
M11		PH4						
M12		PC7		A23/ CS4#-D/ CS7#-D		TxD5		
M13	VSS							
M14		PC0		A16				
M15		PB6		A14	PO30/ TIOCA11			
N1		P25			PO5/ TIOCA4/ TMCI1	RxD1		
N2		P24			PO4/ TIOCA4/ TIOCB4/ TMRI1			
N3		P20			PO0/ TIOCA3/ TIOCB3/ TMRI0	TxD0		
N4		P16	IRQ6-B		TCLKC-B	RxD3/SDA0		
N5		P12	IRQ2-B			RxD2		
N6		P36			PO14/ TIOCA2			
N7		P56						TRDATA2
N8	VSS							
N9		P80						
N10		P50		WR0#/WR#				
N11	VSS							
N12		P76	IRQ14-A					
N13		PH2						
N14		PC2		A18				
N15		PC1		A17				
P1		P23			PO3/ TIOCC3/ TIOCD3			

Pin No. 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
P2		P22			PO2/ TIOCC3/ TMO0	SCK0		
P3	PLLVCC							
P4		P15	IRQ5-B		TCLKB-B	SCK3/SCL1		
P5		P11	IRQ1-B			SCK2		
P6		P84						
P7		P54						TRDATA0
P8	VCC							
P9		P52		RD#				
P10		PH6						
P11	VCC							
P12		P77						
P13		PC6		A22/ CS6#-D		RxD5		
P14		PC4		A20				
P15	VCC							
R1		P21			PO1/ TIOCA3/ TMCI0	RxD0		
R2		P17	IRQ7-B		TCLKD-B	TxD3/SCL0	ADTRG1#	
R3	PLLVSS							
R4		P13	IRQ3-B			TxD2	ADTRG0#	
R5		P10	IRQ0-B					
R6		P35			PO13/ TIOCA1/ TIOCB1/ TCLKC-A			
R7		P55						TRDATA1
R8		P82						TRCLK
R9	BCLK	P53						
R10		PH7						
R11		PH5						
R12		PH3						
R13		P75						
R14		PC5		A21/ CS5#-D		SCK5		
R15		PC3		A19				

Table 1.4 List of Pins and Pin Functions (144-Pin LQFP)

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
1		P04	IRQ12-A		TMCI3	TxD4		TDI
2		P03	IRQ11-A		TMRI3	SCK4		TMS
3		P67					DA1	
4		P66					DA0	
5	AVSS							
6		P02	IRQ10-A		TMO2	SCK6		TRST#
7		P01	IRQ9-A		TMCI2	RxD6		
8		P00	IRQ8-A		TMRI2	TxD6		
9		P65	IRQ15-A					
10	EMLE							
11	WDTOVF#							TDO
12	VSS							
13	MDE							
14	VCL							
15	MD1							
16	MD0							
17		P86						
18		P85						
19	RES#							
20	XTAL							
21	VSS							
22	EXTAL							
23	VCC							
24			NMI					
25		P34	IRQ4-A		PO12/ TIOCA1			
26		P33	IRQ3-A		PO11/ TIOCC0/ TIOCD0/ TCLKB-A			
27		P32	IRQ2-A		PO10/ TIOCC0/ TCLKA-A			
28		P31	IRQ1-A		PO9/ TIOCA0/ TIOCB0			
29		P30	IRQ0-A		PO8/ TIOCA0			
30		P27			PO7/ TIOCA5/ TIOCB5	SCK1		
31		P26			PO6/ TIOCA5/ TMO1	TxD1		

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
32		P25			PO5/ TIOCA4/ TMCI1	RxD1		
33		P24			PO4/ TIOCA4/ TIOCB4/ TMRI1			
34		P23			PO3/ TIOCC3/ TIOCD3			
35		P22			PO2/ TIOCC3/ TMO0	SCK0		
36		P21			PO1/ TIOCA3/ TMCI0	RxD0		
37		P20			PO0/ TIOCA3/ TIOCB3/ TMRI0	TxD0		
38		P17	IRQ7-B		TCLKD-B	TxD3/SCL0	ADTRG1#	
39	PLLVCC							
40		P16	IRQ6-B		TCLKC-B	RxD3/SDA0		
41	PLLVSS							
42		P15	IRQ5-B		TCLKB-B	SCK3/SCL1		
43		P14	IRQ4-B		TCLKA-B	SDA1		
44		P13	IRQ3-B			TxD2	ADTRG0#	
45		P12	IRQ2-B			RxD2		
46		P11	IRQ1-B			SCK2		
47		P10	IRQ0-B					
48		P37			PO15/ TIOCA2/ TIOCB2/ TCLKD-A			
49		P36			PO14/ TIOCA2			
50		P35			PO13/ TIOCA1/ TIOCB1/ TCLKC-A			
51		P84						
52		P57		WAIT#				TRDATA3
53		P56						TRDATA2
54		P55						TRDATA1

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
55		P54						TRDATA0
56		P83						
57	VSS							
58		P82						TRCLK
59	VCC							
60		P81						TRSYNC#
61		P80						
62	BCLK	P53						
63		P52		RD#				
64		P51		WR1#/BC1#				
65		P50		WR0#/WR#				
66		P77						
67		P76	IRQ14-A					
68		P75						
69		PC7		A23/ CS4#-D/ CS7#-D		TxD5		
70		PC6		A22/ CS6#-D		RxD5		
71		PC5		A21/ CS5#-D		SCK5		
72		PC4		A20				
73		PC3		A19				
74	VCC							
75		PC2		A18				
76	VSS							
77		PC1		A17				
78		PC0		A16				
79		PB7		A15	PO31/ TIOCA11/ TIOCB11			
80		PB6		A14	PO30/ TIOCA11			
81		PB5		A13	PO29/ TIOCA10/ TIOCB10			
82		PB4		A12	PO28/ TIOCA10			
83		PB3		A11	PO27/ TIOCC9/ TIOCD9			
84		PB2		A10	PO26/ TIOCC9			

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
85		PB1		A9	PO25/ TIOCA9/ TIOCB9			
86		P74					ADTRG3#	
87		P73						
88		P72						
89		P71		CS4#-C/ CS5#-C/ CS6#-C/ CS7#-C				
90		P70		CS3#-B			ADTRG2#	
91	VCC							
92		PB0		A8	PO24/ TIOCA9			
93	VSS							
94		PA7		A7	PO23/ TIOCA8/ TIOCB8/ TCLKH			
95		PA6		A6	PO22/ TIOCA8			
96		PA5		A5	PO21/ TIOCA7/ TIOCB7/ TCLKG			
97		PA4		A4	PO20/ TIOCA7			
98		PA3		A3	PO19/ TIOCC6/ TIOCD6/ TCLKF			
99		PA2		A2	PO18/ TIOCC6/ TCLKE			
100		PA1		A1	PO17/ TIOCA6/ TIOCB6			
101		PA0		A0/BC0#	PO16/ TIOCA6			
102		PE7	IRQ7-A	D15				
103		PE6	IRQ6-A	D14				
104		PE5	IRQ5-A	D13				
105		PE4		D12				
106		PE3		D11				
107		PE2		D10				

Pin No. 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Interrupt	External Bus	Timer	Communi-cation	Analog	On-Chip Emulator
108		PE1		D9				
109		PE0		D8				
110		PD7		D7				
111		PD6		D6				
112		PD5		D5				
113		PD4		D4				
114		P64		CS4#-B				
115		P63		CS3#-A/ CS7#-A				
116		P62		CS2#-A/ CS6#-A				
117		P61		CS1#/ CS2#-B/ CS5#-A/ CS6#-B/ CS7#-B				
118		P60		CS0#/ CS4#-A/ CS5#-B				
119		PD3		D3				
120		PD2		D2				
121		PD1		D1				
122		PD0		D0				
123		P97					AN15	
124		P96					AN14	
125		P95					AN13	
126		P94					AN12	
127		P93					AN11	
128		P92					AN10	
129		P91					AN9	
130	VSS							
131		P90					AN8	
132	VCC							
133		P47	IRQ15-B				AN7	
134		P46	IRQ14-B				AN6	
135		P45	IRQ13-B				AN5	
136		P44	IRQ12-B				AN4	
137		P43	IRQ11-B				AN3	
138		P42	IRQ10-B				AN2	
139		P41	IRQ9-B				AN1	
140	VREFL							
141		P40	IRQ8-B				AN0	
142	VREFH							
143	AVCC							
144		P05	IRQ13-A		TMO3	RxD4		TCK

1.5 Pin Functions

Table 1.5 lists the pin functions.

Table 1.5 Pin Functions

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	Input	Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	PLLVCC	Input	Power supply pin for the PLL circuit. Connect it to the system power supply.
	PLLVSS	Input	Ground pin for the PLL circuit
Clock	XTAL	Input	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the system clock for external devices.
Operating mode control	MD0, MD1, MDE	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	EMLE	Input	Input pin to enable on-chip emulator signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
	BSCANP	Input	Input pin to enable boundary-scan signal. When this pin is driven high, the boundary scan is enabled. When the boundary scan is not used, this pin should be driven low.
On-chip emulator	TRST#	Input	On-chip emulator pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TRSYNC	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid.
	TRDATA0 to TRDATA3	Output	These pins output the trace information.
Address bus	A0 to A23*1	Output	Output pins for the address
Data bus	D0 to D15	I/O	Input and output pins for the bidirectional data bus

Classifications	Pin Name	I/O	Description
Bus control	RD#	Output	Strobe signal which indicates that reading from the external address space is in progress.
	WR0#	Output	Strobe signal which indicates that the lower-order byte (D0 to D7) is valid in writing to the external address space, in byte strobe mode.
	WR1#	Output	Strobe signal which indicates that the higher-order byte (D8 to D15) is valid in writing to the external address space, in byte strobe mode.
	WR#	Output	Strobe signal which indicates that writing to the external address space is in progress, in 1-write strobe mode.
	BC0# *1, *2	Output	Strobe signal which indicates that the lower-order byte (D0 to D7) is valid in access to the external address space, in 1-write strobe mode.
	BC1# *2	Output	Strobe signal which indicates that the higher-order byte (D8 to D15) is valid in access to the external address space, in 1-write strobe mode.
	CS0#, CS1# CS2#-A/CS2#-B CS3#-A/CS3#-B CS4#-A/CS4#-B/ CS4#-C/CS4#-D CS5#-A/CS5#-B/ CS5#-C/CS5#-D CS6#-A/CS6#-B/ CS6#-C/CS6#-D CS7#-A/CS7#-B/ CS7#-C/CS7#-D	Output	Select signals for areas 0 to 7
	WAIT#	Input	Requests wait cycles in access to the external address space

Classifications	Pin Name	I/O	Description
Interrupt	NMI	Input	Non-maskable interrupt request signal
	IRQ0-A/IRQ0-B IRQ1-A/IRQ1-B IRQ2-A/IRQ2-B IRQ3-A/IRQ3-B IRQ4-A/IRQ4-B IRQ5-A/IRQ5-B IRQ6-A/IRQ6-B IRQ7-A/IRQ7-B IRQ8-A/IRQ8-B IRQ9-A/IRQ9-B IRQ10-A/IRQ10-B IRQ11-A/IRQ11-B IRQ12-A/IRQ12-B IRQ13-A/IRQ13-B IRQ14-A/IRQ14-B IRQ15-A/IRQ15-B	Input	Maskable request signals
16-bit timer pulse unit	TIOCA0, TIOCB0 TIOCC0, TIOCD0	I/O	Signals for TGRA0 to TGRD0. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA1, TIOCB1	I/O	Signals for TGRA1 and TGRB1. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA2, TIOCB2	I/O	Signals for TGRA2 and TGRB2. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA3, TIOCB3 TIOCC3, TIOCD3	I/O	Signals for TGRA3 to TGRD3. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA4, TIOCB4	I/O	Signals for TGRA4 and TGRB4. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA5, TIOCB5	I/O	Signals for TGRA5 and TGRB5. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA6, TIOCB6 TIOCC6, TIOCD6	I/O	Signals for TGRA6 to TGRD6. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA7, TIOCB7	I/O	Signals for TGRA7 and TGRB7. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA8, TIOCB8	I/O	Signals for TGRA8 and TGRB8. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA9, TIOCB9 TIOCC9, TIOCD9	I/O	Signals for TGRA9 to TGRD9. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA10, TIOCB10	I/O	Signals for TGRA10 and TGRB10. These pins are used as input capture inputs, output compare outputs, or PWM outputs.
	TIOCA11, TIOCB11	I/O	Signals for TGRA11 and TGRB11. These pins are used as input capture inputs, output compare outputs, or PWM outputs.

Classifications	Pin Name	I/O	Description
16-bit timer pulse unit	TCLKA-A/TCLKA-B TCLKB-A/TCLKB-B TCLKC-A/TCLKC-B TCLKD-A/TCLKD-B TCLKE, TCLKF TCLKG, TCLKH	Input	Input pins for external clock signals
Programmable pulse generator	PO0 to PO31	Output	Output pins for the pulse signals
8-bit timer	TMO0 to TMO3	Output	Output pins for the compare match signals
	TMCI0 to TMCI3	Input	Input pins for the external clock signals that drive for the counters
	TMRI0 to TMRI3	Input	Input pins for the counter-reset signals
Watchdog timer	WDTOVF#	Output	Output pin for the counter-overflow signal in watchdog-timer mode
Serial communication interface	TxD0, TxD1, TxD2, TxD3, TxD4, TxD5, TxD6	Output	Output pins for data transmission
	RxD0, RxD1, RxD2, RxD3, RxD4, RxD5, RxD6	Input	Input pins for data reception
	SCK0, SCK1, SCK2, SCK3, SCK4, SCK5, SCK6	I/O	Input/output pins for clock signals
I^2C bus interface	SCL0, SCL1	I/O	Input/output pins for RIIC clocks. Bus can be directly driven by the NMOS open drain output.
	SDA0, SDA1	I/O	Input/output pins for RIIC data. Bus can be directly driven by the NMOS open drain output.
A/D converter	AN0 to AN15	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0# to ADTRG3#	Input	Input pins for the external trigger signals that start the A/D conversion
D/A converter	DA0, DA1	Output	Output pins for the analog signals from the D/A converter

Classifications	Pin Name	I/O	Description
Analog power supply	AVCC	Input	Analog power supply pin for the A/D and D/A converters. When the A/D and D/A converters are not in use, connect this pin to the system power supply.
	AVSS	Input	Ground pin for the A/D and D/A converters. Connect this pin to the system power supply (0 V).
	VREFH	Input	Reference power supply pin for the A/D and D/A converters. When the A/D and D/A converters are not in use, connect this pin to the system power supply.
	VREFL	Input	Reference ground pin for the A/D and D/A converters. Make sure to connect this pin to the analog reference power supply (0 V). When the A/D and D/A converters are not in use, connect this pin to the system power supply (0 V). For details, see section 23.6.7, Ranges of Settings for Analog Power Supply and Other Pins.
I/O ports	P00 to P05	I/O	6-bit input/output pins
	P10 to P17	I/O	8-bit input/output pins
	P20 to P27	I/O	8-bit input/output pins
	P30 to P37	I/O	8-bit input/output pins
	P40 to P47	I/O	8-bit input/output pins
	P50 to P57	I/O	8-bit input/output pins. (P53 is an input-only pin.)
	P60 to P67	I/O	8-bit input/output pins
	P70 to P77	I/O	8-bit input/output pins
	P80 to P86	I/O	7-bit input/output pins
	P90 to P97	I/O	8-bit input/output pins
	PA0 to PA7	I/O	8-bit input/output pins
	PB0 to PB7	I/O	8-bit input/output pins
	PC0 to PC7	I/O	8-bit input/output pins
	PD0 to PD7	I/O	8-bit input/output pins
	PE0 to PE7	I/O	8-bit input/output pins
	PF0 to PF6	I/O	7-bit input/output pins
	PG0 to PG7	I/O	8-bit input/output pins
	PH0 to PH7	I/O	8-bit input/output pins

Note 1: The A0 and BC0# pin functions are multiplexed on the same pin: the A0 pin is valid in byte-write mode and the BC0# pin becomes valid in single write-strobe mode. The setting for an eight-bit external bus width is prohibited in single write-strobe mode. For other multiplexed pin functions, refer to section 14, I/O Ports.

Note 2: The BC0# and BC1# signals are valid in both reading and writing.

2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

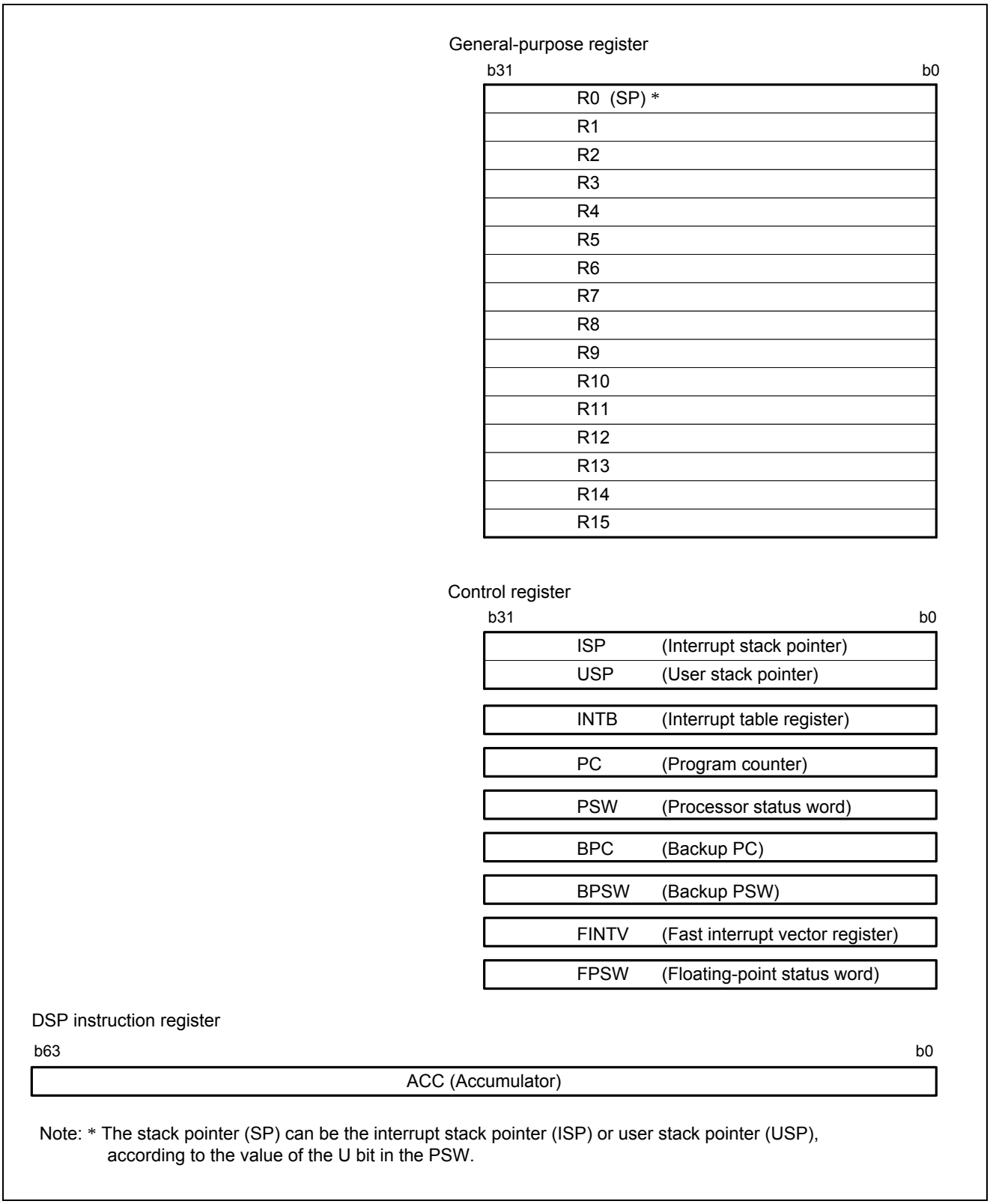


Figure 2.1 Register Set of the CPU

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers.

R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).

Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.

The FINTV specifies a branch destination address when a fast interrupt has been generated.

(8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.

When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the corresponding Cj flag indicates the source of the exception within the exception handling routine. If the exception handling is masked (Ej = 0), check the Fj flag at the end of a series of processing whether an exception is generated or not. The Fj flag is the accumulation type flag (j = X, U, Z, O, or V).

(9) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.

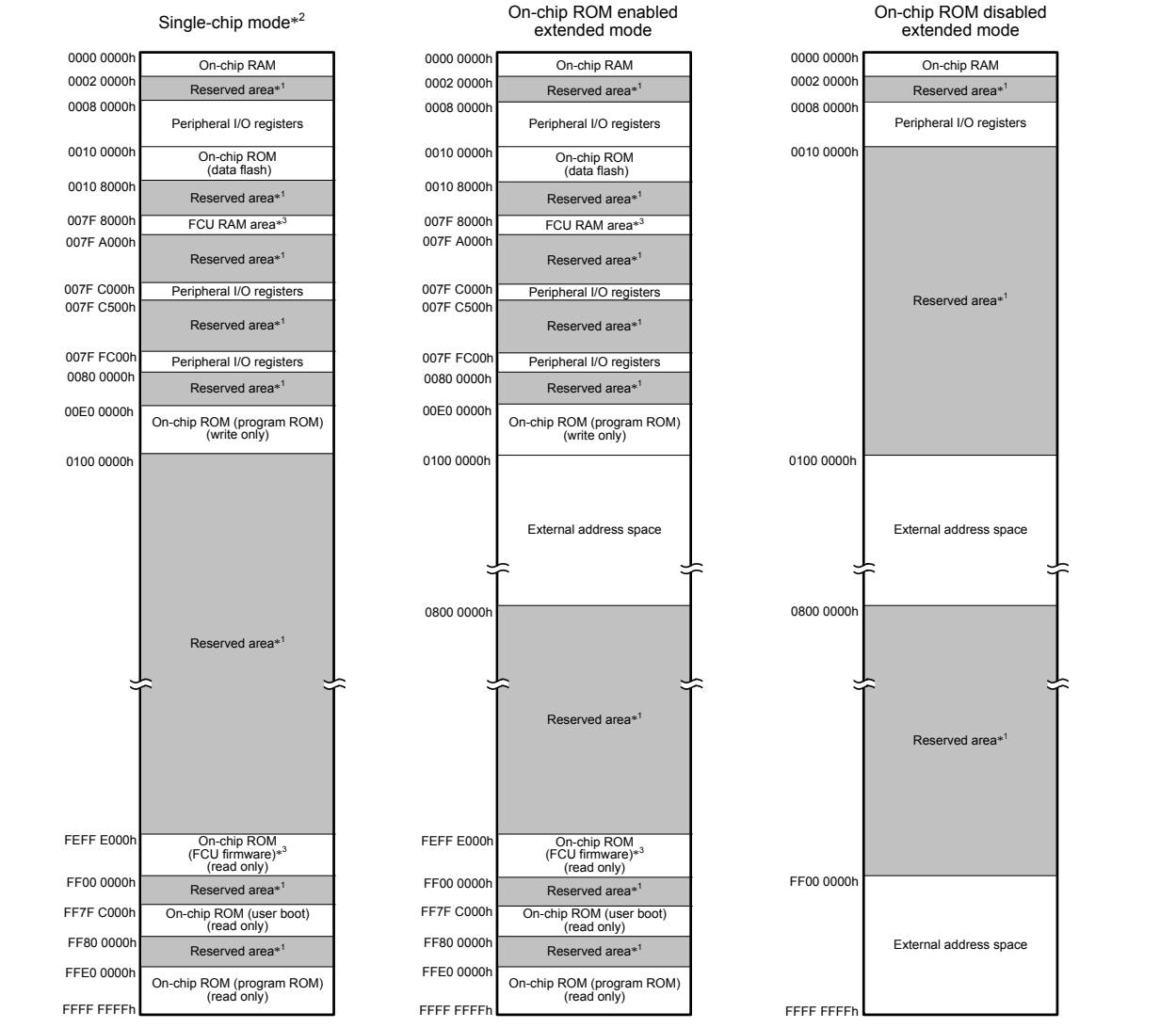
Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

3. Address Space

3.1 Address Space

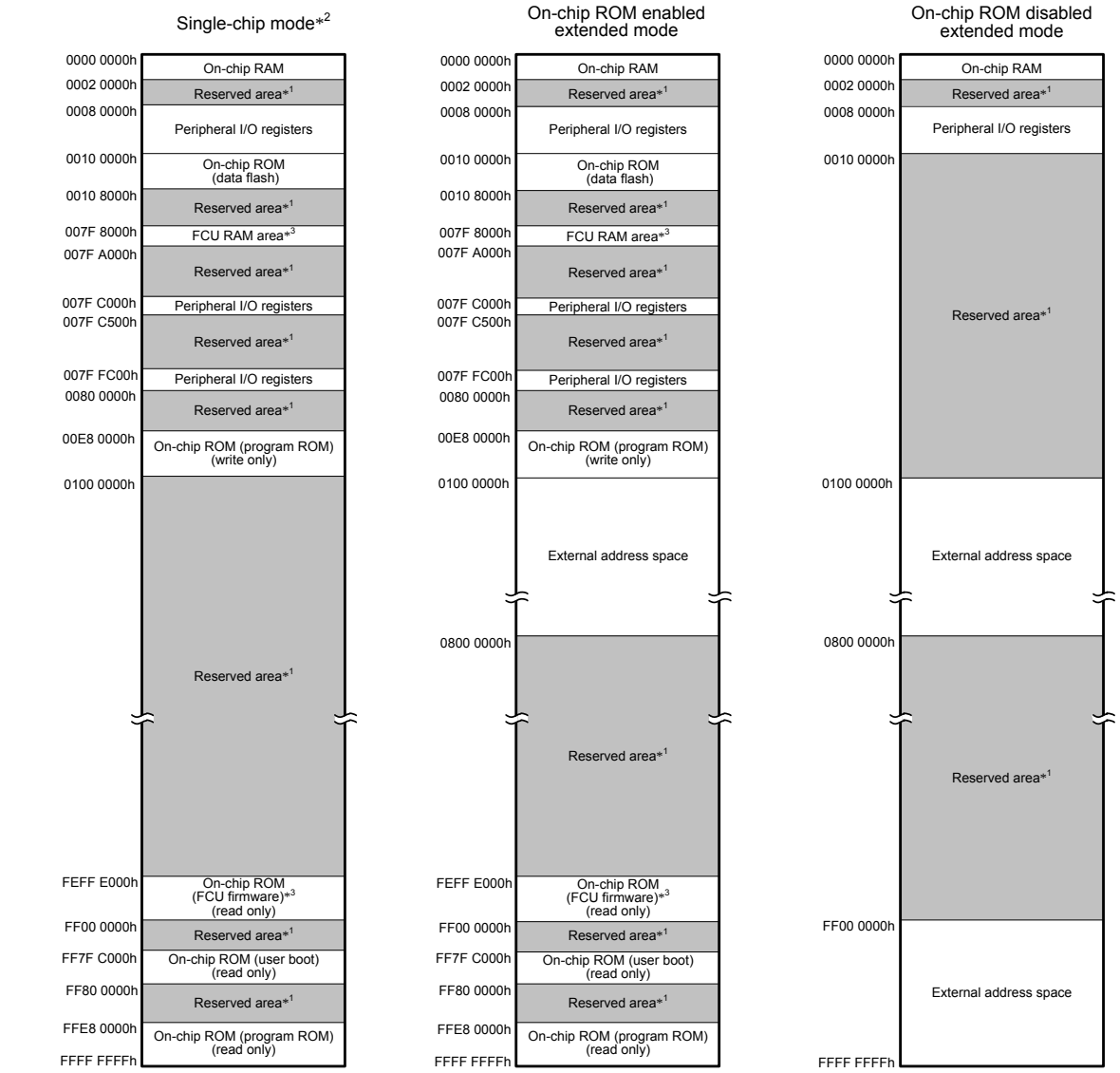
This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figures 3.1 to 3.4 show the memory maps in the respective operating modes of each product. Accessible areas will differ according to the operating mode and states of control bits.



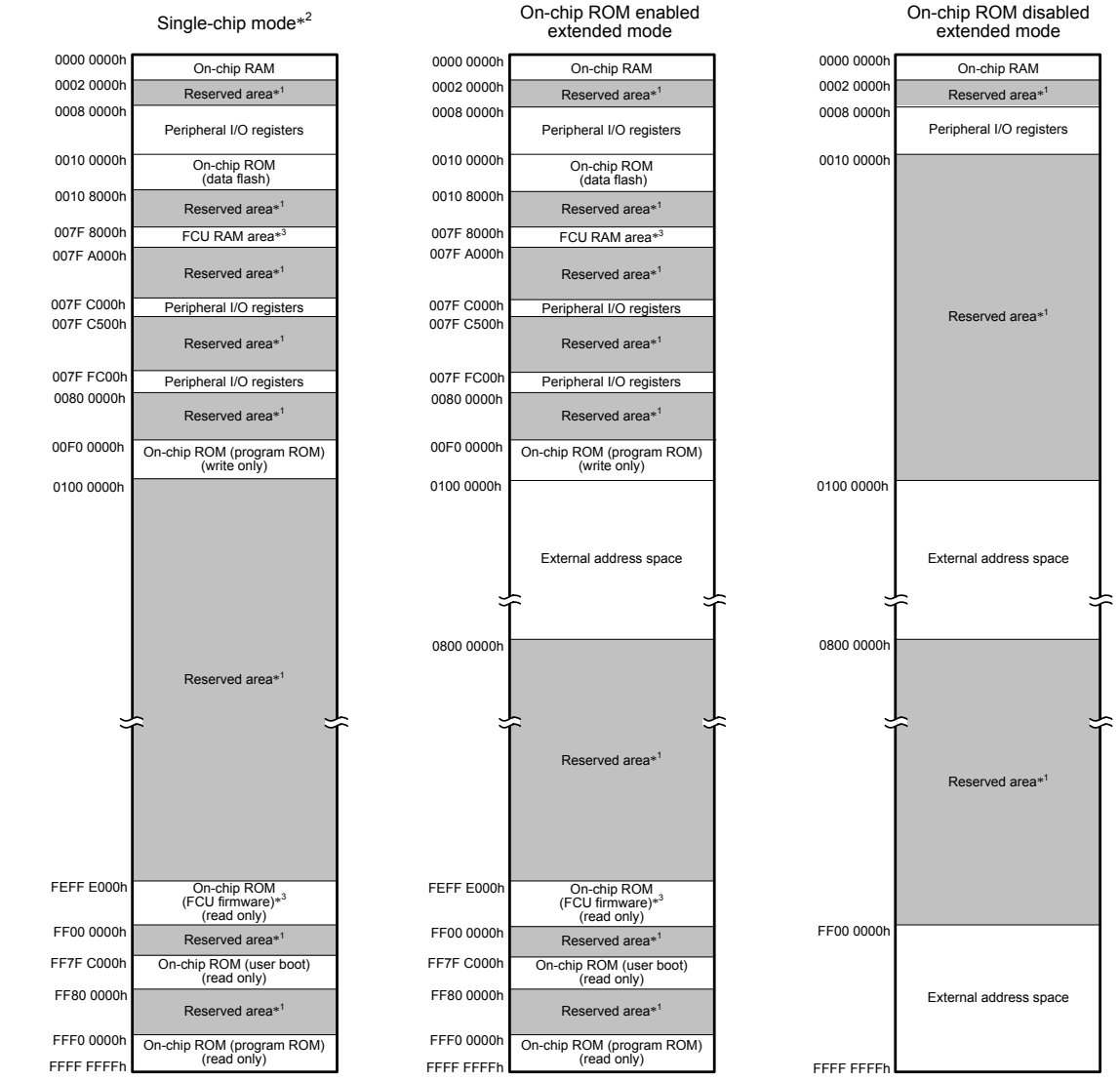
Notes: 1. A reserved area should not be accessed.
2. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
3. For details on the FCU, see section 26, ROM (Flash Memory for Code Storage) and section 27, Data Flash (Flash Memory for Data Storage) in the User's manual: Hardware.

Figure 3.1 Memory Map of the R5F56108



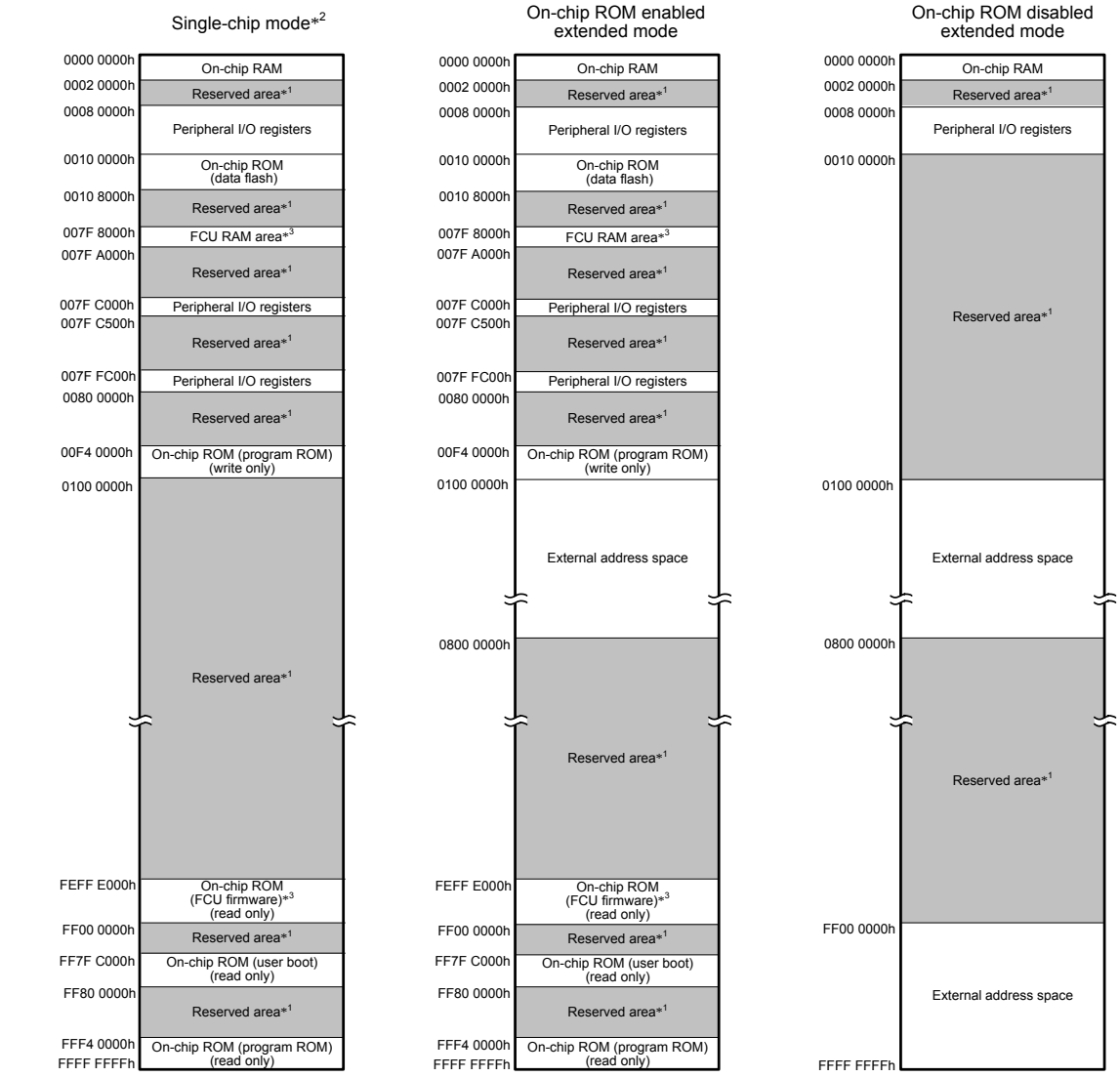
Notes: 1. A reserved area should not be accessed.
2. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
3. For details on the FCU, see section 26, ROM (Flash Memory for Code Storage) and section 27, Data Flash (Flash Memory for Data Storage) in the User's manual: Hardware.

Figure 3.2 Memory Map of the R5F56107



Notes: 1. A reserved area should not be accessed.
2. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
3. For details on the FCU, see section 26, ROM (Flash Memory for Code Storage) and section 27, Data Flash (Flash Memory for Data Storage) in the User's manual: Hardware.

Figure 3.3 Memory Map of the R5F56106



Notes: 1. A reserved area should not be accessed.
2. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
3. For details on the FCU, see section 26, ROM (Flash Memory for Code Storage) and section 27, Data Flash (Flash Memory for Data Storage) in the User's manual: Hardware.

Figure 3.4 Memory Map of the R5F56104

3.2 External Address Space

The external address space is divided into up to 8 areas, each corresponding to the CSi# signal output from a CSi# (i = 0 to 7) pin. Figure 4.5 shows the address ranges corresponding to the individual CSi# signals (CSi areas, i = 0 to 7) in on-chip ROM disabled external extended mode.

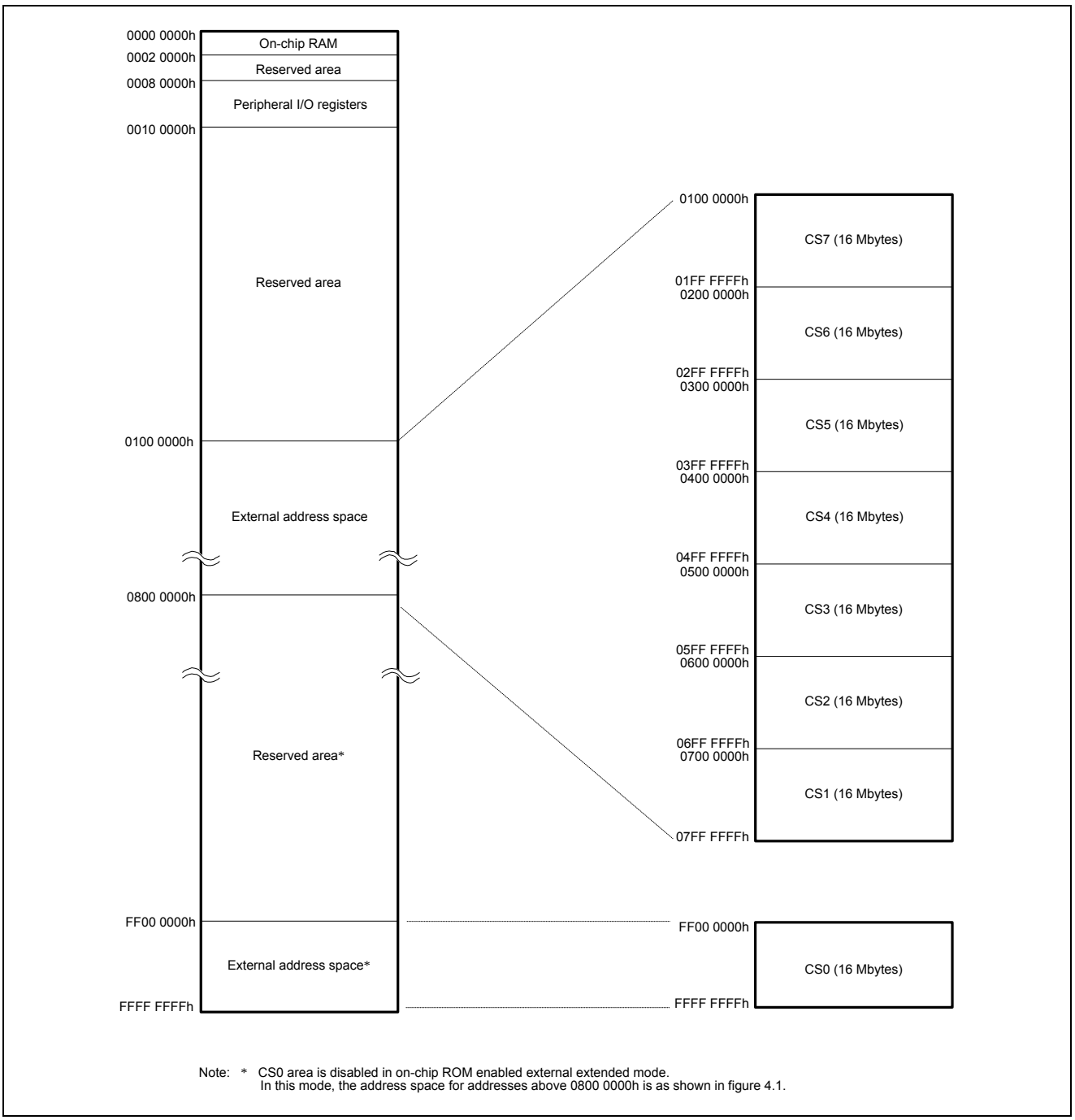


Figure 3.5 Correspondence between External Address Spaces and CSi Areas (In On-Chip ROM Disabled External Extended Mode)

4. I/O Registers

Table 4.1 List of I/O Registers (Address Order)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16	3 ICLK
0008 0002h	SYSTEM	Mode status register	MDSR	16	16	3 ICLK
0008 0006h	SYSTEM	System control register 0	SYSCR0	16	16	3 ICLK
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32	3 ICLK
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32	3 ICLK
0008 1300h	BSC	Bus error source clear register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus error monitor enable register	BEREN	8	8	2 ICLK
0008 1306h	BSC	Bus error interrupt enable register	BERIE	8	8	2 ICLK
0008 2000h	DMAC0	DMA current transfer source address register	DMCSA	32	32	4 to 5 ICLK
0008 2004h	DMAC0	DMA current transfer destination address register	DMCDA	32	32	4 to 5 ICLK
0008 2008h	DMAC0	DMA current transfer byte count register	DMCBC	32	32	4 to 5 ICLK
0008 200Ch	DMAC0	DMA mode register	DMMOD	32	32	4 to 5 ICLK
0008 2010h	DMAC1	DMA current transfer source address register	DMCSA	32	32	4 to 5 ICLK
0008 2014h	DMAC1	DMA current transfer destination address register	DMCDA	32	32	4 to 5 ICLK
0008 2018h	DMAC1	DMA current transfer byte count register	DMCBC	32	32	4 to 5 ICLK
0008 201Ch	DMAC1	DMA mode register	DMMOD	32	32	4 to 5 ICLK
0008 2020h	DMAC2	DMA current transfer source address register	DMCSA	32	32	4 to 5 ICLK
0008 2024h	DMAC2	DMA current transfer destination address register	DMCDA	32	32	4 to 5 ICLK
0008 2028h	DMAC2	DMA current transfer byte count register	DMCBC	32	32	4 to 5 ICLK
0008 202Ch	DMAC2	DMA mode register	DMMOD	32	32	4 to 5 ICLK
0008 2030h	DMAC3	DMA current transfer source address register	DMCSA	32	32	4 to 5 ICLK
0008 2034h	DMAC3	DMA current transfer destination address register	DMCDA	32	32	4 to 5 ICLK
0008 2038h	DMAC3	DMA current transfer byte count register	DMCBC	32	32	4 to 5 ICLK
0008 203Ch	DMAC3	DMA mode register	DMMOD	32	32	4 to 5 ICLK
0008 2200h	DMAC0	DMA reload transfer source address register	DMRSA	32	32	4 to 5 ICLK *8
0008 2204h	DMAC0	DMA reload transfer destination address register	DMRDA	32	32	4 to 5 ICLK *8
0008 2208h	DMAC0	DMA reload transfer byte count register	DMRBC	32	32	4 to 5 ICLK *8
0008 2210h	DMAC1	DMA reload transfer source address register	DMRSA	32	32	4 to 5 ICLK *8
0008 2214h	DMAC1	DMA reload transfer destination address register	DMRDA	32	32	4 to 5 ICLK *8
0008 2218h	DMAC1	DMA reload transfer byte count register	DMRBC	32	32	4 to 5 ICLK *8
0008 2220h	DMAC2	DMA reload transfer source address register	DMRSA	32	32	4 to 5 ICLK *8
0008 2224h	DMAC2	DMA reload transfer destination address register	DMRDA	32	32	4 to 5 ICLK *8
0008 2228h	DMAC2	DMA reload transfer byte count register	DMRBC	32	32	4 to 5 ICLK *8
0008 2230h	DMAC3	DMA reload transfer source address register	DMRSA	32	32	4 to 5 ICLK *8
0008 2234h	DMAC3	DMA reload transfer destination address register	DMRDA	32	32	4 to 5 ICLK *8
0008 2238h	DMAC3	DMA reload transfer byte count register	DMRBC	32	32	4 to 5 ICLK *8

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 2400h	DMAC0	DMA control register A	DMCRA	32	32	3 ICLK
0008 2404h	DMAC0	DMA control register B	DMCRB	8	8	3 ICLK
0008 2405h	DMAC0	DMA control register C	DMCRC	8	8	3 ICLK
0008 2406h	DMAC0	DMA control register D	DMCRD	8	8	3 ICLK
0008 2407h	DMAC0	DMA control register E	DMCRE	8	8	3 ICLK
0008 2408h	DMAC1	DMA control register A	DMCRA	32	32	3 ICLK
0008 240Ch	DMAC1	DMA control register B	DMCRB	8	8	3 ICLK
0008 240Dh	DMAC1	DMA control register C	DMCRC	8	8	3 ICLK
0008 240Eh	DMAC1	DMA control register D	DMCRD	8	8	3 ICLK
0008 240Fh	DMAC1	DMA control register E	DMCRE	8	8	3 ICLK
0008 2410h	DMAC2	DMA control register A	DMCRA	32	32	3 ICLK
0008 2414h	DMAC2	DMA control register B	DMCRB	8	8	3 ICLK
0008 2415h	DMAC2	DMA control register C	DMCRC	8	8	3 ICLK
0008 2416h	DMAC2	DMA control register D	DMCRD	8	8	3 ICLK
0008 2417h	DMAC2	DMA control register E	DMCRE	8	8	3 ICLK
0008 2418h	DMAC3	DMA control register A	DMCRA	32	32	3 ICLK
0008 241Ch	DMAC3	DMA control register B	DMCRB	8	8	3 ICLK
0008 241Dh	DMAC3	DMA control register C	DMCRC	8	8	3 ICLK
0008 241Eh	DMAC3	DMA control register D	DMCRD	8	8	3 ICLK
0008 241Fh	DMAC3	DMA control register E	DMCRE	8	8	3 ICLK
0008 2502h	DMAC common	DMA start control register	DMSCNT	8	8	3 ICLK
0008 250Bh	DMAC common	DMA interrupt control register	DMICNT	8	8	3 ICLK
0008 2517h	DMAC common	DMA transfer end detect register	DMEDET	8	8	3 ICLK
0008 251Bh	DMAC common	DMA arbitration status register	DMASTS	8	8	3 ICLK
0008 3002h	BSC	CS0 mode register	CS0MOD	16	16	1 to 2 BCLK *7
0008 3004h	BSC	CS0 wait control register 1	CS0WCNT1	32	32	1 to 2 BCLK *7
0008 3008h	BSC	CS0 wait control register 2	CS0WCNT2	32	32	1 to 2 BCLK *7
0008 3012h	BSC	CS1 mode register	CS1MOD	16	16	1 to 2 BCLK *7
0008 3014h	BSC	CS1 wait control register 1	CS1WCNT1	32	32	1 to 2 BCLK *7
0008 3018h	BSC	CS1 wait control register 2	CS1WCNT2	32	32	1 to 2 BCLK *7
0008 3022h	BSC	CS2 mode register	CS2MOD	16	16	1 to 2 BCLK *7
0008 3024h	BSC	CS2 wait control register 1	CS2WCNT1	32	32	1 to 2 BCLK *7
0008 3028h	BSC	CS2 wait control register 2	CS2WCNT2	32	32	1 to 2 BCLK *7
0008 3032h	BSC	CS3 mode register	CS3MOD	16	16	1 to 2 BCLK *7
0008 3034h	BSC	CS3 wait control register 1	CS3WCNT1	32	32	1 to 2 BCLK *7
0008 3038h	BSC	CS3 wait control register 2	CS3WCNT2	32	32	1 to 2 BCLK *7
0008 3042h	BSC	CS4 mode register	CS4MOD	16	16	1 to 2 BCLK *7
0008 3044h	BSC	CS4 wait control register 1	CS4WCNT1	32	32	1 to 2 BCLK *7
0008 3048h	BSC	CS4 wait control register 2	CS4WCNT2	32	32	1 to 2 BCLK *7
0008 3052h	BSC	CS5 mode register	CS5MOD	16	16	1 to 2 BCLK *7
0008 3054h	BSC	CS5 wait control register 1	CS5WCNT1	32	32	1 to 2 BCLK *7
0008 3058h	BSC	CS5 wait control register 2	CS5WCNT2	32	32	1 to 2 BCLK *7
0008 3062h	BSC	CS6 mode register	CS6MOD	16	16	1 to 2 BCLK *7
0008 3064h	BSC	CS6 wait control register 1	CS6WCNT1	32	32	1 to 2 BCLK *7
0008 3068h	BSC	CS6 wait control register 2	CS6WCNT2	32	32	1 to 2 BCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 3072h	BSC	CS7 mode register	CS7MOD	16	16	1 to 2 BCLK *7
0008 3074h	BSC	CS7 wait control register 1	CS7WCNT1	32	32	1 to 2 BCLK *7
0008 3078h	BSC	CS7 wait control register 2	CS7WCNT2	32	32	1 to 2 BCLK *7
0008 3802h	BSC	CS0 control register	CS0CNT	16	16	1 to 2 BCLK *7
0008 380Ah	BSC	CS0 recovery cycle register	CS0REC	16	16	1 to 2 BCLK *7
0008 3812h	BSC	CS1 control register	CS1CNT	16	16	1 to 2 BCLK *7
0008 381Ah	BSC	CS1 recovery cycle register	CS1REC	16	16	1 to 2 BCLK *7
0008 3822h	BSC	CS2 control register	CS2CNT	16	16	1 to 2 BCLK *7
0008 382Ah	BSC	CS2 recovery cycle register	CS2REC	16	16	1 to 2 BCLK *7
0008 3832h	BSC	CS3 control register	CS3CNT	16	16	1 to 2 BCLK *7
0008 383Ah	BSC	CS3 recovery cycle register	CS3REC	16	16	1 to 2 BCLK *7
0008 3842h	BSC	CS4 control register	CS4CNT	16	16	1 to 2 BCLK *7
0008 384Ah	BSC	CS4 recovery cycle register	CS4REC	16	16	1 to 2 BCLK *7
0008 3852h	BSC	CS5 control register	CS5CNT	16	16	1 to 2 BCLK *7
0008 385Ah	BSC	CS5 recovery cycle register	CS5REC	16	16	1 to 2 BCLK *7
0008 3862h	BSC	CS6 control register	CS6CNT	16	16	1 to 2 BCLK *7
0008 386Ah	BSC	CS6 recovery cycle register	CS6REC	16	16	1 to 2 BCLK *7
0008 3872h	BSC	CS7 control register	CS7CNT	16	16	1 to 2 BCLK *7
0008 387Ah	BSC	CS7 recovery cycle register	CS7REC	16	16	1 to 2 BCLK *7
0008 7010h	ICU	Interrupt request register 016	IR016	8	8	2 ICLK
0008 7015h	ICU	Interrupt request register 021	IR021	8	8	2 ICLK
0008 7017h	ICU	Interrupt request register 023	IR023	8	8	2 ICLK
0008 701Ch	ICU	Interrupt request register 028	IR028	8	8	2 ICLK
0008 701Dh	ICU	Interrupt request register 029	IR029	8	8	2 ICLK
0008 701Eh	ICU	Interrupt request register 030	IR030	8	8	2 ICLK
0008 701Fh	ICU	Interrupt request register 031	IR031	8	8	2 ICLK
0008 7040h	ICU	Interrupt request register 064	IR064	8	8	2 ICLK
0008 7041h	ICU	Interrupt request register 065	IR065	8	8	2 ICLK
0008 7042h	ICU	Interrupt request register 066	IR066	8	8	2 ICLK
0008 7043h	ICU	Interrupt request register 067	IR067	8	8	2 ICLK
0008 7044h	ICU	Interrupt request register 068	IR068	8	8	2 ICLK
0008 7045h	ICU	Interrupt request register 069	IR069	8	8	2 ICLK
0008 7046h	ICU	Interrupt request register 070	IR070	8	8	2 ICLK
0008 7047h	ICU	Interrupt request register 071	IR071	8	8	2 ICLK
0008 7048h	ICU	Interrupt request register 072	IR072	8	8	2 ICLK
0008 7049h	ICU	Interrupt request register 073	IR073	8	8	2 ICLK
0008 704Ah	ICU	Interrupt request register 074	IR074	8	8	2 ICLK
0008 704Bh	ICU	Interrupt request register 075	IR075	8	8	2 ICLK
0008 704Ch	ICU	Interrupt request register 076	IR076	8	8	2 ICLK
0008 704Dh	ICU	Interrupt request register 077	IR077	8	8	2 ICLK
0008 704Eh	ICU	Interrupt request register 078	IR078	8	8	2 ICLK
0008 704Fh	ICU	Interrupt request register 079	IR079	8	8	2 ICLK
0008 7060h	ICU	Interrupt request register 096	IR096	8	8	2 ICLK
0008 7062h	ICU	Interrupt request register 098	IR098	8	8	2 ICLK
0008 7063h	ICU	Interrupt request register 099	IR099	8	8	2 ICLK

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7064h	ICU	Interrupt request register 100	IR100	8	8	2 ICLK
0008 7065h	ICU	Interrupt request register 101	IR101	8	8	2 ICLK
0008 7068h	ICU	Interrupt request register 104	IR104	8	8	2 ICLK
0008 7069h	ICU	Interrupt request register 105	IR105	8	8	2 ICLK
0008 706Ah	ICU	Interrupt request register 106	IR106	8	8	2 ICLK
0008 706Bh	ICU	Interrupt request register 107	IR107	8	8	2 ICLK
0008 706Ch	ICU	Interrupt request register 108	IR108	8	8	2 ICLK
0008 706Fh	ICU	Interrupt request register 111	IR111	8	8	2 ICLK
0008 7070h	ICU	Interrupt request register 112	IR112	8	8	2 ICLK
0008 7073h	ICU	Interrupt request register 115	IR115	8	8	2 ICLK
0008 7074h	ICU	Interrupt request register 116	IR116	8	8	2 ICLK
0008 7075h	ICU	Interrupt request register 117	IR117	8	8	2 ICLK
0008 7076h	ICU	Interrupt request register 118	IR118	8	8	2 ICLK
0008 7078h	ICU	Interrupt request register 120	IR120	8	8	2 ICLK
0008 7079h	ICU	Interrupt request register 121	IR121	8	8	2 ICLK
0008 707Ah	ICU	Interrupt request register 122	IR122	8	8	2 ICLK
0008 707Bh	ICU	Interrupt request register 123	IR123	8	8	2 ICLK
0008 707Ch	ICU	Interrupt request register 124	IR124	8	8	2 ICLK
0008 707Dh	ICU	Interrupt request register 125	IR125	8	8	2 ICLK
0008 707Eh	ICU	Interrupt request register 126	IR126	8	8	2 ICLK
0008 707Fh	ICU	Interrupt request register 127	IR127	8	8	2 ICLK
0008 7080h	ICU	Interrupt request register 128	IR128	8	8	2 ICLK
0008 7083h	ICU	Interrupt request register 131	IR131	8	8	2 ICLK
0008 7084h	ICU	Interrupt request register 132	IR132	8	8	2 ICLK
0008 7085h	ICU	Interrupt request register 133	IR133	8	8	2 ICLK
0008 7086h	ICU	Interrupt request register 134	IR134	8	8	2 ICLK
0008 7088h	ICU	Interrupt request register 136	IR136	8	8	2 ICLK
0008 7089h	ICU	Interrupt request register 137	IR137	8	8	2 ICLK
0008 708Ah	ICU	Interrupt request register 138	IR138	8	8	2 ICLK
0008 708Bh	ICU	Interrupt request register 139	IR139	8	8	2 ICLK
0008 708Ch	ICU	Interrupt request register 140	IR140	8	8	2 ICLK
0008 708Dh	ICU	Interrupt request register 141	IR141	8	8	2 ICLK
0008 708Eh	ICU	Interrupt request register 142	IR142	8	8	2 ICLK
0008 7091h	ICU	Interrupt request register 145	IR145	8	8	2 ICLK
0008 7092h	ICU	Interrupt request register 146	IR146	8	8	2 ICLK
0008 7095h	ICU	Interrupt request register 149	IR149	8	8	2 ICLK
0008 7096h	ICU	Interrupt request register 150	IR150	8	8	2 ICLK
0008 7097h	ICU	Interrupt request register 151	IR151	8	8	2 ICLK
0008 7098h	ICU	Interrupt request register 152	IR152	8	8	2 ICLK
0008 709Ah	ICU	Interrupt request register 154	IR154	8	8	2 ICLK
0008 709Bh	ICU	Interrupt request register 155	IR155	8	8	2 ICLK
0008 709Ch	ICU	Interrupt request register 156	IR156	8	8	2 ICLK
0008 709Dh	ICU	Interrupt request register 157	IR157	8	8	2 ICLK
0008 709Eh	ICU	Interrupt request register 158	IR158	8	8	2 ICLK
0008 709Fh	ICU	Interrupt request register 159	IR159	8	8	2 ICLK

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 70A0h	ICU	Interrupt request register 160	IR160	8	8	2 ICLK
0008 70A1h	ICU	Interrupt request register 161	IR161	8	8	2 ICLK
0008 70A2h	ICU	Interrupt request register 162	IR162	8	8	2 ICLK
0008 70A5h	ICU	Interrupt request register 165	IR165	8	8	2 ICLK
0008 70A6h	ICU	Interrupt request register 166	IR166	8	8	2 ICLK
0008 70A7h	ICU	Interrupt request register 167	IR167	8	8	2 ICLK
0008 70A8h	ICU	Interrupt request register 168	IR168	8	8	2 ICLK
0008 70AAh	ICU	Interrupt request register 170	IR170	8	8	2 ICLK
0008 70ABh	ICU	Interrupt request register 171	IR171	8	8	2 ICLK
0008 70AEh	ICU	Interrupt request register 174	IR174	8	8	2 ICLK
0008 70AFh	ICU	Interrupt request register 175	IR175	8	8	2 ICLK
0008 70B0h	ICU	Interrupt request register 176	IR176	8	8	2 ICLK
0008 70B1h	ICU	Interrupt request register 177	IR177	8	8	2 ICLK
0008 70B2h	ICU	Interrupt request register 178	IR178	8	8	2 ICLK
0008 70B3h	ICU	Interrupt request register 179	IR179	8	8	2 ICLK
0008 70B4h	ICU	Interrupt request register 180	IR180	8	8	2 ICLK
0008 70B5h	ICU	Interrupt request register 181	IR181	8	8	2 ICLK
0008 70B6h	ICU	Interrupt request register 182	IR182	8	8	2 ICLK
0008 70B7h	ICU	Interrupt request register 183	IR183	8	8	2 ICLK
0008 70B8h	ICU	Interrupt request register 184	IR184	8	8	2 ICLK
0008 70B9h	ICU	Interrupt request register 185	IR185	8	8	2 ICLK
0008 70C6h	ICU	Interrupt request register 198	IR198	8	8	2 ICLK
0008 70C7h	ICU	Interrupt request register 199	IR199	8	8	2 ICLK
0008 70C8h	ICU	Interrupt request register 200	IR200	8	8	2 ICLK
0008 70C9h	ICU	Interrupt request register 201	IR201	8	8	2 ICLK
0008 70D6h	ICU	Interrupt request register 214	IR214	8	8	2 ICLK
0008 70D7h	ICU	Interrupt request register 215	IR215	8	8	2 ICLK
0008 70D8h	ICU	Interrupt request register 216	IR216	8	8	2 ICLK
0008 70D9h	ICU	Interrupt request register 217	IR217	8	8	2 ICLK
0008 70DAh	ICU	Interrupt request register 218	IR218	8	8	2 ICLK
0008 70DBh	ICU	Interrupt request register 219	IR219	8	8	2 ICLK
0008 70DCh	ICU	Interrupt request register 220	IR220	8	8	2 ICLK
0008 70DDh	ICU	Interrupt request register 221	IR221	8	8	2 ICLK
0008 70DEh	ICU	Interrupt request register 222	IR222	8	8	2 ICLK
0008 70DFh	ICU	Interrupt request register 223	IR223	8	8	2 ICLK
0008 70E0h	ICU	Interrupt request register 224	IR224	8	8	2 ICLK
0008 70E1h	ICU	Interrupt request register 225	IR225	8	8	2 ICLK
0008 70E2h	ICU	Interrupt request register 226	IR226	8	8	2 ICLK
0008 70E3h	ICU	Interrupt request register 227	IR227	8	8	2 ICLK
0008 70E4h	ICU	Interrupt request register 228	IR228	8	8	2 ICLK
0008 70E5h	ICU	Interrupt request register 229	IR229	8	8	2 ICLK
0008 70E6h	ICU	Interrupt request register 230	IR230	8	8	2 ICLK
0008 70E7h	ICU	Interrupt request register 231	IR231	8	8	2 ICLK
0008 70E8h	ICU	Interrupt request register 232	IR232	8	8	2 ICLK
0008 70E9h	ICU	Interrupt request register 233	IR233	8	8	2 ICLK

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 70EAh	ICU	Interrupt request register 234	IR234	8	8	2 ICLK
0008 70EBh	ICU	Interrupt request register 235	IR235	8	8	2 ICLK
0008 70ECh	ICU	Interrupt request register 236	IR236	8	8	2 ICLK
0008 70EDh	ICU	Interrupt request register 237	IR237	8	8	2 ICLK
0008 70EEh	ICU	Interrupt request register 238	IR238	8	8	2 ICLK
0008 70EFh	ICU	Interrupt request register 239	IR239	8	8	2 ICLK
0008 70F0h	ICU	Interrupt request register 240	IR240	8	8	2 ICLK
0008 70F1h	ICU	Interrupt request register 241	IR241	8	8	2 ICLK
0008 70F6h	ICU	Interrupt request register 246	IR246	8	8	2 ICLK
0008 70F7h	ICU	Interrupt request register 247	IR247	8	8	2 ICLK
0008 70F8h	ICU	Interrupt request register 248	IR248	8	8	2 ICLK
0008 70F9h	ICU	Interrupt request register 249	IR249	8	8	2 ICLK
0008 70FAh	ICU	Interrupt request register 250	IR250	8	8	2 ICLK
0008 70FBh	ICU	Interrupt request register 251	IR251	8	8	2 ICLK
0008 70FCh	ICU	Interrupt request register 252	IR252	8	8	2 ICLK
0008 70FDh	ICU	Interrupt request register 253	IR253	8	8	2 ICLK
0008 711Ch	ICU	Interrupt request destination setting register 028	ISELR028	8	8	2 ICLK
0008 711Dh	ICU	Interrupt request destination setting register 029	ISELR029	8	8	2 ICLK
0008 711Eh	ICU	Interrupt request destination setting register 030	ISELR030	8	8	2 ICLK
0008 711Fh	ICU	Interrupt request destination setting register 031	ISELR031	8	8	2 ICLK
0008 7140h	ICU	Interrupt request destination setting register 064	ISELR064	8	8	2 ICLK
0008 7141h	ICU	Interrupt request destination setting register 065	ISELR065	8	8	2 ICLK
0008 7142h	ICU	Interrupt request destination setting register 066	ISELR066	8	8	2 ICLK
0008 7143h	ICU	Interrupt request destination setting register 067	ISELR067	8	8	2 ICLK
0008 7144h	ICU	Interrupt request destination setting register 068	ISELR068	8	8	2 ICLK
0008 7145h	ICU	Interrupt request destination setting register 069	ISELR069	8	8	2 ICLK
0008 7146h	ICU	Interrupt request destination setting register 070	ISELR070	8	8	2 ICLK
0008 7147h	ICU	Interrupt request destination setting register 071	ISELR071	8	8	2 ICLK
0008 7148h	ICU	Interrupt request destination setting register 072	ISELR072	8	8	2 ICLK
0008 7149h	ICU	Interrupt request destination setting register 073	ISELR073	8	8	2 ICLK
0008 714Ah	ICU	Interrupt request destination setting register 074	ISELR074	8	8	2 ICLK
0008 714Bh	ICU	Interrupt request destination setting register 075	ISELR075	8	8	2 ICLK
0008 714Ch	ICU	Interrupt request destination setting register 076	ISELR076	8	8	2 ICLK
0008 714Dh	ICU	Interrupt request destination setting register 077	ISELR077	8	8	2 ICLK
0008 714Eh	ICU	Interrupt request destination setting register 078	ISELR078	8	8	2 ICLK
0008 714Fh	ICU	Interrupt request destination setting register 079	ISELR079	8	8	2 ICLK
0008 7162h	ICU	Interrupt request destination setting register 098	ISELR098	8	8	2 ICLK
0008 7163h	ICU	Interrupt request destination setting register 099	ISELR099	8	8	2 ICLK
0008 7164h	ICU	Interrupt request destination setting register 100	ISELR100	8	8	2 ICLK
0008 7165h	ICU	Interrupt request destination setting register 101	ISELR101	8	8	2 ICLK
0008 7168h	ICU	Interrupt request destination setting register 104	ISELR104	8	8	2 ICLK
0008 7169h	ICU	Interrupt request destination setting register 105	ISELR105	8	8	2 ICLK
0008 716Ah	ICU	Interrupt request destination setting register 106	ISELR106	8	8	2 ICLK
0008 716Bh	ICU	Interrupt request destination setting register 107	ISELR107	8	8	2 ICLK
0008 716Fh	ICU	Interrupt request destination setting register 111	ISELR111	8	8	2 ICLK

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7170h	ICU	Interrupt request destination setting register 112	ISELR112	8	8	2 ICLK
0008 7175h	ICU	Interrupt request destination setting register 117	ISELR117	8	8	2 ICLK
0008 7176h	ICU	Interrupt request destination setting register 118	ISELR118	8	8	2 ICLK
0008 717Ah	ICU	Interrupt request destination setting register 122	ISELR122	8	8	2 ICLK
0008 717Bh	ICU	Interrupt request destination setting register 123	ISELR123	8	8	2 ICLK
0008 717Ch	ICU	Interrupt request destination setting register 124	ISELR124	8	8	2 ICLK
0008 717Dh	ICU	Interrupt request destination setting register 125	ISELR125	8	8	2 ICLK
0008 717Fh	ICU	Interrupt request destination setting register 127	ISELR127	8	8	2 ICLK
0008 7180h	ICU	Interrupt request destination setting register 128	ISELR128	8	8	2 ICLK
0008 7185h	ICU	Interrupt request destination setting register 133	ISELR133	8	8	2 ICLK
0008 7186h	ICU	Interrupt request destination setting register 134	ISELR134	8	8	2 ICLK
0008 718Ah	ICU	Interrupt request destination setting register 138	ISELR138	8	8	2 ICLK
0008 718Bh	ICU	Interrupt request destination setting register 139	ISELR139	8	8	2 ICLK
0008 718Ch	ICU	Interrupt request destination setting register 140	ISELR140	8	8	2 ICLK
0008 718Dh	ICU	Interrupt request destination setting register 141	ISELR141	8	8	2 ICLK
0008 7191h	ICU	Interrupt request destination setting register 145	ISELR145	8	8	2 ICLK
0008 7192h	ICU	Interrupt request destination setting register 146	ISELR146	8	8	2 ICLK
0008 7197h	ICU	Interrupt request destination setting register 151	ISELR151	8	8	2 ICLK
0008 7198h	ICU	Interrupt request destination setting register 152	ISELR152	8	8	2 ICLK
0008 719Ch	ICU	Interrupt request destination setting register 156	ISELR156	8	8	2 ICLK
0008 719Dh	ICU	Interrupt request destination setting register 157	ISELR157	8	8	2 ICLK
0008 719Eh	ICU	Interrupt request destination setting register 158	ISELR158	8	8	2 ICLK
0008 719Fh	ICU	Interrupt request destination setting register 159	ISELR159	8	8	2 ICLK
0008 71A1h	ICU	Interrupt request destination setting register 161	ISELR161	8	8	2 ICLK
0008 71A2h	ICU	Interrupt request destination setting register 162	ISELR162	8	8	2 ICLK
0008 71A7h	ICU	Interrupt request destination setting register 167	ISELR167	8	8	2 ICLK
0008 71A8h	ICU	Interrupt request destination setting register 168	ISELR168	8	8	2 ICLK
0008 71AEh	ICU	Interrupt request destination setting register 174	ISELR174	8	8	2 ICLK
0008 71AFh	ICU	Interrupt request destination setting register 175	ISELR175	8	8	2 ICLK
0008 71B1h	ICU	Interrupt request destination setting register 177	ISELR177	8	8	2 ICLK
0008 71B2h	ICU	Interrupt request destination setting register 178	ISELR178	8	8	2 ICLK
0008 71B4h	ICU	Interrupt request destination setting register 180	ISELR180	8	8	2 ICLK
0008 71B5h	ICU	Interrupt request destination setting register 181	ISELR181	8	8	2 ICLK
0008 71B7h	ICU	Interrupt request destination setting register 183	ISELR183	8	8	2 ICLK
0008 71B8h	ICU	Interrupt request destination setting register 184	ISELR184	8	8	2 ICLK
0008 71C6h	ICU	Interrupt request destination setting register 198	ISELR198	8	8	2 ICLK
0008 71C7h	ICU	Interrupt request destination setting register 199	ISELR199	8	8	2 ICLK
0008 71C8h	ICU	Interrupt request destination setting register 200	ISELR200	8	8	2 ICLK
0008 71C9h	ICU	Interrupt request destination setting register 201	ISELR201	8	8	2 ICLK
0008 71D7h	ICU	Interrupt request destination setting register 215	ISELR215	8	8	2 ICLK
0008 71D8h	ICU	Interrupt request destination setting register 216	ISELR216	8	8	2 ICLK
0008 71DBh	ICU	Interrupt request destination setting register 219	ISELR219	8	8	2 ICLK
0008 71DCh	ICU	Interrupt request destination setting register 220	ISELR220	8	8	2 ICLK
0008 71DFh	ICU	Interrupt request destination setting register 223	ISELR223	8	8	2 ICLK
0008 71E0h	ICU	Interrupt request destination setting register 224	ISELR224	8	8	2 ICLK

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 71E3h	ICU	Interrupt request destination setting register 227	ISELR227	8	8	2 ICLK
0008 71E4h	ICU	Interrupt request destination setting register 228	ISELR228	8	8	2 ICLK
0008 71E7h	ICU	Interrupt request destination setting register 231	ISELR231	8	8	2 ICLK
0008 71E8h	ICU	Interrupt request destination setting register 232	ISELR232	8	8	2 ICLK
0008 71EBh	ICU	Interrupt request destination setting register 235	ISELR235	8	8	2 ICLK
0008 71ECh	ICU	Interrupt request destination setting register 236	ISELR236	8	8	2 ICLK
0008 71EFh	ICU	Interrupt request destination setting register 239	ISELR239	8	8	2 ICLK
0008 71F0h	ICU	Interrupt request destination setting register 240	ISELR240	8	8	2 ICLK
0008 71F7h	ICU	Interrupt request destination setting register 247	ISELR247	8	8	2 ICLK
0008 71F8h	ICU	Interrupt request destination setting register 248	ISELR248	8	8	2 ICLK
0008 71FBh	ICU	Interrupt request destination setting register 251	ISELR251	8	8	2 ICLK
0008 71FCh	ICU	Interrupt request destination setting register 252	ISELR252	8	8	2 ICLK
0008 71FDh	ICU	Interrupt request destination setting register 253	ISELR253	8	8	2ICLK
0008 7202h	ICU	Interrupt request enable register 02	IER02	8	8	2 ICLK
0008 7203h	ICU	Interrupt request enable register 03	IER03	8	8	2 ICLK
0008 7208h	ICU	Interrupt request enable register 08	IER08	8	8	2 ICLK
0008 7209h	ICU	Interrupt request enable register 09	IER09	8	8	2 ICLK
0008 720Ch	ICU	Interrupt request enable register 0C	IER0C	8	8	2 ICLK
0008 720Dh	ICU	Interrupt request enable register 0D	IER0D	8	8	2 ICLK
0008 720Eh	ICU	Interrupt request enable register 0E	IER0E	8	8	2 ICLK
0008 720Fh	ICU	Interrupt request enable register 0F	IER0F	8	8	2 ICLK
0008 7210h	ICU	Interrupt request enable register 10	IER10	8	8	2 ICLK
0008 7211h	ICU	Interrupt request enable register 11	IER11	8	8	2 ICLK
0008 7212h	ICU	Interrupt request enable register 12	IER12	8	8	2 ICLK
0008 7213h	ICU	Interrupt request enable register 13	IER13	8	8	2 ICLK
0008 7214h	ICU	Interrupt request enable register 14	IER14	8	8	2 ICLK
0008 7215h	ICU	Interrupt request enable register 15	IER15	8	8	2 ICLK
0008 7216h	ICU	Interrupt request enable register 16	IER16	8	8	2 ICLK
0008 7217h	ICU	Interrupt request enable register 17	IER17	8	8	2 ICLK
0008 7218h	ICU	Interrupt request enable register 18	IER18	8	8	2 ICLK
0008 7219h	ICU	Interrupt request enable register 19	IER19	8	8	2 ICLK
0008 721Ah	ICU	Interrupt request enable register 1A	IER1A	8	8	2 ICLK
0008 721Bh	ICU	Interrupt request enable register 1B	IER1B	8	8	2 ICLK
0008 721Ch	ICU	Interrupt request enable register 1C	IER1C	8	8	2 ICLK
0008 721Dh	ICU	Interrupt request enable register 1D	IER1D	8	8	2 ICLK
0008 721Eh	ICU	Interrupt request enable register 1E	IER1E	8	8	2 ICLK
0008 721Fh	ICU	Interrupt request enable register 1F	IER1F	8	8	2 ICLK
0008 7300h	ICU	Interrupt priority register 00	IPR00	8	8	2 ICLK
0008 7301h	ICU	Interrupt priority register 01	IPR01	8	8	2 ICLK
0008 7302h	ICU	Interrupt priority register 02	IPR02	8	8	2 ICLK
0008 7304h	ICU	Interrupt priority register 04	IPR04	8	8	2 ICLK
0008 7305h	ICU	Interrupt priority register 05	IPR05	8	8	2 ICLK
0008 7306h	ICU	Interrupt priority register 06	IPR06	8	8	2 ICLK
0008 7307h	ICU	Interrupt priority register 07	IPR07	8	8	2 ICLK
0008 7320h	ICU	Interrupt priority register 20	IPR20	8	8	2 ICLK

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7321h	ICU	Interrupt priority register 21	IPR21	8	8	2 ICLK
0008 7322h	ICU	Interrupt priority register 22	IPR22	8	8	2 ICLK
0008 7323h	ICU	Interrupt priority register 23	IPR23	8	8	2 ICLK
0008 7324h	ICU	Interrupt priority register 24	IPR24	8	8	2 ICLK
0008 7325h	ICU	Interrupt priority register 25	IPR25	8	8	2 ICLK
0008 7326h	ICU	Interrupt priority register 26	IPR26	8	8	2 ICLK
0008 7327h	ICU	Interrupt priority register 27	IPR27	8	8	2 ICLK
0008 7328h	ICU	Interrupt priority register 28	IPR28	8	8	2 ICLK
0008 7329h	ICU	Interrupt priority register 29	IPR29	8	8	2 ICLK
0008 732Ah	ICU	Interrupt priority register 2A	IPR2A	8	8	2 ICLK
0008 732Bh	ICU	Interrupt priority register 2B	IPR2B	8	8	2 ICLK
0008 732Ch	ICU	Interrupt priority register 2C	IPR2C	8	8	2 ICLK
0008 732Dh	ICU	Interrupt priority register 2D	IPR2D	8	8	2 ICLK
0008 732Eh	ICU	Interrupt priority register 2E	IPR2E	8	8	2 ICLK
0008 732Fh	ICU	Interrupt priority register 2F	IPR2F	8	8	2 ICLK
0008 7340h	ICU	Interrupt priority register 40	IPR40	8	8	2 ICLK
0008 7344h	ICU	Interrupt priority register 44	IPR44	8	8	2 ICLK
0008 7345h	ICU	Interrupt priority register 45	IPR45	8	8	2 ICLK
0008 7346h	ICU	Interrupt priority register 46	IPR46	8	8	2 ICLK
0008 7347h	ICU	Interrupt priority register 47	IPR47	8	8	2 ICLK
0008 734Ch	ICU	Interrupt priority register 4C	IPR4C	8	8	2 ICLK
0008 734Dh	ICU	Interrupt priority register 4D	IPR4D	8	8	2 ICLK
0008 734Eh	ICU	Interrupt priority register 4E	IPR4E	8	8	2 ICLK
0008 734Fh	ICU	Interrupt priority register 4F	IPR4F	8	8	2 ICLK
0008 7350h	ICU	Interrupt priority register 50	IPR50	8	8	2 ICLK
0008 7351h	ICU	Interrupt priority register 51	IPR51	8	8	2 ICLK
0008 7352h	ICU	Interrupt priority register 52	IPR52	8	8	2 ICLK
0008 7353h	ICU	Interrupt priority register 53	IPR53	8	8	2 ICLK
0008 7354h	ICU	Interrupt priority register 54	IPR54	8	8	2 ICLK
0008 7355h	ICU	Interrupt priority register 55	IPR55	8	8	2 ICLK
0008 7356h	ICU	Interrupt priority register 56	IPR56	8	8	2 ICLK
0008 7357h	ICU	Interrupt priority register 57	IPR57	8	8	2 ICLK
0008 7358h	ICU	Interrupt priority register 58	IPR58	8	8	2 ICLK
0008 7359h	ICU	Interrupt priority register 59	IPR59	8	8	2 ICLK
0008 735Ah	ICU	Interrupt priority register 5A	IPR5A	8	8	2 ICLK
0008 735Bh	ICU	Interrupt priority register 5B	IPR5B	8	8	2 ICLK
0008 735Ch	ICU	Interrupt priority register 5C	IPR5C	8	8	2 ICLK
0008 735Dh	ICU	Interrupt priority register 5D	IPR5D	8	8	2 ICLK
0008 735Eh	ICU	Interrupt priority register 5E	IPR5E	8	8	2 ICLK
0008 735Fh	ICU	Interrupt priority register 5F	IPR5F	8	8	2 ICLK
0008 7360h	ICU	Interrupt priority register 60	IPR60	8	8	2 ICLK
0008 7361h	ICU	Interrupt priority register 61	IPR61	8	8	2 ICLK
0008 7362h	ICU	Interrupt priority register 62	IPR62	8	8	2 ICLK
0008 7363h	ICU	Interrupt priority register 63	IPR63	8	8	2 ICLK
0008 7368h	ICU	Interrupt priority register 68	IPR68	8	8	2 ICLK

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7369h	ICU	Interrupt priority register 69	IPR69	8	8	2 ICLK
0008 736Ah	ICU	Interrupt priority register 6A	IPR6A	8	8	2 ICLK
0008 736Bh	ICU	Interrupt priority register 6B	IPR6B	8	8	2 ICLK
0008 7370h	ICU	Interrupt priority register 70	IPR70	8	8	2 ICLK
0008 7371h	ICU	Interrupt priority register 71	IPR71	8	8	2 ICLK
0008 7372h	ICU	Interrupt priority register 72	IPR72	8	8	2 ICLK
0008 7373h	ICU	Interrupt priority register 73	IPR73	8	8	2 ICLK
0008 7380h	ICU	Interrupt priority register 80	IPR80	8	8	2 ICLK
0008 7381h	ICU	Interrupt priority register 81	IPR81	8	8	2 ICLK
0008 7382h	ICU	Interrupt priority register 82	IPR82	8	8	2 ICLK
0008 7383h	ICU	Interrupt priority register 83	IPR83	8	8	2 ICLK
0008 7384h	ICU	Interrupt priority register 84	IPR84	8	8	2 ICLK
0008 7385h	ICU	Interrupt priority register 85	IPR85	8	8	2 ICLK
0008 7386h	ICU	Interrupt priority register 86	IPR86	8	8	2 ICLK
0008 7388h	ICU	Interrupt priority register 88	IPR88	8	8	2 ICLK
0008 7389h	ICU	Interrupt priority register 89	IPR89	8	8	2 ICLK
0008 738Ah	ICU	Interrupt priority register 8A	IPR8A	8	8	2 ICLK
0008 738Bh	ICU	Interrupt priority register 8B	IPR8B	8	8	2 ICLK
0008 738Ch	ICU	Interrupt priority register 8C	IPR8C	8	8	2 ICLK
0008 738Dh	ICU	Interrupt priority register 8D	IPR8D	8	8	2 ICLK
0008 738Eh	ICU	Interrupt priority register 8E	IPR8E	8	8	2 ICLK
0008 738Fh	ICU	Interrupt priority register 8F	IPR8F	8	8	2 ICLK
0008 73F0h	ICU	Fast interrupt register	FIR	16	16	2 ICLK
0008 7400h	DTC	DTC control register	DTCCR	8	8	2 ICLK
0008 7404h	DTC	DTC vector base register	DTCVBR	32	32	2 ICLK
0008 7408h	DTC	DTC address mode register	DTCADMOD	8	8	2 ICLK
0008 740Ch	DTC	DTC module start register	DTCST	8	8	2 ICLK
0008 8000h	CMT (unit 0)	Compare match timer start register 0	CMSTR0	16	16	2 to 3 PCLK *7
0008 8002h	CMT0	Compare match timer control register	CMCR	16	16	2 to 3 PCLK *7
0008 8004h	CMT0	Compare match timer counter	CMCNT	16	16	2 to 3 PCLK *7
0008 8006h	CMT0	Compare match timer constant register	CMCOR	16	16	2 to 3 PCLK *7
0008 8008h	CMT1	Compare match timer control register	CMCR	16	16	2 to 3 PCLK *7
0008 800Ah	CMT1	Compare match timer counter	CMCNT	16	16	2 to 3 PCLK *7
0008 800Ch	CMT1	Compare match timer constant register	CMCOR	16	16	2 to 3 PCLK *7
0008 8010h	CMT (unit 1)	Compare match timer start register 1	CMSTR1	16	16	2 to 3 PCLK *7
0008 8012h	CMT2	Compare match timer control register	CMCR	16	16	2 to 3 PCLK *7
0008 8014h	CMT2	Compare match timer counter	CMCNT	16	16	2 to 3 PCLK *7
0008 8016h	CMT2	Compare match timer constant register	CMCOR	16	16	2 to 3 PCLK *7
0008 8018h	CMT3	Compare match timer control register	CMCR	16	16	2 to 3 PCLK *7
0008 801Ah	CMT3	Compare match timer counter	CMCNT	16	16	2 to 3 PCLK *7
0008 801Ch	CMT3	Compare match timer constant register	CMCOR	16	16	2 to 3 PCLK *7
0008 8028h	WDT	Timer control/status register	TCSR	8	8	2 to 3 PCLK *7
0008 8028h	WDT	Write window A register	WINA	16	16	2 to 3 PCLK *7
0008 8029h	WDT	Timer counter	TCNT	8	8	2 to 3 PCLK *7
0008 802Ah	WDT	Write window B register	WINB	16	16	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 802Bh	WDT	Reset control/status register	RSTCSR	8	8	2 to 3 PCLK *7
0008 8040h	AD0	A/D data register A	ADDRA	16	16	2 to 3 PCLK *7
0008 8042h	AD0	A/D data register B	ADDRB	16	16	2 to 3 PCLK *7
0008 8044h	AD0	A/D data register C	ADDRC	16	16	2 to 3 PCLK *7
0008 8046h	AD0	A/D data register D	ADDRD	16	16	2 to 3 PCLK *7
0008 8050h	AD0	A/D control/status register	ADCSR	8	8	2 to 3 PCLK *7
0008 8051h	AD0	A/D control register	ADCR	8	8	2 to 3 PCLK *7
0008 8052h	AD0	ADDRy format select register	ADDPR	8	8	2 to 3 PCLK *7
0008 8053h	AD0	A/D sampling state register	ADSSTR	8	8	2 to 3 PCLK *7
0008 8060h	AD1	A/D data register A	ADDRA	16	16	2 to 3 PCLK *7
0008 8062h	AD1	A/D data register B	ADDRB	16	16	2 to 3 PCLK *7
0008 8064h	AD1	A/D data register C	ADDRC	16	16	2 to 3 PCLK *7
0008 8066h	AD1	A/D data register D	ADDRD	16	16	2 to 3 PCLK *7
0008 8070h	AD1	A/D control/status register	ADCSR	8	8	2 to 3 PCLK *7
0008 8071h	AD1	A/D control register	ADCR	8	8	2 to 3 PCLK *7
0008 8072h	AD1	ADDRy format select register	ADDPR	8	8	2 to 3 PCLK *7
0008 8073h	AD1	A/D sampling state register	ADSSTR	8	8	2 to 3 PCLK *7
0008 8080h	AD2	A/D data register A	ADDRA	16	16	2 to 3 PCLK *7
0008 8082h	AD2	A/D data register B	ADDRB	16	16	2 to 3 PCLK *7
0008 8084h	AD2	A/D data register C	ADDRC	16	16	2 to 3 PCLK *7
0008 8086h	AD2	A/D data register D	ADDRD	16	16	2 to 3 PCLK *7
0008 8090h	AD2	A/D control/status register	ADCSR	8	8	2 to 3 PCLK *7
0008 8091h	AD2	A/D control register	ADCR	8	8	2 to 3 PCLK *7
0008 8092h	AD2	ADDRy format select register	ADDPR	8	8	2 to 3 PCLK *7
0008 8093h	AD2	A/D sampling state register	ADSSTR	8	8	2 to 3 PCLK *7
0008 80A0h	AD3	A/D data register A	ADDRA	16	16	2 to 3 PCLK *7
0008 80A2h	AD3	A/D data register B	ADDRB	16	16	2 to 3 PCLK *7
0008 80A4h	AD3	A/D data register C	ADDRC	16	16	2 to 3 PCLK *7
0008 80A6h	AD3	A/D data register D	ADDRD	16	16	2 to 3 PCLK *7
0008 80B0h	AD3	A/D control/status register	ADCSR	8	8	2 to 3 PCLK *7
0008 80B1h	AD3	A/D control register	ADCR	8	8	2 to 3 PCLK *7
0008 80B2h	AD3	ADDRy format select register	ADDPR	8	8	2 to 3 PCLK *7
0008 80B3h	AD3	A/D sampling state register	ADSSTR	8	8	2 to 3 PCLK *7
0008 80C0h	D/A	D/A data register 0	DADR0	16	16	2 to 3 PCLK *7
0008 80C2h	D/A	D/A data register 1	DADR1	16	16	2 to 3 PCLK *7
0008 80C4h	D/A	D/A control register	DACR	8	8	2 to 3 PCLK *7
0008 80C5h	D/A	DADRy format select register	DADPR	8	8	2 to 3 PCLK *7
0008 8100h	TPU (unit 0)	Timer start register	TSTRA	8	8	2 to 3 PCLK *7
0008 8101h	TPU (unit 0)	Timer synchronous register	TSYRA	8	8	2 to 3 PCLK *7
0008 8110h	TPU0	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8111h	TPU0	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8112h	TPU0	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK *7
0008 8113h	TPU0	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK *7
0008 8114h	TPU0	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8115h	TPU0	Timer status register	TSR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8116h	TPU0	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8118h	TPU0	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 811Ah	TPU0	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 811Ch	TPU0	Timer general register C	TGRC	16	16	2 to 3 PCLK *7
0008 811Eh	TPU0	Timer general register D	TGRD	16	16	2 to 3 PCLK *7
0008 8120h	TPU1	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8121h	TPU1	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8122h	TPU1	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8124h	TPU1	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8125h	TPU1	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8126h	TPU1	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8128h	TPU1	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 812Ah	TPU1	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 8130h	TPU2	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8131h	TPU2	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8132h	TPU2	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8134h	TPU2	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8135h	TPU2	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8136h	TPU2	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8138h	TPU2	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 813Ah	TPU2	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 8140h	TPU3	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8141h	TPU3	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8142h	TPU3	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK *7
0008 8143h	TPU3	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK *7
0008 8144h	TPU3	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8145h	TPU3	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8146h	TPU3	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8148h	TPU3	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 814Ah	TPU3	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 814Ch	TPU3	Timer general register C	TGRC	16	16	2 to 3 PCLK *7
0008 814Eh	TPU3	Timer general register D	TGRD	16	16	2 to 3 PCLK *7
0008 8150h	TPU4	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8151h	TPU4	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8152h	TPU4	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8154h	TPU4	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8155h	TPU4	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8156h	TPU4	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8158h	TPU4	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 815Ah	TPU4	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 8160h	TPU5	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8161h	TPU5	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8162h	TPU5	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8164h	TPU5	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8165h	TPU5	Timer status register	TSR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8166h	TPU5	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8168h	TPU5	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 816Ah	TPU5	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 8170h	TPU (unit 1)	Timer start register	TSTRB	8	8	2 to 3 PCLK *7
0008 8171h	TPU (unit 1)	Timer synchronous register	TSYRB	8	8	2 to 3 PCLK *7
0008 8180h	TPU6	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8181h	TPU6	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8182h	TPU6	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK *7
0008 8183h	TPU6	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK *7
0008 8184h	TPU6	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8185h	TPU6	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8186h	TPU6	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8188h	TPU6	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 818Ah	TPU6	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 818Ch	TPU6	Timer general register C	TGRC	16	16	2 to 3 PCLK *7
0008 818Eh	TPU6	Timer general register D	TGRD	16	16	2 to 3 PCLK *7
0008 8190h	TPU7	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8191h	TPU7	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 8192h	TPU7	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 8194h	TPU7	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 8195h	TPU7	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 8196h	TPU7	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 8198h	TPU7	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 819Ah	TPU7	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 81A0h	TPU8	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 81A1h	TPU8	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 81A2h	TPU8	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 81A4h	TPU8	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 81A5h	TPU8	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 81A6h	TPU8	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 81A8h	TPU8	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 81AAh	TPU8	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 81B0h	TPU9	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 81B1h	TPU9	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 81B2h	TPU9	Timer I/O control register H	TIORH	8	8	2 to 3 PCLK *7
0008 81B3h	TPU9	Timer I/O control register L	TIORL	8	8	2 to 3 PCLK *7
0008 81B4h	TPU9	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 81B5h	TPU9	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 81B6h	TPU9	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 81B8h	TPU9	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 81BAh	TPU9	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 81BCh	TPU9	Timer general register C	TGRC	16	16	2 to 3 PCLK *7
0008 81BEh	TPU9	Timer general register D	TGRD	16	16	2 to 3 PCLK *7
0008 81C0h	TPU10	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 81C1h	TPU10	Timer mode register	TMDR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 81C2h	TPU10	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 81C4h	TPU10	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 81C5h	TPU10	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 81C6h	TPU10	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 81C8h	TPU10	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 81CAh	TPU10	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 81D0h	TPU11	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 81D1h	TPU11	Timer mode register	TMDR	8	8	2 to 3 PCLK *7
0008 81D2h	TPU11	Timer I/O control register	TIOR	8	8	2 to 3 PCLK *7
0008 81D4h	TPU11	Timer interrupt enable register	TIER	8	8	2 to 3 PCLK *7
0008 81D5h	TPU11	Timer status register	TSR	8	8	2 to 3 PCLK *7
0008 81D6h	TPU11	Timer counter	TCNT	16	16	2 to 3 PCLK *7
0008 81D8h	TPU11	Timer general register A	TGRA	16	16	2 to 3 PCLK *7
0008 81DAh	TPU11	Timer general register B	TGRB	16	16	2 to 3 PCLK *7
0008 81E6h	PPG0	PPG output control register	PCR	8	8	2 to 3 PCLK *7
0008 81E7h	PPG0	PPG output mode register	PMR	8	8	2 to 3 PCLK *7
0008 81E8h	PPG0	Next data enable register H	NDERH	8	8	2 to 3 PCLK *7
0008 81E9h	PPG0	Next data enable register L	NDERL	8	8	2 to 3 PCLK *7
0008 81EAh	PPG0	Output data register H	PODRH	8	8	2 to 3 PCLK *7
0008 81EBh	PPG0	Output data register L	PODRL	8	8	2 to 3 PCLK *7
0008 81ECh*1	PPG0	Next data register H	NDRH	8	8	2 to 3 PCLK *7
0008 81EDh*2	PPG0	Next data register L	NDRL	8	8	2 to 3 PCLK *7
0008 81EEh*1	PPG0	Next data register H	NDRH	8	8	2 to 3 PCLK *7
0008 81EFh*2	PPG0	Next data register L	NDRL	8	8	2 to 3 PCLK *7
0008 81F0h	PPG1	PPG trigger select register	PTRSLR	8	8	2 to 3 PCLK *7
0008 81F6h	PPG1	PPG output control register	PCR	8	8	2 to 3 PCLK *7
0008 81F7h	PPG1	PPG output mode register	PMR	8	8	2 to 3 PCLK *7
0008 81F8h	PPG1	Next data enable register H	NDERH	8	8	2 to 3 PCLK *7
0008 81F9h	PPG1	Next data enable register L	NDERL	8	8	2 to 3 PCLK *7
0008 81FAh	PPG1	Output data register H	PODRH	8	8	2 to 3 PCLK *7
0008 81FBh	PPG1	Output data register L	PODRL	8	8	2 to 3 PCLK *7
0008 81FCh*3	PPG1	Next data register H	NDRH	8	8	2 to 3 PCLK *7
0008 81FDh*4	PPG1	Next data register L	NDRL	8	8	2 to 3 PCLK *7
0008 81FEh*3	PPG1	Next data register H	NDRH	8	8	2 to 3 PCLK *7
0008 81FFh*4	PPG1	Next data register L	NDRL	8	8	2 to 3 PCLK *7
0008 8200h	TMR0	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8201h	TMR1	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8202h	TMR0	Timer control/status register	TCSR	8	8	2 to 3 PCLK *7
0008 8203h	TMR1	Timer control/status register	TCSR	8	8	2 to 3 PCLK *7
0008 8204h	TMR0	Time constant register A	TCORA	8	8 or 16	2 to 3 PCLK *7
0008 8205h	TMR1	Time constant register A	TCORA	8	8 or 16*5	2 to 3 PCLK *7
0008 8206h	TMR0	Time constant register B	TCORB	8	8 or 16	2 to 3 PCLK *7
0008 8207h	TMR1	Time constant register B	TCORB	8	8 or 16*5	2 to 3 PCLK *7
0008 8208h	TMR0	Timer counter	TCNT	8	8 or 16	2 to 3 PCLK *7
0008 8209h	TMR1	Timer counter	TCNT	8	8 or 16*5	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 820Ah	TMR0	Timer counter control register	TCCR	8	8 or 16	2 to 3 PCLK *7
0008 820Bh	TMR1	Timer counter control register	TCCR	8	8 or 16	2 to 3 PCLK *7
0008 8210h	TMR2	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8211h	TMR3	Timer control register	TCR	8	8	2 to 3 PCLK *7
0008 8212h	TMR2	Timer control/status register	TCSR	8	8	2 to 3 PCLK *7
0008 8213h	TMR3	Timer control/status register	TCSR	8	8	2 to 3 PCLK *7
0008 8214h	TMR2	Time constant register A	TCORA	8	8 or 16	2 to 3 PCLK *7
0008 8215h	TMR3	Time constant register A	TCORA	8	8 or 16*5	2 to 3 PCLK *7
0008 8216h	TMR2	Time constant register B	TCORB	8	8 or 16	2 to 3 PCLK *7
0008 8217h	TMR3	Time constant register B	TCORB	8	8 or 16*5	2 to 3 PCLK *7
0008 8218h	TMR2	Timer counter	TCNT	8	8 or 16	2 to 3 PCLK *7
0008 8219h	TMR3	Timer counter	TCNT	8	8 or 16*5	2 to 3 PCLK *7
0008 821Ah	TMR2	Timer counter control register	TCCR	8	8 or 16	2 to 3 PCLK *7
0008 821Bh	TMR3	Timer counter control register	TCCR	8	8 or 16	2 to 3 PCLK *7
0008 8240h	SCI0	Serial mode register	SMR*6	8	8	2 to 3 PCLK *7
0008 8241h	SCI0	Bit rate register	BRR	8	8	2 to 3 PCLK *7
0008 8242h	SCI0	Serial control register	SCR*6	8	8	2 to 3 PCLK *7
0008 8243h	SCI0	Transmit data register	TDR	8	8	2 to 3 PCLK *7
0008 8244h	SCI0	Serial status register	SSR*6	8	8	2 to 3 PCLK *7
0008 8245h	SCI0	Receive data register	RDR	8	8	2 to 3 PCLK *7
0008 8246h	SCI0	Smart card mode register	SCMR	8	8	2 to 3 PCLK *7
0008 8247h	SCI0	Serial extended mode register	SEMR	8	8	2 to 3 PCLK *7
0008 8248h	SCI1	Serial mode register	SMR*6	8	8	2 to 3 PCLK *7
0008 8249h	SCI1	Bit rate register	BRR	8	8	2 to 3 PCLK *7
0008 824Ah	SCI1	Serial control register	SCR*6	8	8	2 to 3 PCLK *7
0008 824Bh	SCI1	Transmit data register	TDR	8	8	2 to 3 PCLK *7
0008 824Ch	SCI1	Serial status register	SSR*6	8	8	2 to 3 PCLK *7
0008 824Dh	SCI1	Receive data register	RDR	8	8	2 to 3 PCLK *7
0008 824Eh	SCI1	Smart card mode register	SCMR	8	8	2 to 3 PCLK *7
0008 824Fh	SCI1	Serial extended mode register	SEMR	8	8	2 to 3 PCLK *7
0008 8250h	SCI2	Serial mode register	SMR*6	8	8	2 to 3 PCLK *7
0008 8251h	SCI2	Bit rate register	BRR	8	8	2 to 3 PCLK *7
0008 8252h	SCI2	Serial control register	SCR*6	8	8	2 to 3 PCLK *7
0008 8253h	SCI2	Transmit data register	TDR	8	8	2 to 3 PCLK *7
0008 8254h	SCI2	Serial status register	SSR*6	8	8	2 to 3 PCLK *7
0008 8255h	SCI2	Receive data register	RDR	8	8	2 to 3 PCLK *7
0008 8256h	SCI2	Smart card mode register	SCMR	8	8	2 to 3 PCLK *7
0008 8257h	SCI2	Serial extended mode register	SEMR	8	8	2 to 3 PCLK *7
0008 8258h	SCI3	Serial mode register	SMR*6	8	8	2 to 3 PCLK *7
0008 8259h	SCI3	Bit rate register	BRR	8	8	2 to 3 PCLK *7
0008 825Ah	SCI3	Serial control register	SCR*6	8	8	2 to 3 PCLK *7
0008 825Bh	SCI3	Transmit data register	TDR	8	8	2 to 3 PCLK *7
0008 825Ch	SCI3	Serial status register	SSR*6	8	8	2 to 3 PCLK *7
0008 825Dh	SCI3	Receive data register	RDR	8	8	2 to 3 PCLK *7
0008 825Eh	SCI3	Smart card mode register	SCMR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 825Fh	SCI3	Serial extended mode register	SEMR	8	8	2 to 3 PCLK *7
0008 8260h	SCI4	Serial mode register	SMR*6	8	8	2 to 3 PCLK *7
0008 8261h	SCI4	Bit rate register	BRR	8	8	2 to 3 PCLK *7
0008 8262h	SCI4	Serial control register	SCR*6	8	8	2 to 3 PCLK *7
0008 8263h	SCI4	Transmit data register	TDR	8	8	2 to 3 PCLK *7
0008 8264h	SCI4	Serial status register	SSR*6	8	8	2 to 3 PCLK *7
0008 8265h	SCI4	Receive data register	RDR	8	8	2 to 3 PCLK *7
0008 8266h	SCI4	Smart card mode register	SCMR	8	8	2 to 3 PCLK *7
0008 8267h	SCI4	Serial extended mode register	SEMR	8	8	2 to 3 PCLK *7
0008 8268h	SCI5	Serial mode register	SMR*6	8	8	2 to 3 PCLK *7
0008 8269h	SCI5	Bit rate register	BRR	8	8	2 to 3 PCLK *7
0008 826Ah	SCI5	Serial control register	SCR*6	8	8	2 to 3 PCLK *7
0008 826Bh	SCI5	Transmit data register	TDR	8	8	2 to 3 PCLK *7
0008 826Ch	SCI5	Serial status register	SSR*6	8	8	2 to 3 PCLK *7
0008 826Dh	SCI5	Receive data register	RDR	8	8	2 to 3 PCLK *7
0008 826Eh	SCI5	Smart card mode register	SCMR	8	8	2 to 3 PCLK *7
0008 826Fh	SCI5	Serial extended mode register	SEMR	8	8	2 to 3 PCLK *7
0008 8270h	SCI6	Serial mode register	SMR*6	8	8	2 to 3 PCLK *7
0008 8271h	SCI6	Bit rate register	BRR	8	8	2 to 3 PCLK *7
0008 8272h	SCI6	Serial control register	SCR*6	8	8	2 to 3 PCLK *7
0008 8273h	SCI6	Transmit data register	TDR	8	8	2 to 3 PCLK *7
0008 8274h	SCI6	Serial status register	SSR*6	8	8	2 to 3 PCLK *7
0008 8275h	SCI6	Receive data register	RDR	8	8	2 to 3 PCLK *7
0008 8276h	SCI6	Smart card mode register	SCMR	8	8	2 to 3 PCLK *7
0008 8277h	SCI6	Serial extended mode register	SEMR	8	8	2 to 3 PCLK *7
0008 8280h	CRC	CRC control register	CRCCR	8	8	2 to 3 PCLK *7
0008 8281h	CRC	CRC data input register	CRCDIR	8	8	2 to 3 PCLK *7
0008 8282h	CRC	CRC data output register	CRCDOR	16	16	2 to 3 PCLK *7
0008 8300h	RIIC0	I^2C bus control register 1	ICCR1	8	8	2 to 3 PCLK *7
0008 8301h	RIIC0	I^2C bus control register 2	ICCR2	8	8	2 to 3 PCLK *7
0008 8302h	RIIC0	I^2C bus mode register 1	ICMR1	8	8	2 to 3 PCLK *7
0008 8303h	RIIC0	I^2C bus mode register 2	ICMR2	8	8	2 to 3 PCLK *7
0008 8304h	RIIC0	I^2C bus mode register 3	ICMR3	8	8	2 to 3 PCLK *7
0008 8305h	RIIC0	I^2C bus function enable register	ICFER	8	8	2 to 3 PCLK *7
0008 8306h	RIIC0	I^2C bus status enable register	ICSER	8	8	2 to 3 PCLK *7
0008 8307h	RIIC0	I^2C bus interrupt enable register	ICIER	8	8	2 to 3 PCLK *7
0008 8308h	RIIC0	I^2C bus status register 1	ICSR1	8	8	2 to 3 PCLK *7
0008 8309h	RIIC0	I^2C bus status register 2	ICSR2	8	8	2 to 3 PCLK *7
0008 830Ah	RIIC0	Slave address register L0	SARL0	8	8	2 to 3 PCLK *7
0008 830Ah	RIIC0	Internal control for timeout L	TMOCNTL	16	16	2 to 3 PCLK *7
0008 830Bh	RIIC0	Slave address register U0	SARU0	8	8	2 to 3 PCLK *7
0008 830Bh	RIIC0	Internal control for timeout U	TMOCNTU	16	16	2 to 3 PCLK *7
0008 830Ch	RIIC0	Slave address register L1	SARL1	8	8	2 to 3 PCLK *7
0008 830Dh	RIIC0	Slave address register U1	SARU1	8	8	2 to 3 PCLK *7
0008 830Eh	RIIC0	Slave address register L2	SARL2	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 830Fh	RIIC0	Slave address register U2	SARU2	8	8	2 to 3 PCLK *7
0008 8310h	RIIC0	I²C bus bit rate low-level register	ICBRL	8	8	2 to 3 PCLK *7
0008 8311h	RIIC0	I²C bus bit rate high-level register	ICBRH	8	8	2 to 3 PCLK *7
0008 8312h	RIIC0	I²C bus transmit data register	ICDRT	8	8	2 to 3 PCLK *7
0008 8313h	RIIC0	I²C bus receive data register	ICDRR	8	8	2 to 3 PCLK *7
0008 8320h	RIIC1	I²C bus control register 1	ICCR1	8	8	2 to 3 PCLK *7
0008 8321h	RIIC1	I²C bus control register 2	ICCR2	8	8	2 to 3 PCLK *7
0008 8322h	RIIC1	I²C bus mode register 1	ICMR1	8	8	2 to 3 PCLK *7
0008 8323h	RIIC1	I²C bus mode register 2	ICMR2	8	8	2 to 3 PCLK *7
0008 8324h	RIIC1	I²C bus mode register 3	ICMR3	8	8	2 to 3 PCLK *7
0008 8325h	RIIC1	I²C bus function enable register	ICFER	8	8	2 to 3 PCLK *7
0008 8326h	RIIC1	I²C bus status enable register	ICSER	8	8	2 to 3 PCLK *7
0008 8327h	RIIC1	I²C bus interrupt enable register	ICIER	8	8	2 to 3 PCLK *7
0008 8328h	RIIC1	I²C bus status register 1	ICSR1	8	8	2 to 3 PCLK *7
0008 8329h	RIIC1	I²C bus status register 2	ICSR2	8	8	2 to 3 PCLK *7
0008 832Ah	RIIC1	Slave address register L0	SARL0	8	8	2 to 3 PCLK *7
0008 832Ah	RIIC1	Internal control for timeout L	TMOCNTL	16	16	2 to 3 PCLK *7
0008 832Bh	RIIC1	Slave address register U0	SARU0	8	8	2 to 3 PCLK *7
0008 832Bh	RIIC1	Internal control for timeout U	TMOCNTU	16	16	2 to 3 PCLK *7
0008 832Ch	RIIC1	Slave address register L1	SARL1	8	8	2 to 3 PCLK *7
0008 832Dh	RIIC1	Slave address register U1	SARU1	8	8	2 to 3 PCLK *7
0008 832Eh	RIIC1	Slave address register L2	SARL2	8	8	2 to 3 PCLK *7
0008 832Fh	RIIC1	Slave address register U2	SARU2	8	8	2 to 3 PCLK *7
0008 8330h	RIIC1	I²C bus bit rate low-level register	ICBRL	8	8	2 to 3 PCLK *7
0008 8331h	RIIC1	I²C bus bit rate high-level register	ICBRH	8	8	2 to 3 PCLK *7
0008 8332h	RIIC1	I²C bus transmit data register	ICDRT	8	8	2 to 3 PCLK *7
0008 8333h	RIIC1	I²C bus receive data register	ICDRR	8	8	2 to 3 PCLK *7
0008 C000h	P0	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C001h	P1	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C002h	P2	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C003h	P3	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C004h	P4	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C005h	P5	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C006h	P6	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C007h	P7	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C008h	P8	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C009h	P9	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Ah	PA	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Bh	PB	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Ch	PC	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Dh	PD	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Eh	PE	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C00Fh	PF	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C010h	PG	Data direction register	DDR	8	8	2 to 3 PCLK *7
0008 C011h	PH	Data direction register	DDR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C020h	P0	Data register	DR	8	8	2 to 3 PCLK *7
0008 C021h	P1	Data register	DR	8	8	2 to 3 PCLK *7
0008 C022h	P2	Data register	DR	8	8	2 to 3 PCLK *7
0008 C023h	P3	Data register	DR	8	8	2 to 3 PCLK *7
0008 C024h	P4	Data register	DR	8	8	2 to 3 PCLK *7
0008 C025h	P5	Data register	DR	8	8	2 to 3 PCLK *7
0008 C026h	P6	Data register	DR	8	8	2 to 3 PCLK *7
0008 C027h	P7	Data register	DR	8	8	2 to 3 PCLK *7
0008 C028h	P8	Data register	DR	8	8	2 to 3 PCLK *7
0008 C029h	P9	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Ah	PA	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Bh	PB	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Ch	PC	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Dh	PD	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Eh	PE	Data register	DR	8	8	2 to 3 PCLK *7
0008 C02Fh	PF	Data register	DR	8	8	2 to 3 PCLK *7
0008 C030h	PG	Data register	DR	8	8	2 to 3 PCLK *7
0008 C031h	PH	Data register	DR	8	8	2 to 3 PCLK *7
0008 C040h	P0	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C041h	P1	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C042h	P2	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C043h	P3	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C044h	P4	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C045h	P5	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C046h	P6	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C047h	P7	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C048h	P8	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C049h	P9	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Ah	PA	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Bh	PB	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Ch	PC	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Dh	PD	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Eh	PE	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C04Fh	PF	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C050h	PG	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C051h	PH	Port register	PORT	8	8	2 to 3 PCLK *7
0008 C060h	P0	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C061h	P1	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C062h	P2	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C063h	P3	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C064h	P4	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C065h	P5	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C066h	P6	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C067h	P7	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C068h	P8	Input buffer control register	ICR	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C069h	P9	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C06Ah	PA	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C06Bh	PB	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C06Ch	PC	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C06Dh	PD	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C06Eh	PE	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C06Fh	PF	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C070h	PG	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C071h	PH	Input buffer control register	ICR	8	8	2 to 3 PCLK *7
0008 C082h	P2	Open drain control register	ODR	8	8	2 to 3 PCLK *7
0008 C08Ch	PC	Open drain control register	ODR	8	8	2 to 3 PCLK *7
0008 C0CAh	PA	Pull-Up resistor control register	PCR	8	8	2 to 3 PCLK *7
0008 C0CBh	PB	Pull-Up resistor control register	PCR	8	8	2 to 3 PCLK *7
0008 C0CCh	PC	Pull-Up resistor control register	PCR	8	8	2 to 3 PCLK *7
0008 C0CDh	PD	Pull-Up resistor control register	PCR	8	8	2 to 3 PCLK *7
0008 C0CEh	PE	Pull-Up resistor control register	PCR	8	8	2 to 3 PCLK *7
0008 C100h	I/O PORT	Port function control register 0	PFCR0	8	8	2 to 3 PCLK *7
0008 C101h	I/O PORT	Port function control register 1	PFCR1	8	8	2 to 3 PCLK *7
0008 C102h	I/O PORT	Port function control register 2	PFCR2	8	8	2 to 3 PCLK *7
0008 C103h	I/O PORT	Port function control register 3	PFCR3	8	8	2 to 3 PCLK *7
0008 C104h	I/O PORT	Port function control register 4	PFCR4	8	8	2 to 3 PCLK *7
0008 C105h	I/O PORT	Port function control register 5	PFCR5	8	8	2 to 3 PCLK *7
0008 C106h	I/O PORT	Port function control register 6	PFCR6	8	8	2 to 3 PCLK *7
0008 C107h	I/O PORT	Port function control register 7	PFCR7	8	8	2 to 3 PCLK *7
0008 C108h	I/O PORT	Port function control register 8	PFCR8	8	8	2 to 3 PCLK *7
0008 C109h	I/O PORT	Port function control register 9	PFCR9	8	8	2 to 3 PCLK *7
0008 C280h	SYSTEM	Deep standby control register	DPSBYCR	8	8	4 to 5 PCLK *7
0008 C281h	SYSTEM	Deep standby wait control register	DPSWCR	8	8	4 to 5 PCLK *7
0008 C282h	SYSTEM	Deep standby interrupt enable register	DPSIER	8	8	4 to 5 PCLK *7
0008 C283h	SYSTEM	Deep standby interrupt flag register	DPSIFR	8	8	4 to 5 PCLK *7
0008 C284h	SYSTEM	Deep standby interrupt edge register	DPSIEGR	8	8	4 to 5 PCLK *7
0008 C285h	SYSTEM	Reset status register	RSTSR	8	8	4 to 5 PCLK *7
0008 C289h	FLASH	Flash write erase protection register	FWEPROR	8	8	4 to 5 PCLK *7
0008 C290h	SYSTEM	Deep standby backup register 0	DPSBKR0	8	8	4 to 5 PCLK *7
0008 C291h	SYSTEM	Deep standby backup register 1	DPSBKR1	8	8	4 to 5 PCLK *7
0008 C292h	SYSTEM	Deep standby backup register 2	DPSBKR2	8	8	4 to 5 PCLK *7
0008 C293h	SYSTEM	Deep standby backup register 3	DPSBKR3	8	8	4 to 5 PCLK *7
0008 C294h	SYSTEM	Deep standby backup register 4	DPSBKR4	8	8	4 to 5 PCLK *7
0008 C295h	SYSTEM	Deep standby backup register 5	DPSBKR5	8	8	4 to 5 PCLK *7
0008 C296h	SYSTEM	Deep standby backup register 6	DPSBKR6	8	8	4 to 5 PCLK *7
0008 C297h	SYSTEM	Deep standby backup register 7	DPSBKR7	8	8	4 to 5 PCLK *7
0008 C298h	SYSTEM	Deep standby backup register 8	DPSBKR8	8	8	4 to 5 PCLK *7
0008 C299h	SYSTEM	Deep standby backup register 9	DPSBKR9	8	8	4 to 5 PCLK *7
0008 C29Ah	SYSTEM	Deep standby backup register 10	DPSBKR10	8	8	4 to 5 PCLK *7
0008 C29Bh	SYSTEM	Deep standby backup register 11	DPSBKR11	8	8	4 to 5 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C29Ch	SYSTEM	Deep standby backup register 12	DPSBKR12	8	8	4 to 5 PCLK *7
0008 C29Dh	SYSTEM	Deep standby backup register 13	DPSBKR13	8	8	4 to 5 PCLK *7
0008 C29Eh	SYSTEM	Deep standby backup register 14	DPSBKR14	8	8	4 to 5 PCLK *7
0008 C29Fh	SYSTEM	Deep standby backup register 15	DPSBKR15	8	8	4 to 5 PCLK *7
0008 C2A0h	SYSTEM	Deep standby backup register 16	DPSBKR16	8	8	4 to 5 PCLK *7
0008 C2A1h	SYSTEM	Deep standby backup register 17	DPSBKR17	8	8	4 to 5 PCLK *7
0008 C2A2h	SYSTEM	Deep standby backup register 18	DPSBKR18	8	8	4 to 5 PCLK *7
0008 C2A3h	SYSTEM	Deep standby backup register 19	DPSBKR19	8	8	4 to 5 PCLK *7
0008 C2A4h	SYSTEM	Deep standby backup register 20	DPSBKR20	8	8	4 to 5 PCLK *7
0008 C2A5h	SYSTEM	Deep standby backup register 21	DPSBKR21	8	8	4 to 5 PCLK *7
0008 C2A6h	SYSTEM	Deep standby backup register 22	DPSBKR22	8	8	4 to 5 PCLK *7
0008 C2A7h	SYSTEM	Deep standby backup register 23	DPSBKR23	8	8	4 to 5 PCLK *7
0008 C2A8h	SYSTEM	Deep standby backup register 24	DPSBKR24	8	8	4 to 5 PCLK *7
0008 C2A9h	SYSTEM	Deep standby backup register 25	DPSBKR25	8	8	4 to 5 PCLK *7
0008 C2AAh	SYSTEM	Deep standby backup register 26	DPSBKR26	8	8	4 to 5 PCLK *7
0008 C2ABh	SYSTEM	Deep standby backup register 27	DPSBKR27	8	8	4 to 5 PCLK *7
0008 C2ACh	SYSTEM	Deep standby backup register 28	DPSBKR28	8	8	4 to 5 PCLK *7
0008 C2ADh	SYSTEM	Deep standby backup register 29	DPSBKR29	8	8	4 to 5 PCLK *7
0008 C2AEh	SYSTEM	Deep standby backup register 30	DPSBKR30	8	8	4 to 5 PCLK *7
0008 C2AFh	SYSTEM	Deep standby backup register 31	DPSBKR31	8	8	4 to 5 PCLK *7
0008 C300h	ICU	IRQ detection enable registrar 0	IRQER0	8	8	2 to 3 PCLK *7
0008 C301h	ICU	IRQ detection enable registrar 1	IRQER1	8	8	2 to 3 PCLK *7
0008 C302h	ICU	IRQ detection enable registrar 2	IRQER2	8	8	2 to 3 PCLK *7
0008 C303h	ICU	IRQ detection enable registrar 3	IRQER3	8	8	2 to 3 PCLK *7
0008 C304h	ICU	IRQ detection enable registrar 4	IRQER4	8	8	2 to 3 PCLK *7
0008 C305h	ICU	IRQ detection enable registrar 5	IRQER5	8	8	2 to 3 PCLK *7
0008 C306h	ICU	IRQ detection enable registrar 6	IRQER6	8	8	2 to 3 PCLK *7
0008 C307h	ICU	IRQ detection enable registrar 7	IRQER7	8	8	2 to 3 PCLK *7
0008 C308h	ICU	IRQ detection enable registrar 8	IRQER8	8	8	2 to 3 PCLK *7
0008 C309h	ICU	IRQ detection enable registrar 9	IRQER9	8	8	2 to 3 PCLK *7
0008 C30Ah	ICU	IRQ detection enable registrar 10	IRQER10	8	8	2 to 3 PCLK *7
0008 C30Bh	ICU	IRQ detection enable registrar 11	IRQER11	8	8	2 to 3 PCLK *7
0008 C30Ch	ICU	IRQ detection enable registrar 12	IRQER12	8	8	2 to 3 PCLK *7
0008 C30Dh	ICU	IRQ detection enable registrar 13	IRQER13	8	8	2 to 3 PCLK *7
0008 C30Eh	ICU	IRQ detection enable registrar 14	IRQER14	8	8	2 to 3 PCLK *7
0008 C30Fh	ICU	IRQ detection enable registrar 15	IRQER15	8	8	2 to 3 PCLK *7
0008 C320h	ICU	IRQ control register 0	IRQCR0	8	8	2 to 3 PCLK *7
0008 C321h	ICU	IRQ control register 1	IRQCR1	8	8	2 to 3 PCLK *7
0008 C322h	ICU	IRQ control register 2	IRQCR2	8	8	2 to 3 PCLK *7
0008 C323h	ICU	IRQ control register 3	IRQCR3	8	8	2 to 3 PCLK *7
0008 C324h	ICU	IRQ control register 4	IRQCR4	8	8	2 to 3 PCLK *7
0008 C325h	ICU	IRQ control register 5	IRQCR5	8	8	2 to 3 PCLK *7
0008 C326h	ICU	IRQ control register 6	IRQCR6	8	8	2 to 3 PCLK *7
0008 C327h	ICU	IRQ control register 7	IRQCR7	8	8	2 to 3 PCLK *7
0008 C328h	ICU	IRQ control register 8	IRQCR8	8	8	2 to 3 PCLK *7

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C329h	ICU	IRQ control register 9	IRQCR9	8	8	2 to 3 PCLK *7
0008 C32Ah	ICU	IRQ control register 10	IRQCR10	8	8	2 to 3 PCLK *7
0008 C32Bh	ICU	IRQ control register 11	IRQCR11	8	8	2 to 3 PCLK *7
0008 C32Ch	ICU	IRQ control register 12	IRQCR12	8	8	2 to 3 PCLK *7
0008 C32Dh	ICU	IRQ control register 13	IRQCR13	8	8	2 to 3 PCLK *7
0008 C32Eh	ICU	IRQ control register 14	IRQCR14	8	8	2 to 3 PCLK *7
0008 C32Fh	ICU	IRQ control register 15	IRQCR15	8	8	2 to 3 PCLK *7
0008 C340h	ICU	Software standby release IRQ enable register	SSIER	16	16	2 to 3 PCLK *7
0008 C350h	ICU	Non-maskable interrupt enable register	NMIER	8	8	2 to 3 PCLK *7
0008 C351h	ICU	NMI pin interrupt control register	NMICR	8	8	2 to 3 PCLK *7
0008 C352h	ICU	Non-maskable interrupt status register	NMISR	8	8	2 to 3 PCLK *7
0008 C353h	ICU	Non-maskable interrupt clear register	NMICLR	8	8	2 to 3 PCLK *7
007F C402h	FLASH	Flash mode register	FMODR	8	8	2 to 3 PCLK *7
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2 to 3 PCLK *7
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2 to 3 PCLK *7
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2 to 3 PCLK *7
007F C440h	FLASH	Data flash read enable register	DFLRE	16	16	2 to 3 PCLK *7
007F C450h	FLASH	Data flash programming/erasure enable register	DFLWE	16	16	2 to 3 PCLK *7
007F C454h	FLASH	FCU RAM enable register	FCURAME	16	16	2 to 3 PCLK *7
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2 to 3 PCLK *7
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2 to 3 PCLK *7
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2 to 3 PCLK *7
007F FFB4h	FLASH	Flash protection register	FPROTR	16	16	2 to 3 PCLK *7
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2 to 3 PCLK *7
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2 to 3 PCLK *7
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2 to 3 PCLK *7
007F FFCAh	FLASH	Data flash blank check control register	DFLBCCNT	16	16	2 to 3 PCLK *7
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2 to 3 PCLK *7
007F FFCEh	FLASH	Data flash blank check status register	DFLBCSTAT	16	16	2 to 3 PCLK *7
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2 to 3 PCLK *7

Notes:
1. When the same output trigger is specified for pulse output groups 2 and 3 by the PPG0.PCR setting, the PPG0.NDRH address is 000881ECh. When different output triggers are specified, the PPG0.NDRH addresses for pulse output groups 2 and 3 are 000881EEh and 000881ECh, respectively.
2. When the same output trigger is specified for pulse output groups 0 and 1 by the PPG0.PCR setting, the PPG0.NDRL address is 000881EDh. When different output triggers are specified, the PPG0.NDRL addresses for pulse output groups 0 and 1 are 000881EFh and 000881EDh, respectively.
3. When the same output trigger is specified for pulse output groups 6 and 7 by the PPG1.PCR setting, the PPG1.NDRH address is 000881FCh. When different output triggers are specified, the PPG1.NDRH addresses for pulse output groups 6 and 7 are 000881FEh and 000881FCh, respectively.
4. When the same output trigger is specified for pulse output groups 4 and 5 by the PPG1.PCR setting, the PPG1.NDRL address is 000881FDh. When different output triggers are specified, the PPG1.NDRL addresses for pulse output groups 4 and 5 are 000881FFh and 000881FDh, respectively.
5. 16-bit access to odd addresses is prohibited. When 16-bit access is required, access is at the address corresponding to TMR0 or TMR2.
6. For certain bits, functions differ according to whether the mode is serial communications or smart card interface.
7. The number of access cycles varies depending on the number of divided cycles for clock synchronization (0 to one PCLK).
8. The number of access cycles may be 5 ICLK if the register is accessed during the DMAC operation.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}, $PLLV_{CC}$	-0.3 to +4.6	V
Input voltage (except for ports 0, 14 to 17)	V_{in}	-0.3 to V_{CC} +0.3	V
Input voltage (ports 0, 14 to 17*1)	V_{in}	-0.3 to +6.5	V
Reference power supply voltage	V_{REFH}	-0.3 to V_{CC} +0.3	V
Analog power supply voltage	AV_{CC}*2	-0.3 to +4.6	V
Analog input voltage	V_{AN}	-0.3 to V_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: -20 to +85	°C
		Wide-range specifications: -40 to +85	
Storage temperature	T_{stg}	-55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Notes: 1. Ports 0, and 14 to 17 are 5 V tolerant.

2. Connect AV_{CC} to V_{CC}. When neither the A/D converter nor the D/A converter is in use, do not leave the AV_{SS}, V_{REFH}, and V_{REFL} pins open. Connect the AV_{CC} and V_{REFH} pins to V_{CC}, and the AV_{SS} and V_{REFL} pins to V_{SS}, respectively.

5.2 DC Characteristics

Table 5.2 DC Characteristics

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin*1 TPU input pin*1 TMR input pin*1 SCI input pin*1 ADTRG# input pin*1 RES#, NMI	V_{IH}	V_{CC} x 0.8	—	V_{CC} + 0.3	V	
		V_{IL}	-0.3	—	V_{CC} x 0.2		
		ΔV_T	V_{CC} x 0.06	—	—		
	RIIC input pin	V_{IH}	V_{CC} x 0.7	—	5.8		
		V_{IL}	-0.3	—	V_{CC} x 0.3		
		ΔV_T	V_{CC} x 0.05	—	—		
	Ports 0, 14 to 17*2	V_{IH}	V_{CC} x 0.8	—	5.8		
		V_{IL}	-0.3	—	V_{CC} x 0.2		
	Ports 10 to 13, ports 2 to E (144-pin LQFP) ports 2 to H (176-pin LFBGA) Other input pins	V_{IH}	V_{CC} x 0.8	—	V_{CC} + 0.3		
		V_{IL}	-0.3	—	V_{CC} x 0.2		
Input high voltage (except Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	V_{CC} x 0.9	—	V_{CC} + 0.3	V	
	EXTAL		V_{CC} x 0.8	—	V_{CC} + 0.3		
	D0 to D15		V_{CC} x 0.7	—	V_{CC} + 0.3		
Input low voltage (except Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	-0.3	—	V_{CC} x 0.1	V	
	EXTAL		-0.3	—	V_{CC} x 0.2		
	D0 to D15		-0.3	—	V_{CC} x 0.3		
Output high voltage	All output pins	V_{OH}	V_{CC}-0.5	—	—	V	I_{OH} = -1 mA
Output low voltage	All output pins (except for RIIC pins)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	RIIC pins		—	—	0.4		I_{OL} = 3.0 mA
			—	—	0.6		I_{OL} = 6.0 mA
	RIIC pins (only P14 and P15 in channel 1)		—	—	0.4		I_{OL} = 15 mA (ICFER.FMPE = 1)
			—	0.4	—		I_{OL} = 20 mA (ICFER.FMPE = 1)
Input leakage current	RES#, MD pin, EMLE, NMI	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, V_{CC}
Three-state leakage current (off state)	Ports 10 to 13, ports 2 to E (144-pin LQFP) ports 2 to H (176-pin LFBGA)	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V, V_{CC}
	Port 0, ports 14 to 17		—	—	5.0		

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input pull-up resistor current	Ports A to E			$-I_p$	10	—	300	µA	V_{CC} = 3.0 to 3.6 V, V_{in} = 0 V
Input capacitance	All input pins (except port 0, ports 14 to 17)			C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	Port 0, ports 14 to 17				—	—	30		
Supply current*3	In operation	Max.*4		I_{CC}*5	—	—	100	mA	ICLK = 100 MHz PCLK = 50 MHz BCLK = 25 MHz
		Normal*6			—	35	—		
		Increased by BGO operation*7			—	15	—		
	Sleep				—	18	52		
	All-module-clock-stop mode*8				—	14	28		
	Standby mode	Software standby mode			—	0.08	3.0		
		Deep software standby mode	RAM retained		—	15	200	µA	
			RAM power supply halted		—	0.9	26		
Analog power supply current	During A/D conversion (per unit)			AI_{CC}	—	0.8	1.2	mA	
	During D/A conversion (per unit)				—	0.3	1.0	µA	
	Idle (all units)				—	0.3	1.0		
Reference power supply current	During A/D conversion (per unit)				—	0.06	0.1	mA	
	During D/A conversion (per unit)				—	0.4	0.6		
	Idle (all units)				—	0.3	1.0	µA	
RAM standby voltage				V_{RAM}	2.5	—	—	V	
V_{CC} start voltage*9				$V_{CCSTART}$	—	—	0.8	V	
V_{CC} rising gradient*9				SV_{CC}	—	—	20	ms/V	

Notes:
1. This does not include the pins, which are multiplexed as ports 0, and 14 to 17 for 5 V tolerant.
2. This includes the multiplexed pins, but RIIC input pins for ports 14 to 17 are excluded.
3. Supply current values are with all output pins unloaded, all input pins for V_{IH} = V_{CC} and V_{IL}= 0 V, and all input pull-up resistors in the off state.
4. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
5. I_{CC} depends on f (ICLK) as follows. (ICLK : PCLK : BCLK = 8 : 4: 2)

   I_{CC} max. = 0.89 x f + 11 (max.)
   I_{CC} typ. = 0.30 x f + 5 (normal operation)
   I_{CC} max. = 0.41 x f + 11 (sleep mode)
6. Measured with clocks not supplied to the peripheral functions. This does not include the BGO operation.
7. Incremented if data is written to or erased from the ROM or data flash for data storage during the program execution.
8. The values are for reference.
9. This can be applied when the RES# pin is held low at power-on.

Table 5.3 Permissible Output Currents

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item		Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins except for RIIC pins	I_{OL}	—	—	2.0	mA
	RIIC pins (ICFER.FMPE = 0)	I_{OL}	—	—	6.0	mA
	RIIC pins (ICFER.FMPE = 1)	I_{OL}	—	—	20.0	mA
Permissible output low current (max. value per pin)	All output pins except for RIIC pins	I_{OL}	—	—	4.0	mA
	RIIC pins (ICFER.FMPE = 0)	I_{OL}	—	—	6.0	mA
	RIIC pins (ICFER.FMPE = 1)	I_{OL}	—	—	20.0	mA
Permissible output low current (total)	Total of all output pins	ΣI_{OL}	—	—	80	mA
Permissible output high current (average value per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (max. value per pin)	All output pins	$-I_{OH}$	—	—	4.0	mA
Permissible output high current (total)	Total of all output pins	$\Sigma-I_{OH}$	—	—	80	mA

Caution: To protect the LSI's reliability, do not exceed the output current values in table 5.3.

5.3 AC Characteristics

Table 5.4 Operation Frequency Value

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

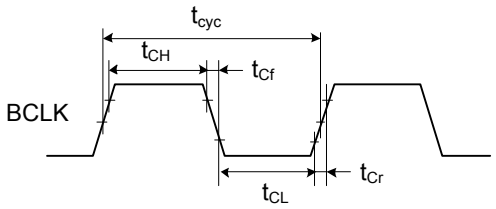
Item		Symbol	Min.	Typ.	Max.	Unit
Operation frequency	System clock (ICLK)	f	8	—	100	MHz
	Peripheral module clock (PCLK)		8	—	50	
	External bus clock (BCLK)		8	—	25	

5.3.1 Clock Timing

Table 5.5 Clock Timing

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V
ICLK = 8 to 100 MHz, BCLK = 8 to 25 MHz, PCLK = 8 to 50 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item	Symbol	Min.	Max.	Unit	Test Conditions
Clock cycle time	t_{cyc}	40	125	ns	Figure 5.1
Clock high pulse width	t_{CH}	15	—	ns	
Clock low pulse width	t_{CL}	15	—	ns	
Clock rising time	t_{Cr}	—	5	ns	
Clock falling time	t_{Cf}	—	5	ns	
Oscillation settling time after reset (crystal)	t_{OSC1}	10	—	ms	Figure 5.4
Oscillation settling time after leaving software standby mode (crystal)	t_{OSC2}	10	—	ms	Figure 5.2
Oscillation settling time after leaving deep software standby mode (crystal)	t_{OSC3}	10	—	ms	Figure 5.3
External clock output delay settling time	t_{DEXT}	1	—	ms	Figure 5.4
External clock input low pulse width	t_{EXL}	30.71	—	ns	Figure 5.5
External clock input high pulse width	t_{EXH}	30.71	—	ns	
External clock rising time	t_{EXr}	—	5	ns	
External clock falling time	t_{EXf}	—	5	ns	



Test conditions V_{OH} = V_{CC} × 0.7, V_{OL} = V_{CC} × 0.3, I_{OH} = - 1.0mA, I_{OL} = 1.0mA, C = 30pF

Figure 5.1 External Bus Clock Timing

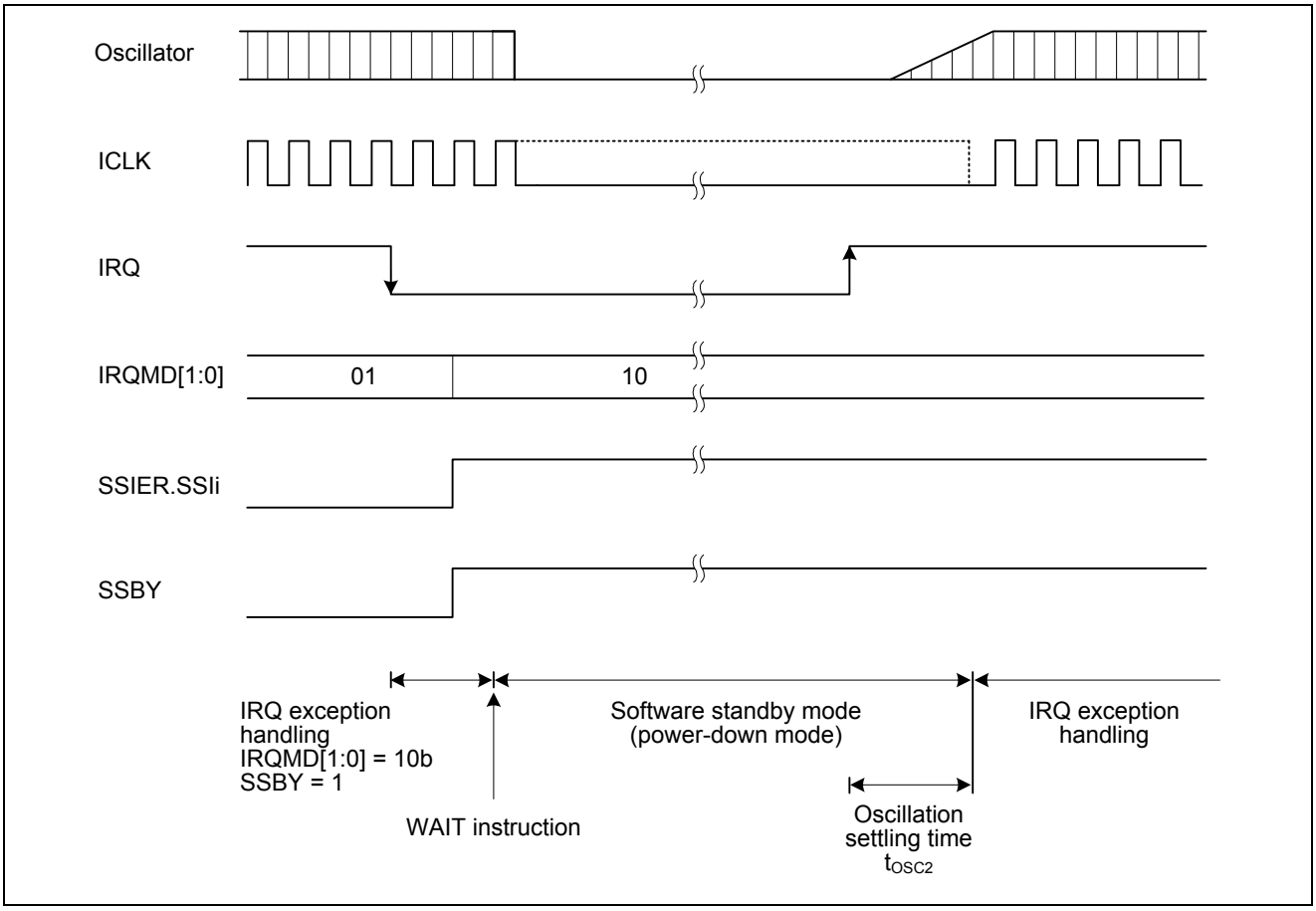


Figure 5.2 Oscillation Settling Timing after Software Standby Mode

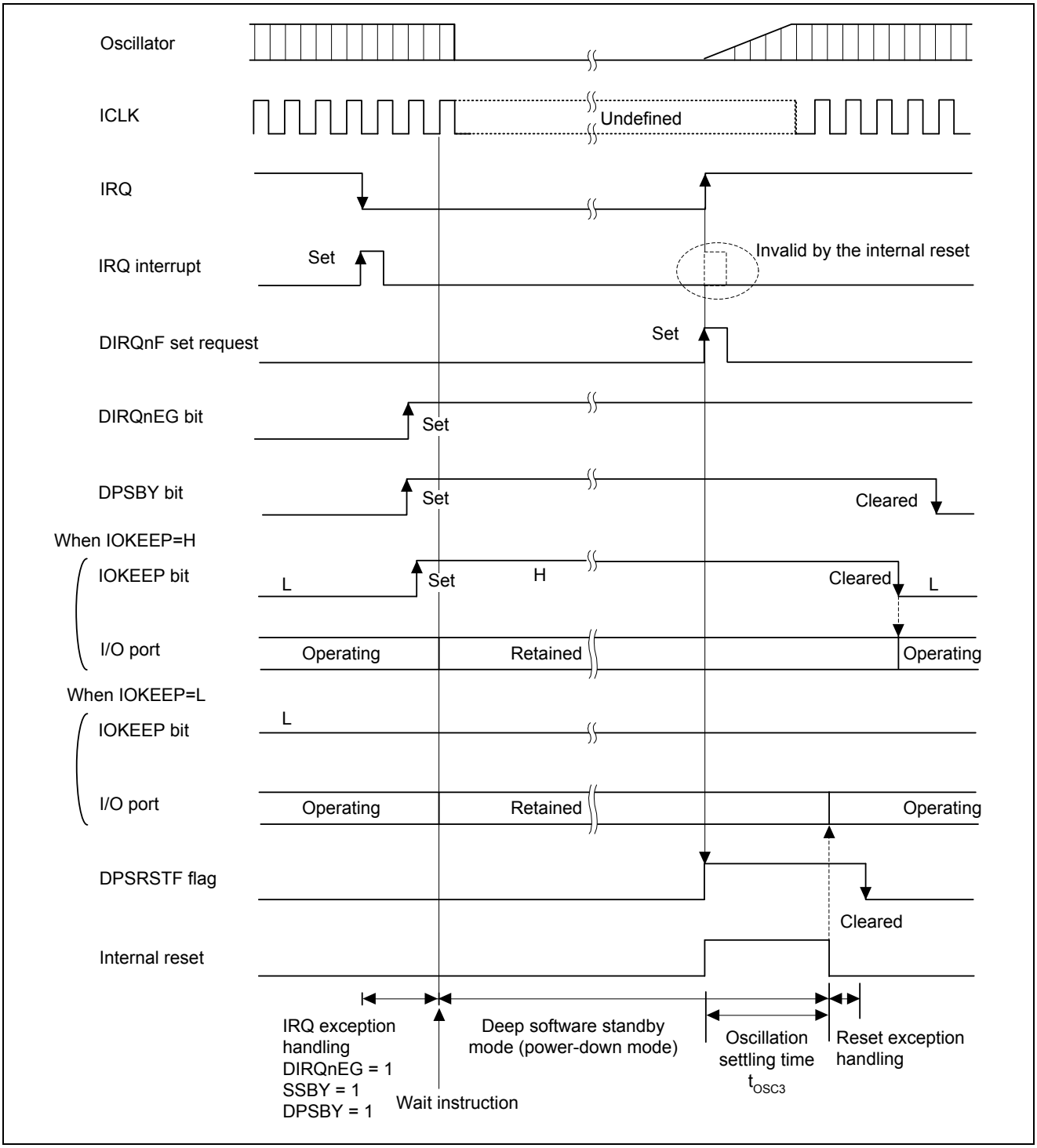


Figure 5.3 Oscillation Settling Timing after Deep Software Standby Mode

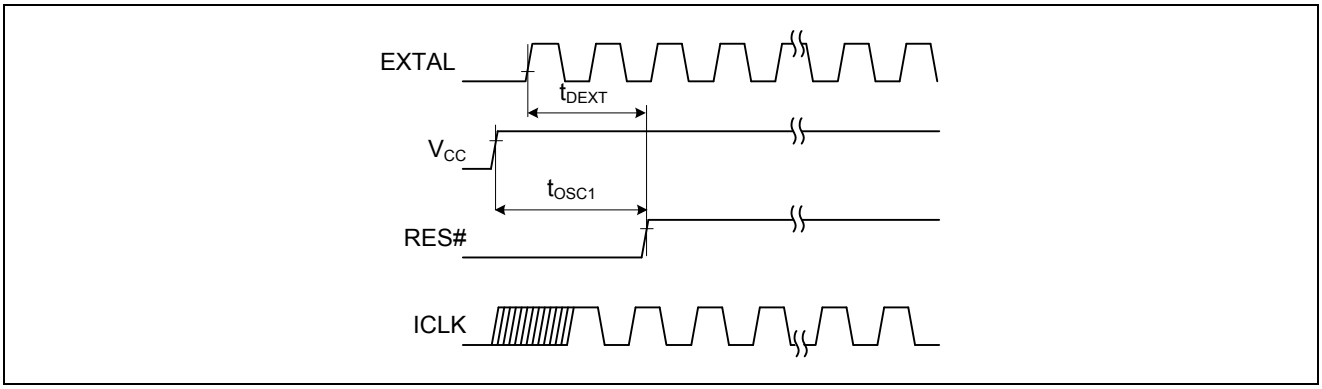


Figure 5.4 Oscillation Settling Timing

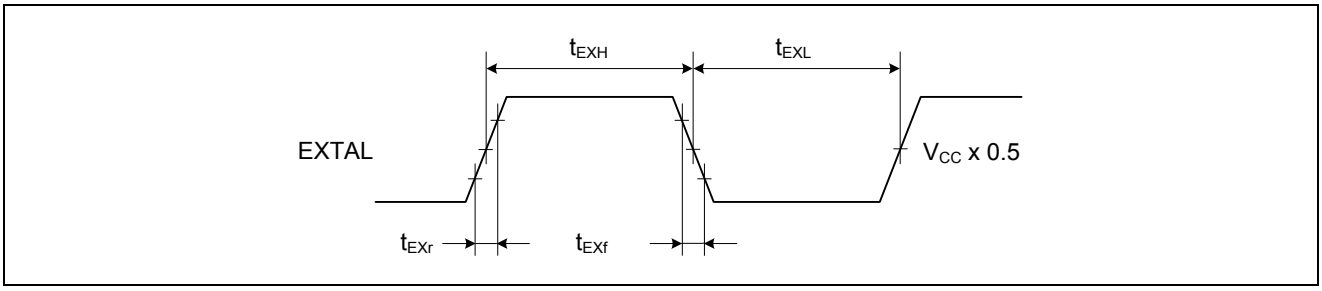


Figure 5.5 External Input Clock Timing

5.3.2 Control Signal Timing

Table 5.6 Control Signal Timing

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V
ICLK = 8 to 100 MHz, BCLK = 8 to 25 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item	Symbol	Min.	Max.	Unit	Test Conditions
RES# pulse width (except for ROM, data flash programming/erasure)	t_{RESW}*1	20	—	t_{cyc}	Figure 5.6
		1.5	—	μs	
Internal reset time (during ROM, data flash programming/erasure)	t_{RESW2} *2	35	—	μs	
NMI pulse width	t_{NMIW}	200	—	ns	Figure 5.7
IRQ pulse width	t_{IRQW}	200	—	ns	Figure 5.8

Notes: 1. Both the time and the number of cycles should satisfy the specifications.
2. This is to specify the FCU reset and the WDT reset.

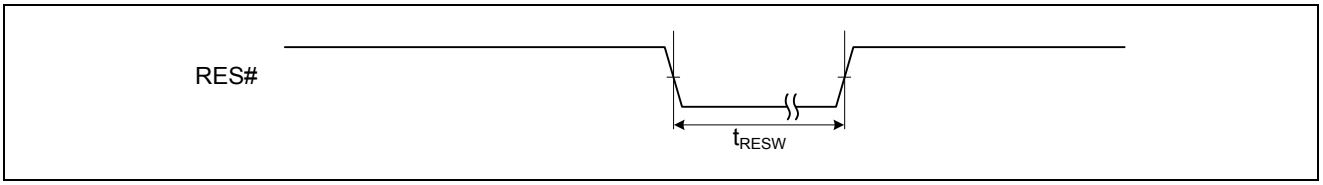


Figure 5.6 Reset Input Timing

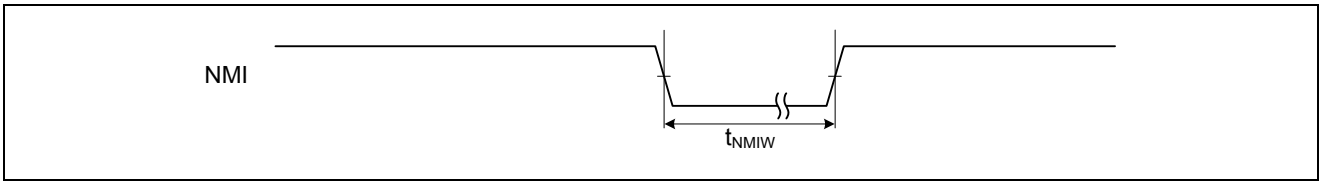


Figure 5.7 NMI Interrupt Input Timing

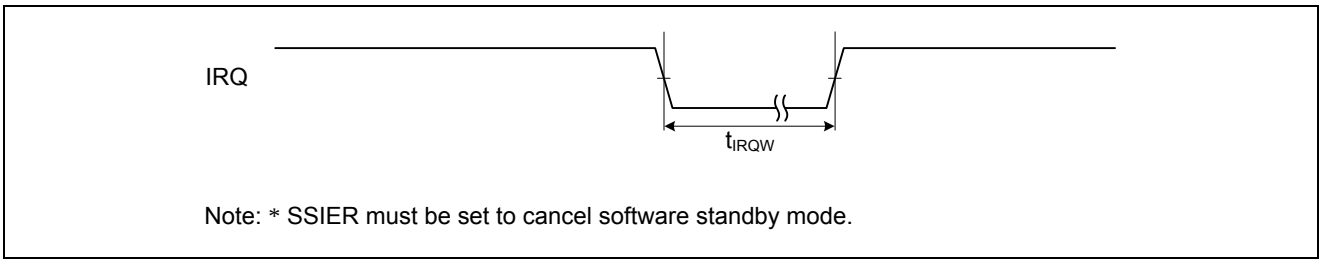


Figure 5.8 IRQ Interrupt Input Timing

5.3.3 Bus Timing

Table 5.7 Bus Timing

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V, BCLK = 8 to 25 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)
Output load conditions: V_{OH} = V_{CC} x 0.5, V_{OL} = V_{CC} x 0.5, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	30	ns	Figures 5.9 to 5.12
Byte control delay time	t_{BCD}	—	30	ns	
CS# delay time	t_{CSD}	—	30	ns	
RD# delay time	t_{RSD}	—	20	ns	
RD# setup time	t_{RSS}	0.5 × (1/BCLK) - 20	—	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	20	ns	
WR# setup time	t_{WRS}	0.5 × (1/BCLK) - 20	—	ns	
Write data delay time	t_{WDD}	—	35	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	15	—	ns	Figure 5.13
WAIT# hold time	t_{WTH}	0	—	ns	

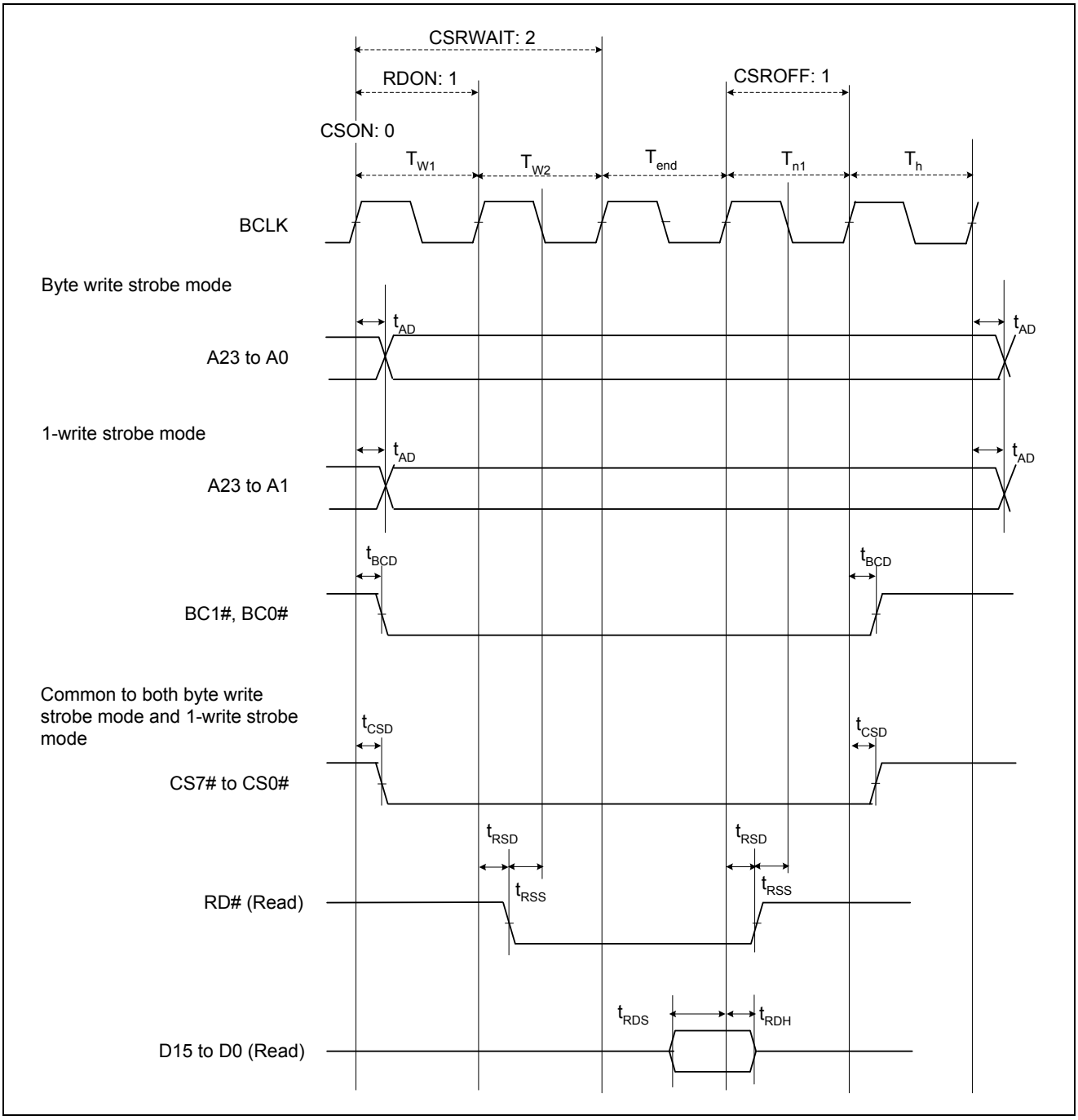
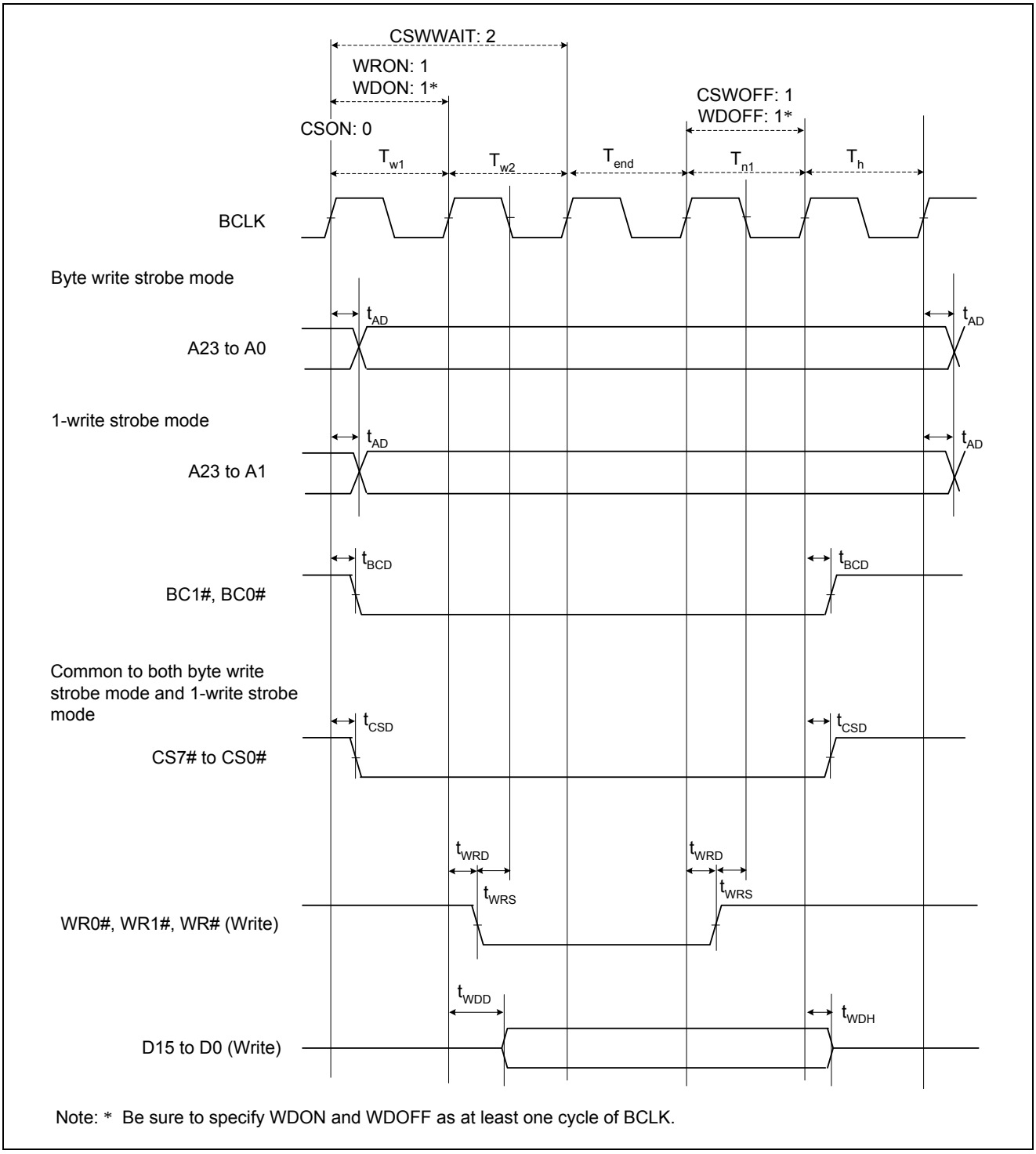


Figure 5.9 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)



Note: * Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 5.10 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

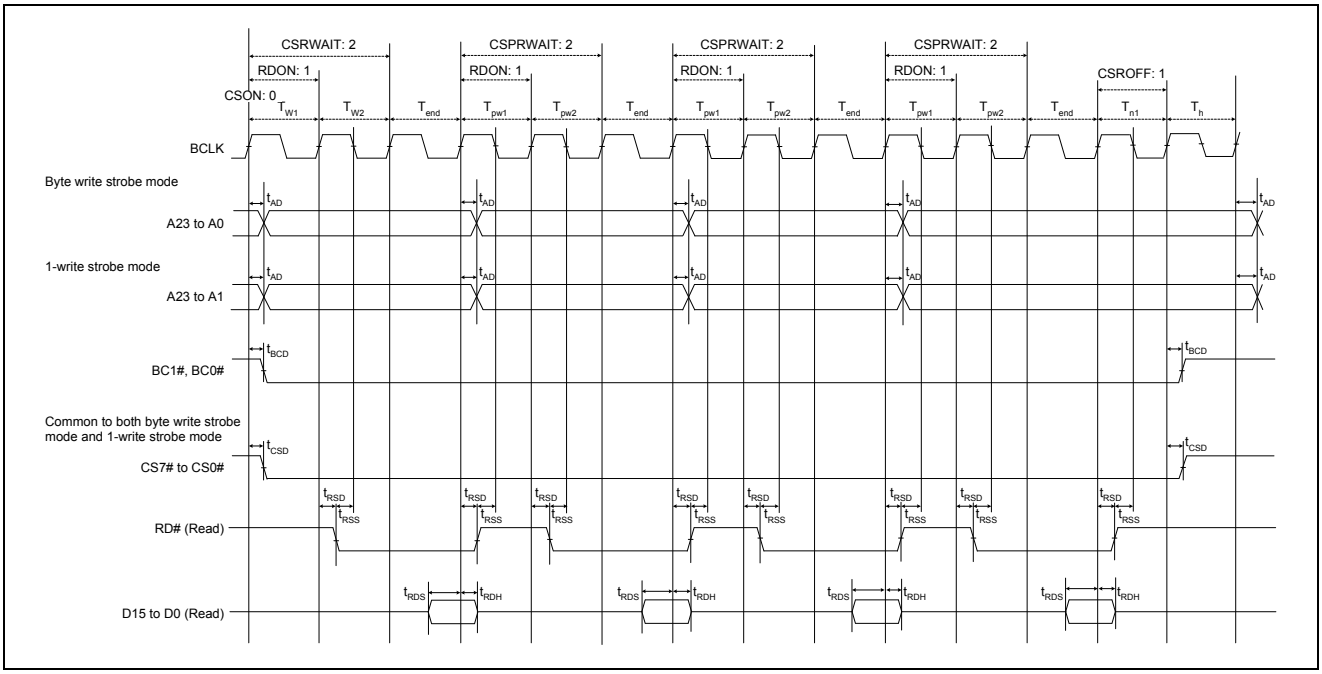


Figure 5.11 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)

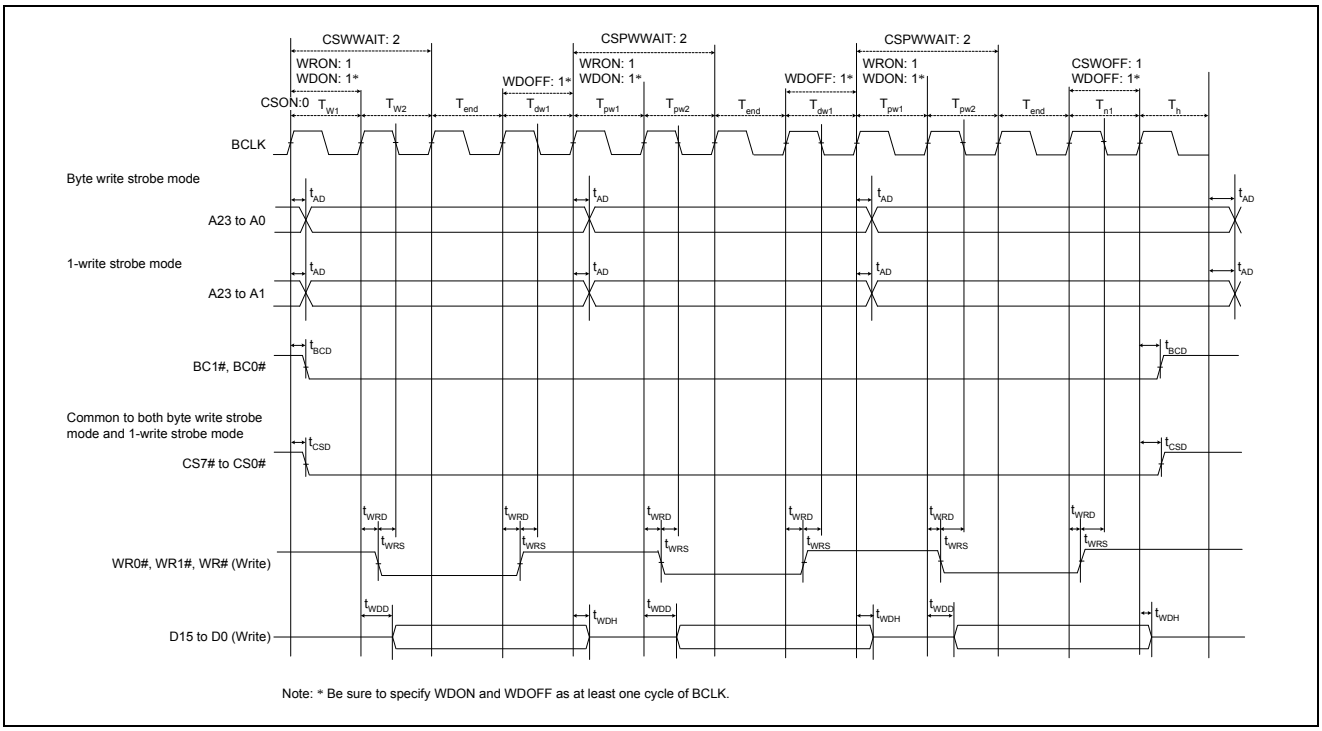


Figure 5.12 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

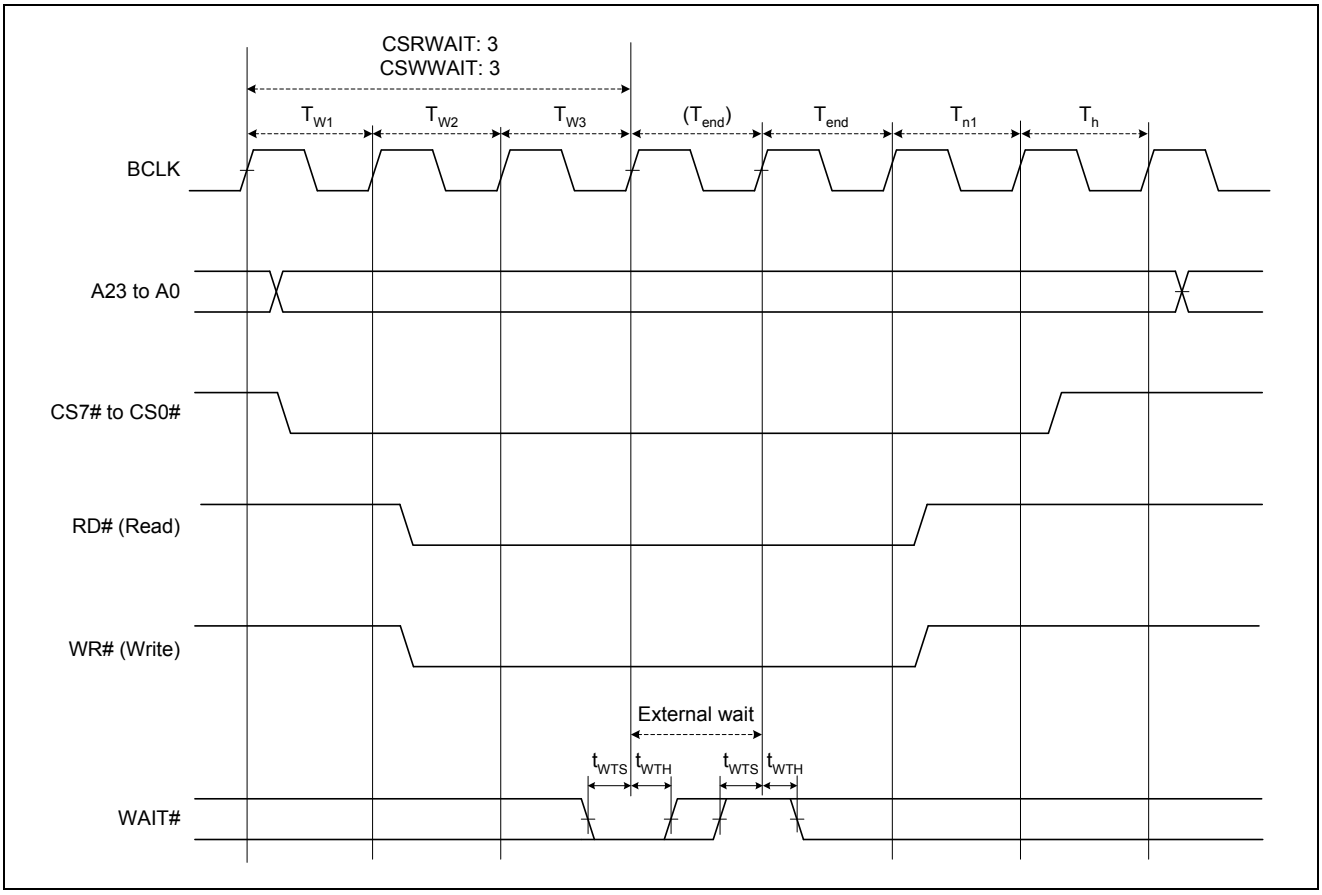


Figure 5.13 External Bus Timing/External Wait Control

5.3.4 Timing of On-Chip Peripheral Modules

Table 5.8 Timing of On-Chip Peripheral Modules (1)

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V, PCLK = 8 to 50 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)
Output load conditions: V_{OH} = V_{CC} x 0.5, V_{OL} = V_{CC} x 0.5, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Item			Symbol	Min.	Max.	Unit	Test Conditions
I/O ports	Output data delay time		t_{PWD}	—	40	ns	Figure 5.14
	Input data setup time		t_{PRS}	25	—	ns	
	Input data hold time		t_{PRH}	25	—	ns	
TPU	Timer output delay time		t_{TOCD}	—	40	ns	Figure 5.15
	Timer input setup time		t_{TICS}	25	—	ns	
	Timer clock input setup time		t_{TCKS}	25	—	ns	Figure 5.16
	Timer clock pulse width	Single-edge setting	t_{TCKWH}	1.5 x (1/PCLK)	—	t_{cyc}	
		Both-edge setting	t_{TCKWL}	2.5 x (1/PCLK)	—	t_{cyc}	
PPG	Pulse output delay time		t_{POD}	—	40	ns	Figure 5.17
8-bit timer	Timer output delay time		t_{TMOD}	—	40	ns	Figure 5.18
	Timer reset input setup time		t_{TMRS}	25	—	ns	Figure 5.19
	Timer clock input setup time		t_{TMCS}	25	—	ns	Figure 5.20
	Timer clock pulse width	Single-edge setting	t_{TMCWH}	1.5 x (1/PCLK)	—	t_{cyc}	
		Both-edge setting	t_{TMCWL}	2.5 x (1/PCLK)	—	t_{cyc}	
WDT	Overflow output delay time		t_{WOVD}	—	40	ns	Figure 5.21
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4 x (1/PCLK)	—	t_{cyc}	Figure 5.22
		Clock synchronous		6 x (1/PCLK)	—		
	Input clock pulse width		t_{SCKW}	0.4 x t_{Scyc}	0.6 x t_{Scyc}	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	20	ns	
	Input clock fall time		t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	4 x (1/PCLK)	—	t_{cyc}	
		Clock synchronous		6 x (1/PCLK)	—		
	Output clock pulse width		t_{SCKW}	0.4 x t_{Scyc}	0.6 x t_{Scyc}	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	20	ns	
	Output clock fall time		t_{SCKf}	—	20	ns	
	Transmit data delay time		t_{TXD}	—	40	ns	Figure 5.23
	Receive data setup time (clock synchronous)		t_{RXS}	40	—	ns	
	Receive data hold time (clock synchronous)		t_{RXH}	40	—	ns	
A/D converter	Trigger input setup time		t_{TRGS}	25	—	ns	Figure 5.24

Table 5.8 Timing of On-Chip Peripheral Modules (2)

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V, PCLK = 8 to 50 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item		Symbol	Min. *1*2	Max.	Unit	Test Conditions
RIIC (Standard-mode) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	8(10) x (1/PCLK) + 1300	—	ns	Figure 5.25
	SCL input high pulse width	t_{SCLH}	3(5) x (1/PCLK) + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	5x (1/PCLK) + 1000	—	ns	
	SCL, SDA input rising time	t_{Sr}	—	1000	ns	
	SCL, SDA input falling time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 x (1/PCLK)	ns	
	SDA input bus free time	t_{BUF}	5x (1/PCLK) + 1000	—	ns	
	Start condition input hold time	t_{STAH}	3(5) x (1/PCLK) + 300	—	ns	
	Re-start condition input setup time	t_{STAS}	5x (1/PCLK) + 1000	—	ns	
	Stop condition input setup time	t_{STOS}	3(5) x (1/PCLK) + 300	—	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	8(10) x (1/PCLK) + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(5) x (1/PCLK) + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	5 x (1/PCLK) + 300	—	ns	
	SCL, SDA input rising time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input falling time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 x (1/PCLK)	ns	
	SDA input bus free time	t_{BUF}	5 x (1/PCLK) + 300	—	ns	
	Start condition input hold time	t_{STAH}	3(5) x (1/PCLK) + 300	—	ns	
	Re-start condition input setup time	t_{STAS}	5 x (1/PCLK) + 300	—	ns	
	Stop condition input setup time	t_{STOS}	3(5) x (1/PCLK) + 300	—	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Table 5.8 Timing of On-Chip Peripheral Modules (3)

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V,
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item		Symbol	Min. *1*2	Max.	Unit	Test Conditions
RIIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	8(10) x (1/PCLK) + 240	—	ns	Figure 5.25
	SCL input high pulse width	t_{SCLH}	3(5) x (1/PCLK) + 120	—	ns	
	SCL input low pulse width	t_{SCLL}	5 x (1/PCLK) + 120	—	ns	
	SCL, SDA input rising time	t_{Sr}	—	120	ns	
	SCL, SDA input falling time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 x (1/PCLK)	ns	
	SDA input bus free time	t_{BUF}	5 x (1/PCLK) + 120	—	ns	
	Start condition input hold time	t_{STAH}	3(5) x (1/PCLK) + 120	—	ns	
	Re-start condition input setup time	t_{STAS}	5 x (1/PCLK) + 120	—	ns	
	Stop condition input setup time	t_{STOS}	3(5) x (1/PCLK) + 120	—	ns	
	Data input setup time	t_{SDAS}	50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	550	pF	
Boundary scan (176-pin LFBGA)	TCK clock cycle time	tTCKcyc	100	—	ns	Figure 5.26
	TCK clock high level pulse width	tTCKH	45	—	ns	
	TCK clock low level pulse width	tTCKL	45	—	ns	
	TCK clock rising time	tTCKr	—	5	ns	
	TCK clock falling time	tTCKf	—	5	ns	
	TRST# pulse width	tTRSTW	20	—	Tcyc	Figure 5.27
	TMS setup time	tTMSS	20	—	ns	Figure 5.28
	TMS hold time	tTMSH	20	—	ns	
	TDI setup time	tTDIS	20	—	ns	
	TDI hold time	tTDIH	20	—	ns	
	TDO data delay time	tTDOD	—	40	ns	

Notes:1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.

2. Cb indicates the total capacity of the bus line.

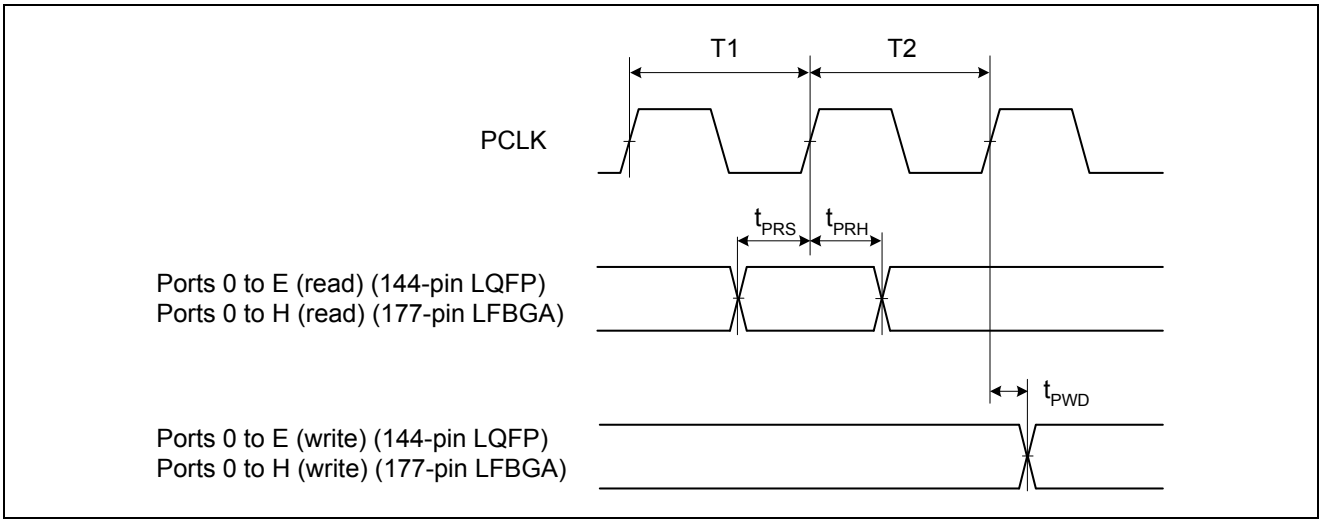


Figure 5.14 I/O Port Input/Output Timing

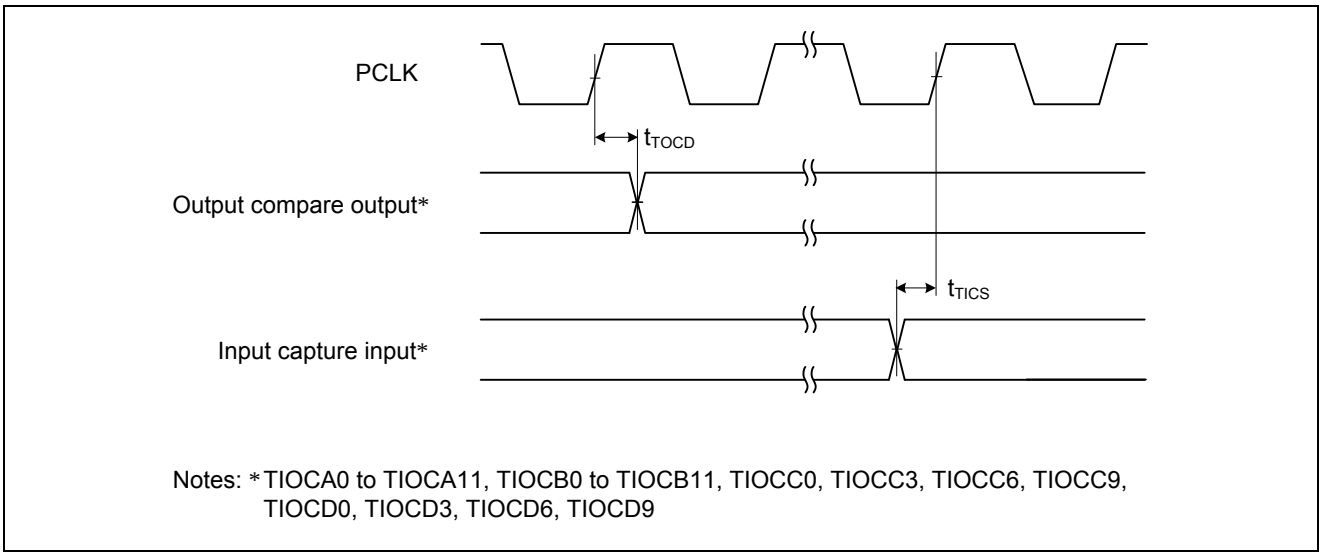


Figure 5.15 TPU Input/Output Timing

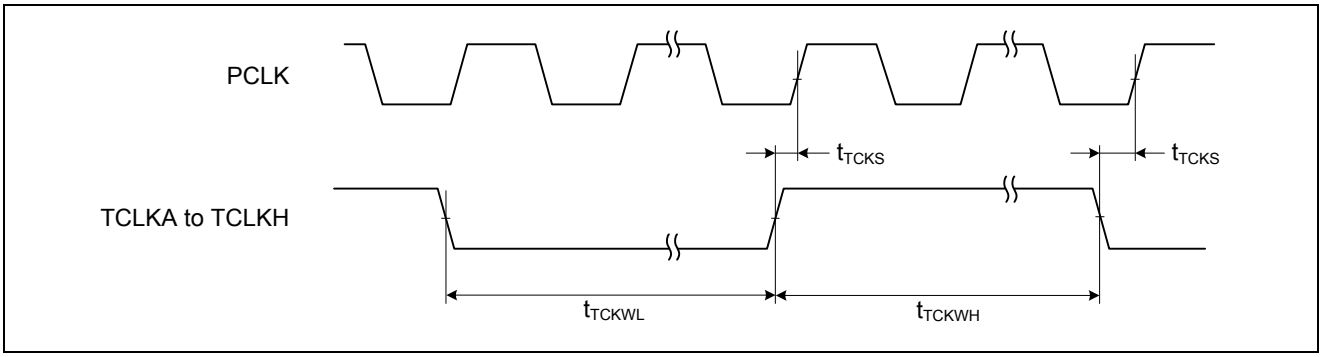


Figure 5.16 TPU Clock Input Timing

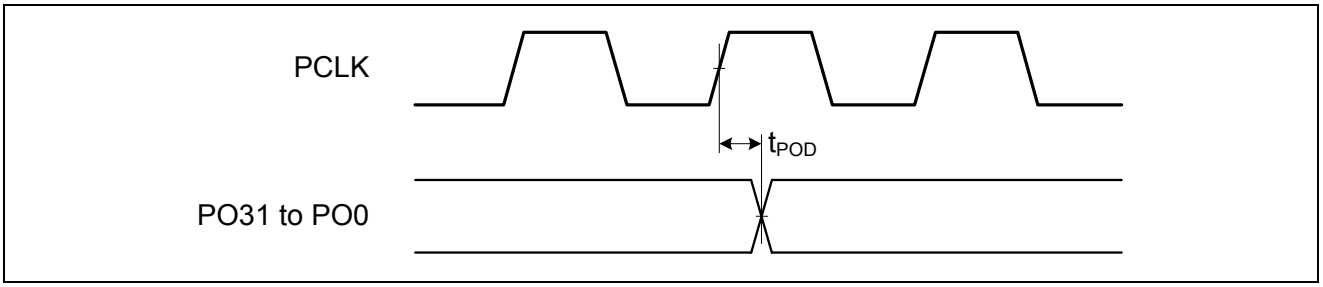


Figure 5.17 PPG Output Timing

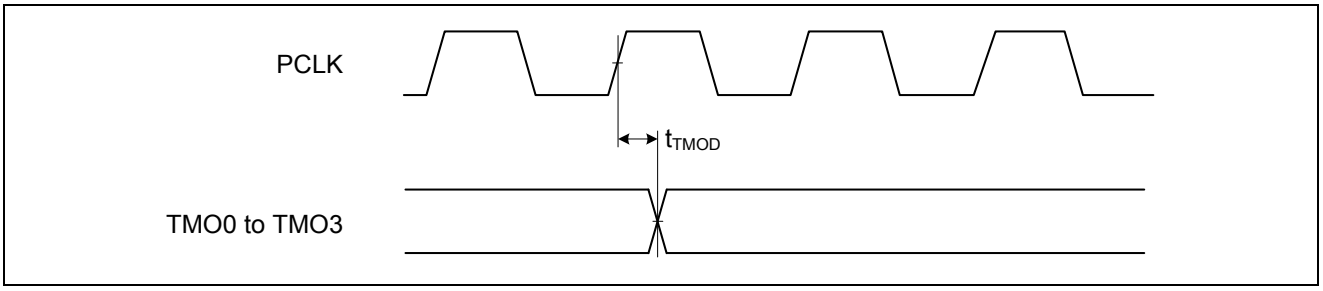


Figure 5.18 8-Bit Timer Output Timing

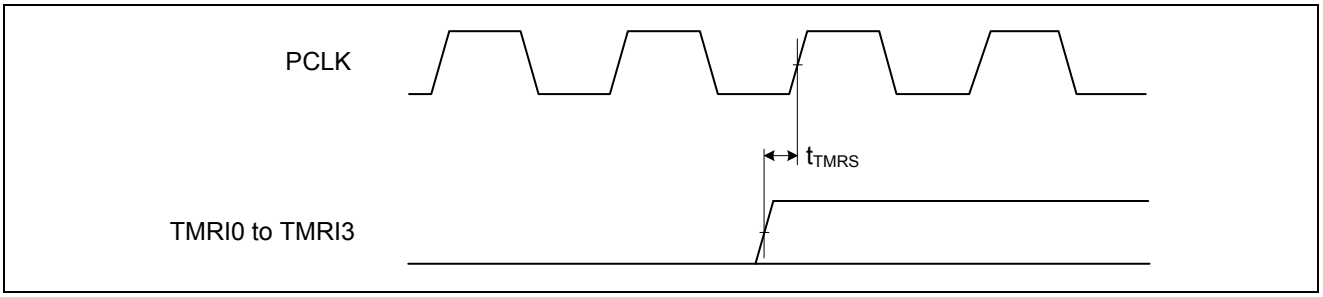


Figure 5.19 8-Bit Timer Reset Input Timing

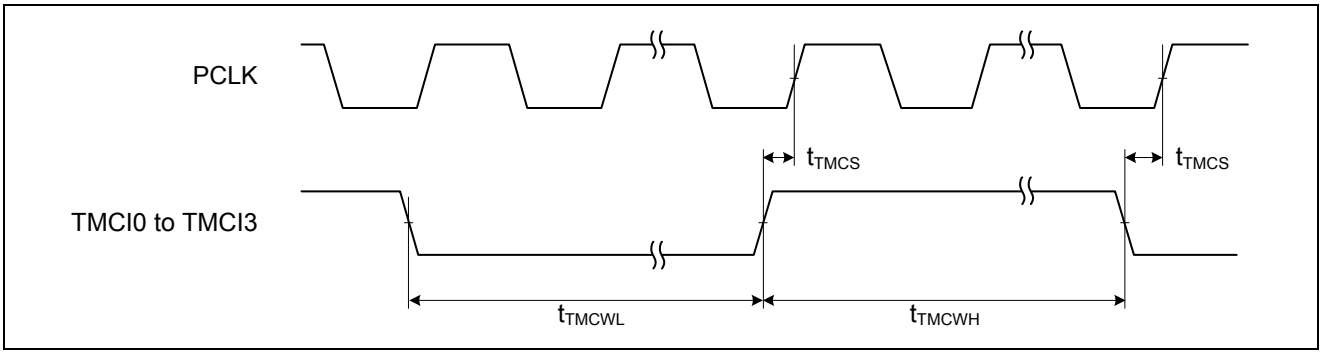


Figure 5.20 8-Bit Timer Clock Input Timing

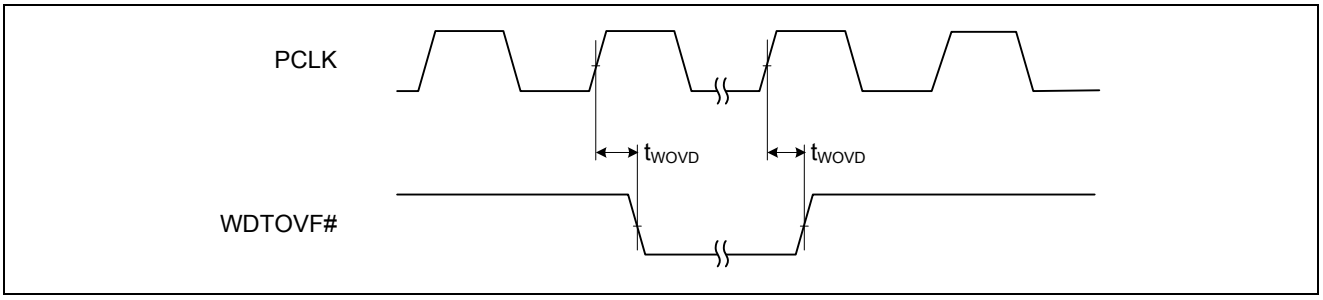


Figure 5.21 WDT Output Timing

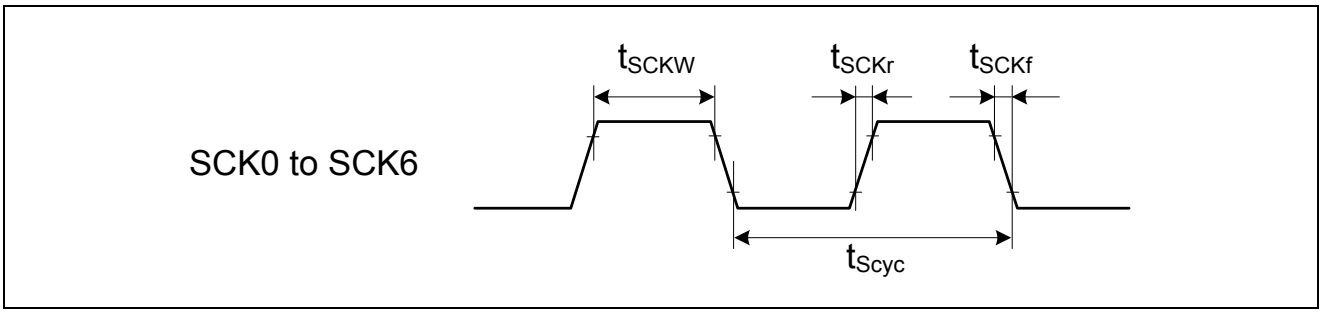


Figure 5.22 SCK Clock Input Timing

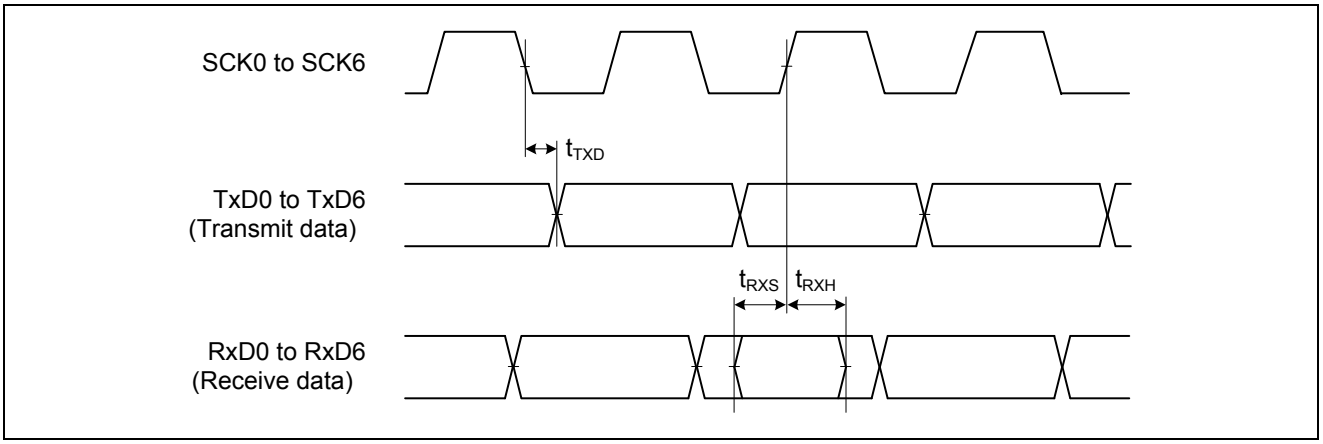


Figure 5.23 SCI Input/Output Timing: Clock Synchronous Mode

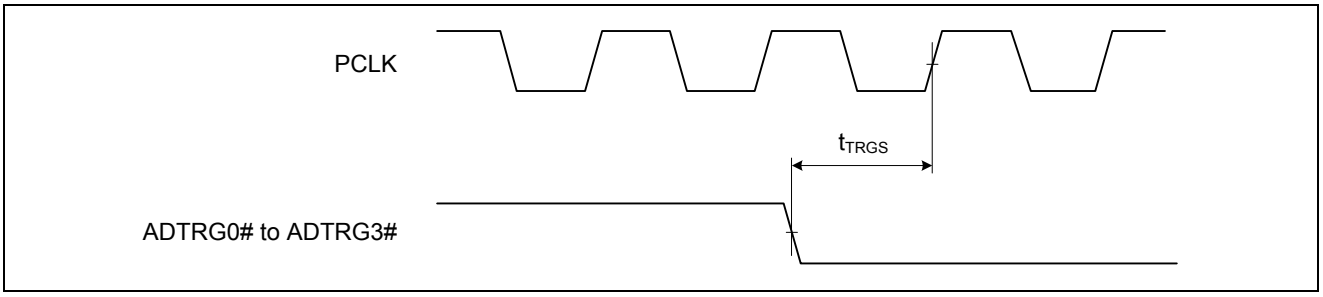


Figure 5.24 A/D Converter External Trigger Input Timing

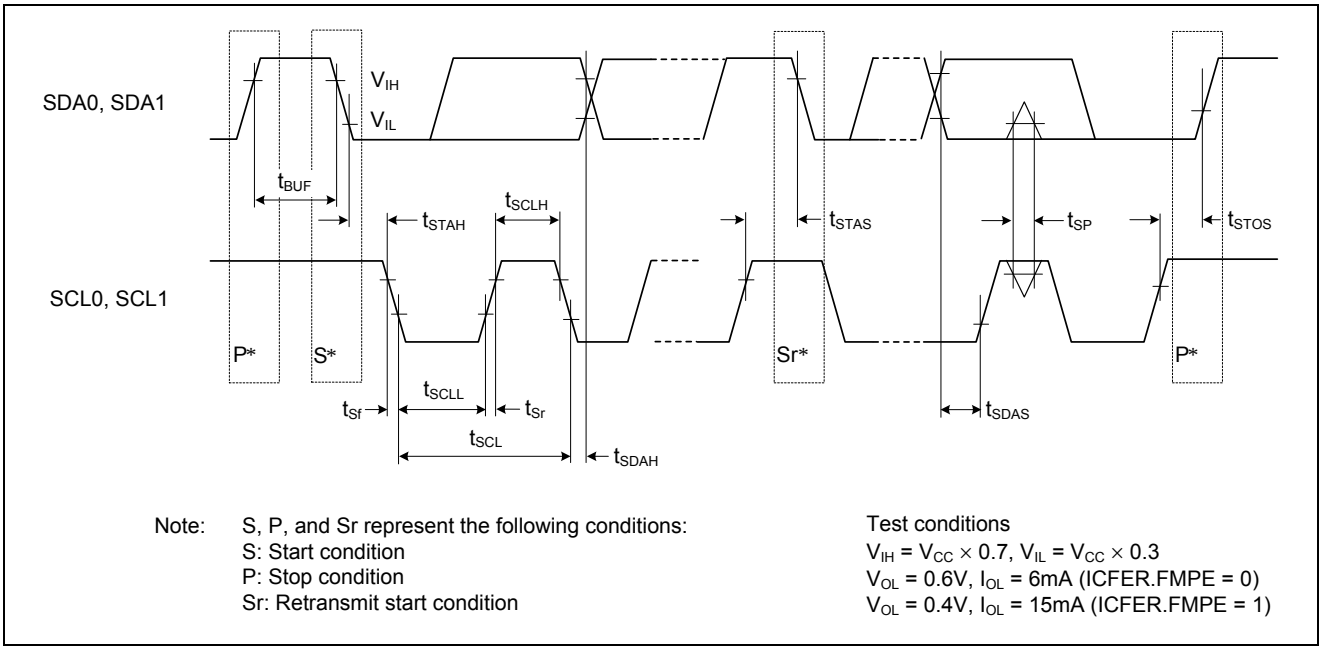


Figure 5.25 I²C Bus Interface Input/Output Timing

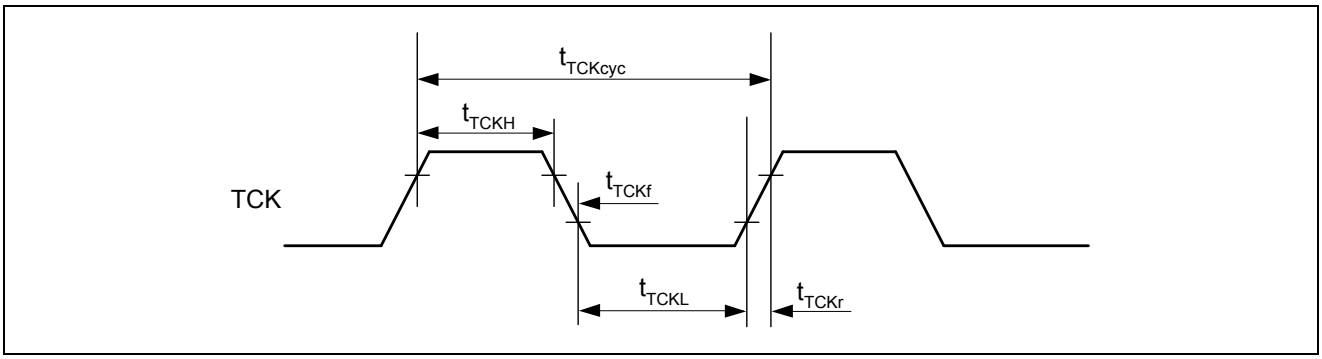


Figure 5.26 Boundary Scan TCK Timing

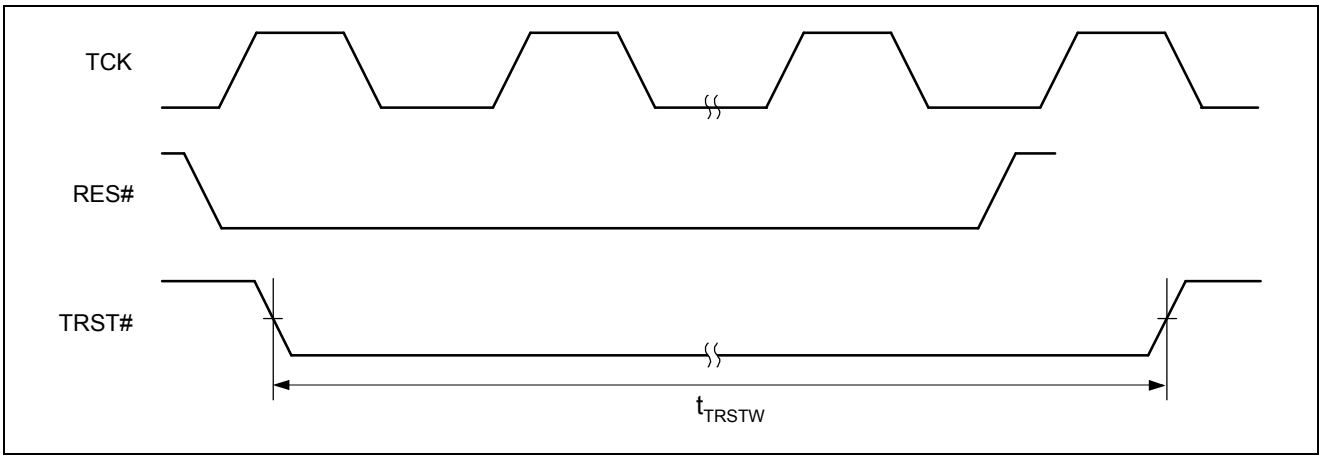


Figure 5.27 Boundary Scan TRST# Timing

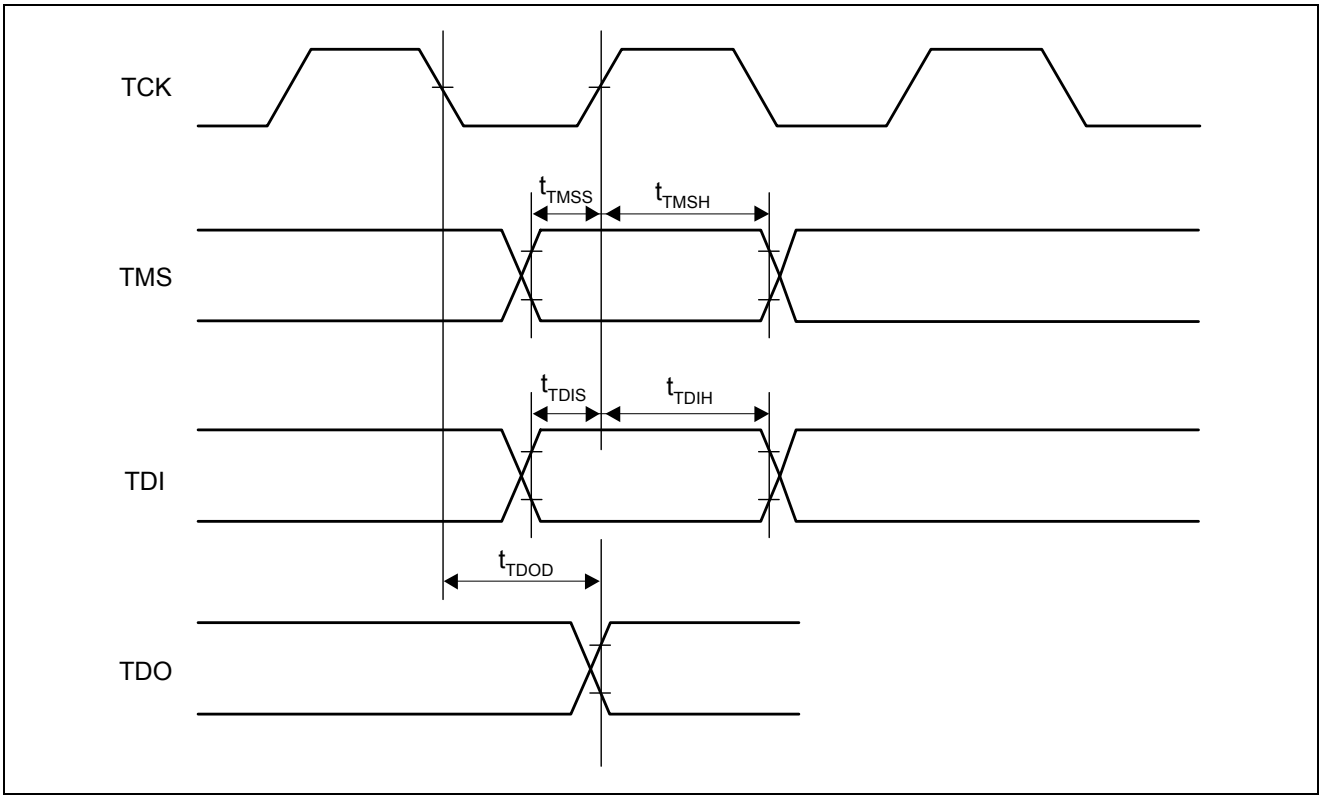


Figure 5.28 Boundary Scan Input/Output Timing

5.4 A/D Conversion Characteristics

Table 5.9 A/D Conversion Characteristics

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V, PCLK = 8 to 50 MHz, ADCLK = 4 to 50 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			10	10	10	Bit	
Conversion time*1 (ADCLK = 50-MHz operation)	With 0.1-µF external capacitor	When the capacitor is charged enough*2	0.8 (0.3)*3	—	—	µs	Sampling 15 states
	Without external capacitor	Permissible signal source impedance (max.) = 1.0 kΩ	1.0 (0.5)*3	—	—		Sampling 25 states
		Permissible signal source impedance (max.) = 5.0 kΩ	2.6 (2.1)*3	—	—		Sampling 105 states
Analog input capacitance			—	—	6.0	pF	
INL integral nonlinearity error (INL)			—	±1.5	±3.0	LSB	
Offset error			—	±1.5	±3.0	LSB	
Full-scale error			—	±1.5	±3.0	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	±1.5	±3.0	LSB	
DNL differential nonlinearity error (DNL)			—	±0.5	±1.0	LSB	

Notes: 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
2. The scanning is not supported.
3. The value in parentheses indicates the sampling time.

5.5 D/A Conversion Characteristics

Table 5.10 D/A Conversion Characteristics

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V, PCLK = 8 to 50 MHz
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time	—	—	3	µs	20-pF capacitive load
Absolute accuracy	—	±2.0	±4.0	LSB	2-MΩ resistive load
	—	—	±3.0	LSB	4-MΩ resistive load
	—	—	±2.0	LSB	10-MΩ resistive load
RO output resistance	—	3.6	—	kΩ	

5.6 ROM (Flash Memory for Code Storage) Characteristics

Table 5.11 ROM (Flash Memory for Code Storage) Characteristics

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V
Operating temperature range during programming/erasing:
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time	256 bytes	t_{P256}	—	2	12	ms	PCLK = 50 MHz $N_{PEC} \leq 100$
	8 Kbytes	t_{P8K}	—	45	100	ms	
	256 bytes	t_{P256}	—	2.4	14.4	ms	PCLK = 50 MHz $N_{PEC} > 100$
	8 Kbytes	t_{P8K}	—	54	120	ms	
Erasure time	8 Kbytes	t_{E8K}	—	50	120	ms	PCLK = 50 MHz $N_{PEC} \leq 100$
	64 Kbytes	t_{E64K}	—	400	875	ms	
	128 Kbytes	t_{E128K}	—	800	1750	ms	
	8 Kbytes	t_{E8K}	—	60	144	ms	PCLK = 50 MHz $N_{PEC} > 100$
	64 Kbytes	t_{E64K}	—	480	1050	ms	
	128 Kbytes	t_{E128K}	—	960	2100	ms	
Rewrite/erase cycle*[1]		N_{PEC}	1000*[2]	—	—	Times	
Suspend delay time during writing		t_{SPD}	—	—	120	µs	Figure 5.29 PCLK = 50 MHz
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t_{SEED}	—	—	1.7	ms	
Data hold time*[3]		T_{DRP}	10	—	—	Year	

Notes: 1. Definition of rewrite/erase cycle:
The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte writing is performed 32 times for different addresses in 8-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (over writing is prohibited).
2. This indicates the minimum number that guarantees the characteristics after rewriting. (The guaranteed value is in the range from one to the minimum number.)
3. This indicates the characteristic when rewrite is performed within the specification range including the minimum number.

5.7 Data Flash (Flash Memory for Data Storage) Characteristics

Table 5.12 Data Flash (Flash Memory for Data Storage) Characteristics

Conditions: V_{CC} = $PLLV_{CC}$ = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = V_{REFL} = 0 V
Operating temperature range during programming/erasing:
T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time	8 bytes	t_{DP8}	—	0.4	2	ms	PCLK = 50-MHz operation
	128 bytes	t_{DP128}	—	1	5	ms	
Erasure time	8 Kbytes	t_{DE8K}	—	300	900	ms	PCLK = 50-MHz operation
Blank check time	8 bytes	t_{DBC8}	—	—	30	µs	PCLK = 50-MHz operation
	8 Kbytes	t_{DBC8K}	—	—	2.5	ms	
Rewrite/erase cycle*1		N_{DPEC}	30000*2	—	—	Times	
Suspend delay time during writing		t_{DSPD}	—	—	120	µs	Figure 5.29 PCLK = 50-MHz operation
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t_{DSEED}	—	—	1.7	ms	
Data hold time*3		T_{DDRP}	10	—	—	Year	

Notes: 1. Definition of rewrite/erase cycle:
The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 30000), erasing can be performed n times for each block. For instance, when 128-byte writing is performed 64 times for different addresses in 8-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (over writing is prohibited).
2. This indicates the minimum number that guarantees the characteristics after rewriting. (The guaranteed value is in the range from one to the minimum number.)
3. This indicates the characteristic when rewrite is performed within the specification range including the minimum number.

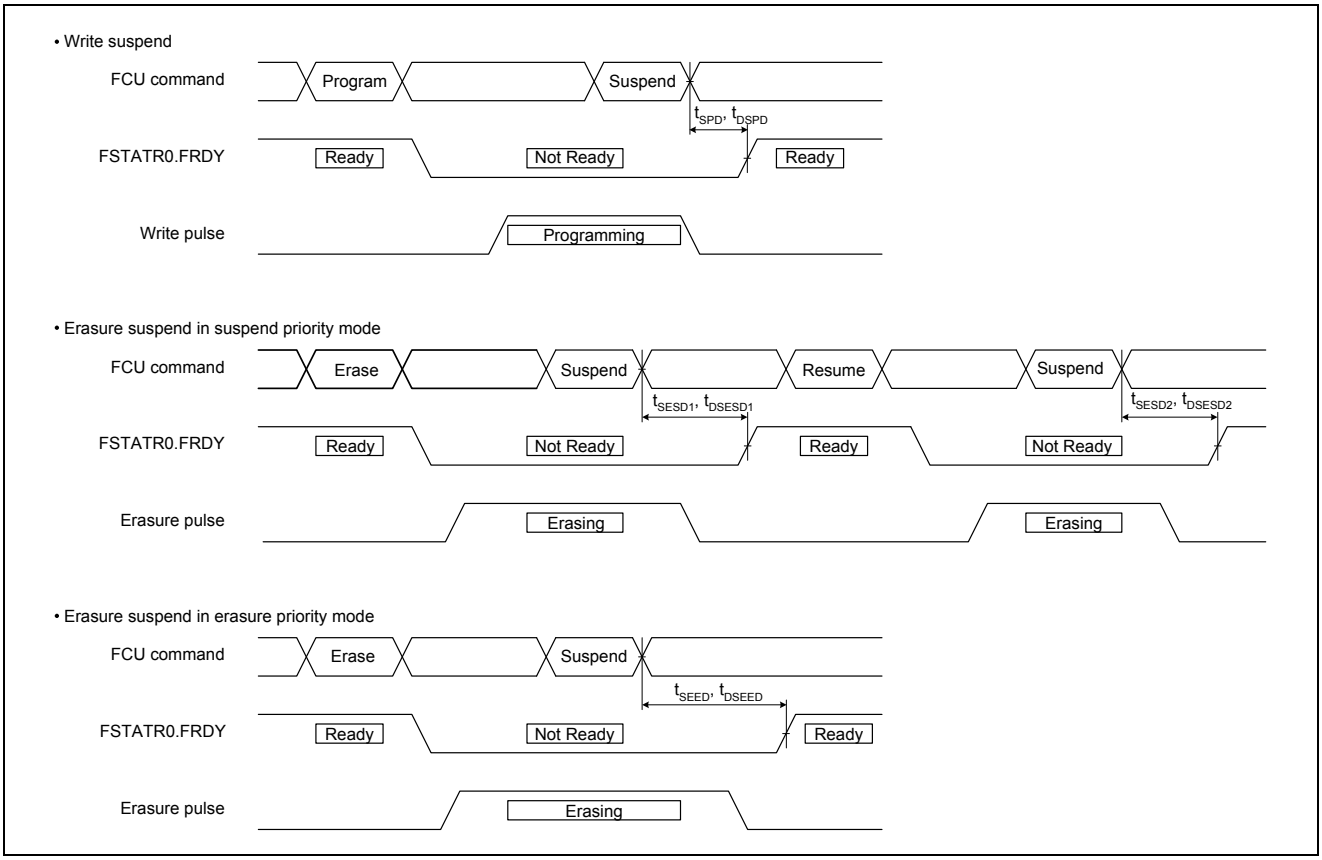
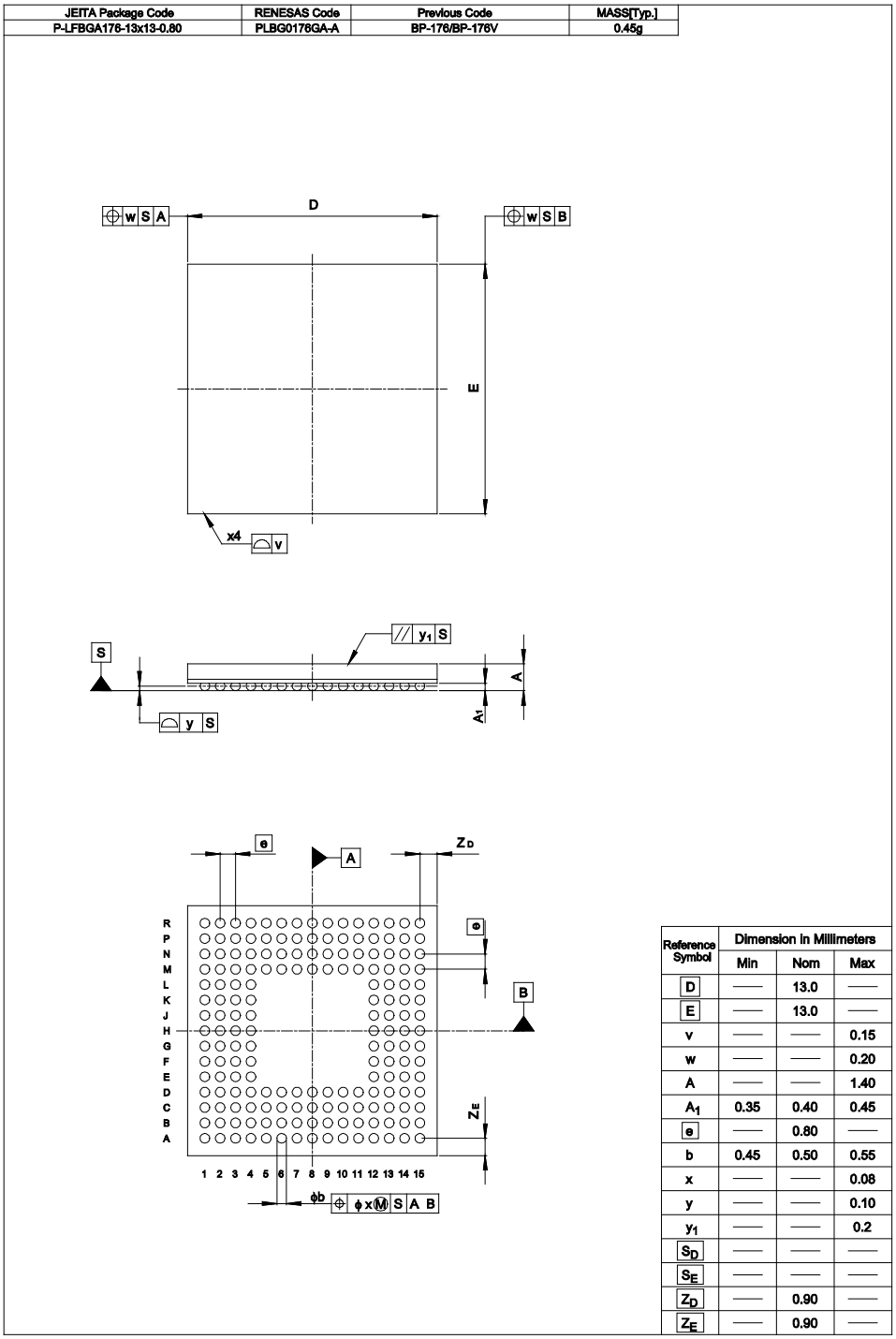


Figure 5.29 ROM, Data Flash Write/Erase Suspend Timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in "Packages" on Renesas Technology Corp. website.

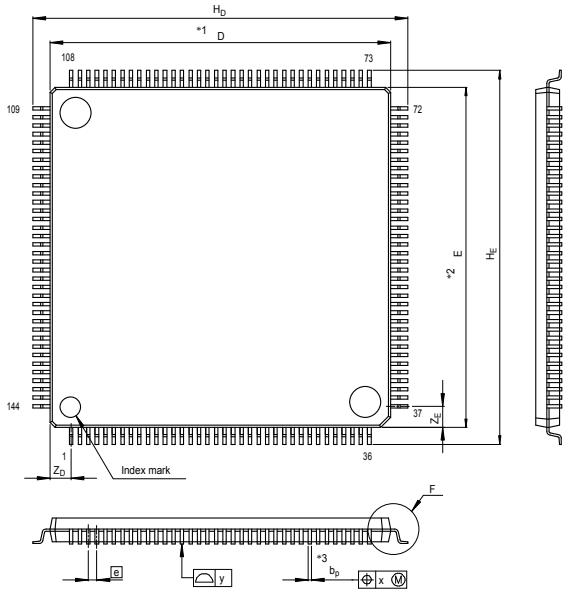
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA176-13x13-0.80	PLBG0176GA-A	BP-176/BP-176V	0.45g

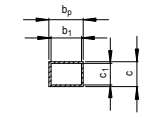


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	13.0	—
E	—	13.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.90	—
Z_E	—	0.90	—

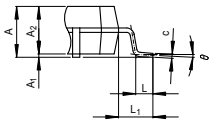
176-pin LFBGA (PLBG0176GA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

144-pin LQFP (PLQP0144KA-A)

REVISION HISTORY — RX610 Group Datasheet

		Description	
Rev.	**Data**	**Page**	**Summary**
0.50	Mar. 24, 2009	–	First edition issued
1.00	Apr. 22, 2011		1. Overview
		6	Figure 1.2 Block Diagram: Ports F to H added
		7	Figure 1.3 Pin Assignment of the 176-pin LFBGA, added
		10 to 15	Table 1.3 List of Pins and Pin Functions (176-Pin LFBGA), added
			Table 1.5 Pin Functions:
		21, 25	Description on the BSCANP, PF0 to PF6, PG0 to PG7, and PH0 to PH7 pins added
			4. I/O Registers
		34 to 54	Table 4.1 List of I/O Registers (Address Order), changed
			5. Electrical Characteristics
		58	Table 5.3 Permissible Output Currents, changed
		59	Table 5.5 Clock Timing: Oscillation settling time after leaving deep software standby mode (crystal), $t_{OSC3,}$ added
		60	Figure 5.2 Oscillation Settling Timing after Software Standby Mode, changed
		61	Figure 5.3 Oscillation Settling Timing after Deep Software Standby Mode, added
		71	Table 5.8 Timing of On-Chip Peripheral Modules (3), changed
		75	Figure 5.26 Boundary Scan TCK Timing, added
		75	Figure 5.27 Boundary Scan TRST# Timing, added
		76	Figure 5.28 Boundary Scan Input/Output Timing, added
1.20	Feb.20, 2013		1. Overview
		5	Table 1.2 List of Products, product lineup added
		23, 26	Table 1.5 Pin Functions, description on bus control changed, note added
			5. I/O register
		35 to 55	Table 5.1 List of I/O Registers (Address Order), changed

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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