2.5 VOLT 32M x 64 HIGH PERFORMANCE UNBUFFERED DDR SDRAM MODULE

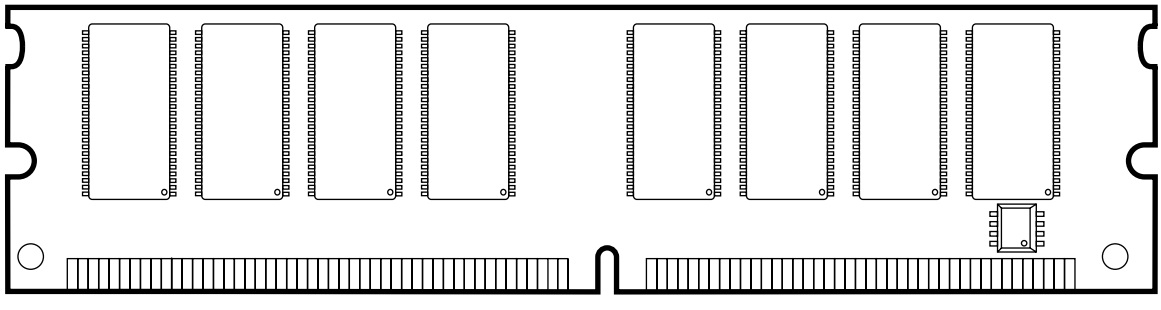
Features

- 184 Pin Unbuffered 33,554,432 x 64 bit Organization DDR SDRAM Modules
- Utilizes High Performance 16M x 8 DDR SDRAM in TSOPII-66 Packages
- Single +2.5V (± 0.2V) Power Supply
- Programmable $\overline{CAS}$ Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All Inputs, Outputs are SSTL-2 Compatible
- 4096 Refresh Cycles every 64 ms
- Serial Presence Detect (SPD)
- DDR SDRAM Performance

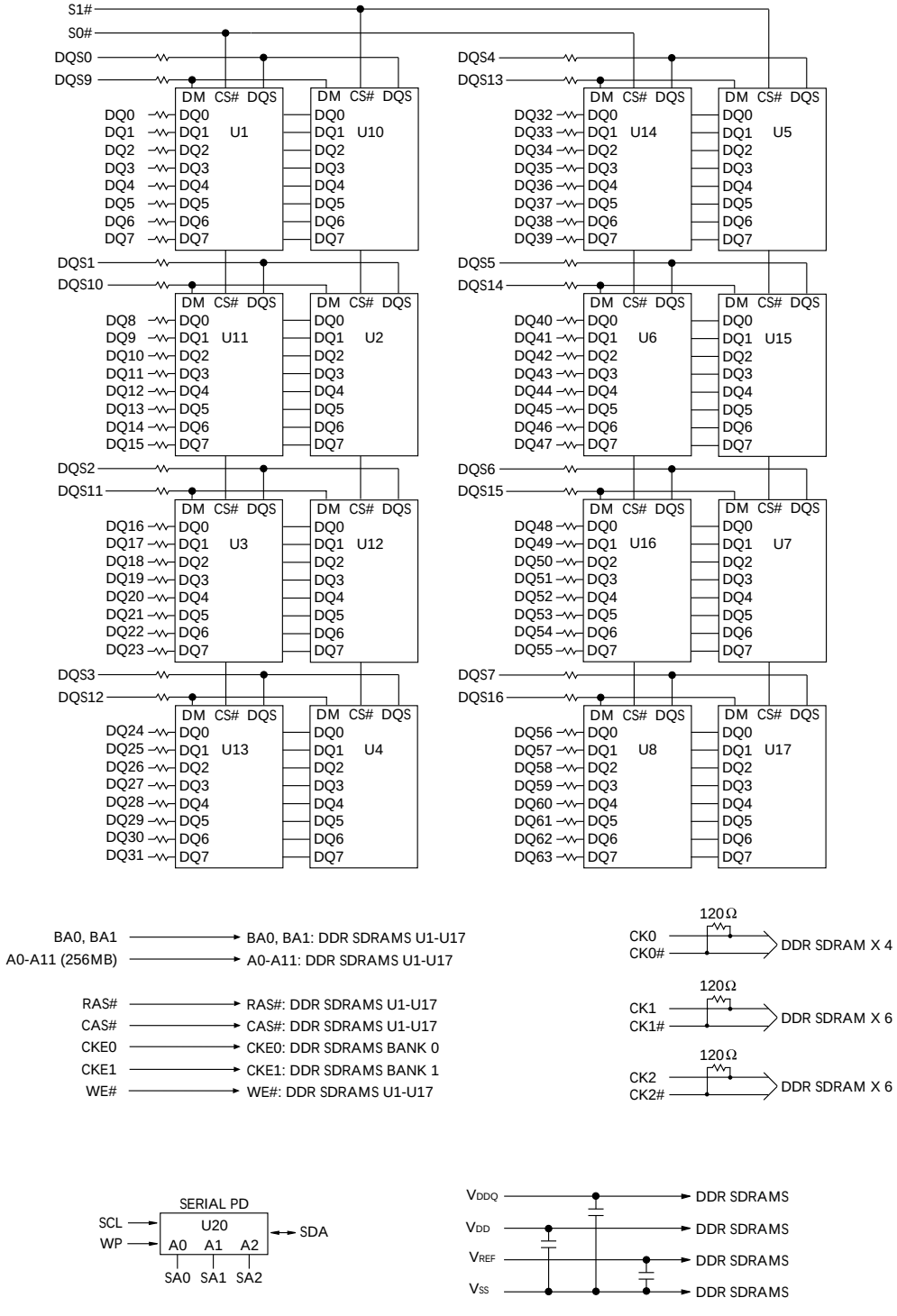
Description

The V826532K04S memory module is organized 33,554,432 x 64 bits in a 184 pin memory module. The 32M x 64 memory module uses 16 Mosel-Vitelic 16M x 8 DDR SDRAM. The x64 modules are ideal for use in high performance computer systems where increased memory density and fast access times are required.

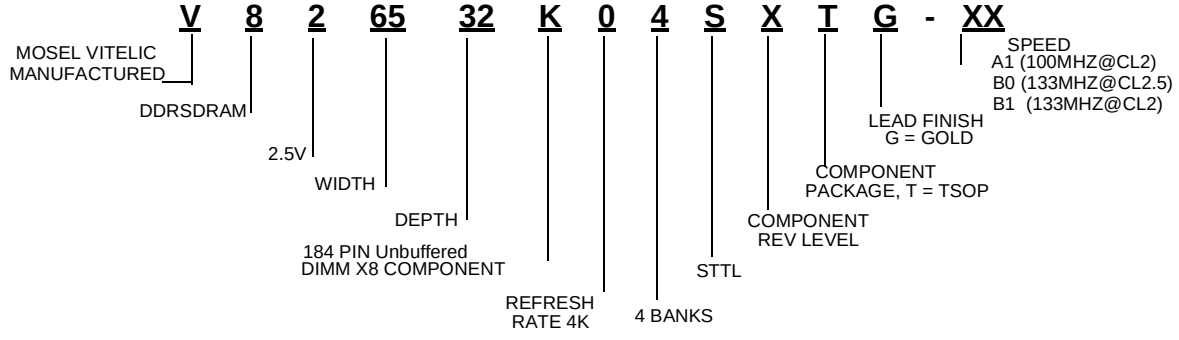
	Component Used	B1	B0	A1	Units
t_{CK}	Clock Frequency (max.)	143 (PC266A)	133 (PC266B)	125 (PC200)	MHz
t_{AC}	Clock Cycle Time $\overline{CAS}$ Latency = 2.5	7	7.5	8	ns



FUNCTIONAL BLOCK DIAGRAM



Part Number Information



Pin Configurations (Front Side/Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	$\overline{RAS}$
2	DQ0	33	DQ24	63	$\overline{WE}$	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	$\overline{CAS}$	96	VDDQ	127	DQ29	157	$\overline{CS0}$
5	DQS0	36	DQS3	66	VSS	97	DM0	128	VDDQ	158	$\overline{CS1}$
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3	159	DM5
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	NC	41	A2	71	NC	102	NC	133	DQ31	163	NC
11	VSS	42	Vss	72	DQ48	103	A13*	134	CB4*	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5*	165	DQ52
13	DQ9	44	CB0*	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	CB1*	75	$\overline{CK2}$	106	DQ13	137	CK0*	167	NC
15	VDDQ	46	VDD	76	CK2	107	DM1	138	$\overline{CK0}$*	168	VDD
16	CK1	47	DQS8*	77	VDDQ	108	VDD	139	VSS	169	DM6
17	$\overline{CK1}$	48	A0	78	DQS6	109	DQ14	140	DM8*	170	DQ54
18	VSS	49	CB2*	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	CKE1	142	CB6*	172	VDDQ
20	DQ11	51	CB3*	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	BA2*	144	CB7*	174	DQ60
22	VDDQ	Key		83	DQ56	114	DQ20	Key		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12*	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2	149	DM4	180	VDDQ
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	NC	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

Notes:

* These pins are not used in this module.

Pin Names

Pin	Pin Description
CK1, $\overline{CK1}$, CK2, $\overline{CK2}$	Differential Clock Inputs
$\overline{CS0}$	Chip Select Input
CKE0	Clock Enable Input
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Commend Sets Inputs
A0 ~ A11	Address
BA0, BA1	Bank Address
DQ0~DQ63	Data Inputs/Outputs
DQS0~DQS7	Data Strobe Inputs/Outputs
DM0~DM7	Data-in Mask
VDD	Power Supply

Pin	Pin Description
VDDQ	DQs Power Supply
VSS	Ground
VREF	Reference Power Supply
VDDSPD	Power Supply for SPD
SA0~SA2	E^2 PROM Address Inputs
SCL	E^2 PROM Clock
SDA	E^2 PROM Data I/O
VDDID	VDD Identification Flag
DU	Do not Use
NC	No Connection

Serial Presence Detect Information

Bin Sort:
B1 (PC266A @ CL = 2)
B0 (PC266B @ CL = 2.5)
A1 (PC200 @ CL = 2)

Byte #	Function described	Function Supported			Hex value		
		A1	B0	B1	A1	B0	B1
0	Defines # of Bytes written into serial memory at module manufacturer	128bytes			80h		
1	Total # of Bytes of SPD memory device	256bytes			08h		
2	Fundamental memory type	SDRAM DDR			07h		
3	# of row address on this assembly	12			0Ch		
4	# of column address on this assembly	10			0Ah		
5	# of module Rows on this assembly	2 Bank			02h		
6	Data width of this assembly	64 bits			40h		
7	.....Data width of this assembly	-			00h		
8	VDDQ and interface standard of this assembly	SSTL 2.5V			04h		
9	DDR SDRAM cycle time at CAS Latency =2.5	8ns	7.5ns	7ns	80h	75h	70h
10	DDR SDRAM Access time from clock at CL=2.5	±0.8ns	±0.75n	±0.70n	80h	75h	70h
11	DIMM configuration type(Non-parity, Parity, ECC)	Non-parity, ECC			00h		
12	Refresh rate & type	15.6us & Self refresh			80h		
13	Primary DDR SDRAM width	x8			08h		
14	Error checking DDR SDRAM data width	N/A			00h		
15	Minimum clock delay for back-to-back random column address	t_{CCD}=1CLK			01h		
16	DDR SDRAM device attributes : Burst lengths supported	2,4,8			0Eh		
17	DDR SDRAM device attributes : # of banks on each DDR SDRAM	4 banks			04h		
18	DDR SDRAM device attributes : CAS Latency supported	2,2.5			0Ch		
19	DDR SDRAM device attributes : CS Latency	0CLK			01h		
20	DDR SDRAM device attributes : WE Latency	1CLK			02h		
21	DDR SDRAM module attributes	Differential clock / non Registered			20h		
22	DDR SDRAM device attributes : General	+/-0.2V voltage tolerance			00h		
23	DDR SDRAM cycle time at CL =2	10ns	10ns	7.5ns	A0h	A0h	75h
24	DDR SDRAM Access time from clock at CL =2	±0.8ns	±0.8n	±0.75	80h	80h	75h
25	DDR SDRAM cycle time at CL =1.5	-	-	-	00h		
26	DDR SDRAM Access time from clock at CL =1.5	-	-	-	00h		
27	Minimum row precharge time (=t_{RP})	20ns	20ns	18ns	50h	50h	48h
28	Minimum row activate to row active delay(=t_{RRD})	15ns	15ns	14ns	3Ch	3Ch	38h

Serial Presence Detect Information (cont.)

Byte #	Function described	Function Supported			Hex value		
		A1	B0	B1	A1	B0	B1
29	Minimum RAS to CAS delay(=t_{RCD})	20ns	20ns	18ns	50h	50h	48h
30	Minimum active to precharge time(=t_{RAS})	50ns	45ns	45ns	32h	2Dh	2Dh
31	Module ROW density	128MB			20h		
32	Command and address signal input setup time	1.1ns	0.9ns	0.9ns	B0h	90h	90h
33	Command and address signal input hold time	1.1ns	0.9ns	0.9ns	B0h	90h	90h
34	Data signal input setup time	0.6ns	0.5ns	0.5ns	60h	50h	50h
35	Data signal input hold time	0.6ns	0.5ns	0.5ns	60h	50h	50h
36-40	Superset information (may be used in future)				00h		
41	SDRAM device minimum active to active/auto-refresh time (=t_{RC})	70ns	65ns	60ns	46h	41h	3Ch
42	SDRAM device minimum active to autorefresh to active/auto-refresh time (=t_{RFC})	80ns	75ns	67ns	50h	4Bh	43h
43	SDRAM device maximum device cycle time (=$t_{CK\ MAX}$)	12ns	12ns	12ns	30h	30h	30h
44	SDRAM device maximum skew between DQS and DQ signals (=t_{DQSQ})	0.6ns	0.5ns	0.5ns	3Ch	32h	32h
45	SDRAM device maximum read datahold skew factor (=t_{QHS})	1ns	0.75ns	0.75ns	A0h	75h	75h
46-61	Superset information (may be used in future)	-			00h		
62	SPD data revision code	Initial release			00h		
63	Checksum for Bytes 0 ~ 62	-			C5h	0Bh	AAh
64	Manufacturer JEDEC ID code	Mosel Vitelic			40h		
65 -71	..... Manufacturer JEDEC ID code	Mosel Vitelic			40h		
72	Manufacturing location				01h		
73-90	Module part number (ASCII)	V826532K04S					
91	Manufacturer revison code (For PCB)	0			00		
92	Manufacturer revison code (For component)	0			00		
93	Manufacturing date (Week)	-			-		
94	Manufacturing date (Year)	-			-		
95~98	Assembly serial #	-			-		
99~127	Manufacturer specific data (may be used in future)	Undefined			00h		
128~255	Open for customer use	Undefined			00h		

DC Operating Conditions

(T_A = 0 to 70°C, Voltage referenced to V_{SS} = 0V)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	V_{DD}	2.3	2.5	2.7	V	
Power Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	1
Input High Voltage	V_{IH}	V_{REF} + 0.15	-	V_{DDQ} + 0.3	V	
Input Low Voltage	V_{IL}	-0.3	-	V_{REF} - 0.15	V	2
I/O Termination Voltage	V_{TT}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V	
Reference Voltage	V_{REF}	1.15	1.25	1.35	V	3
Input Leakage Current	I_I	-2	-	2	µA	
Output Leakage Current	IO_z	-5	-	5	µA	
Output High Current (V_{OUT} = 1.95V)	IO_H	-16.8	-	-	mA	
Output Low Current (V_{OUT} = 0.35V)	IO_L	16.8	-	-	mA	

Notes: 1. V_{DDQ} must not exceed the level of V_{DD}.
2. V_{IL} (min) is acceptable -1.5V AC pulse width with ð 5ns of duration.
3. The value of V_{REF} is approximately equal to 0.5V_{DDQ}.

AC Operating Conditions

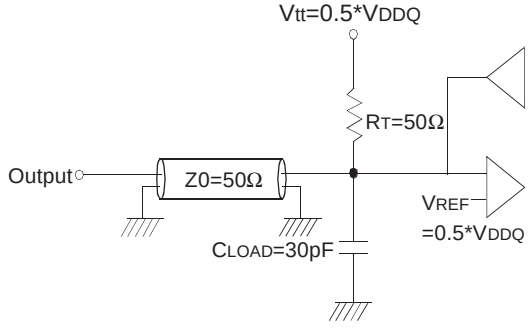
(T_A = 0 to 70 °C, Voltage referenced to V_{SS} = 0V)

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	$V_{IH(AC)}$	V_{REF} + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	$V_{IL(AC)}$		V_{REF} - 0.31	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	$V_{ID(AC)}$	0.7	V_{DDQ} + 0.6	V	1
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	$V_{IX(AC)}$	0.5*$V_{DDQ-0.2}$	0.5*$V_{DDQ+0.2}$	V	2

Notes: 1. VID is the magnitude of the difference between the input level on CK and the input on CK.
2. The value of VIX is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

AC Operating Test Conditions (T_A = 0 to 70°C, Voltage referenced to V_{SS} = 0V)

Parameter	Value	Unit
Reference Voltage	V_{DDQ} x 0.5	V
Termination Voltage	V_{DDQ} x 0.5	V
AC Input High Level Voltage (V_{IH}, min)	V_{REF} + 0.31	V
AC Input Low Level Voltage (V_{IL}, max)	V_{REF} - 0.31	V
Input Timing Measurement Reference Level Voltage	V_{REF}	V
Output Timing Measurement Reference Level Voltage	V_{TT}	V
Input Signal maximum peak swing	1.5	V
Input minimum Signal Slew Rate	1	V/ns
Termination Resistor (R_T)	50	Ohm
Series Resistor (R_S)	25	Ohm
Output Load Capacitance for Access Time Measurement (C_L)	30	pF



Output Load Circuit (SSTL_2)

Input/Output Capacitance

(V_{DD} = 2.5V, V_{DDQ} = 2.5V, T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA_0 ~ BA_1, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	CIN_1	60	75	pF
Input capacitance (CKE_0)	CIN_2	40	48	pF
Input capacitance ($\overline{CS_0}$)	CIN_3	40	48	pF
Input capacitance (CLK_1, CLK_2)	CIN_4	30	32	pF
Data & DQS input/output capacitance (DQ_0~DQ_{63})	C_{OUT}	10	12	pF
Input capacitance (DM0~DM8)	CIN_5	10	12	pF

DDR SDRAM MODULE I_{DD} SPEC TABLE

Symbol		B1 (DDR266@CL=2)		B0 (DDR266@ CL=2.5)		A1 (DDR200@CL=2)		Unit
		Typical	Worst	Typical	Worst	Typical	Worst	
IDD0		1210	1230	1210	1230	980	1050	mA
IDD1		1440	1530	1440	1530	1130	1250	mA
IDD2P		610	650	610	650	490	530	mA
IDD2F		770	850	770	850	650	690	mA
IDD2Q		690	730	690	730	570	600	mA
IDD3P		650	690	650	690	530	570	mA
IDD3N		810	890	810	890	650	730	mA
IDD4R		1770	2000	1770	2000	1450	1650	mA
IDD4W		1890	2200	1890	2200	1530	1690	mA
IDD5		1890	2200	1890	2200	1530	1690	mA
IDD6	Normal	32	32	32	32	32	32	mA
	Low power	16	16	16	16	16	16	mA
IDD7		3100	3500	3100	3500	2450	2850	mA

* Module I_{DD} was calculated on the basis of component I_{DD} and can be differently measured according to DQ loading cap.

Detailed test conditions for DDR SDRAM IDD1 & IDD

IDD1 : Operating current: One bank operation

1. Typical Case : Vdd = 2.5V, T=25' C

2. Worst Case : Vdd = 2.7V, T= 10' C

3. Only one bank is accessed with tRC(min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. Iout = 0mA

4. Timing patterns
 - DDR200(100Mhz, CL=2) : tCK = 10ns, CL2, BL=4, tRCD = 2*tCK, tRAS = 5*tCK
   Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing
   *50% of data changing at every burst
 - DDR266B(133Mhz, CL=2.5) : tCK = 7.5ns, CL=2.5, BL=4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
   Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
   *50% of data changing at every burst
 - DDR266A (133Mhz, CL=2) : tCK = 7.5ns, CL=2, BL=4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
   Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
   *50% of data changing at every burst

Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

AC Characteristics (AC operating conditions unless otherwise noted)

Parameter		Symbol	(PC266A)		(PC266B)		(PC200)		Unit	Note
			Min	Max	Min	Max	Min	Max		
Row Cycle Time		t_{RC}	60	-	65	-	70	-	ns	
Auto Refresh Row Cycle Time		t_{RFC}	67	-	75	-	80	-	ns	
Row Active Time		t_{RAS}	45	120K	48	120K	50	120K	ns	
Row Address to Column Address Delay		t_{RCD}	18	-	20	-	20	-	ns	
Row Active to Row Active Delay		t_{RRD}	14	-	15	-	15	-	ns	
Column Address to Column Address Delay		t_{CCD}	1	-	1	-	1	-	CLK	
Row Precharge Time		t_{RP}	18	-	20	-	20	-	ns	
Write Recovery Time		t_{WR}	15	-	15	-	15	-	ns	
Last Data-In to Read Command		t_{DRL}	1	-	1	-	1	-	CLK	
Auto Precharge Write Recovery + Precharge Time		t_{DAL}	35	-	35	-	35	-	ns	
System Clock Cycle Time	$\overline{CAS}$ Latency = 2.5	t_{CK}	7	12	7.5	12	8	12	ns	
	$\overline{CAS}$ Latency = 2		7.5	12	10	12	10	12	ns	
Clock High Level Width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	CLK	
Clock Low Level Width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	CLK	
Data-Out edge to Clock edge Skew		t_{AC}	-0.75	0.75	-0.75	0.75	-0.8	0.8	ns	
DQS-Out edge to Clock edge Skew		t_{DQSCK}	-0.75	0.75	-0.75	0.75	-0.8	0.8	ns	
DQS-Out edge to Data-Out edge Skew		t_{DQSQ}	-	0.5	-	0.5	-	0.6	ns	
Data-Out hold time from DQS		t_{QH}	t_{HPmin} -0.75ns	-	t_{HPmin} -0.75ns	-	t_{HPmin} -0.75ns	-	ns	1
Clock Half Period		t_{HP}	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	ns	1
Input Setup Time (fast slew rate)		t_{IS}	0.9	-	0.9	-	1.1	-	ns	2,3,5,6
Input Hold Time (fast slew rate)		t_{IH}	0.9	-	0.9	-	1.1	-	ns	2,3,5,6
Input Setup Time (slow slew rate)		t_{IS}	1.0	-	1.0	-	1.1	-	ns	2,4,5,6
Input Hold Time (slow slew rate)		t_{IH}	1.0	-	1.0	-	1.1	-	ns	2,4,5,6
Input Pulse Width		t_{IPW}	2.2	-	2.2	-	-	-	ns	6
Write DQS High Level Width		t_{DQSH}	0.4	0.6	0.4	0.6	0.4	0.6	CLK	
Write DQS Low Level Width		t_{DQSL}	0.4	0.6	0.4	0.6	0.4	0.6	CLK	
CLK to First Rising edge of DQS-In		t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	CLK	
Data-In Setup Time to DQS-In (DQ & DM)		t_{DS}	0.5	-	0.5	-	0.6	-	ns	7
Data-in Hold Time to DQS-In (DQ & DM)		t_{DH}	0.5	-	0.5	-	0.6	-	ns	7
DQ & DM Input Pulse Width		t_{DIPW}	1.75	-	1.75	-	2	-	ns	
Read DQS Preamble Time		t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	CLK	
Read DQS Postamble Time		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	CLK	

AC Characteristics (cont.)

Parameter	Symbol	(PC266A)		(PC266B)		(PC200)		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write DQS Preamble Setup Time	t_{WPRES}	0	-	0	-	0	-	CLK	
Write DQS Preamble Hold Time	t_{WPREH}	0.25	-	0.25	-	0.25	-	CLK	
Write DQS Postamble Time	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	CLK	
Mode Register Set Delay	t_{MRD}	2	-	2	-	2	-	CLK	
Power Down Exit Time	t_{PDEX}	10	-	10	-	10	-	ns	
Exit Self Refresh to Non-Read Command	t_{XSNR}	75	-	75	-	80	-	ns	
Exit Self Refresh to Read Command	t_{XSRD}	200	-	200	-	200	-	CLK	8
Average Periodic Refresh Interval	t_{REFI}	-	15.6	-	15.6	-	15.6	us	

Notes: 1. This calculation accounts for tDQSQ(max), the pulse width distortion of on-chip circuit and jitter.
2. Data sampled at the rising edges of the clock : A0~A11, BA0~BA1, CKE, CS, RAS, CAS, WE.
3. For command/address input slew rate >=1.0V/ns
4. For command/address input slew rate >=0.5V/ns and <1.0V/ns
5. CK, $\overline{CK}$ slew rates are >=1.0V/ns
6. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester correlation.
7. Data latched at both rising and falling edges of Data Strobes(DQS) : DQ, DM
8. Minimum of 200 cycles of stable input clocks after Self Refresh Exit command, where CKE is held high, is required to complete Self Refresh Exit and lock the internal DLL circuit of DDR SDRAM.

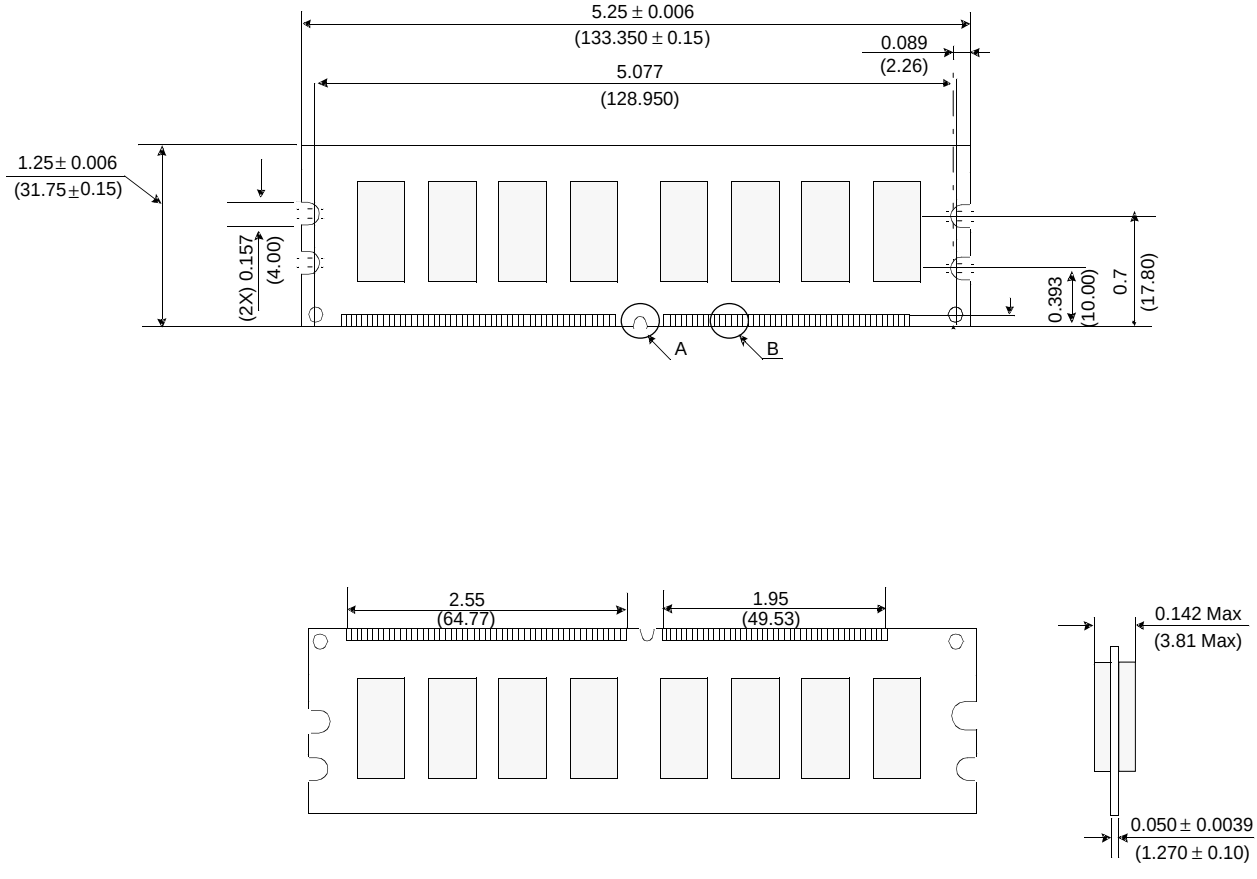
Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Ambient Temperature	T_A	0 ~ 70	°C
Storage Temperature	T_{STG}	-55 ~ 125	°C
Voltage on Any Pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-0.5 ~ 3.6	V
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	-0.5 ~ 3.6	V
Output Short Circuit Current	I_{OS}	50	mA
Power Dissipation	P_D	9	W
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • Sec

Note: Operation at above absolute maximum rating can adversely affect device reliability

Package Dimensions

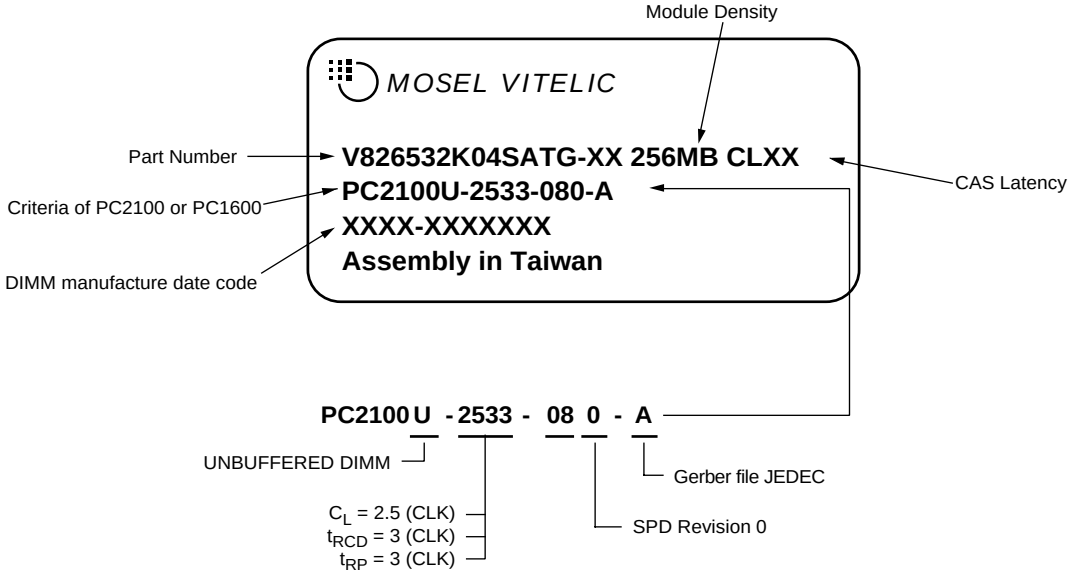
Units : Inches (Millimeters)



Detail A

Detail B

Label Information



WORLDWIDE OFFICES

U.S.A.
3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0952

TAIWAN
7F, NO. 102
MIN-CHUAN E. ROAD, SEC. 3
TAIPEI
PHONE: 886-2-2545-1213
FAX: 886-2-2545-1209

NO 19 LI HSIN ROAD
SCIENCE BASED IND. PARK
HSIN CHU, TAIWAN, R.O.C.
PHONE: 886-3-579-5888
FAX: 886-3-566-5888

SINGAPORE
10 ANSON ROAD #23-13
INTERNATIONAL PLAZA
SINGAPORE 079903
PHONE: 65-3231801
FAX: 65-3237013

JAPAN
ONZE 1852 BUILDING 6F
2-14-6 SHINTOMI, CHUO-KU
TOKYO 104-0041
PHONE: 03-3537-1400
FAX: 03-3537-1402

UK & IRELAND
SUITE 50, GROVEWOOD
BUSINESS CENTRE
STRATHCLYDE BUSINESS
PARK
BELLSHILL, LANARKSHIRE,
SCOTLAND, ML4 3NQ
PHONE: 44-1698-748515
FAX: 44-1698-748516

GERMANY (CONTINENTAL EUROPE & ISRAEL)
BENZSTRASSE 32
71083 HERRENBERG
GERMANY
PHONE: +49 7032 2796-0
FAX: +49 7032 2796 22

U.S. SALES OFFICES

WEST
3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0952

CENTRAL / EAST
604 FIELDWOOD CIRCLE
RICHARDSON, TX 75081
PHONE: 214-352-3775
FAX: 214-904-9029

© Copyright , MOSEL VITELIC Corp.

Printed in U.S.A.

The information in this document is subject to change without notice.

MOSEL VITELIC makes no commitment to update or keep current the information contained in this document. No part of this document may be copied or reproduced in any form or by any means without the prior written consent of MOSEL-VITELIC.

MOSEL VITELIC subjects its products to normal quality control sampling techniques which are intended to provide an assurance of high quality products suitable for usual commercial applications. MOSEL VITELIC does not do testing appropriate to provide 100% product quality assurance and does not assume any liability for consequential or incidental arising from any use of its products. If such products are to be used in applications in which personal injury might occur from failure, purchaser must do its own quality assurance testing appropriate to such applications.