ISL5314

Direct Digital Synthesizer

FN4901
Rev 3.00
January 19, 2010

The 14-bit ISL5314 provides a complete Direct Digital Synthesizer (DDS) system in a single 48 Ld LQFP package. A 48-bit Programmable Carrier NCO (numerically controlled oscillator) and a high speed 14-bit DAC (digital-to-analog converter) are integrated into a stand alone DDS.

The DDS accepts 48-bit center and offset frequency control information via a parallel processor interface. A 40-bit frequency tuning word can also be loaded via an asynchronous serial interface. Modulation control is provided by 3 external pins. The PH0 and PH1 pins select phase offsets of 0°, 90°, 180° and 270°, while the ENOFR pin enables or zeros the offset frequency word to the phase accumulator.

The parallel processor interface has an 8-bit write-only data input C(7:0), a 4-bit address A(3:0) bus, a Write Strobe (WR), and a Write Enable ($\overline{WE}$). The processor can update all registers simultaneously by loading a set of master registers, then transfer all master registers to the slave registers by asserting the $\overline{UPDATE}$ pin.

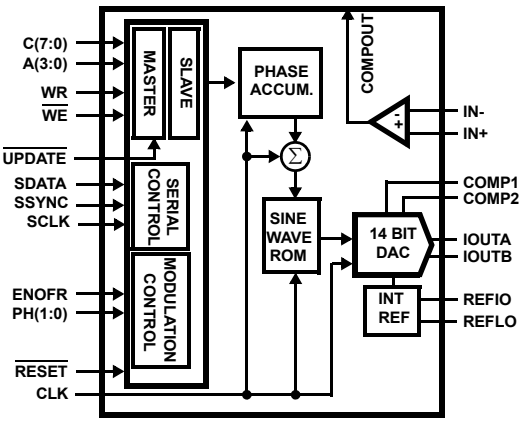
Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL5314INZ	ISL5314 INZ	-40 to +85	48 Ld LQFP	Q48.7x7A
ISL5314EVAL2		25	Evaluation Board	

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), please see device information page for ISL5314. For more information on MSL please see techbrief TB363.

Block Diagram



Features

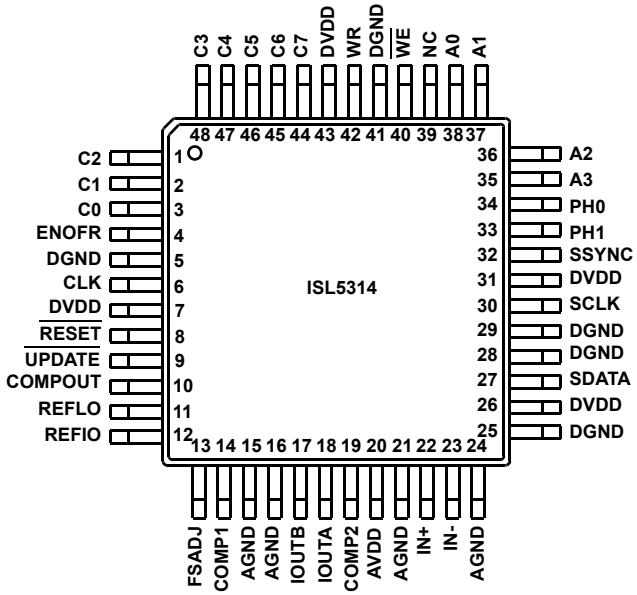
- 125MSPS output sample rate with 5V digital supply
- 100MSPS output sample rate with 3.3V digital supply
- 14-bit digital-to-analog (DAC) with internal reference
- Parallel control interface for fast tuning (50MSPS control register write rate) and serial control interface
- 48-bit programmable frequency control
- Offset frequency register and enable pin for fast FSK
- Small 48 Ld LQFP packaging
- Pb-Free (RoHS compliant)

Applications

- Programmable local oscillator
- FSK, PSK modulation
- Direct digital synthesis
- Clock generation

Pinout

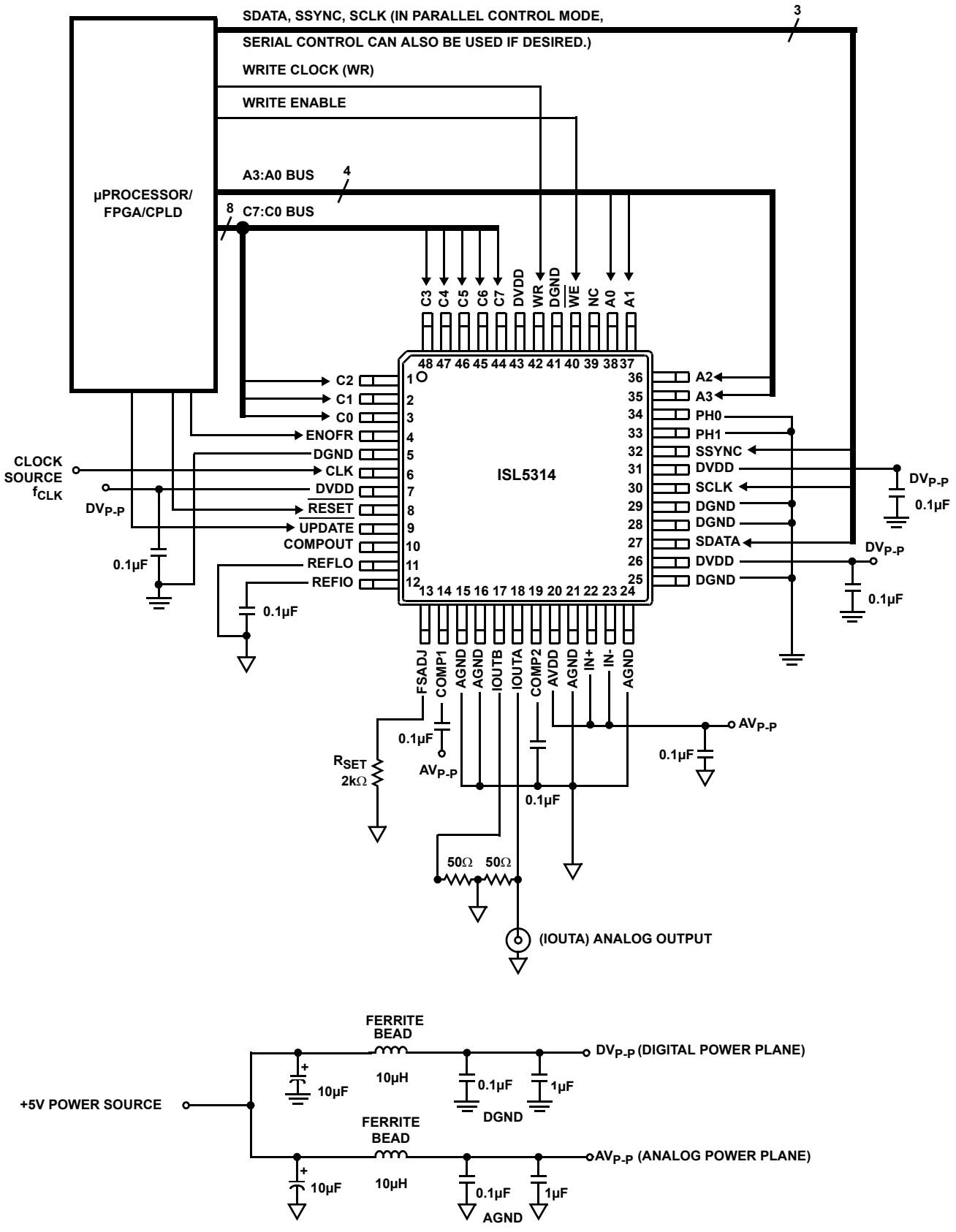
ISL5314
(48 LD LQFP)
TOP VIEW



Pin Descriptions

PIN NO.	PIN NAME	TYPE	PIN DESCRIPTION
44-48, 1-3	C(7:0)	Input	8-bit processor input data bus. C7 is the MSB. Data is written to the control register selected on A(3:0) on the rising edge of WR when $\overline{WE}$ is active.
42	WR	Input	Write clock for the processor interface. Parallel data is clocked into the chip on the rising edge of WR.
40	$\overline{WE}$	Input	Write enable. Active low. $\overline{WE}$ must be active when writing data to the chip.
35-38	A(3:0)	Input	Processor interface address bus. These pins select the destination register for data on the C(7:0) bus. A3 is the MSB.
6	CLK	Clock	NCO and DAC clock. The phase accumulator and DAC output update on the rising edge of this clock. CLK can be asynchronous to the WR clock.
8	$\overline{RESET}$	Input	Reset. Active low. Resets control registers to their default states (see register description table) and zeroes the feedback in the phase accumulator. $\overline{UPDATE}$ must be low for Reset to occur.
30	SCLK	Input	Serial clock. Polarity is programmable. See control word 12. May be asynchronous to CLK. If not used, connect to DGND.
27	SDATA	Input	Serial data. See control word 12. If not used, connect to DGND.
32	SSYNC	Input	Serial sync. See control word 12. If not used, connect to DGND.
9	$\overline{UPDATE}$	Input	Active low. Updates the active control registers only. It has no effect on the ENOFR or PH(1:0) pins. This pin is provided for updating an entire frequency word at once rather than byte by byte.
33, 34	PH(1:0)	Input	Phase offset bits. The phase of the output is shifted. If not used, these pins should be grounded. 00 – 0° reference 01 – 90° shift 10 – 180° shift 11 – 270° shift
4	ENOFR	Input	Enable offset frequency. Active high. When high, the offset frequency bus is enabled to the phase accumulator. When low, the offset frequency bus is zeroed. This pin does not affect the contents of the offset frequency registers. If not used, the pin should be grounded.
10	COMPOUT	Output	Comparator output.
11	REFLO	Input	Connect to analog ground to enable the DAC's internal 1.2V reference or connect to AV_{DD} to disable the internal reference.
12	REFIO	Input	Reference voltage input for the DAC if internal reference is disabled. Recommend the use of a 0.1µF cap to ground from the REFIO pin when a DC reference voltage is used.
13	FSADJ		Full scale current adjust for the DAC. Use a resistor to ground (R_{SET}) to adjust the full scale output current. Full Scale Output Current = 32 x V_{FSADJ}/R_{SET}, where V_{FSADJ} equals the reference voltage.
14	COMP1		Noise reduction for the DAC. Connect a 0.1µF cap to AV_{DD} plane.
19	COMP2		Noise reduction for the DAC. Connect a 0.1µF cap to AGND plane.
18	IOUTA	Output	DAC current output.
17	IOUTB	Output	DAC complementary current output.
20	AVDD	Power	Analog supply voltage.
15, 16, 21, 24	AGND	GND	Analog ground.
7, 26, 31, 43	DVDD	Power	Digital supply voltage.
5, 25, 28, 29, 41	DGND	GND	Digital ground.
22, 23	IN+, IN-	Input	Comparator inputs. To power down the comparator, connect both of these pins to the analog power supply. This will conserve ~4mA of current.
39	NC	NC	No connect.

Typical Application Circuit (Parallel Control Mode, Sinewave Generation)



Functional Description

The ISL5314 is an NCO with an integrated 14-bit DAC designed to run in excess of 125MSPS. The NCO is a 16-bit output design, which is rounded to fourteen bits for input to the DAC. The frequency control is the sum of a 48-bit center frequency word, a 48-bit offset frequency word, and a 40-bit serially loaded tuning word. The three components are added modulo 48 bits with the alignment shown in Table 1. Each of the three terms can be zeroed independently (via the microprocessor interface for the center and serial frequency registers and via the ENOFR pin for the offset frequency term).

Frequency Generation

The output frequency of the part is determined by the summation of three registers as shown in Equation 1:

$$f_{OUT} = f_{CLK} \times ((CF + OF + SF) \bmod (2^{48}))/ (2^{48}) \quad \text{(EQ. 1)}$$

where CF is the center frequency register, OF is the offset frequency register, SF is the serial frequency register and f_{CLK} is the DDS clock rate.

With a 125MSPS clock rate, the center frequency can be programmed to Equation 2:

$$(125 \times 10^6)/(2^{48}) = 0.4\mu Hz \text{ resolution} \quad \text{(EQ. 2)}$$

The addition of the frequency control words can be interpreted as two's complement if convenient. For example, if the center frequency is set to 4000...00h and the offset frequency set to C000..00h, the programmed center frequency would be $f_{CLK}/4$ and the programmed offset frequency $-f_{CLK}/4$. The sum would be 10000..00h, but because only the lower 48 bits are retained, the effective frequency would be 0. In reality, frequencies above 8000...00h alias below $f_{CLK}/2$ (the output of the part is real), so the MSB is only provided as a convenience for two's complement calculations.

The frequency control of the NCO is the change in phase per clock period or $d\phi/dt$. This is integrated by the phase accumulator to obtain frequency. The most significant 24 bits of phase are then mapped to 16 bits of amplitude in a sine look-up table function. The range of $d\phi/dt$ is 0–1 with 1 equaling 360° or (2 x pi) per clock period. The phase accumulator output is also 0–1 with 1 equaling 360°. The operations are modulo 48 bits because the MSB (Bit 47) aligns with the most significant address bit of the sine ROM and the ROM contains one cycle of a sinusoid. The MSB is weighted at 180°. Full scale is 360° minus one LSB and the phase then rolls over to 0° for the next cycle of the sinusoid.

The DDS can be clocked with either a sinusoidal or a square wave. Refer to the digital inputs V_{IH} and V_{IL} values in the electrical specifications table.

Parallel Interface

The processor interface is an 8-bit parallel write only interface. The interface consists of eight data bits (C7:C0), four address pins (A3:A0), a write strobe (WR), and a write enable ($\overline{WE}$). The interface is a master/slave type. The processor interface loads a set of master registers. The contents of the master set of registers is then transferred to a slave set of registers by asserting a pin ($\overline{UPDATE}$). This allows all of the bits of the frequency control to be updated simultaneously.

The rate which the user writes (WR) to these registers does not have to be the same rate as the DDS clock rate (the rate of the NCO and DAC; pin CLK). It is expected that most applications will have a slower register write rate than the DDS clock rate. It takes one WR cycle at the write rate for each register that is written and another eleven CLK cycles at the DDS rate to write and obtain a new output, assuming that the $\overline{UPDATE}$ pin is always active. If the $\overline{UPDATE}$ pin is not active until after the new word has been written, it takes fourteen CLK cycles, rather than eleven. For cases which require the output to be updated with all of the new frequency information present, it is necessary that the $\overline{UPDATE}$ be inactive until after all of the new frequency word has been written to the device. See the Timing Diagrams for more information. The parallel registers can be written at a rate of CLK/2, such that updated control words can be pipelined. If the application does not require all registers to be written, then the output frequency can be changed more quickly. For example, if only 32 bits of frequency information are needed and it is desired that the output be updated all at once, then it takes four WR cycles, then the assertion low of the $\overline{UPDATE}$ pin, plus another fourteen CLK cycles at the DDS rate to write and update a new frequency.

The timing is the same whether writing to the center or offset frequency registers. For faster frequency update, consider the ENOFR (Enable Offset Frequency Register) option. Once the values have been written to the center and offset frequency registers, the user can enable and disable the offset frequency register, which is added to the center frequency value when enabled. The ENOFR pin has a latency of fourteen CLK cycles, but simplifies the interface because the only pin that has to be toggled is the ENOFR pin. See "FSK Modulation" on page 6 for a detailed explanation.

Serial Interface

A serial interface is provided for loading a tuning frequency. This interface can be asynchronous to the master clock of the part. When the tuning word has been shifted into the part, it is loaded into a holding register by the serial interface clock, SCLK. This loading triggers a synchronization circuit to transfer the data to a slave register synchronous with the master clock. A minimum of eleven serial clocks (at minimum serial word size of eight) are necessary to complete the transfer to the slave register. Another twelve DDS CLK cycles are necessary before the output of the DDS reflects the new frequency as shown in Equation 3.

$$\text{Serial loading latency} = ((8 \times N + 3) \times SCLK) + 12 \times f_{CLK} \quad \text{(EQ. 3)}$$

TABLE 1. FREQUENCY CONTROL BIT ALIGNMENTS

48 Bits (Individual Bit Alignment)	4444 4444	3333 3333	3322 2222	2222 1111	1111 1100	0000 0000
	7654 3210	9876 5432	1098 7654	3210 9876	5432 1098	7654 3210
Phase Accumulator	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
Center Frequency	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
Offset Frequency	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
Serial Frequency, 8 Bits	xxxx xxxx	0000 0000	0000 0000	0000 0000	0000 0000	0000 0000
Serial Frequency, 16 Bits	xxxx xxxx	xxxx xxxx	0000 0000	0000 0000	0000 0000	0000 0000
Serial Frequency, 24 Bits	xxxx xxxx	xxxx xxxx	xxxx xxxx	0000 0000	0000 0000	0000 0000
Serial Frequency, 32 Bits	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	0000 0000	0000 0000
Serial Frequency, 40 Bits	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	0000 0000

where N = 1–5 (for 8–40 bit serial data) and f_{CLK} is the DDS clock rate. Three extra SCLKs are required (one for the SYNC pulse plus two additional for register transfer). The latency in seconds depends on how many bits of serial data are being written and the speeds of both clocks. The center and offset frequency registers cannot be written using the serial pins. They must be programmed using the parallel interface.

In order to use the three-wire serial interface in a mode that is not the default mode, the parallel control bus must be used to reprogram Register 12. Register 12 can be set according to the desired options of the serial interface that are described in the register description table. Since the serial register defaults enabled, it must be disabled in register 13 (Bit 6) if it is not used.

Register 14

The parallel control bus must be used to program register 14 with 0x00h or 0x30h after assertion of $\overline{\text{RESET}}$. See “Control Register Description” on page 16 for more information.

Control Pins

There are three control pins provided for phase and frequency control. The PH0 and PH1 pins select phase offsets of 0°, 90°, 180°, and 270° and can be used for low speed, unfiltered BPSK or QPSK modulation. These pins can also be used for providing sine/cosine when using two ISL5314s together as quadrature local oscillators. The ENOFR pin enables or zeros the offset frequency word to the phase accumulator and can be used for FSK or MSK modulation. These control pins and the $\overline{\text{UPDATE}}$ pin are passed through special cells to minimize the probability of metastability. Writing anything to register 15 behaves like an $\overline{\text{UPDATE}}$ so that the user can save one control pin if desired.

Reset

A $\overline{\text{RESET}}$ pin is available which resets all registers to their defaults. Register 14 **must** always be written with 0x00h or 0x30h after a $\overline{\text{RESET}}$. In order to reset the part, the user must take the $\overline{\text{RESET}}$ pin low, allow at least one CLK rising edge, and then take the $\overline{\text{RESET}}$ pin high again. The latency from the $\overline{\text{RESET}}$ pin going high until the output reflects the reset is eleven CLK cycles. See “Control Register Description” on page 16 for the default states of all bits in all registers. After $\overline{\text{RESET}}$ goes high, one rising edge of CLK is required before the control registers can be written to again. The center frequency register resets to $f_{CLK}/4$. The offset frequency register resets to an unknown frequency but is disabled. The serial frequency register resets to an unknown frequency and is enabled. If the serial register is not used, disable it in register 13 using the parallel interface.

Comparator

A comparator is provided for square wave output generation. The user can take the DDS analog output, filter it, and then send it back into the comparator. A square wave will be generated at the comparator output (COMPOUT pin) at an amplitude level that is dependent on the digital power supply (DV_{DD}). The comparator was designed to operate at speeds comparable to the DDS output frequency range (approximately 0MHz to 50MHz). It is not intended for low jitter applications (<0.5ns). The comparator has a sleep mode that is activated by connecting both inputs (IN- and IN+) to the analog power supply plane. This will save approximately 4mA of current (as shown in “Typical Application Circuit (Parallel Control Mode, Sinewave Generation)” on page 3. If the comparator is not used, leave the COMPOUT pin floating.

DAC Voltage Reference

The internal voltage reference for the DAC has a nominal value of +1.2V with a ±60ppm/°C drift coefficient over the full temperature range of the converter. It is recommended that a 0.1µF capacitor be placed as close as possible to the REFIO pin, connected to the analog ground. The REFLO pin (11) selects the reference. The internal reference can be selected if Pin 11 is tied low (ground). If an external reference is desired, then Pin 11 should be tied high (the analog supply voltage) and the external reference driven into REFIO, Pin 12. The full-scale output current of the converter is a function of the voltage reference used and the value of R_{SET}. I_{OUT} should be within the 2mA to 20mA range, though operation below 2mA is possible, with performance degradation.

If the internal reference is used, V_{FSADJ} will equal approximately 1.2V (Pin 13). If an external reference is used, V_{FSADJ} will equal the external reference as shown in Equation 4.

$I_{OUT}(\text{Full Scale}) = (V_{FSADJ}/R_{SET}) \times 32$ (EQ. 4)

Analog Output

IOUTA and IOUTB are complementary current outputs. They are generated by a 14-bit DAC that is capable of running at the full 125MSPS rate. The DDS clock also clocks the DAC. The sum of the two output currents is always equal to the full scale output current minus one LSB. If single-ended use is desired, a load resistor can be used to convert the output current to a voltage. It is recommended that the unused output be equally terminated. The voltage developed at the output must not violate the output voltage compliance range of -1.0V to +1.25V. R_{LOAD} (the impedance loading each current output) should be chosen so that the desired output voltage is produced in conjunction with the output full scale current. If a known line impedance is to be driven, then the output load resistor should be chosen to match this impedance. The output voltage is shown in Equation 5:

$V_{OUT} = I_{OUT} \times R_{LOAD}$ (EQ. 5)

These outputs can be used in a differential-to-single-ended arrangement. This is typically done to achieve better harmonic rejection. Because of a mismatch in IOUTA and IOUTB, the transformer does not improve the harmonic rejection. However, it can provide voltage gain without adding distortion. The SFDR measurements in this data sheet were performed with a 1:1 transformer on the output of the DDS (see Figure 1). With the center tap grounded, the output swing of pins 17 and 18 will be biased at 0V. The loading as shown in Figure 1 will result in a 500mV_{P-P} signal at the output of the transformer if the full scale output current of the DAC is set to 20mA.

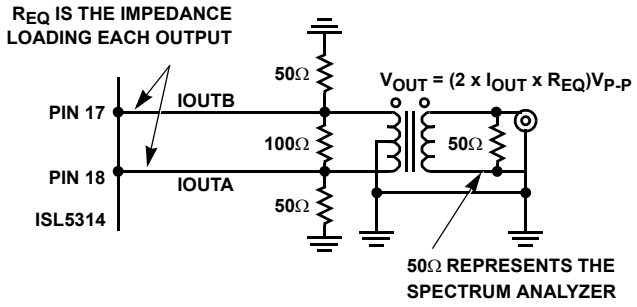


FIGURE 1. TRANSFORMER OUTPUT CIRCUIT OPTION

$V_{OUT} = 2 \times I_{OUT} \times R_{EQ}$, where R_{EQ} is 12.5Ω. Allowing the center tap to float will result in identical transformer output, however, the output pins of the DAC will have positive DC offset, which could limit the voltage swing available due to the output voltage compliance range. The 50Ω load on the output of the transformer represents the load at the end of a 'transmission line', typically a spectrum analyzer, oscilloscope, or the next function in the signal chain. The necessity to have a 50Ω impedance looking back into the transformer is negated if the DDS is only driving a short trace. The output voltage compliance range does limit the impedance that is loading the DDS output.

Application Considerations

Ground Plane

Separate digital and analog ground planes should be used. All of the digital functions of the device and their corresponding components should be located over the digital ground plane and terminated to the digital ground plane. The same is true for the analog components and the analog ground plane. Pins 11 through 24 are analog pins, while all the others are digital.

Noise Reduction

To minimize power supply noise, 0.1µF capacitors should be placed as close as possible to the power supply pins, AV_{DD} and DV_{DD}. Also, the layout should be designed using separate digital and analog ground planes and these capacitors should be terminated to the digital ground for DV_{DD} and to the analog ground for AV_{DD}. Additional filtering of the power supplies on the board is recommended.

Power Supplies

The DDS will provide the best SFDR (spurious free dynamic range) when using +5V analog and +5V digital power supply. The analog supply must always be +5V (±10%). The digital supply can be either a +3.3V (±10%), a +5V (±10%) supply, or anything in between. The DDS is rated to 125MSPS when using a +5V digital supply and 100MSPS when using a +3.3V digital supply.

Improving SFDR

+5V power supplies provides the best SFDR. Under some clock and output frequency combinations, particularly when the f_{CLK}/f_{OUT} ratio is less than 4, the user can improve SFDR even further by connecting the COMP2 pin (19) of the DDS to the analog power supply. The digital supply must be +5V if this option is explored. Improvements as much as 6dBc in the SFDR-to-Nyquist measurement were seen in the lab.

FSK Modulation

Binary frequency shift keying (BFSK) can be done by using the offset frequency register and the ENOFR pin. M-ary FSK or GFSK (Gaussian) can be done by continuously loading in new frequency words. The maximum FSK data rate of the ISL5314 depends on the way the user programs the device to do FSK, and the form of FSK.

For example, simple BFSK is efficiently performed with the ISL5314 by loading the center frequency register with one frequency, the offset frequency register with another frequency, and toggling the ENOFR (enable offset frequency register) pin. The latency is fourteen CLK cycles between assertion of the ENOFR pin and the change occurring at the analog output. However, the change in frequency can be pipelined such that the ENOFR can be toggled at a rate up to as shown in Equation 6:

$ENOFR_{MAX} = f_{CLK}/2$ (EQ. 6)

where f_{CLK} is the frequency of the master CLK.

If M-ary FSK is required (more than two frequencies), the user will have to continually reprogram the center frequency register. The maximum write rate to the same parallel register is the lesser of 50MSPS or $f_{CLK}/2$. One WR clock cycle is required for every register updated. The maximum possible rate occurs if the user only needs to change eight bits (one register). For M-ary FSK, the output frequency rate of change is as shown in Equation 7:

$$\text{M-ary FSK Rate} = \text{WR/REG} \quad \text{(EQ. 7)}$$

where REG = quantity of registers being written and WR = write rate.

PSK Modulation

Binary or quadrature phase shift keying (PSK) can be done by using the phase pins, PH0 and PH1. The change in phase can be pipelined such that the PH pins can be toggled at a rate up to as shown in Equation 8:

$$PH_{MAX} = f_{CLK}/2 \quad \text{(EQ. 8)}$$

where f_{CLK} is the frequency of the master CLK.

Quadrature Local Oscillators

Two ISL5314s can be used as sine/cosine generators for quadrature local oscillator applications. It is important to note that the phase accumulator feedback needs to be zeroed in both devices if it is desired that both DDSs restart with a known phase, which is determined by the use of the phase control pins, PH1 and PH0. To zero the phase accumulator, pull Bit 5 of address 13 low and then high again at the same time in both devices.

Squarewave Clock Source

The on-chip comparator can be used to generate a square wave. The analog output is filtered and then fed into the comparator input. Because the analog output is a sampled-waveform, a high DAC output frequency (relative to the clock rate) creates large amplitude steps in the sampled waveform. These steps have to be smoothed with a lowpass filter in order for the comparator to operate properly, otherwise the zero-order hold nature of the sampled analog output could possibly hold at the comparator's trigger point temporarily causing the comparator to toggle unexpectedly.

For this reason, it is very important that a lowpass filter be used on the analog output prior to the input of the comparator. The user can set one input to the comparator at a DC reference point (typically the mid-point of the filtered signal) and feed the filtered analog output into the other input. See Figure 2 for an example of a square wave circuit using this method. Since IOUTA and IOUTB are differential, the mid-point between the 10k resistors will always be the average value of each signal. The large resistors have to be used so that the parallel resistance of the intended load and the extra load of the averaging circuit yields a negligible

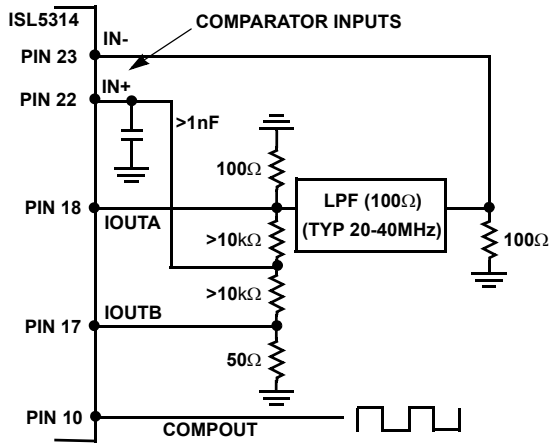


FIGURE 2. SQUAREWAVE GENERATION USING THE ON-CHIP COMPARATOR

effect on the intended load. The average value is used as the reference voltage for one input to the comparator, with a capacitor to filter off any high frequency noise. The other comparator input is connected to the lowpass filter output. It is important that both IOUTA and IOUTB are equally loaded so that each generates the same amplitude and therefore has the same average value.

The user can filter both IOUTA and IOUTB and feed them differentially into the comparator. It is difficult to perfectly match the differential option, so the single-ended option is recommended. The jitter of the comparator is typically 500ps peak to peak. The actual jitter achieved is partially dependent on the quality of the signal at the comparator input, which is dictated by the amount of oversampling of the analog output and the quality of the lowpass filter.

The user also has the option to evaluate the comparator circuit in Figure 2 with lower output current in order to save power consumption in the ISL5314. The DAC output current can be set to 5mA or 10mA instead of 20mA and evaluated to determine if the comparator performance is still suitable for the application. Since the output current is derived from the +5V analog supply, reducing the output from 20mA to 10mA saves approximately 50mW of power. The recommended minimum amplitude of the comparator input is 100mV, so operation of the analog outputs with less than 20mA of output current should be possible with appropriate resistive loading (for example, 5mA into a 50Ω load provides 250mV of amplitude).

If needed, series resistance on the comparator output can be used to reduce overshoot and/or ringing. The comparator can be used to drive a 50Ω load.

Absolute Maximum Ratings

Digital Supply Voltage DV_{DD} to DGND . . . . . +5.5V
Analog Supply Voltage AV_{DD} to AGND . . . . . +5.5V
Grounds, AGND To DGND . . . . . -0.3V To +0.3V
Digital Input Voltages . . . . . DV_{DD} + 0.3V
Reference Input Voltage Range. . . . . AV_{DD} + 0.3V
Analog Output Current (I_{OUT}) 24mA

Operating Conditions

Temperature Range . . . . . .-40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA}(°C/W)
LQFP Package	68

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range. . . . . .-65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

3. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

AV_{DD} = DV_{DD} = +5V (unless otherwise noted), V_{REF} = Internal 1.2V, IOUTFS = 20mA, T_A = -40°C to +85°C for all Min and Max Values. T_A = +25°C for All Typical Values. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNITS
DAC CHARACTERISTICS					
DAC Resolution		**14**	-	-	Bits
Integral Linearity Error, INL	“Best Fit” Straight Line (Note 10)	**-5**	±2.5	**+6**	LSB
Differential Linearity Error, DNL	(Note 10)	**-2**	±1.5	**+4**	LSB
Offset Error, I_{OS}	(Note 10)	**-0.025**		**+0.025**	% FSR
Offset Drift Coefficient	(Note 10)	-	0.1	-	ppm FSR/°C
Full Scale Gain Error	With Internal Reference (Notes 5, 10)	**-10**	±1	**+10**	% FSR
Full Scale Gain Drift	With Internal Reference (Note 10)	-	±50	-	ppm FSR/°C
Full Scale Output Current	(Note 6)	**2**	-	**20**	mA
Output Voltage Compliance Range	(Note 6, 10)	**-1.0**	-	**1.25**	V
DAC DYNAMIC CHARACTERISTICS					
Maximum Clock Rate, f_{CLK}	+5V DV_{DD}, +5V AV_{DD} (Note 6)	**125**	-	-	MSPS
Maximum Clock Rate, f_{CLK}	+3.3V DV_{DD}, +5V AV_{DD} (Note 6)	**100**	-	-	MSPS
Output Settling Time, (t_{SETT})	±0.05% (±8 LSB) (Note 10)	-	35	-	ns
Output Rise Time	Full Scale Step	-	2.5	-	ns
Output Fall Time	Full Scale Step	-	2.5	-	ns
Output Capacitance		-	25	-	pF
Output Noise	IOUTFS = 20mA	-	50	-	pA/$\sqrt{Hz}$
	IOUTFS = 2mA	-	30	-	pA/$\sqrt{Hz}$
AC CHARACTERISTICS					
Spurious Free Dynamic Range, SFDR Within a Window (Notes 7, 10)	f_{CLK} = 100MSPS, f_{OUT} = 20MHz, 5MHz Span	-	93	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 5MHz, 8MHz Span	-	93	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 5MHz, 8MHz Span	-	93	-	dBc

Electrical Specifications AV_{DD} = DV_{DD} = +5V (unless otherwise noted), V_{REF} = Internal 1.2V, IOUTFS = 20mA, T_A = -40°C to +85°C for all Min and Max Values. T_A = +25°C for All Typical Values. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNITS
Spurious Free Dynamic Range, SFDR to Nyquist (f_{CLK}/2) (Notes 7, 10)	f_{CLK} = 125MSPS, f_{OUT} = 40.4MHz	-	40	-	dBc
	f_{CLK} = 125MSPS, f_{OUT} = 10.1MHz	**57**	63	-	dBc
	f_{CLK} = 125MSPS, f_{OUT} = 5.02MHz	-	72	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 40.4MHz	-	40	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 20.2MHz	-	49	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 5.04MHz	-	72	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 2.51MHz	-	73	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 20.2MHz	-	45	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 5.02MHz	-	68	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 2.51MHz	-	72	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 1.00MHz	-	71	-	dBc
	f_{CLK} = 25MSPS, f_{OUT} = 1.0MHz	-	72	-	dBc
DAC REFERENCE VOLTAGE					
Internal Reference Voltage, V_{FSADJ}	Pin 13 Voltage with Internal Reference	**1.13**	1.2	**1.28**	V
Internal Reference Voltage Drift		-	±60	-	ppm/°C
Internal Reference Output Current Sink/Source Capability		-	±0.1	-	µA
Reference Input Impedance		-	1	-	MΩ
Reference Input Multiplying Bandwidth	(Notes 7, 10)	-	1.4	-	MHz
DIGITAL INPUTS					
Input Logic High Voltage with 5V Digital Supply, V_{IH}	(Note 6)	**3.5**	5	-	V
Input Logic High Voltage with 3V Digital Supply, V_{IH}	(Note 6)	**2.0**	3	-	V
Input Logic Low Voltage with 5V Digital Supply, V_{IL}	(Note 6)	-	0	**1.3**	V
Input Logic Low Voltage with 3V Digital Supply, V_{IL}	(Note 6)	-	0	**0.8**	V
Input Logic Current, I_{IH}		**-10**	-	**+10**	µA
Input Logic Current, I_{IL}		**-10**	-	**+10**	µA
Digital Input Capacitance, C_{IN}		-	4	-	pF
TIMING CHARACTERISTICS					
Maximum Clock Rate, f_{CLK}	+5V DV_{DD}, +5V AV_{DD} (Note 6)	**125**	-	-	MSPS
Maximum Clock Rate, f_{CLK}	+3.3V DV_{DD}, +5V AV_{DD} (Note 6)	**100**	-	-	MSPS
CLK Pulse Width, t_{CW}	CLK pin (Note 6)	**5**	-	-	ns
Maximum Parallel Write Rate	Rate of WR pin	**50**	-	-	MSPS
WR Pulse Width, t_{WW}	(Note 6)	**5**	-	-	ns
Data Setup Time, t_{DS}	Between DATA and WR (Note 6)	**10**	-	-	ns
Data Hold Time, t_{DH}	Between DATA and WR (Note 6)	**0**	-	-	ns

Electrical Specifications AV_{DD} = DV_{DD} = +5V (unless otherwise noted), V_{REF} = Internal 1.2V, IOUTFS = 20mA, T_A = -40°C to +85°C for all Min and Max Values. T_A = +25°C for All Typical Values. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNITS
Address Setup Time, t_{AS}	Between ADDR and WR (Note 6)	**12**	-	-	ns
Address Hold Time, t_{AH}	Between ADDR and WR (Note 6)	**0**	-	-	ns
$\overline{\text{UPDATE}}$ Pulse Width, t_{UW}	(Note 6)	**5**	-	-	ns
$\overline{\text{UPDATE}}$ Setup Time, t_{US}	Between $\overline{\text{UPDATE}}$ and CLK (Note 6)	**1**	-	-	ns
$\overline{\text{UPDATE}}$ Hold Time, t_{UH}	Between $\overline{\text{UPDATE}}$ and CLK (Note 6)	**3**	-	-	ns
$\overline{\text{UPDATE}}$ Latency, t_{UL}	After $\overline{\text{UPDATE}}$, before analog output change, if asserted after writing to the control registers	-	14	-	Clock Cycles
$\overline{\text{UPDATE}}$ Latency, t_{UL}	After $\overline{\text{UPDATE}}$, before analog output change, if asserted before writing to the control registers	-	11	-	Clock Cycles
Maximum PH Rate	Rate of PH1 and PH0 pins (Note 6)	**$f_{CLK}/2$**	-	-	Hz
Phase Pulse Width, t_{PW}	PH(1:0) (Note 6)	**5**	-	-	ns
Phase Setup Time, t_{PS}	Between PH(1:0) change and CLK (Note 6)	**1**	-	-	ns
Phase Hold Time, t_{PH}	Between PH(1:0) change and CLK (Note 6)	**3**	-	-	ns
Phase Latency, t_{PL}	Between PH(1:0) change and analog output change	-	12	-	Clock Cycles
Maximum ENOFR Rate	Rate of ENOFR (Note 6)	**$f_{CLK}/2$**	-	-	Hz
ENOFR Pulse Width, t_{EW}	ENOFR (Note 6)	**5**	-	-	ns
ENOFR Setup Time, t_{ES}	Between ENOFR and CLK (Note 6)	**1**	-	-	ns
ENOFR Hold Time, t_{EH}	Between ENOFR and CLK (Note 6)	**3**	-	-	ns
ENOFR Latency, t_{EL}	After ENOFR, before analog output change	-	14	-	Clock Cycles
Write Enable Pulse Width, t_{WR}	$\overline{\text{WE}}$ (Note 6)	**5**	-	-	ns
Write Enable Setup Time, t_{WS}	Between $\overline{\text{WE}}$ and WR (Note 6)	**2**	-	-	ns
Write Enable Hold Time, t_{WH}	Between $\overline{\text{WE}}$ and WR (Note 6)	**4**	-	-	ns
$\overline{\text{RESET}}$ Pulse Width, t_{RW}	$\overline{\text{RESET}}$ (Note 6)	**5**	-	-	ns
$\overline{\text{RESET}}$ Setup Time, t_{RS}	Between $\overline{\text{RESET}}$ and CLK	**1**	-	-	ns
$\overline{\text{RESET}}$ Latency to Output, t_{RL}	After $\overline{\text{RESET}}$, before analog output reflects reset values	-	11	-	Clock Cycles
$\overline{\text{RESET}}$ Latency to Write, t_{RE}	After $\overline{\text{RESET}}$, before the control registers can be written to	-	1	-	Clock Cycles
Maximum SCLK Rate	See Figure 6 on page 14 (Note 6)	**50**	-	-	MSPS
SCLK Pulse Width, t_{SCW}	See Figure 6 on page 14 (Note 6)	**5**	-	-	ns
SDATA Pulse Width, t_{SDW}	See Figure 6 on page 14 (Note 6)	**5**	-	-	ns
SDATA Setup Time, t_{SDS}	Between SDATA and SCLK. See Figure 6 on page 14. (Note 6)	**6**	-	-	ns
SDATA Hold Time, t_{SDH}	Between SDATA and SCLK. See Figure 6 on page 14. (Note 6)	**1**	-	-	ns
SSYNC Pulse Width, t_{SSW}	See Figure 6 on page 14 (Note 6)	**5**	-	-	ns
SSYNC Setup Time, t_{SSS}	Between SSYNC and SCLK. See Figure 6 on page 14. (Note 6)	**6**	-	-	ns
SSYNC Hold Time, t_{SSH}	Between SSYNC and SCLK. See Figure 6 on page 14. (Note 6)	**1**	-	-	ns
COMPARATOR CHARACTERISTICS					
Input Capacitance		-	4	-	pF

Electrical Specifications AV_{DD} = DV_{DD} = +5V (unless otherwise noted), V_{REF} = Internal 1.2V, IOUTFS = 20mA, T_A = -40°C to +85°C for all Min and Max Values. T_A = +25°C for All Typical Values. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNITS
Input Resistance		-	>1	-	MΩ
Input Current		-	1	-	µA
Maximum Input Voltage Allowed	(Excluding Comparator Sleep Mode)	-	4.0	**3.75**	V
Minimum Input Voltage, Peak-to-Peak	(Dependent on Noise)	-	0.1	-	V_{P-P}
Propagation Delay, High to Low	(Note 11)	-	6	-	ns
Propagation Delay, Low to High	(Note 11)	-	5	-	ns
Output Rise Time	(Note 11)	-	1.5	-	ns
Output Fall Time	(Note 11)	-	1.3	-	ns
Output High Voltage, V_{OH}	I_{OH} = -4mA	**2.6**	-	-	V
Output Low Voltage, V_{OL}	I_{OL} = +4mA	-	-	**0.4**	V
Output Jitter		-	0.5	-	ns
Maximum Output Toggle Rate	High Z Load (~1MΩ)	-	100	-	MHz
POWER SUPPLY CHARACTERISTICS					
AV_{DD} (Analog) Power Supply		**4.5**	5.0	**5.5**	V
DV_{DD} (Digital) Power Supply		**3.0**	3.3	**5.5**	V
Analog Supply Current (I_{AVDD})	5V, I_{OUTFS} = 20mA (Note 13)	-	25	**30**	mA
	5V, I_{OUTFS} = 2mA	-	7	-	mA
Digital Supply Current (I_{DVDD})	5V (Notes 8, 13)	-	90	**100**	mA
	3.3V (Notes 9, 12)	-	50	**55**	mA
Power Dissipation	AV_{DD} = 5V, DV_{DD} = 3.3V, I_{OUTFS} = 20mA (Notes 9, 12)	-	290	**363**	mW
	AV_{DD} = 5V, DV_{DD} = 5V, I_{OUTFS} = 20mA (Notes 8, 13)	-	625	**715**	mW
Power Supply Rejection	Single 5V Supply (Note 10)	**-0.2**	-	**+0.2**	% FSR/V

NOTES:

4. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
5. Gain error for the DAC is measured as the error in the ratio between the full scale output current and the current through R_{SET} (typically 625µA); ideally the ratio should be 32.
6. Limits established by characterization and are not production tested.
7. Spectral measurements made with differential transformer coupled output and no external filtering.
8. Measured with the clock at 125MSPS and the output frequency at 10MHz.
9. Measured with the clock at 100MSPS and the output frequency at 10MHz.
10. See “Definition of Specifications” on page 12.
11. 50MHz, High Z Load (~1MΩ), 15pF capacitance, (IN- = 0.5V_{P-P}), (IN+ = 0.25V_{DC}).
12. For maximum value, 5.5V AV_{DD} and 3.6V DV_{DD} are used.
13. For maximum value, 5.5V AV_{DD} and 5.5V DV_{DD} are used.

Definition of Specifications

Differential Non-Linearity (DNL) is the measure of the step size output deviation from code to code. Ideally the step size should be one LSB. A DNL specification of one LSB or less guarantees monotonicity.

Integral Non-Linearity (INL) is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Full Scale Gain Drift is measured by setting the DAC inputs to be all logic high (all 1's) and measuring the output voltage through a known resistance as the temperature is varied from T_{MIN} to T_{MAX}. It is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either T_{MIN} or T_{MAX}. The units are ppm of FSR (full scale range) per °C.

Full Scale Gain Error is the error from an ideal ratio of 32 between the DAC output current and the full scale adjust current (through R_{SET}).

Internal Reference Voltage Drift is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either T_{MIN} or T_{MAX}. The units are ppm per °C.

Offset Drift is measured by setting the DAC inputs to all logic low (all 0's) and measuring the output voltage through a known resistance as the temperature is varied from T_{MIN} to T_{MAX}. It is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either T_{MIN} or T_{MAX}. The units are ppm of FSR (Full Scale Range) per °C.

Offset Error is measured by setting the DAC inputs to all logic low (all 0's) and measuring the output voltage through a known resistance. Offset error is defined as the maximum *deviation* of the output current from a value of 0mA.

Output Settling Time is the time required for the output voltage to settle to within a specified error band measured from the beginning of the output transition. The measurement is done by switching quarter scale. Termination impedance was 25Ω due to the parallel resistance of the 50Ω loading on the output and the oscilloscope's 50Ω input. This also aids the ability to resolve the specified error band without overdriving the oscilloscope.

Output Voltage Compliance Range is the voltage limit imposed on the output. The output impedance should be chosen such that the voltage developed at either IOUTA or IOUTB does not violate the compliance range.

Power Supply Rejection is measured using a single power supply. The nominal supply is varied ±10% and the change in the DAC full scale output current is noted.

Reference Input Multiplying Bandwidth is defined as the 3dB bandwidth of the voltage reference input. It is measured by using a sinusoidal waveform as the external reference with the digital inputs to the DAC set to all 1's. The frequency is increased until the amplitude of the output waveform is 0.707 (-3dB) of its original value.

Spurious Free Dynamic Range (SFDR) is the amplitude difference from the fundamental signal to the largest harmonically or non-harmonically related spur within the specified frequency window.

Timing Diagrams

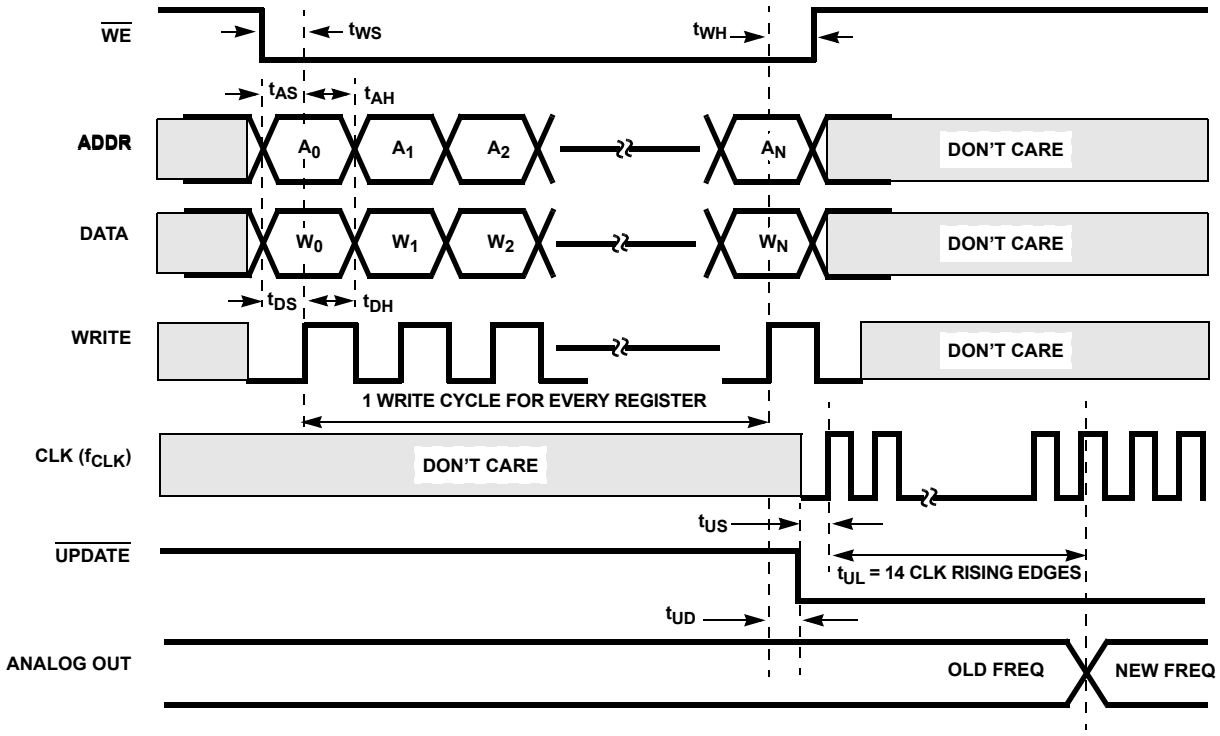


FIGURE 3. PARALLEL-LOAD METHOD 1, $\overline{\text{UPDATE}}$ ACTIVE AFTER LOADING REGISTERS ($\overline{\text{RESET}}$ = HIGH)

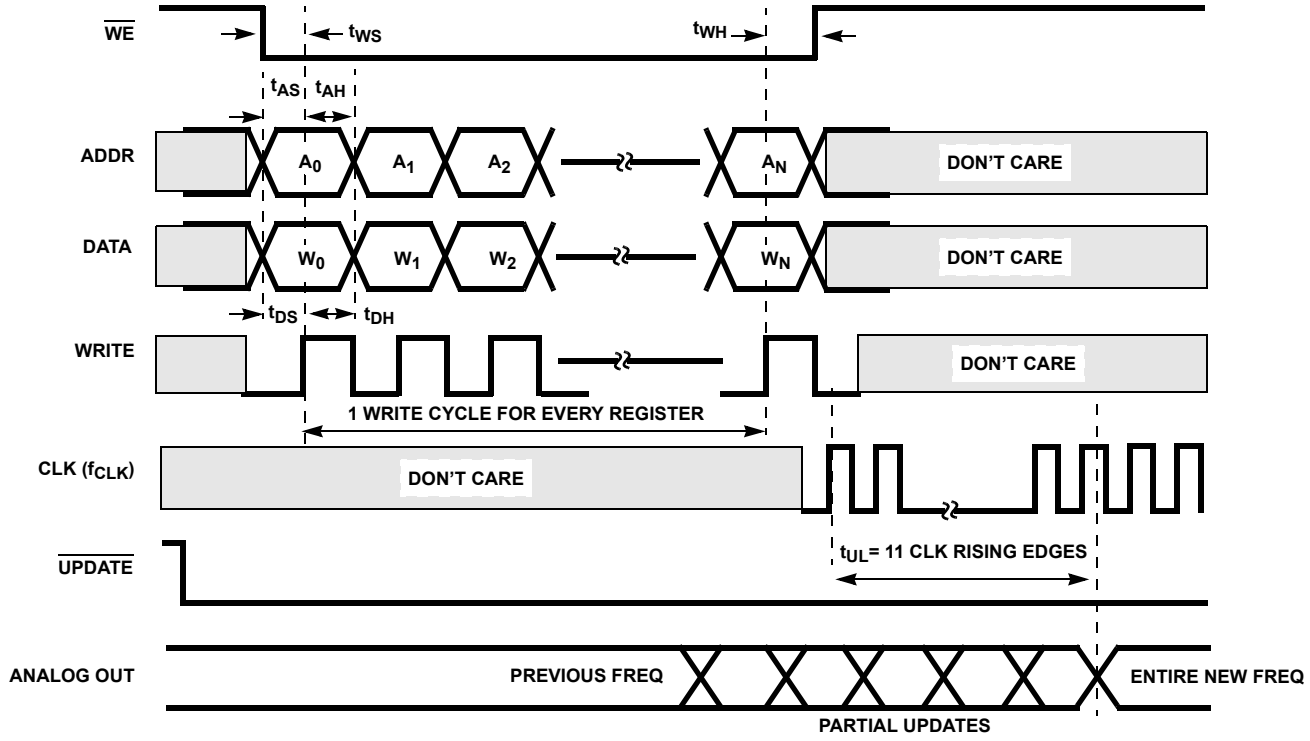


FIGURE 4. PARALLEL-LOAD METHOD 2, $\overline{\text{UPDATE}}$ ACTIVE WHILE LOADING REGISTERS ($\overline{\text{RESET}}$ = HIGH)

Timing Diagrams (Continued)

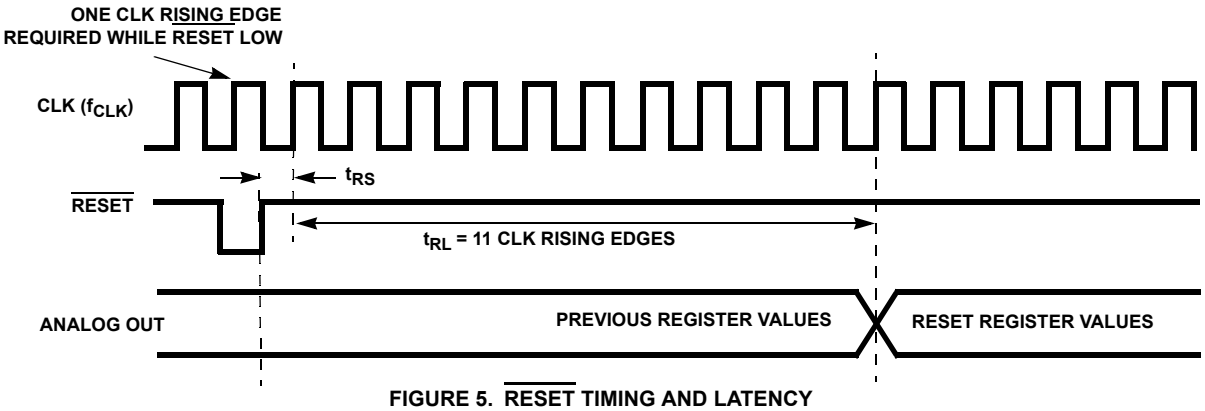


FIGURE 5. $\overline{\text{RESET}}$ TIMING AND LATENCY

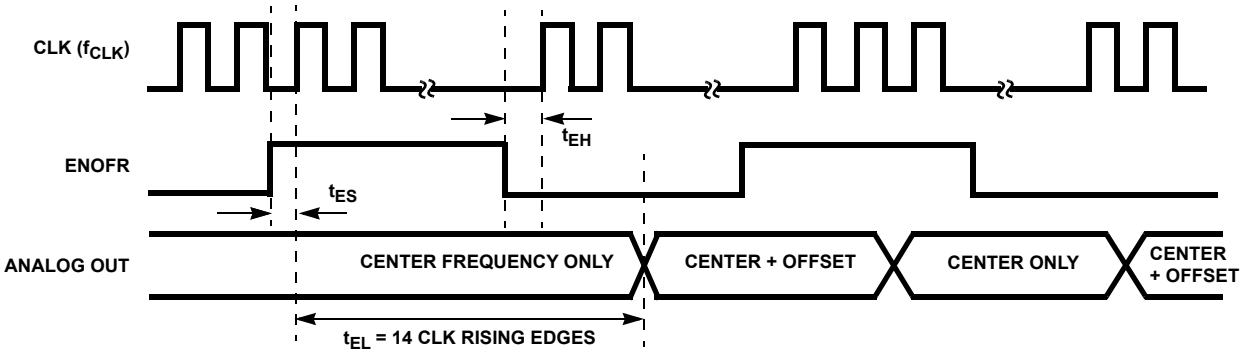


FIGURE 6. ENOFR (ENABLE OFFSET FREQUENCY REGISTER) TIMING AND LATENCY ($\overline{\text{RESET}}$ = HIGH)

Timing Diagrams (Continued)

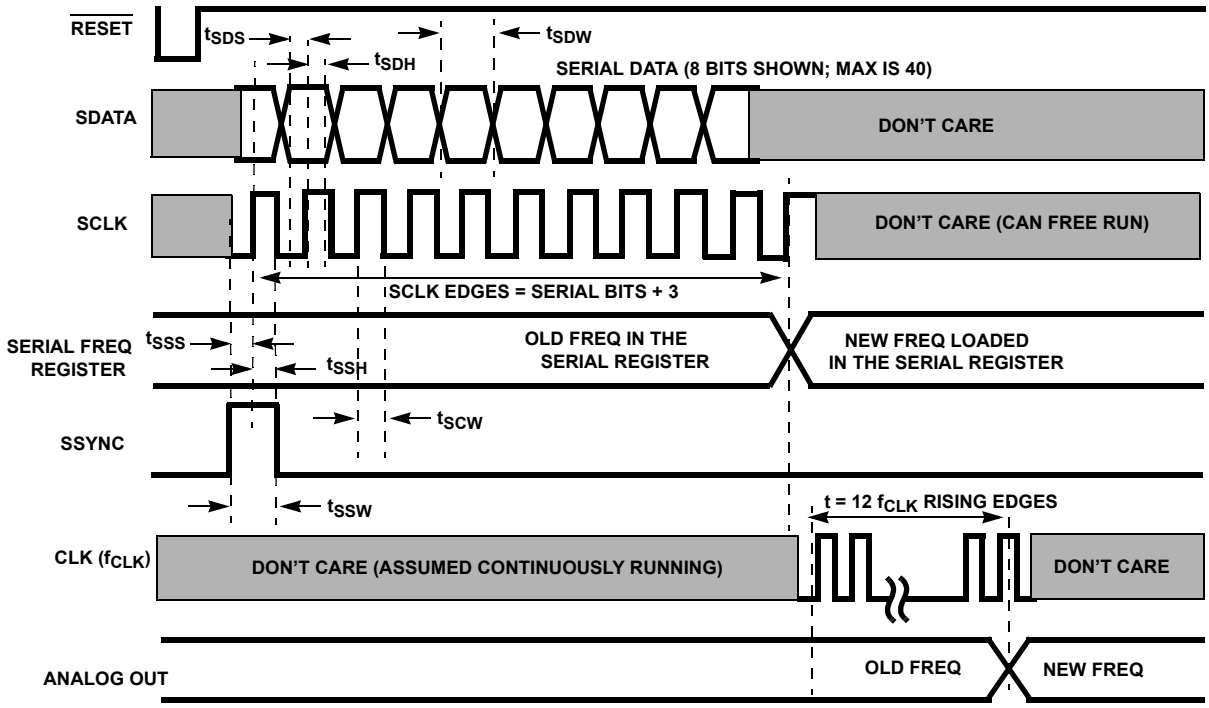


FIGURE 7. SERIAL PROGRAMMING, SYNC EARLY MODE (REPRESENTS MINIMUM SCLKS REQUIRED. SCLK CAN FREE RUN.) CONTROL REGISTER 12 IS SET TO 0001 00XX.

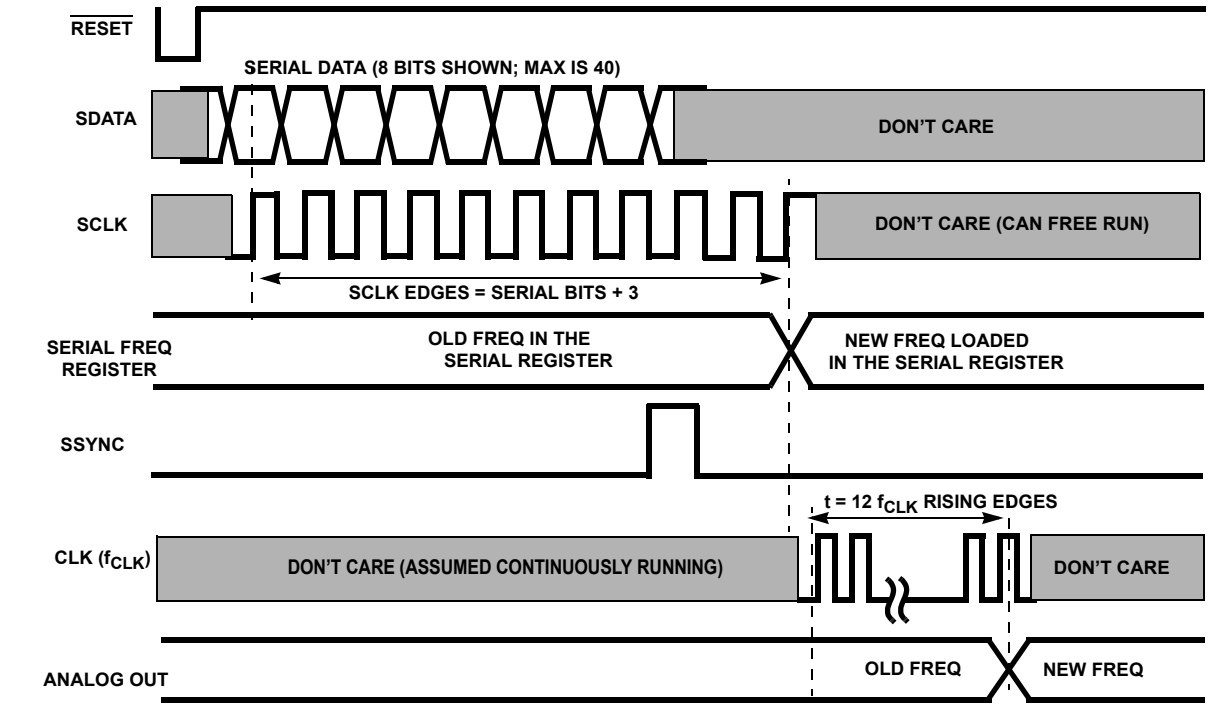


FIGURE 8. SERIAL PROGRAMMING, SYNC LATE BURST MODE (REPRESENTS MINIMUM SCLKS REQUIRED; SCLK CAN FREE RUN); CONTROL REGISTER 12 IS SET TO 0000 00XX.

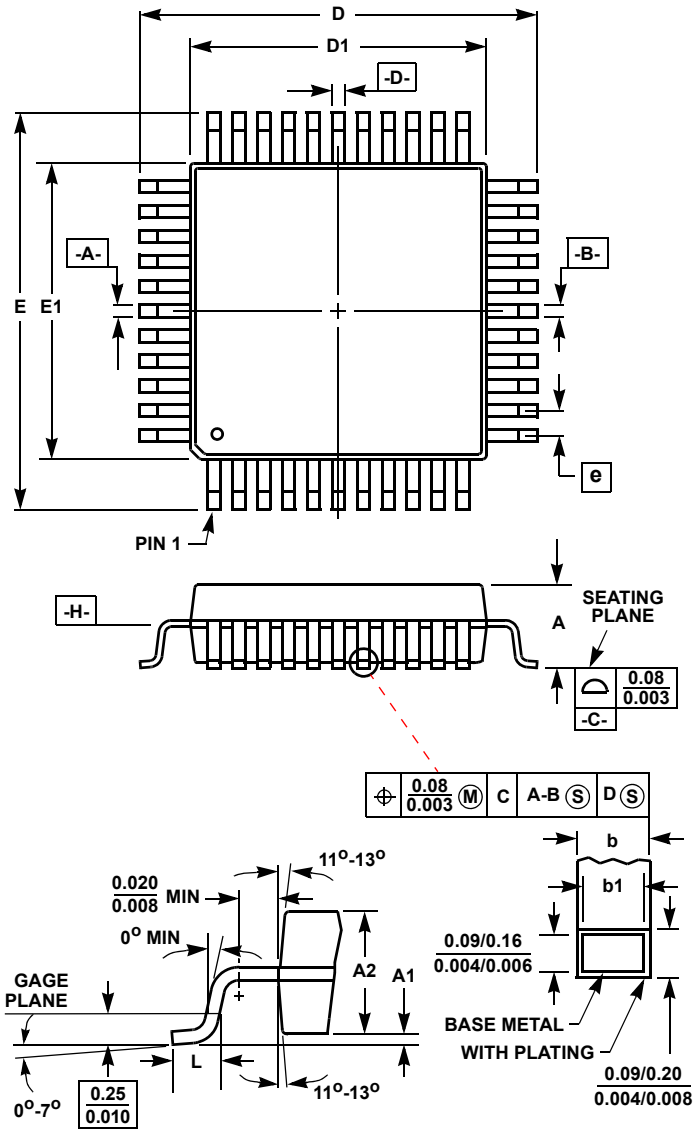
Control Register Description

ADDRESS	BITS	DESCRIPTION	RESET STATE (Note 14)
0	7:0	Center frequency bits CF(7:0) (LSB).	00h
1	7:0	Center frequency bits CF(15:8).	00h
2	7:0	Center frequency bits CF(23:16).	00h
3	7:0	Center frequency bits CF(31:24).	00h
4	7:0	Center frequency bits CF(39:32).	00h
5	7:0	Center frequency bits CF(47:40) (MSB). (Reset gives $f_{CLK}/4$ output).	40h
6	7:0	Offset frequency bits OF(7:0) (LSB).	00h
7	7:0	Offset frequency bits OF(15:8).	00h
8	7:0	Offset frequency bits OF(23:16).	00h
9	7:0	Offset frequency bits OF(31:24).	00h
10	7:0	Offset frequency bits OF(39:32).	00h
11	7:0	Offset frequency bits OF(47:40) (MSB).	00h
12	7:0	Serial input control word.	01h
	7:5	Select number of serial frequency input bits: 1xx = 40-bit word (weighting same as CF(47:8)) 011 = 32-bit word (weighting same as CF(47:16)) 010 = 24-bit word (weighting same as CF(47:24)) 001 = 16-bit word (weighting same as CF(47:32)) 000 = 8-bit word (weighting same as CF(47:40))	000b
	4	Serial input sync position select: 1 = sync early. Sync is expected one serial clock period before the first data bit. 0 = sync late. Sync is expected one serial clock after the last data bit.	0b
	3	Serial sync polarity: 1 = active low, 0 = active high.	0b
	2	Serial clock polarity: 0 = rising edge, 1 = falling edge.	0b
	1	Shift direction: 0 = MSB first, 1 = LSB first.	0b
	0	Center frequency enable: 1 = enable, 0 = disable. This bit can be used to zero the center frequency (CF(47:0)) to the phase accumulator. This does not zero the processor interface registers—just the data path from the center frequency register to the phase accumulator. The center frequency resets to $f_{CLK}/4$.	1b
13	7:0	NCO control word.	F8h
	7	Intersil reserved. Do not change.	1b
	6	Serial output frequency register enable: 1 = enable, 0 = disable. This bit enables/disables the data path from the serial frequency register to the phase accumulator, without changing the value of the register. Should be disabled after $\overline{\text{RESET}}$ if not used.	1b
	5	Phase accumulator feedback: 0 = accumulator feedback disabled, 1 = accumulator enabled.	1b
	4:0	Intersil reserved. Do not change.	11000b
14	7:0	Test and timing control register. User **must** write 00h or 30h to register 14 after $\overline{\text{RESET}}$.	10h
	5:4	NCO-to-DAC setup and hold timing control. Write either 11b or 00b to these bits.	01b
15	7:0	Register 15 does not actually exist. Any write to register 15 is an $\overline{\text{UPDATE}}$. This function is provided to save one microprocessor control pin from being used for the $\overline{\text{UPDATE}}$ pin, if the user chooses.	N/A

NOTE:

14. b = binary, h = hex

Thin Plastic Quad Flatpack Packages (LQFP)



Q48.7x7A (JEDEC MS-026BBC ISSUE B)
48 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.062	-	1.60	-
A1	0.002	0.005	0.05	0.15	-
A2	0.054	0.057	1.35	1.45	-
b	0.007	0.010	0.17	0.27	6
b1	0.007	0.009	0.17	0.23	-
D	0.350	0.358	8.90	9.10	3
D1	0.272	0.280	6.90	7.10	4, 5
E	0.350	0.358	8.90	9.10	3
E1	0.272	0.280	6.90	7.10	4, 5
L	0.018	0.029	0.45	0.75	-
N	48		48		7
e	0.020 BSC		0.50 BSC		-

Rev. 2 1/99

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm (0.003 inch).
7. “N” is the number of terminal positions.

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