# Single, Dual, and Quad 40V Low Noise Precision Amplifiers

**Check for Samples: LMP8671, LMP8672, LMP8674**

## FEATURES

- **Output Short Circuit Protection**
- **PSRR and CMRR Exceed 110dB**
- **Best in Class Linearity (135dB)**

## APPLICATIONS

- **Low Noise Industrial Applications Including Test, Measurement, and Ultrasound**
- **Precision Active Filters**
- **PLL Filters**
- **4-20mA Current Loops**
- **Motor Control**

## KEY SPECIFICATIONS

- **Input Offset Voltage 0.4mV**
- **TC $V_{OS}$ 2µV/°C (max)**
- **Power Supply Voltage Range ±2.5V to ±20V**
- **Voltage Noise Density 2.5nV/$\sqrt{Hz}$**
- **Slew Rate ±20V/µs**
- **Gain Bandwidth Product 55MHz**
- **Open Loop Gain 135dB**
- **Input Bias Current 10nA**

## DESCRIPTION

The LMP8671/2/4 combines great precision, low noise and a large operating voltage range to provide a high SNR and a wide dynamic range. Its AC performance allows it to be used over a wide frequency without degradation. It is the ideal choice for applications requiring DC precision and low noise such as precision PLL filters, multi feedback and multi pole active filters, GPS receivers and precision control loop systems. The LMP8671/2/4 offers an extremely high open loop gain of 135dB, low voltage noise density (2.5nV/$\sqrt{Hz}$), and a superb linearity of 0.000009%. These characteristics drastically reduce gain error which is a challenge in accurate systems requiring higher gains such as data acquisition systems.

To ensure that the most challenging loads are driven without compromise, the LMP8671/2/4 has a high slew rate of ±20V/µs and an output current capability of ±26mA.

The LMP8671/2 family of high-voltage amplifiers are available in SOIC-8, the LMP8674 in SOIC-14.

### Connection Diagrams

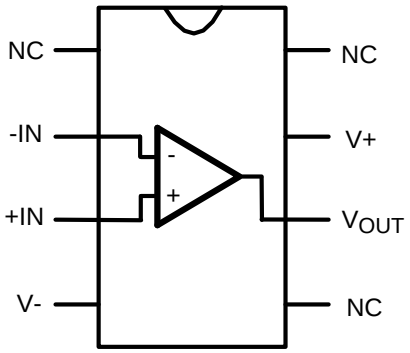



**Figure 1. See Package Number — D0008A**

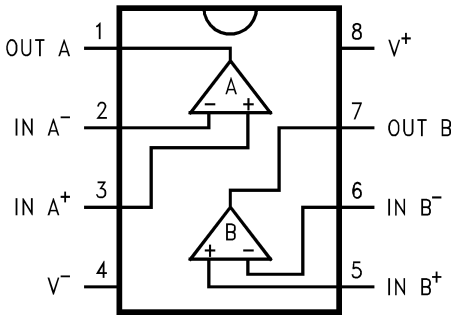



**Figure 2. See Package Number — D0008A**

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2011–2013, Texas Instruments Incorporated

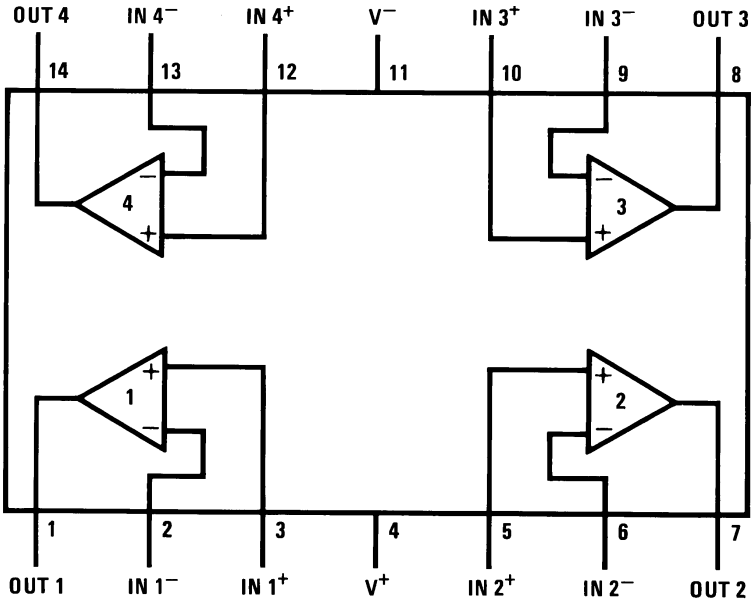



**Figure 3. See Package Number — D0014A**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings[1][2][3]

| | | |
|---|---|---|
| Power Supply Voltage ($V_S = V^+ - V^-$) | | 46V |
| Storage Temperature | | −65°C to 150°C |
| Input Voltage | | (V-) - 0.7V to (V+) + 0.7V |
| Output Short Circuit[4] | | Continuous |
| Power Dissipation | | Internally Limited |
| ESD Rating[5] | | 2000V |
| ESD Rating[6] | Pins 1, 4, 7 and 8 | 200V |
| | Pins 2, 3, 5 and 6 | 100V |
| Junction Temperature | | 150°C |
| Thermal Resistance | $\theta_{JA}$ (SO) | 145°C/W |
| For soldering specifications, http://www.ti.com/lit/SNOA549 | | |

(1) "*Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.

(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{JMAX}$, $\theta_{JA}$, and the ambient temperature, $T_A$. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.

(5) Human body model, applicable std. JESD22-A114C.

(6) Machine model, applicable std. JESD22-A115-A.

## Operating Ratings

| | |
|---|---|
| Temperature Range $T_{MIN} \le T_A \le T_{MAX}$ | $-40°C \le T_A \le 125°C$ |
| Supply Voltage Range LMP8671/2/4 | $\pm 2.5V \le V_S \le \pm 22V$ |


Copyright © 2011–2013, Texas Instruments Incorporated

## Electrical Characteristics for the LMP8671/2/4[1]

The following specifications apply for $V_S$ = ±20V, $R_L$ = 2kΩ, $R_{SOURCE}$ = 10Ω, $f_{IN}$ = 1kHz, $T_A$ = 25°C, unless otherwise specified. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | LMP8671/2/4 | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typical[2] | Limit[3] | |
| $V_{OS}$ | Offset Voltage | | ±100 | ±400<br>**±750** | µV (max) |
| $\Delta V_{OS}/\Delta Temp$ | Average Input Offset Voltage Drift vs Temperature | –40°C ≤ $T_A$ ≤ 125°C | 0.1 | 2 | µV/°C (max) |
| $I_B$ | Input Bias Current | $V_{CM}$ = 0V | | | |
| | | LMP8671/4 | 10 | ±75<br>**±95** | nA (max) |
| | | $V_{CM}$ = 0V | | | |
| | | LMP8672 | 50 | ±200<br>**±250** | nA (max) |
| $I_{OS}$ | Input Offset Current | $V_{CM}$ = 0V | | | |
| | | LMP8671/4 | 11 | ±50<br>**±95** | nA (max) |
| | | $V_{CM}$ = 0V | | | |
| | | LMP8672 | 25 | ±100<br>**±125** | nA (max) |
| $\Delta I_{OS}/\Delta Temp$ | Input Bias Current Drift vs Temperature | –40°C ≤ $T_A$ ≤ 125°C | 0.2 | | nA/°C |
| $V_{IN-CM}$ | Common-Mode Input Voltage Range | | +17.1<br>–16.9 | | V (min)<br>V (min) |
| $Z_{IN}$ | Differential Input Impedance | | 30 | | kΩ |
| | Common Mode Input Impedance | –10V<Vcm<10V | 1000 | | MΩ |
| $e_n$ | Equivalent Input Noise Voltage | 20Hz to 20kHz | 0.34 | 0.65 | $\mu V_{RMS}$ (max) |
| | Equivalent Input Noise Density | f = 1kHz | 2.5 | 4.7 | nV/√Hz (max) |
| $i_n$ | Current Noise Density | f = 1kHz<br>f = 10Hz | 1.6<br>3.1 | | pA/√Hz |
| THD+N | Total Harmonic Distortion + Noise | $A_V$ = 1, $V_{OUT}$ = 3$V_{rms}$, $R_L$ = 600Ω | 0.00003 | 0.00009 | % (max) |
| $t_S$ | Settling time | $A_V$ = –1, 10V step, $C_L$ = 100pF<br>0.1% error range | 1.2 | | µs |
| GBWP | Gain Bandwidth Product | | 55 | 45 | MHz (min) |
| SR | Slew Rate | | ±20 | ±15 | V/µs (min) |
| PSRR | Average Input Offset Voltage Shift vs Power Supply Voltage | See[4] | 125 | 110<br>**100** | dB (min) |
| CMRR | Common-Mode Rejection | –15V≤Vcm≤15V | 115 | 105<br>**100** | dB (min) |
| $A_{VOL}$ | Open Loop Voltage Gain | –15V ≤ Vout ≤ 15V<br>$R_L$ = 2kΩ | 135 | 125 | dB (min) |
| $V_{OUTMAX}$ | Maximum Output Voltage Swing | $R_L$ = 2kΩ | ±19.0 | ±18.8<br>±18.6 | V (min) |
| $I_{OUT-CC}$ | Instantaneous Short Circuit Current | | +53<br>–42 | | mA |

(1) "*Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) Typical values represent most likely parametric norms at $T_A$ = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.
(3) Datasheet min/max specification limits are ensured by test or statistical analysis.
(4) PSRR is measured as follows: For $V_S$, $V_{OS}$ is measured at two supply voltages, ±5V and ±20V, PSRR = |20log($\Delta V_{OS}/\Delta V_S$)|.

Copyright © 2011–2013, Texas Instruments Incorporated

## Electrical Characteristics for the LMP8671/2/4[1] (continued)

The following specifications apply for $V_S$ = ±20V, $R_L$ = 2kΩ, $R_{SOURCE}$ = 10Ω, $f_{IN}$ = 1kHz, $T_A$ = 25°C, unless otherwise specified. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | LMP8671/2/4 | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typical[2] | Limit[3] | |
| $R_{OUT}$ | Output Impedance | $f_{IN}$ = 10kHz<br>Closed-Loop<br>Open-Loop | <br>0.01<br>13 | | Ω |
| $I_{OUT}$ | Output Current | $R_L$ = 2kΩ | 9.5 | 9.3 | mA (min) |
| $I_S$ | Total Quiescent Current | $I_{OUT}$ = 0mA | | | |
| | | LMP8671 | 5 | 6<br>**8** | mA (max) |
| | | LMP8672 | 12.5 | 16 | mA (max) |
| | | LMP8674 | 20 | 22 | mA (max) |


Copyright © 2011–2013, Texas Instruments Incorporated

## Typical Performance Characteristics

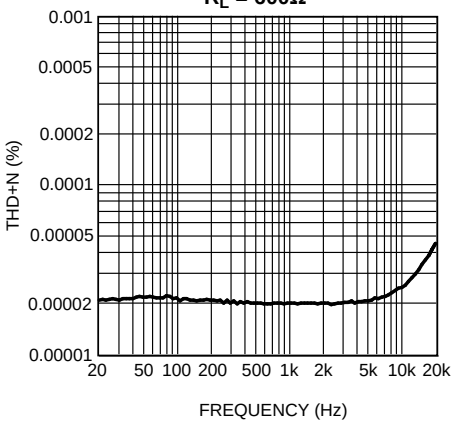



**Figure 4.**

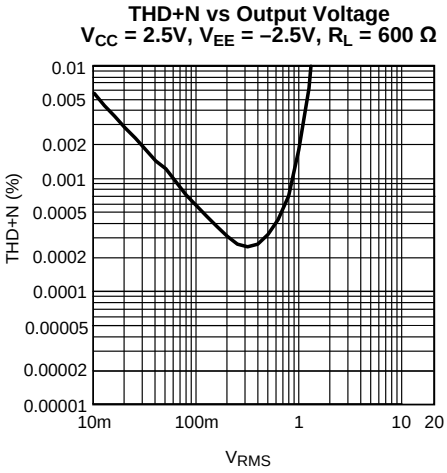



**Figure 5.**

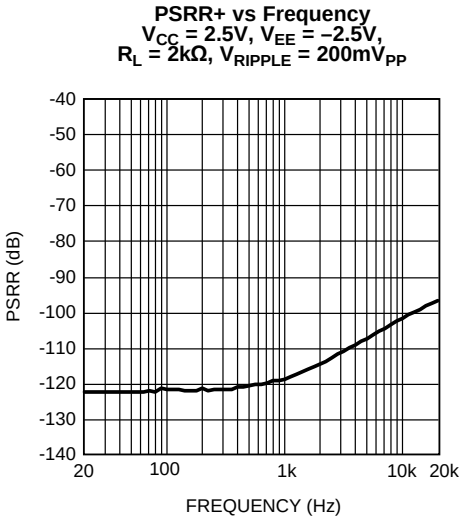



**Figure 6.**

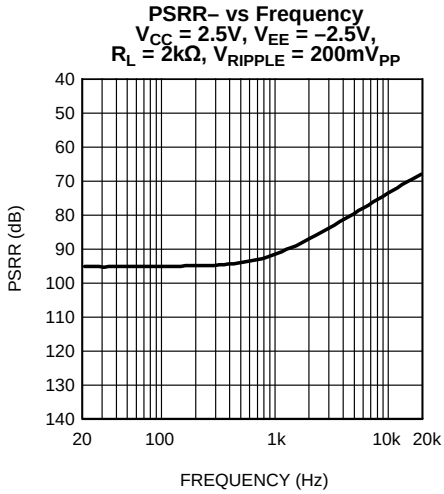



**Figure 7.**

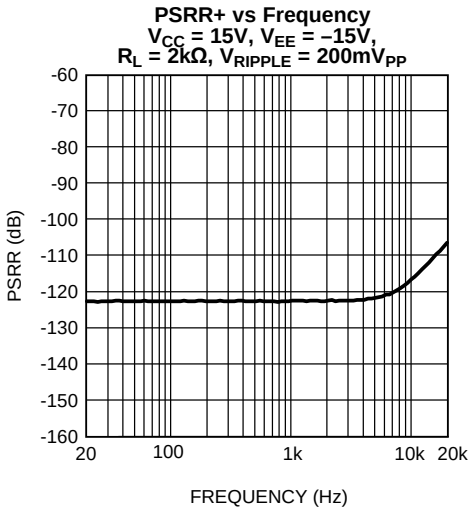



**Figure 8.**

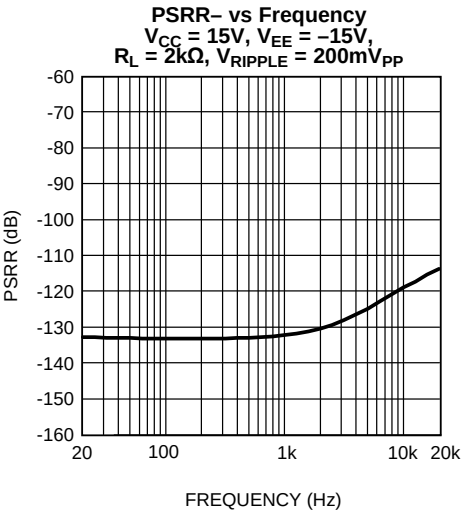



**Figure 9.**

Copyright © 2011–2013, Texas Instruments Incorporated

## Typical Performance Characteristics (continued)

**PSRR+ vs Frequency**
**$V_{CC}$ = 15V, $V_{EE}$ = –15V,**
**$R_L$ = 600Ω, $V_{RIPPLE}$ = 200m$V_{PP}$**

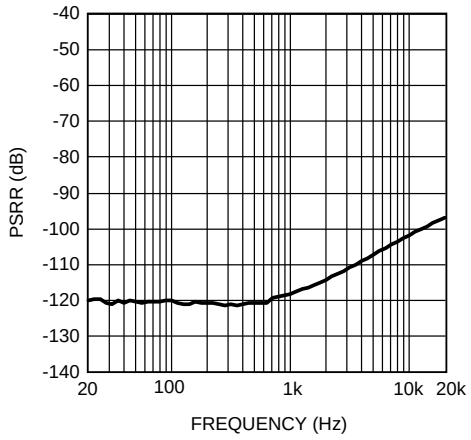



**Figure 10.**

**PSRR– vs Frequency**
**$V_{CC}$ = 15V, $V_{EE}$ = –15V,**
**$R_L$ = 600Ω, $V_{RIPPLE}$ = 200m$V_{PP}$**

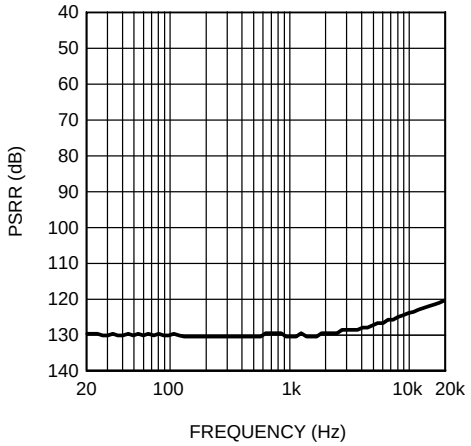



**Figure 11.**

**CMRR vs Frequency**
**$V_{CC}$ = 15V, $V_{EE}$ = –15V, $R_L$ = 600Ω**

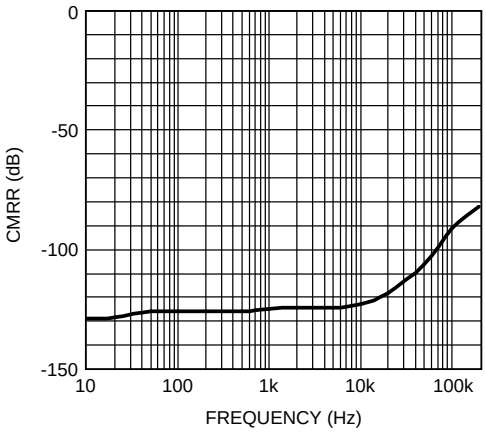



**Figure 12.**

**CMRR vs Frequency**
**$V_{CC}$ = 15V, $V_{EE}$ = –15V, $R_L$ = 2kΩ**

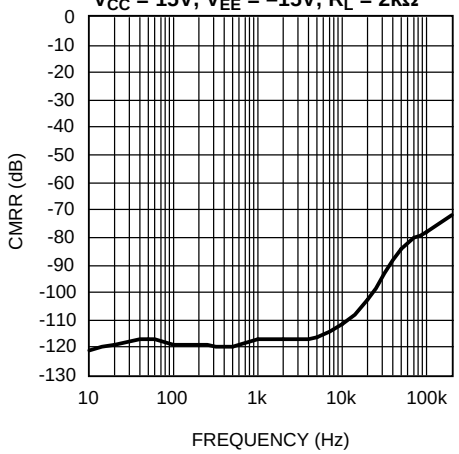



**Figure 13.**

**CMRR vs Frequency**
**$V_{CC}$ = 2.5V, $V_{EE}$ = –2.5V, $R_L$ = 600Ω**

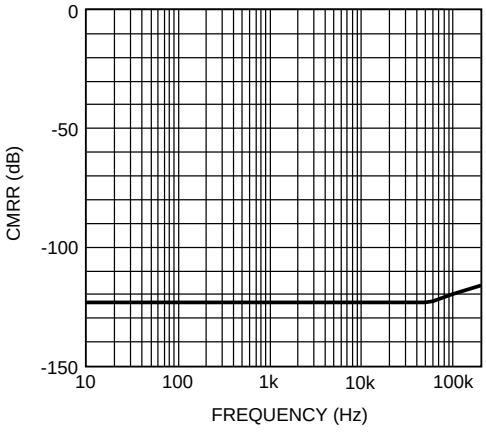



**Figure 14.**

**CMRR vs Frequency**
**$V_{CC}$ = 2.5V, $V_{EE}$ = –2.5V, $R_L$ = 2kΩ**

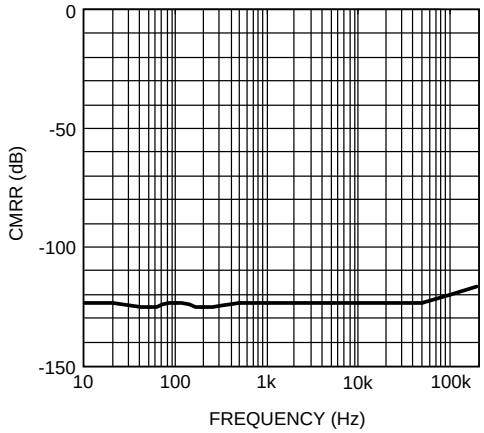



**Figure 15.**


Copyright © 2011–2013, Texas Instruments Incorporated

## Typical Performance Characteristics (continued)

**Output Voltage vs Supply Voltage**
**THD+N = 1%, $R_L$ = 2kΩ**

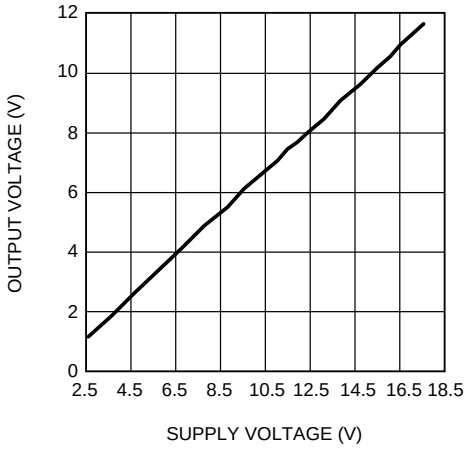



**Figure 16.**

**Output Voltage vs Supply Voltage**
**THD+N = 1%, $R_L$ = 600Ω**

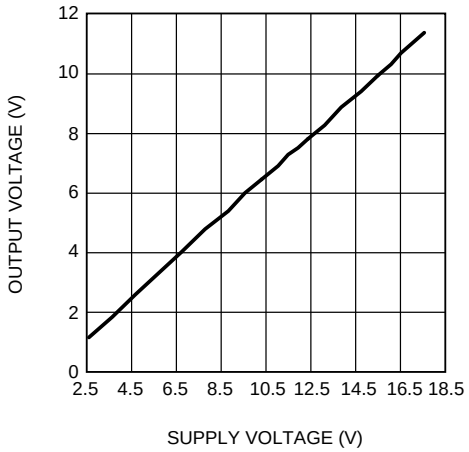



**Figure 17.**

**Crosstalk vs Frequency**
**$V_{CC}$ = 15V, $V_{EE}$ = –15V, $R_L$ = 2kΩ**

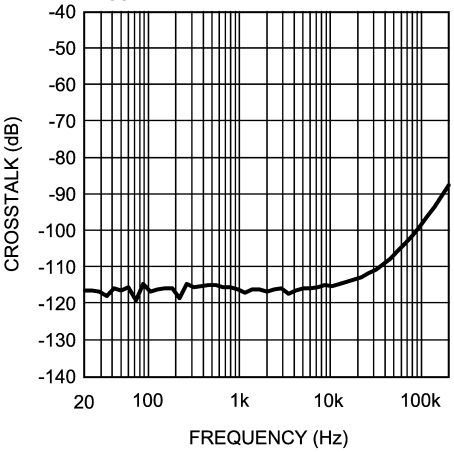



**Figure 18.**

**Full Power Bandwidth vs Frequency**

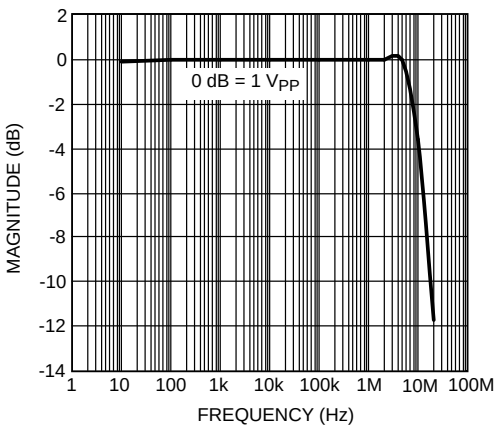



**Figure 19.**

**Gain Phase vs Frequency**

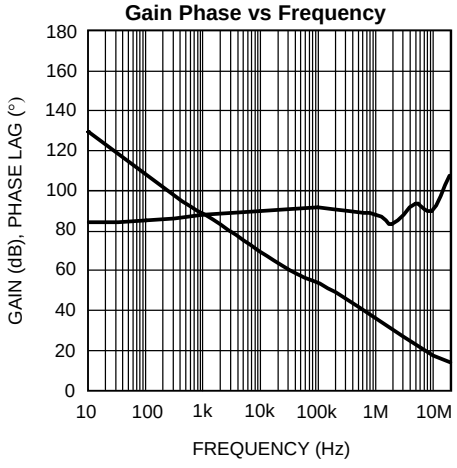



**Figure 20.**

**Voltage Noise Density vs Frequency**

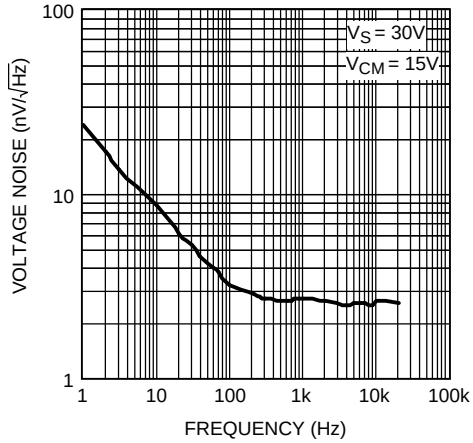



**Figure 21.**

## Typical Performance Characteristics (continued)

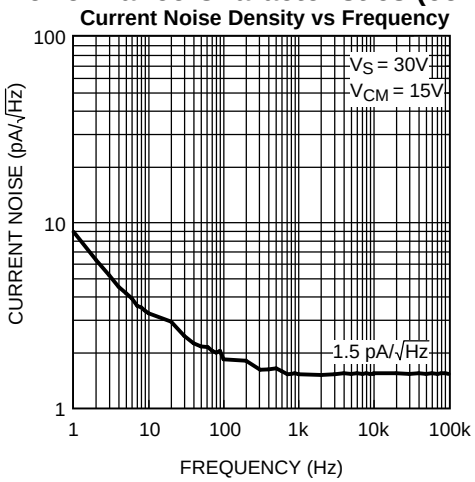



**Figure 22.**

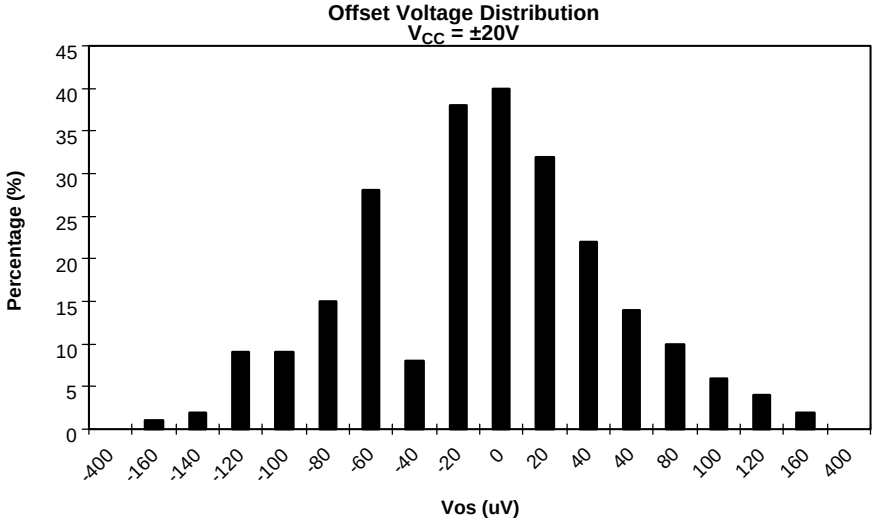



**Figure 23.**

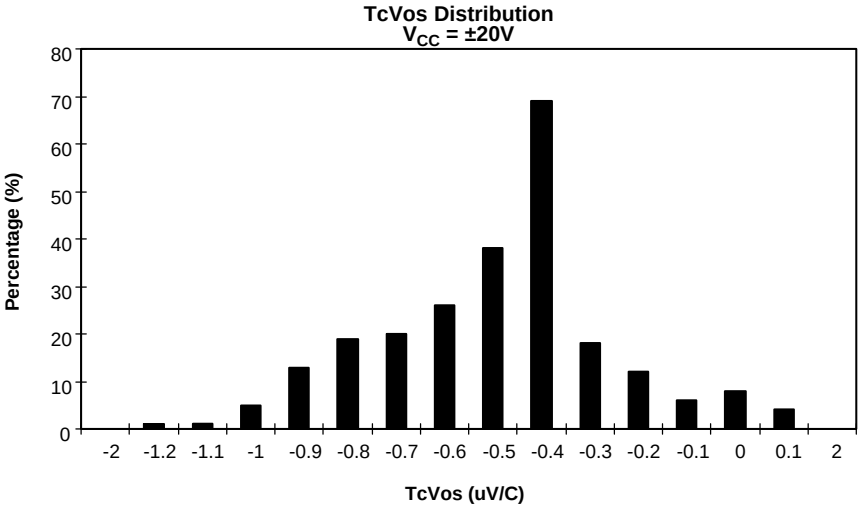



**Figure 24.**


Copyright © 2011–2013, Texas Instruments Incorporated

## REVISION HISTORY

| Changes from Revision A (March 2013) to Revision B | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 8 |

Copyright © 2011–2013, Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LMP8671MA/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LMP86 71MA | Samples |
| LMP8671MAX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LMP86 71MA | Samples |
| LMP8672MA/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LMP86 72MA | Samples |
| LMP8672MAX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LMP86 72MA | Samples |
| LMP8674MA/NOPB | ACTIVE | SOIC | D | 14 | 55 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LMP8674 MA | Samples |
| LMP8674MAX/NOPB | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LMP8674 MA | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

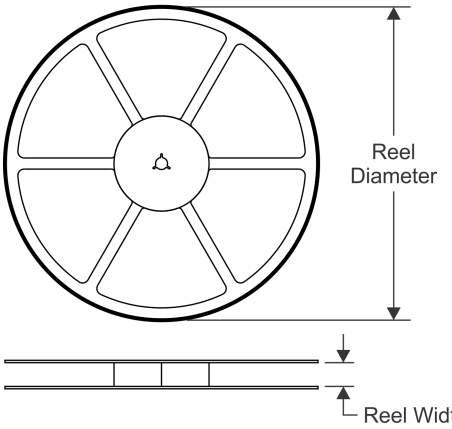
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

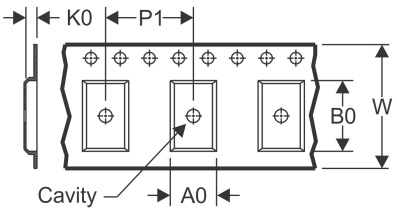
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

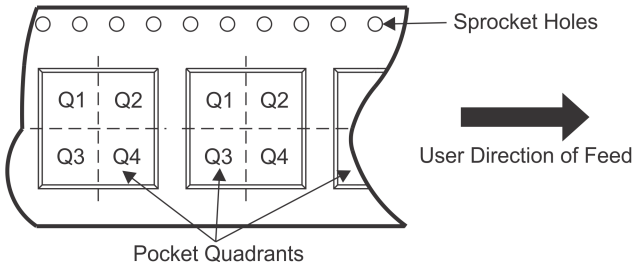



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

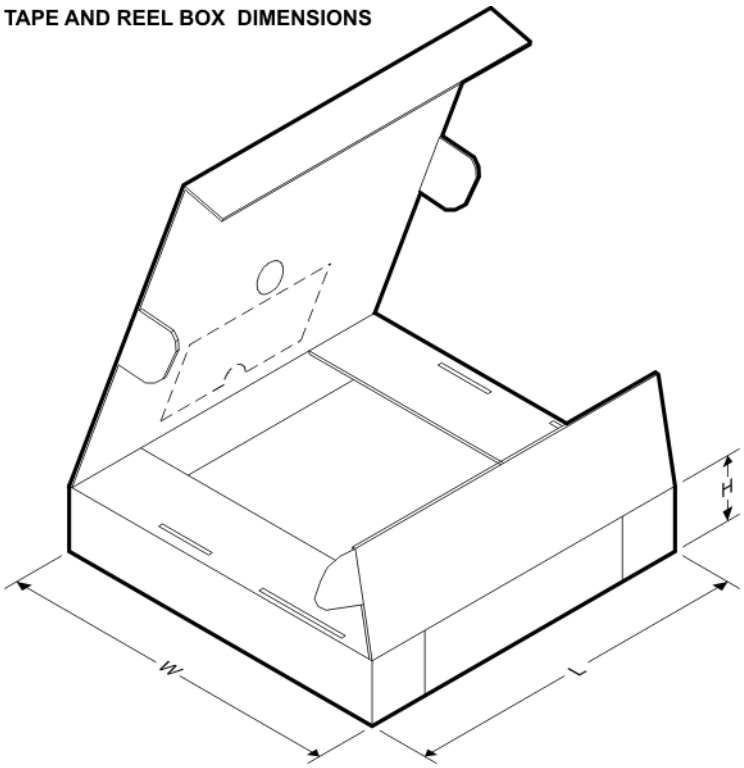
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMP8671MAX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LMP8672MAX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LMP8674MAX/NOPB | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.35 | 2.3 | 8.0 | 16.0 | Q1 |

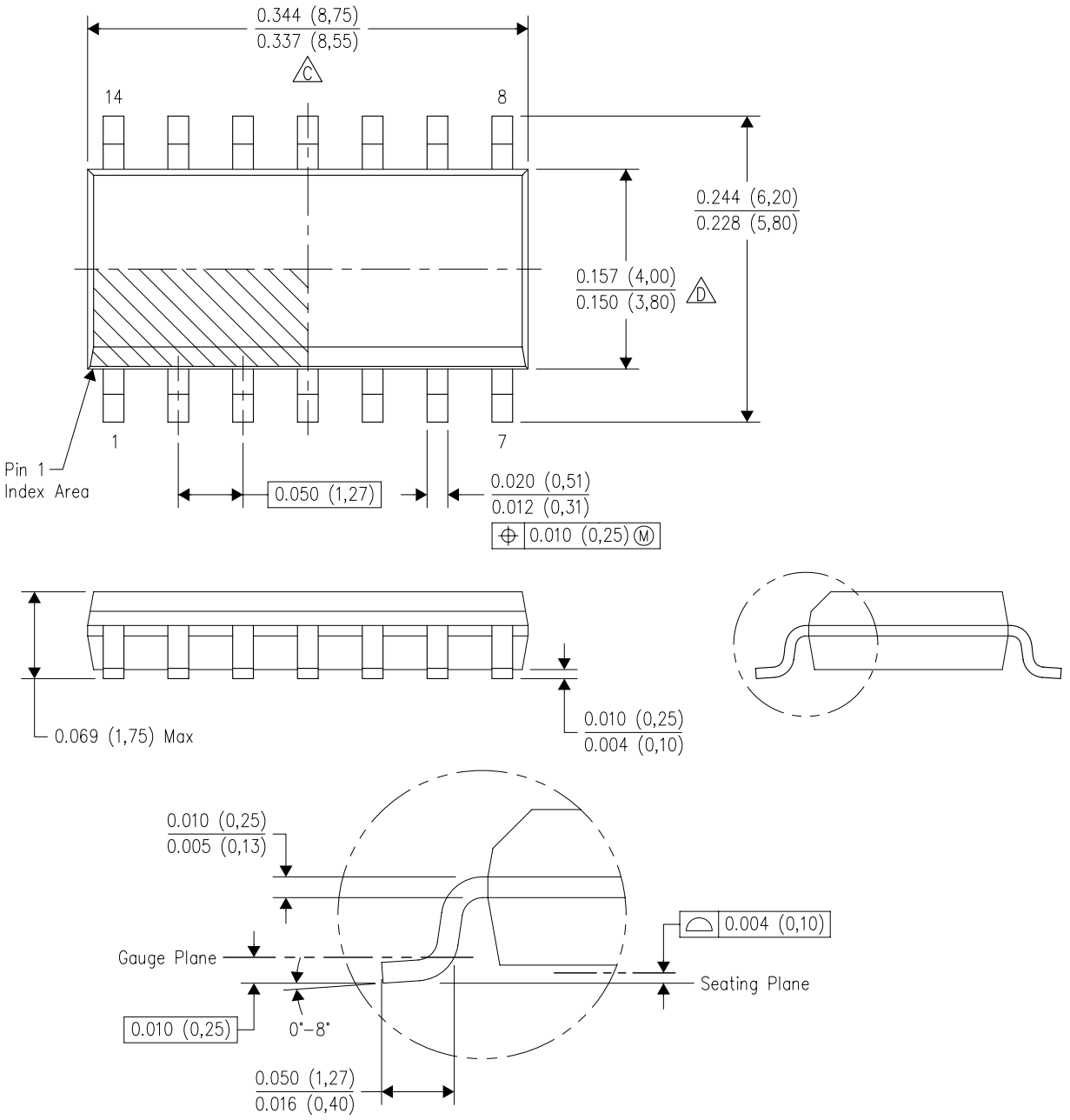
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMP8671MAX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LMP8672MAX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LMP8674MAX/NOPB | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 35.0 |

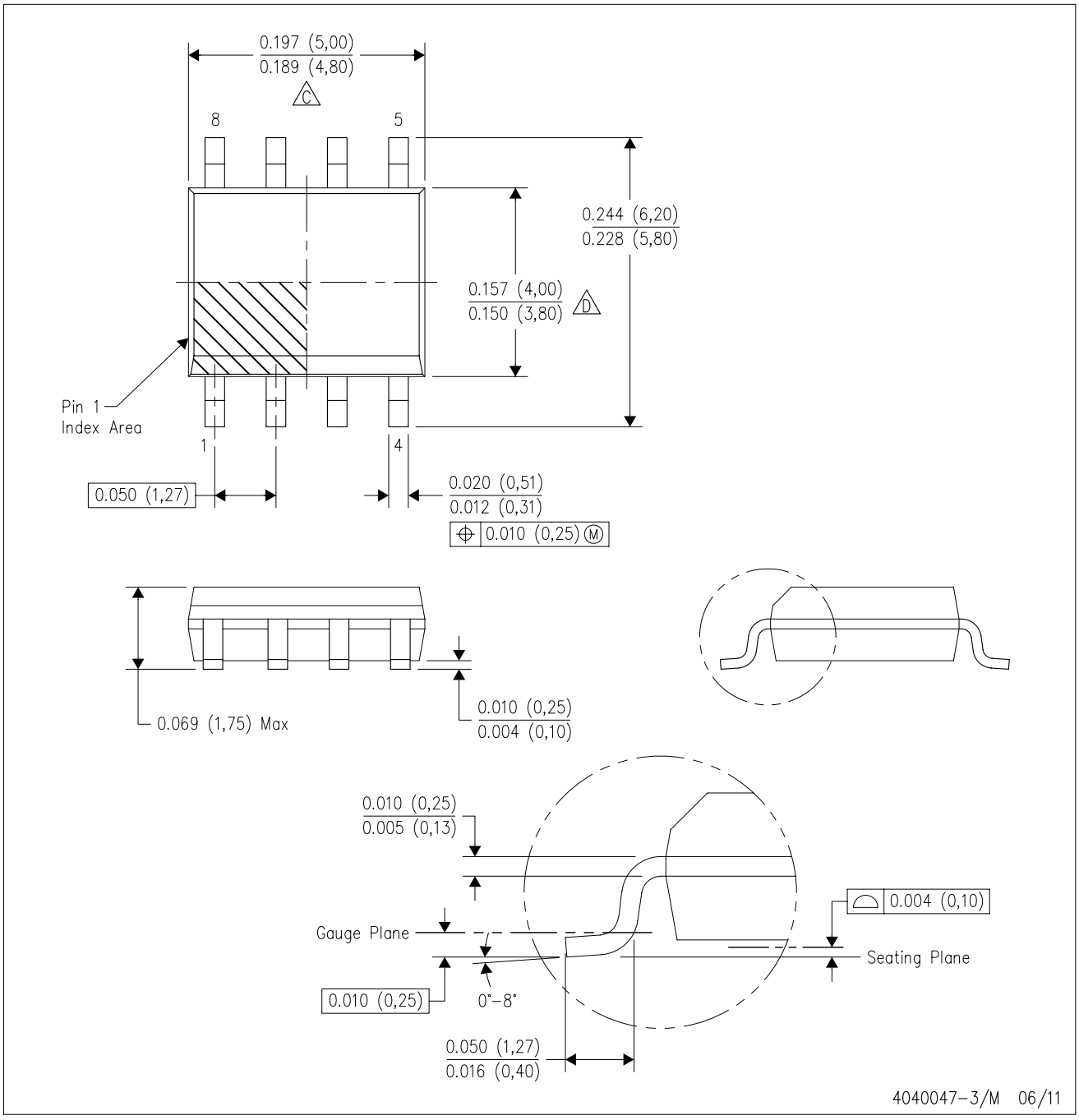
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

| **Products** | | **Applications** | |
|---|---|---|---|
| Audio | www.ti.com/audio | Automotive and Transportation | www.ti.com/automotive |
| Amplifiers | amplifier.ti.com | Communications and Telecom | www.ti.com/communications |
| Data Converters | dataconverter.ti.com | Computers and Peripherals | www.ti.com/computers |
| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Security | www.ti.com/security |
| Power Mgmt | power.ti.com | Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Microcontrollers | microcontroller.ti.com | Video and Imaging | www.ti.com/video |
| RFID | www.ti-rfid.com | | |
| OMAP Applications Processors | www.ti.com/omap | **TI E2E Community** | e2e.ti.com |
| Wireless Connectivity | www.ti.com/wirelessconnectivity | | |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2013, Texas Instruments Incorporated