CMOS/BI-DIRECTIONAL BUS INTERFACE REGISTERS

KEY FEATURES

- **Two Banks of 8 x 16 Registers**
- **Contents of Each Register Available at Output**
- **Provides Temporary Address or Data Storage Between Two Processor Ports or Buses**
- **Bi-Directional Buses Interface — Dual 4-Deep or 8-Deep Registers in Each Direction**
- **Separate Control for Each Register Bank**
- **Direct Processor Bus-to-Bus Interface**
- **TTL Compatible**
- **Replaces Eight WS59520's**

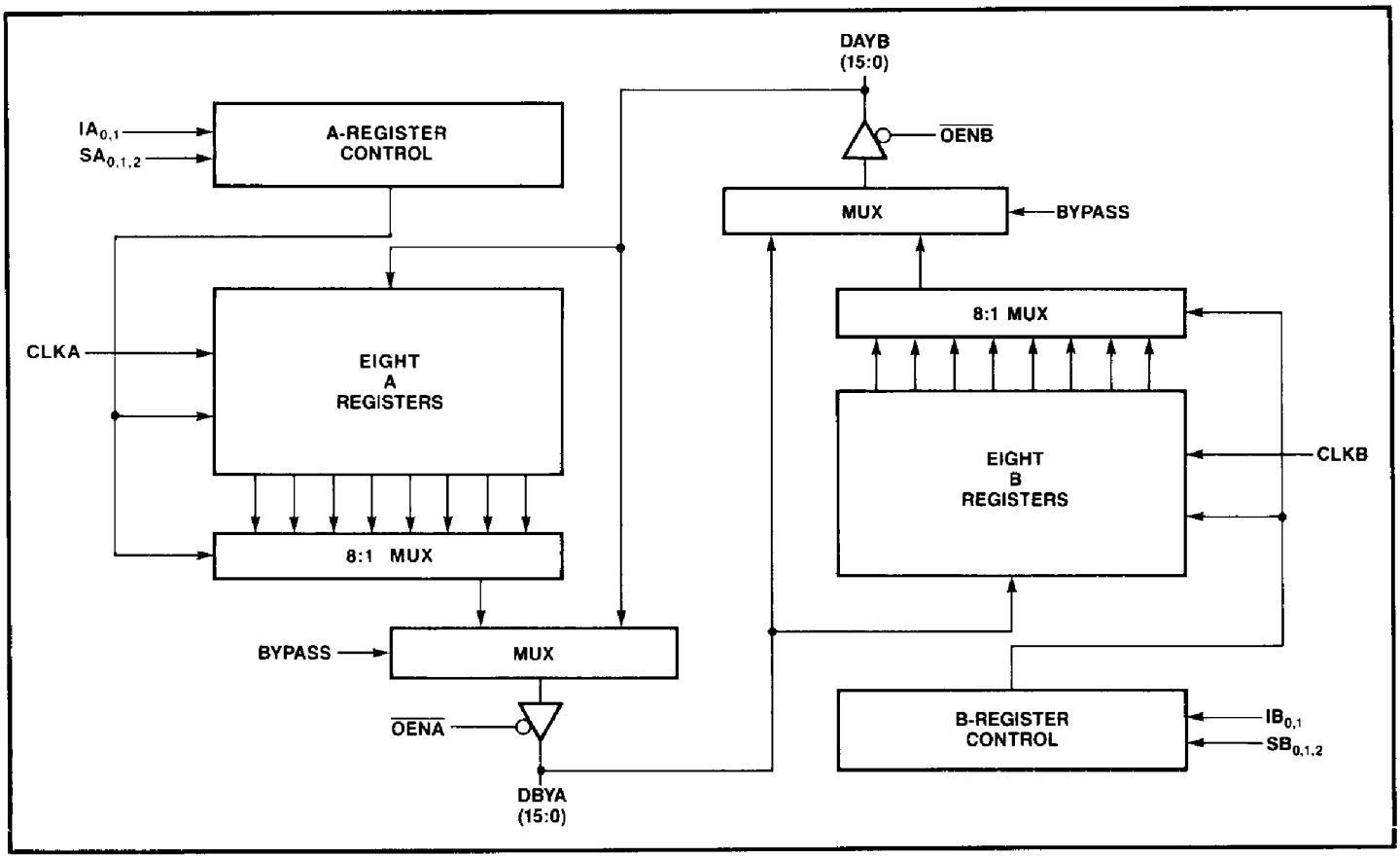
GENERAL DESCRIPTION

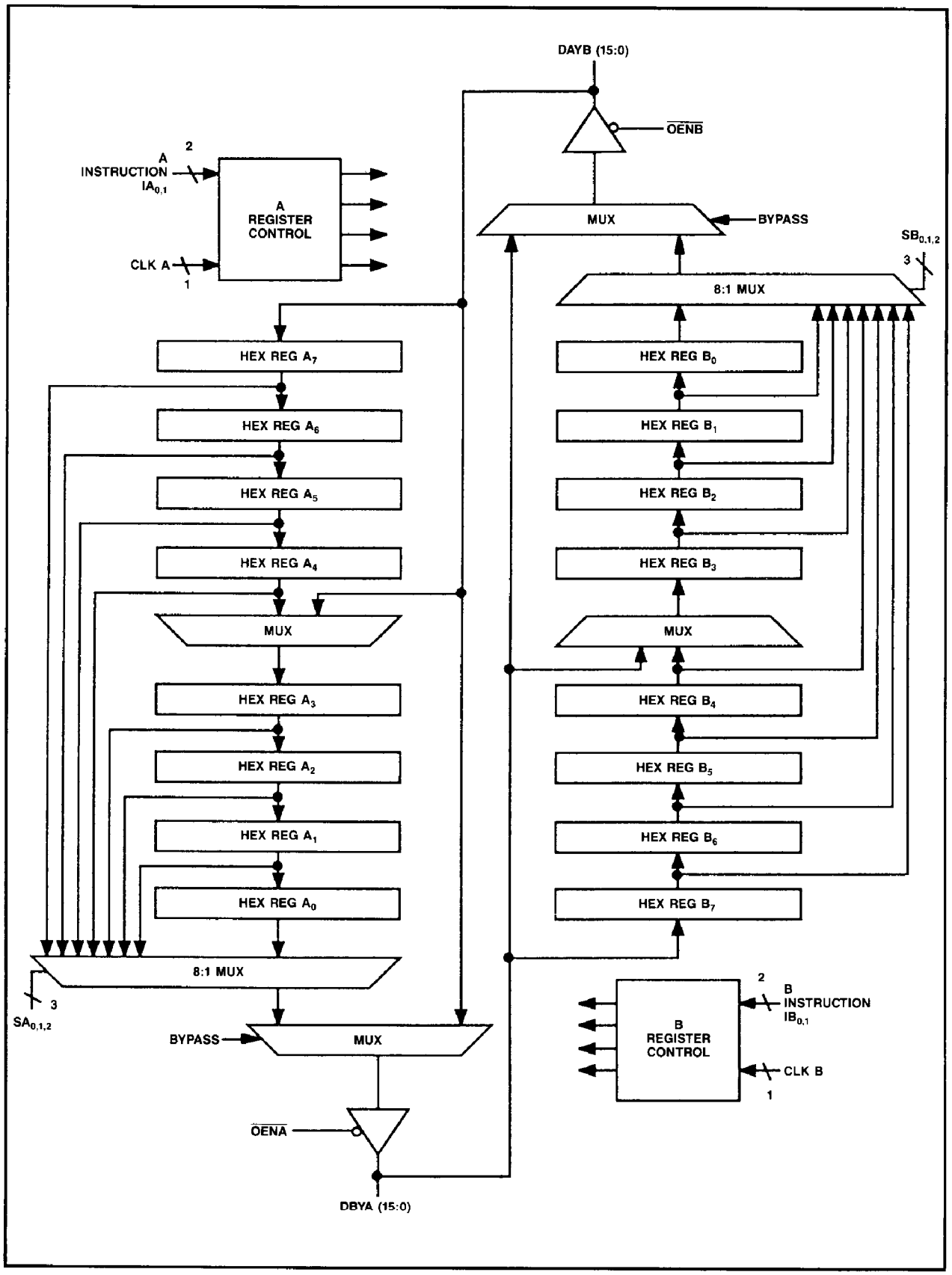
The WS59820/WS59820B consists of two banks of registers, eight registers in each bank, each register 16 bits wide. A single bank can be configured as an eight level pipeline or two each four level pipelines. The architectural configuration is determined by the instruction inputs (I0 and I1) for each register bank.

Each of the eight registers in each bank is available at the multiplex output. The output register is determined by the control inputs (S0, S1, and S2) for each register bank. The multiplexed output is 16 bits wide and is enabled by the $\overline{OEN}$ signal. Each bank of registers has its own clock (CLK), instruction inputs (I0-1) and multiplex controls.

The WS59820 and WS59820B differ only in pin assignments. The WS59820B has additional V_{CC} and ground pin assignments and is recommended for new designs.

BLOCK DIAGRAM



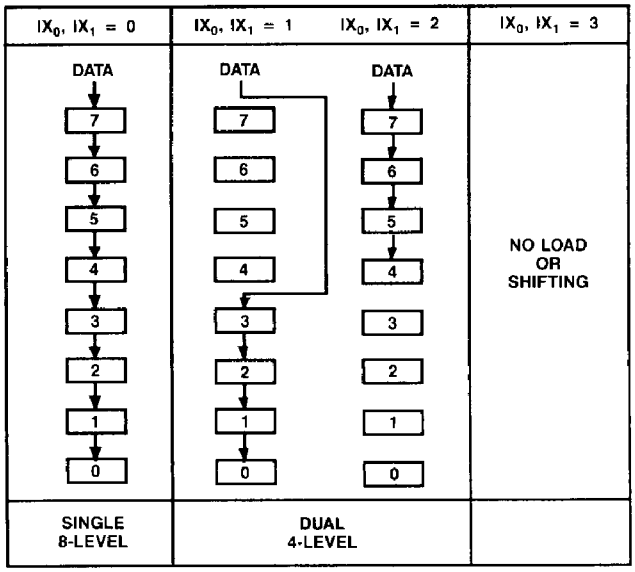

DAYB (15:0)
OENB
2
A
INSTRUCTION
IA0,1
A
REGISTER
CONTROL
CLK A
1
MUX
BYPASS
SB0,1,2
3
8:1 MUX
HEX REG A7
HEX REG A6
HEX REG A5
HEX REG A4
MUX
HEX REG A3
HEX REG A2
HEX REG A1
HEX REG A0
8:1 MUX
3
SA0,1,2
BYPASS
MUX
OENA
DBYA (15:0)
HEX REG B0
HEX REG B1
HEX REG B2
HEX REG B3
MUX
HEX REG B4
HEX REG B5
HEX REG B6
HEX REG B7
2
B
INSTRUCTION
IB0,1
B
REGISTER
CONTROL
CLK B
1

SELECTION TABLE FOR REGISTER A OR B

SX2	SX1	SX0	REGISTER SELECTED
0	0	0	REG 0
0	0	1	REG 1
0	1	0	REG 2
0	1	1	REG 3
1	0	0	REG 4
1	0	1	REG 5
1	1	0	REG 6
1	1	1	REG 7

X = Register A or B.

REGISTER SHIFT OPTIONS FOR REGISTERS A OR B



X = Register A or B.

MULTIPLEX CONTROL

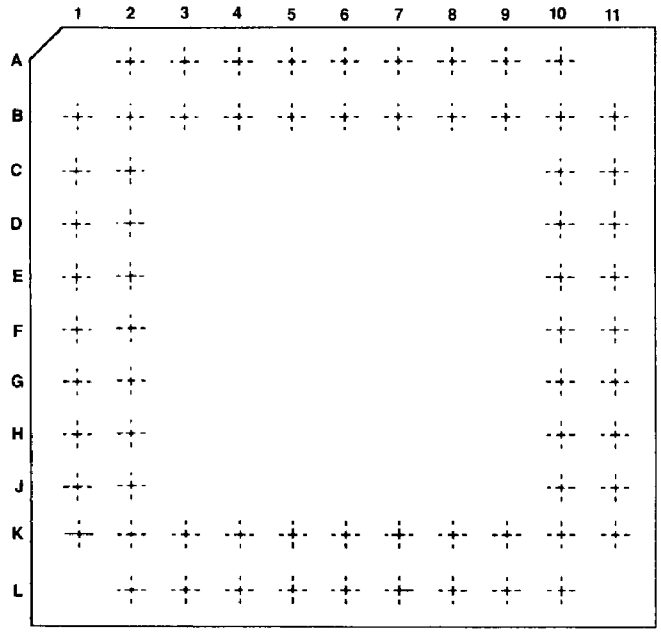
$\overline{OENA}$	$\overline{OENB}$	BYPASS	OPERATION
0	0	1	Pass Output of 8:1 Muxes to Outputs
0	0	0	Not Allowed (Input is Preferred)
0	1	0	Pass Input From DAYB (15:0) to Output DBYA (15:0)
0	1	1	Pass Output From 8:1 Mux to Outputs DBYA (15:0)
1	0	0	Pass Input From DBYA (15:0) to Output DAYB (15:0)
1	0	1	Pass Output From 8:1 Mux to Outputs DAYB (15:0)
1	1	X	Inhibit Outputs (High Impedance)

PIN DESCRIPTION

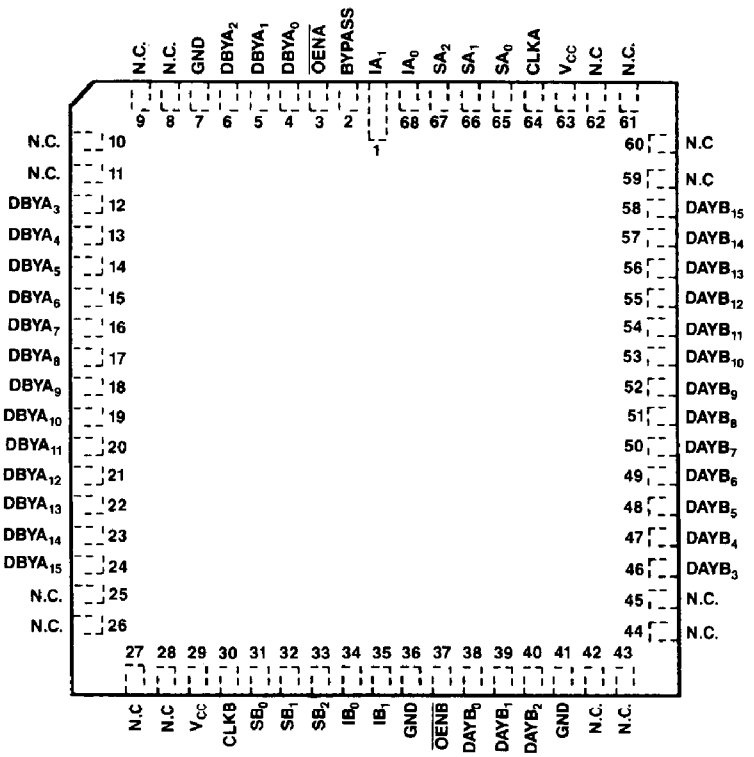
SIGNAL NAME	I/O	DESCRIPTION
IA_0, IA_1	I	Instruction Inputs for Register Bank A
IB_0, IB_1	I	Instruction Inputs for Register Bank B
SA_0-SA_2	I	Multiplex Select for Register Bank A
SB_0-SB_2	I	Multiplex Select for Register Bank B
$\overline{OENA}$	I	Output Enable for Output Port DBYA
$\overline{OENB}$	I	Output Enable for Output Port DAYB
CLKA	I	Clock Input for Register Bank A
CLKB	I	Clock Input for Register Bank B
DBYA 15:0	I/O	Register Bank B Input Port, Register Bank A Output Port
DAYB 15:0	I/O	Register Bank A Input Port, Register Bank B Output Port
BYPASS	I	BYPASS Control (Active Low). See Table on Output Control

PACKAGE ORIENTATION (WS59820)

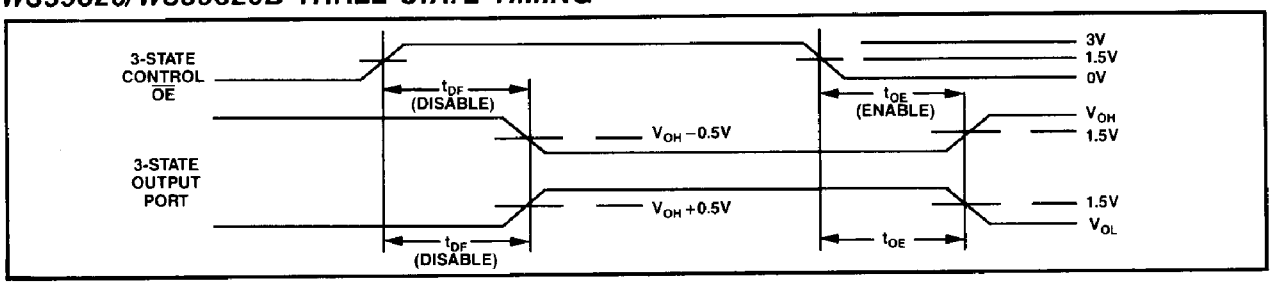
68 PIN CPGA
(Top Through Package View)



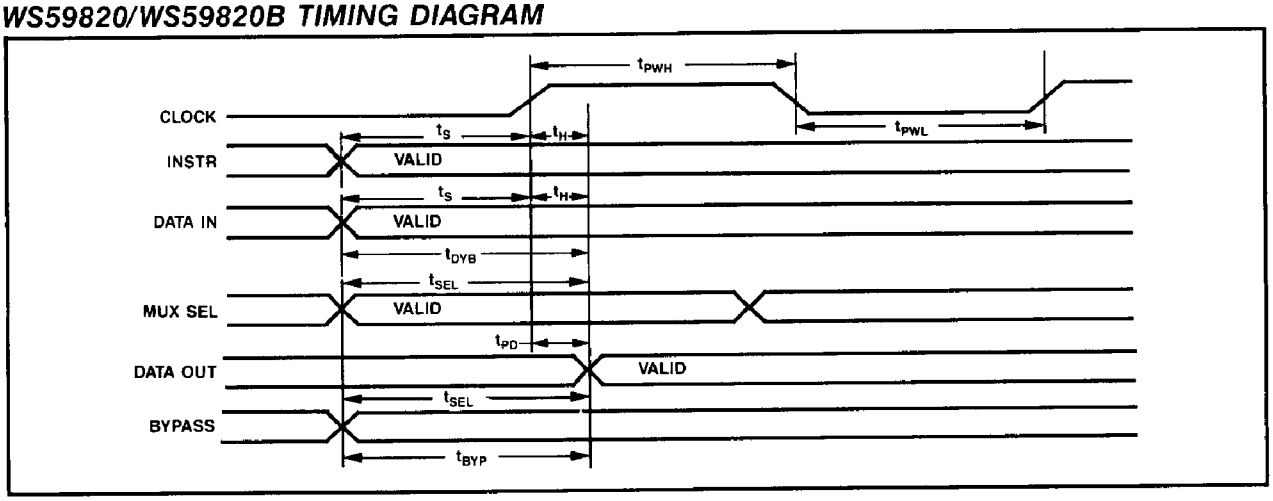
68 PIN PLDCC
(Top Through Package View)



WS59820/WS59820B THREE STATE TIMING



WS59820/WS59820B TIMING DIAGRAM



68 PIN CPGA PIN DESIGNATOR (WS59820)

PIN NAME	SIGNAL NAME	PIN NAME	SIGNAL NAME	PIN NAME	SIGNAL NAME	PIN NAME	SIGNAL NAME
A_6	IA_1	B_6	BYPASS	A_5	$\overline{OENA}$	B_5	$DBYA_0$
A_4	$DBYA_1$	B_4	$DBYA_2$	A_3	GND	B_3	Not Used
A_2	Not Used	B_1	Not Used	B_2	Not Used	C_1	$DBYA_3$
C_2	$DBYA_4$	D_1	$DBYA_5$	D_2	$DBYA_6$	E_1	$DBYA_7$
E_2	$DBYA_8$	F_1	$DBYA_9$	F_2	$DBYA_{10}$	G_1	$DBYA_{11}$
G_2	$DBYA_{12}$	H_1	$DBYA_{13}$	H_2	$DBYA_{14}$	J_1	$DBYA_{15}$
J_2	Not Used	K_1	Not Used	L_2	Not Used	K_2	Not Used
L_3	V_{CC}	K_3	CLKB	L_4	SB_0	K_4	SB_1
L_5	SB_2	K_5	IB_0	L_6	IB_1	K_6	GND
L_7	$\overline{OENB}$	K_7	$DAYB_0$	L_8	$DAYB_1$	K_8	$DAYB_2$
L_9	GND	K_9	Not Used	L_{10}	Not Used	K_{11}	Not Used
K_{10}	Not Used	J_{11}	$DAYB_3$	J_{10}	$DAYB_4$	H_{11}	$DAYB_5$
H_{10}	$DAYB_6$	G_{11}	$DAYB_7$	G_{10}	$DAYB_8$	F_{11}	$DAYB_9$
F_{10}	$DAYB_{10}$	E_{11}	$DAYB_{11}$	E_{10}	$DAYB_{12}$	D_{11}	$DAYB_{13}$
D_{10}	$DAYB_{14}$	C_{11}	$DAYB_{15}$	C_{10}	Not Used	B_{11}	Not Used
A_{10}	Not Used	B_{10}	Not Used	A_9	V_{CC}	B_9	CLKA
A_8	SA_0	B_8	SA_1	A_7	SA_2	B_7	IA_0

ABSOLUTE MAXIMUM RATINGS*

Operating Temp. (Comm'l) . . . . . 0°C to +70°C
(Mil) . . . . . −55°C to +125°C
Storage Temp. (No Bias) . . . . . −65°C to +150°C
Voltage on any pin with
respect to GND . . . . . −0.6V to +7V
Latch Up Protection . . . . . > 200 mA
ESD Protection . . . . . > ±2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC CHARACTERISTICS Over Operating Range (See Notes)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OH}	Output High Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −6.5 mA	2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 mA Comm'l I_{OL} = 16 mA Mil		0.5	V
V_{IH}	Input High Voltage	Guaranteed Input High Voltage		2.0		V
V_{IL}	Input Low Voltage	Guaranteed Input Low Voltage			0.8	V
I_{IX}	Input Load Current	V_{CC} = Max, V_{IN} = GND or V_{CC}		−10	10	µA
I_{OZ}	High Impedance Output Current	V_{CC} = Max, V_O = GND or V_{CC}		−50	50	µA
I_{CC}	Power Supply Current	V_{CC} = Max	0°C to +70°C (Comm'l)		12	mA
			−55°C to +125°C (Mil)		15	mA

NOTES: 1) Commercial: V_{CC} = +5V ± 5%, T_A = 0°C to 70°C.
2) Military: V_{CC} = +5V ± 10%, T_A = −55°C to +125°C.
3) C_L = 50 pF except for t_{DF} where C_L = 5 pF.

SWITCHING CHARACTERISTICS Over Operating Range (See Notes)

PARAMETER	DESCRIPTION	WS59820/WS59820B				UNITS
		COMMERCIAL		MILITARY		
		MIN	MAX	MIN	MAX	
t_{PD}	Clock to Data Out		20		22	ns
t_{SEL}	Mux Select to Data Out		20		22	
t_S	Input (Data/Instr.) Set Up	8		10		
t_H	Input (Data/Instr.) Hold	5		5		
t_{DF}	Output Disable	5	15		16	
t_{OE}	Output Enable	5	18		22	
t_{PWH}	Clock Pulse Width High	10		12		
t_{PWL}	Clock Pulse Width Low	11		12		
t_{BYP}	Bypass to Data Out		30		35	
t_{DYB}	Data Via BYPASS (Data In to Data Out When BYPASS is Active Low)		15		18	

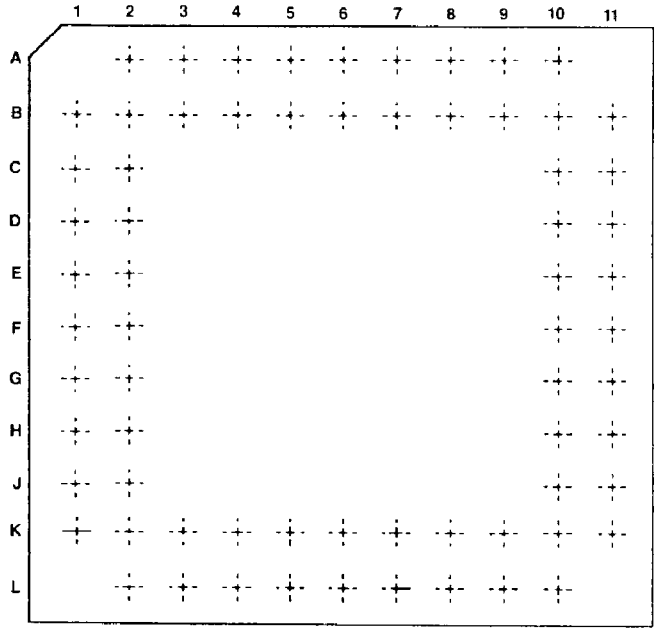
NOTE: Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

68 PIN CPGA PIN DESIGNATOR (WS59820B)

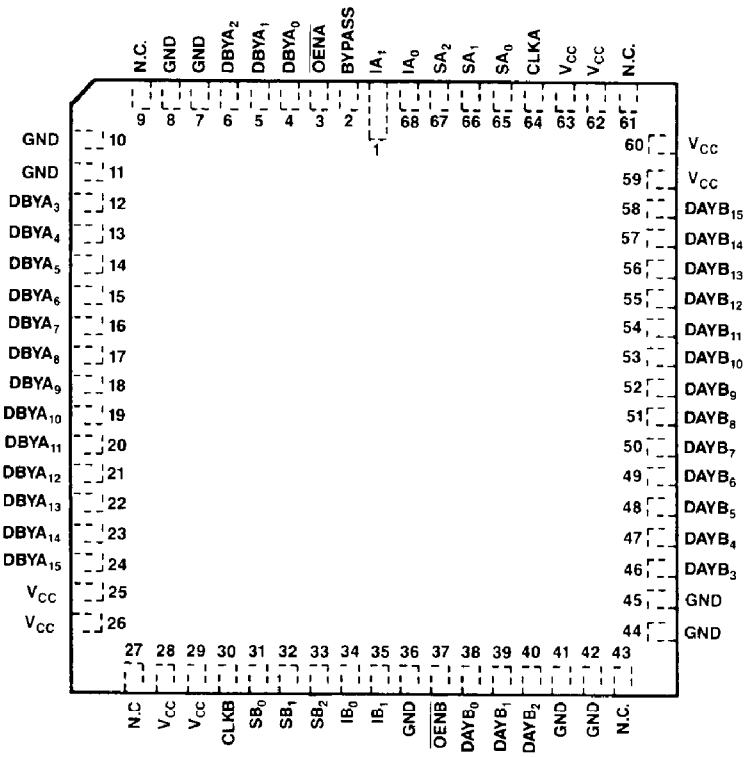
PIN NAME	SIGNAL NAME	PIN NAME	SIGNAL NAME	PIN NAME	SIGNAL NAME	PIN NAME	SIGNAL NAME
A_6	IA_1	B_6	BYPASS	A_5	$\overline{OENA}$	B_5	$DBYA_0$
A_4	$DBYA_1$	B_4	$DBYA_2$	A_3	GND	B_3	GND
A_2	Not Used	B_1	GND	B_2	GND	C_1	$DBYA_3$
C_2	$DBYA_4$	D_1	$DBYA_5$	D_2	$DBYA_6$	E_1	$DBYA_7$
E_2	$DBYA_8$	F_1	$DBYA_9$	F_2	$DBYA_{10}$	G_1	$DBYA_{11}$
G_2	$DBYA_{12}$	H_1	$DBYA_{13}$	H_2	$DBYA_{14}$	J_1	$DBYA_{15}$
J_2	V_{CC}	K_1	V_{CC}	L_2	Not Used	K_2	V_{CC}
L_3	V_{CC}	K_3	CLKB	L_4	SB_0	K_4	SB_1
L_5	SB_2	K_5	IB_0	L_6	IB_1	K_6	GND
L_7	$\overline{OENB}$	K_7	$DAYB_0$	L_8	$DAYB_1$	K_8	$DAYB_2$
L_9	GND	K_9	GND	L_{10}	Not Used	K_{11}	GND
K_{10}	GND	J_{11}	$DAYB_3$	J_{10}	$DAYB_4$	H_{11}	$DAYB_5$
H_{10}	$DAYB_6$	G_{11}	$DAYB_7$	G_{10}	$DAYB_8$	F_{11}	$DAYB_9$
F_{10}	$DAYB_{10}$	E_{11}	$DAYB_{11}$	E_{10}	$DAYB_{12}$	D_{11}	$DAYB_{13}$
D_{10}	$DAYB_{14}$	C_{11}	$DAYB_{15}$	C_{10}	V_{CC}	B_{11}	V_{CC}
A_{10}	Not Used	B_{10}	V_{CC}	A_9	V_{CC}	B_9	CLKA
A_8	SA_0	B_8	SA_1	A_7	SA_2	B_7	IA_0

PACKAGE ORIENTATION (WS59820B)

68 PIN CPGA
(Top Through Package View)



68 PIN PLDCC
(Top Through Package View)



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS59820G	23	68 Pin Ceramic PGA	G1	Comm'l	Standard
WS59820J	23	68 Pin PLDCC	J5	Comm'l	Standard
WS59820BG	23	68 Pin Ceramic PGA	G1	Comm'l	Standard
WS59820BJ	23	68 Pin PLDCC	J5	Comm'l	Standard