适用于 SiC/IGBT 和汽车应用的 UCC5390-Q1 单通道隔离式栅极驱动器

1 特性

- 5kV$_{RMS}$ 单通道隔离式栅极驱动器
- 符合面向汽车应用的 AEC-Q100 标准
  - 温度等级 1
  - HBM ESD 分类等级 H2
  - CDM ESD 分类等级 C6
- 以 GND2 为基准的 12V UVLO
- 8 引脚 DWV（8.5mm 爬电）封装
- 60ns（典型）传播延迟
- 较小的部件间传播延迟偏移
- 100V/ns 最小 CMTI
- 10A 最小峰值电流
- 3V 至 15V 输入电源电压
- 驱动器电源电压高达 33V
- 输入引脚具有负 5V 电压处理能力
- 安全相关认证：
  - 符合 DIN V VDE V 0884-11:2017-01 标准的 7000V$_{PK}$ 隔离 (DWV)（计划）
  - 5000V$_{RMS}$ (DWV) 隔离等级长达 1 分钟（符合 UL 1577 标准）
  - 符合 GB4943.1-2011 的 CQC 认证
- CMOS 输入
- 工作结温范围：–40°C 至 +150°C

2 应用

- 车载充电器
- 适用于电动汽车的牵引逆变器
- 直流充电站

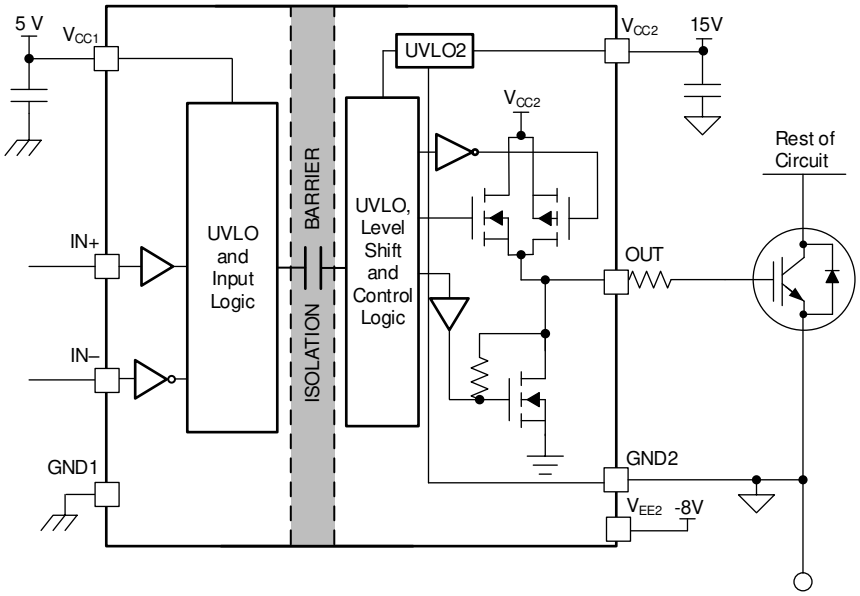
3 说明

UCC5390-Q1 是一款单通道隔离式栅极驱动器，具有 10A 峰值拉电流和 10A 峰值灌电流旨在驱动 MOSFET、IGBT 和 SiC MOSFET。UCC5390-Q1 的 UVLO2 以 GND2 为基准，从而有利于使用双极电源并优化 SiC 和 IGBT 开关行为和稳健性。

UCC5390-Q1 采用 8.5mm SOIC-8 (DWV) 封装，可支持高达 5kV$_{RMS}$ 的隔离电压。输入侧通过 SiO_2 电容隔离技术与输出侧相隔离，隔离层寿命超过 40 年。凭借高驱动强度和真正的 UVLO 检测，该器件非常适用于在车载充电器和牵引逆变器等 应用 中驱动 IGBT 和 SiC MOSFET。

与光耦合器相比，UCC5390-Q1 的部件间偏移更低，传播延迟更小，工作温度更高，并且 CMTI 更高。

4 功能方框图



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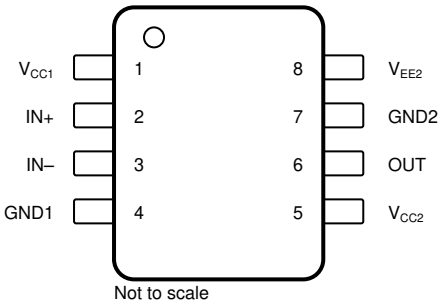
5 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (June 2019) to Revision A	Page
• 已更改 将销售状态从“预告信息”更改为“生产数据”	1

6 Pin Configuration and Function

UCC5390-Q1
8-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
GND1	4	G	Input ground. All signals on the input side are referenced to this ground.
GND2	7	G	Gate-drive common pin. Connect this pin to the IGBT emitter or MOSFET source. UVLO referenced to GND2.
IN+	2	I	Noninverting gate-drive voltage-control input. The IN+ pin has a CMOS input threshold. This pin is pulled low internally if left open. Use 表 4 to understand the input and output logic of these devices.
IN–	3	I	Inverting gate-drive voltage control input. The IN– pin has a CMOS input threshold. This pin is pulled high internally if left open. Use 表 4 to understand the input and output logic of these devices.
OUT	6	O	Gate-drive output.
V_{CC1}	1	P	Input supply voltage. Connect a locally decoupled capacitor to GND1. Use a low-ESR or ESL capacitor located as close to the device as possible.
V_{CC2}	5	P	Positive output supply rail. Connect a locally decoupled capacitor to V_{EE2}. Use a low-ESR or ESL capacitor located as close to the device as possible.
V_{EE2}	8	P	Negative output supply rail. Connect a locally decoupled capacitor to GND2. Use a low-ESR or ESL capacitor located as close to the device as possible.

(1) P = Power, G = Ground, I = Input, O = Output

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input bias pin supply voltage	V_{CC1} – GND1	GND1 – 0.3	18	V
Driver bias supply	V_{CC2} – V_{EE2}	–0.3	35	V
V_{EE2} bipolar supply voltage	V_{EE2} – GND2	–17.5	0.3	V
Output signal voltage	V_{OUT} – V_{EE2}	V_{EE2} – 0.3	V_{CC2} + 0.3	V
Input signal voltage	V_{IN+} – GND1, $V_{IN–}$ – GND1	GND1 – 5	V_{CC1} + 0.3	V
Junction temperature, T_J(2)		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) To maintain the recommended operating conditions for T_J, see the *Thermal Information*.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage, input side	3		15	V
V_{CC2}	Positive supply voltage output side (V_{CC2} – GND2)	13.2		33	V
V_{EE2}	Negative supply voltage output side (V_{EE2} – GND2)	–16		0	V
V_{SUP2}	Total supply voltage output side (V_{CC2} – V_{EE2})	13.2		33	V
T_J	Junction Temperature	-40		150	°C

7.4 Thermal Information

THERMAL METRIC[1]		UCC5390-Q1 DWV (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction–to-ambient thermal resistance	119.8	°C/W
$R_{\theta JC(top)}$	Junction–to-case (top) thermal resistance	64.1	°C/W
$R_{\theta JB}$	Junction–to-board thermal resistance	65.4	°C/W
Ψ_{JT}	Junction–to-top characterization parameter	37.6	°C/W
Ψ_{JB}	Junction–to-board characterization parameter	63.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DWV Package						
P_D	Maximum power dissipation on input and output	V_{CC1} = 15 V, V_{CC2} = 15 V, f = 1.9-MHz, 50% duty cycle, square wave, 2.2-nF load			1.04	W
P_{D1}	Maximum input power dissipation				0.05	W
P_{D2}	Maximum output power dissipation				0.99	W

7.6 Insulation Specifications for DWV Package

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			DWV	
CLR	External Clearance(1)	Shortest pin–to-pin distance through air	≥ 8.5	mm
CPG	External Creepage(1)	Shortest pin–to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 21	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303–11); IEC 60112	> 600	V
	Material Group	According to IEC 60664–1	I	
Overvoltage category per IEC 60664-1		Rated mains voltage ≤ 600 V_{RMS}	I-III	
		Rated mains voltage ≤ 1000 V_{RMS}	I-II	
DIN V VDE 0884–11: 2017–01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time dependent dielectric breakdown (TDDB) test	1500	V_{RMS}
		DC Voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification) ; $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	7000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 62368-1, 1.2/50-µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	8000	V_{PK}
q_{pd}	Apparent charge (4)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	1.2	pF
R_{IO}	Isolation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$> 10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

7.7 Safety-Related Certifications For DWV Package

VDE	UL	CQC
Plan to certify according to DIN V VDE V 0884–11:2017–01 and DIN EN 61010-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1–2011

Safety-Related Certifications For DWV Package (continued)

VDE	UL	CQC
Reinforced Insulation Maximum Transient Isolation Overvoltage, 7000 V_{PK}; Maximum Repetitive Peak Isolation Voltage, 2121 V_{PK}; Maximum Surge Isolation Voltage, 8000 V_{PK}	Single protection, 5000 V_{RMS}	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate
Certification planned	File Number: E181974	Certification Number: CQC19001226950

7.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DWV PACKAGE							
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 119.8°C/W, V_I = 15 V, T_J = 150°C, T_A = 25°C, see 图 1	Output side			66	mA
		$R_{\theta JA}$ = 119.8°C/W, V_I = 30 V, T_J = 150°C, T_A = 25°C, see 图 1	Output side			33	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 119.8°C/W, T_J = 150°C, T_A = 25°C, see 图 2	Input side			0.05	W
			Output side			0.99	
			Total			1.04	
T_S	Maximum safety temperature(1)					150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.

$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

7.9 Electrical Characteristics

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, C_L = 100-pF, T_J = –40°C to +125°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{VCC1}	Input supply quiescent current			1.67	2.4	mA
I_{VCC2}	Output supply quiescent current			1.1	1.8	mA
SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
$V_{IT+(UVLO1)}$	VCC1 Positive-going UVLO threshold voltage			2.6	2.8	V
$V_{IT-(UVLO1)}$	VCC1 Negative-going UVLO threshold voltage		2.4	2.5		V
$V_{hys(UVLO1)}$	VCC1 UVLO threshold hysteresis			0.1		V
OUTPUT SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
$V_{IT+(UVLO2)}$	VCC2 Positive-going UVLO threshold voltage			12	13	V
$V_{IT-(UVLO2)}$	VCC2 Negative-going UVLO threshold voltage		10.3	11		V
$V_{hys(UVLO2)}$	VCC2 UVLO threshold voltage hysteresis			1		V
LOGIC I/O						
$V_{IT+(IN)}$	Positive-going input threshold voltage (IN+, IN–)			0.55 × V_{CC1}	0.7 × V_{CC1}	V
$V_{IT-(IN)}$	Negative-going input threshold voltage (IN+, IN–)		0.3 × V_{CC1}	0.45 × V_{CC1}		V
$V_{hys(IN)}$	Input hysteresis voltage (IN+, IN–)			0.1 × V_{CC1}		V
I_{IH}	High-level input leakage at IN+	IN+ = V_{CC1}		40	240	µA
I_{IL}	Low-level input leakage at IN–	IN– = GND1	–240	–40		µA
		IN– = GND1 – 5 V	–310	–80		
GATE DRIVER STAGE						
V_{OH}	High-level output voltage (OUT)	I_{OUT} = –20 mA	V_{CC2} – 0.1	V_{CC2} – 0.24		V
V_{OL}	Low level output voltage (OUT)	IN+ = low, IN– = high; I_O = 20 mA	2	3		mV
I_{OH}	Peak source current	IN+ = high, IN– = low	10	17		A
I_{OL}	Peak sink current	IN+ = low, IN– = high	10	17		A
SHORT CIRCUIT CLAMPING						
$V_{CLP-OUT}$	Clamping voltage (V_{OUT} –V_{CC2})	IN+ = high, IN– = low, t_{CLAMP} = 10 µs, I_{OUT}= 500 mA		1	1.3	V
$V_{CLP-OUT}$	Clamping voltage (V_{EE2} – V_{OUT})	IN+ = low, IN– = high, t_{CLAMP} = 10 µs, I_{OUT} = –500 mA		1.5		V
		IN+ = low, IN– = high, I_{OUT} = –20 mA		0.9	1	
ACTIVE PULLDOWN						
V_{OUTSD}	Active pulldown voltage on OUT	I_{OUT} = 0.1 × $I_{OUT(typ)}$, V_{CC2} = open		1.8	2.5	V

7.10 Switching Characteristics

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, T_J = –40°C to +125°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output-signal rise time	C_{LOAD} = 1 nF		10	26	ns
t_f	Output-signal fall time	C_{LOAD} = 1 nF		10	22	ns
t_{PLH}	Propagation delay, high	C_{LOAD} = 100 pF		65	100	ns
t_{PHL}	Propagation delay, low	C_{LOAD} = 100 pF		65	100	ns
t_{UVLO1_rec}	UVLO recovery delay of V_{CC1}			30		µs
t_{UVLO2_rec}	UVLO recovery delay of V_{CC2}			50		µs
t_{PWD}	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$	C_{LOAD} = 100 pF		1	20	ns
$t_{sk(pp)}$	Part-to-part skew(1)	C_{LOAD} = 100 pF		1	25	ns
CMTI	Common-mode transient immunity	PWM is tied to GND or V_{CC1}, V_{CM} = 1200 V	100	120		kV/µs

(1) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between the output of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads guaranteed by characterization.

7.11 Insulation Characteristics Curves

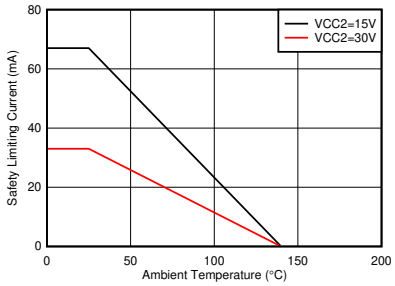


图 1. Thermal Derating Curve for Limiting Current per VDE for DWV Package

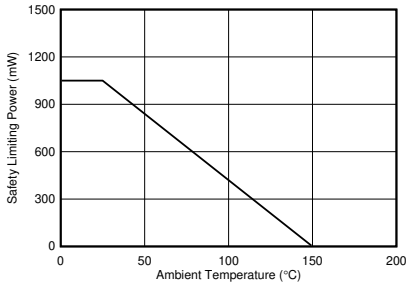
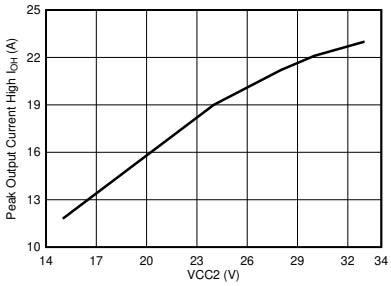


图 2. Thermal Derating Curve for Limiting Power per VDE for DWV Package

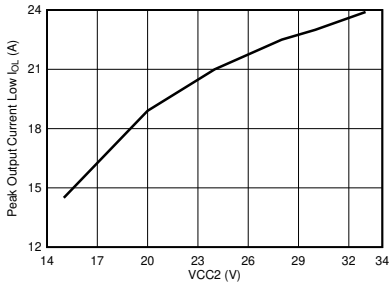
7.12 Typical Characteristics

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} = 1 nF, T_J = –40°C to +125°C, (unless otherwise noted)



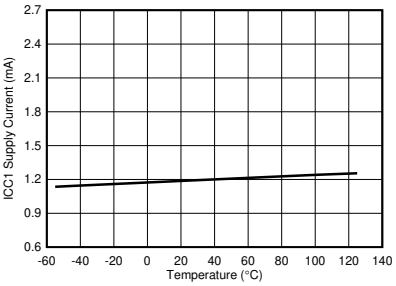
C_{LOAD} = 150 nF

图 3. Output-High Drive Current vs Output Voltage



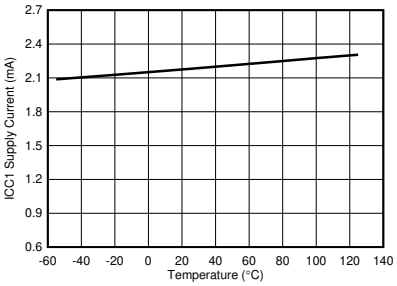
C_{LOAD} = 150 nF

图 4. Output-Low Drive Current vs Output Voltage



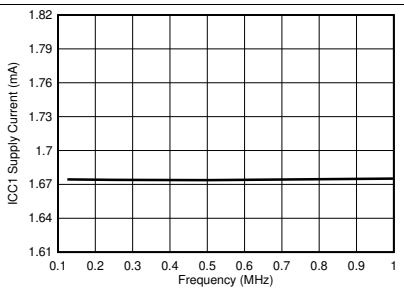
IN+ = L IN– = H

图 5. I_{CC1} Supply Current vs Temperature



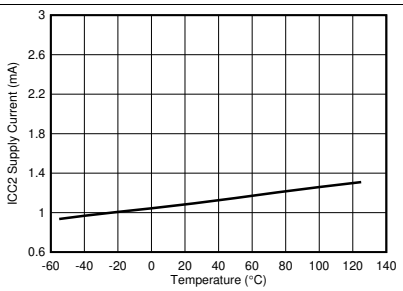
IN+ = H IN– = L

图 6. I_{CC1} Supply Current vs Temperature



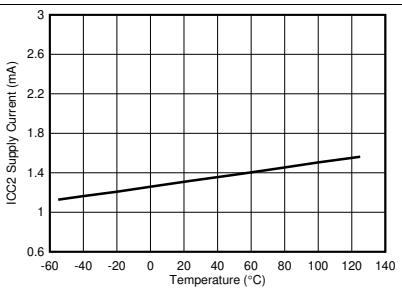
Duty Cycle = 50% T = 25°C

图 7. I_{CC1} Supply Current vs Input Frequency



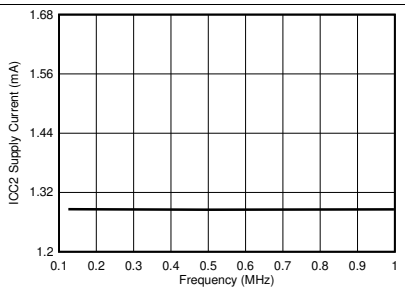
IN+ = L IN– = H

图 8. I_{CC2} Supply Current vs Temperature



IN+ = H IN– = L

图 9. I_{CC2} Supply Current vs Temperature

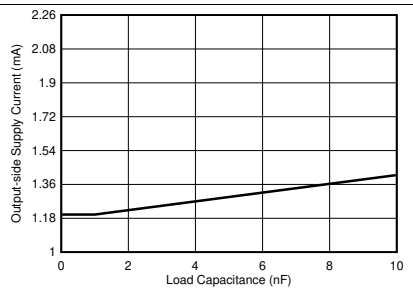


Duty Cycle = 50% T = 25°C

图 10. I_{CC2} Supply Current vs Input Frequency

Typical Characteristics (接下页)

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} = 1 nF, T_J = –40°C to +125°C, (unless otherwise noted)



f_{SW} = 1 kHz

图 11. I_{CC2} Supply Current vs Load Capacitance

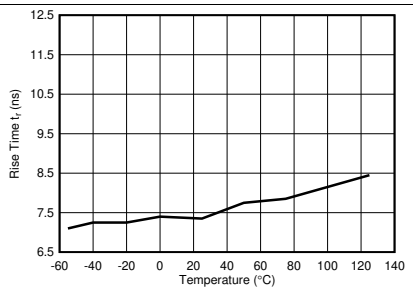


图 12. Rise Time vs Temperature

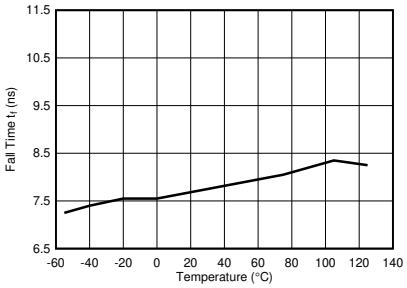


图 13. Fall Time vs Temperature

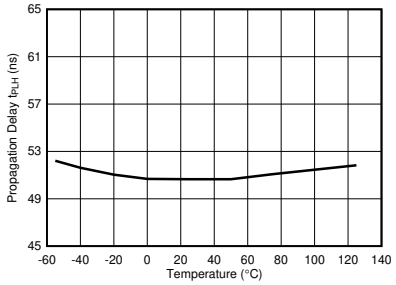


图 14. Propagation Delay t_{PLH} vs Temperature

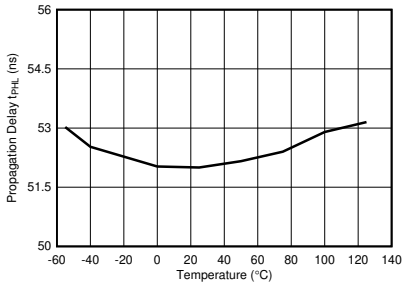
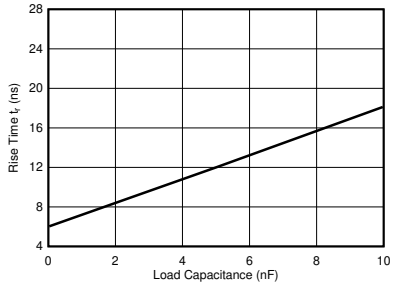
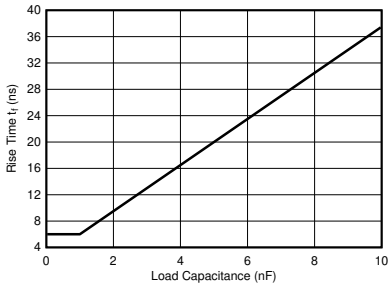


图 15. Propagation Delay t_{PHL} vs Temperature



f_{SW} = 1 kHz R_{GH} = 0 Ω R_{GL} = 0 Ω

图 16. Rise Time vs Load Capacitance



f_{SW} = 1 kHz R_{GH} = 0 Ω R_{GL} = 0 Ω

图 17. Fall Time vs Load Capacitance

8 Parameter Measurement Information

8.1 Propagation Delay, Inverting, and Noninverting Configuration

图 18 shows the propagation delay for noninverting configurations. 图 19 shows the propagation delay with the inverting configuration. These figures also demonstrate the method used to measure the rise (t_r) and fall (t_f) times.

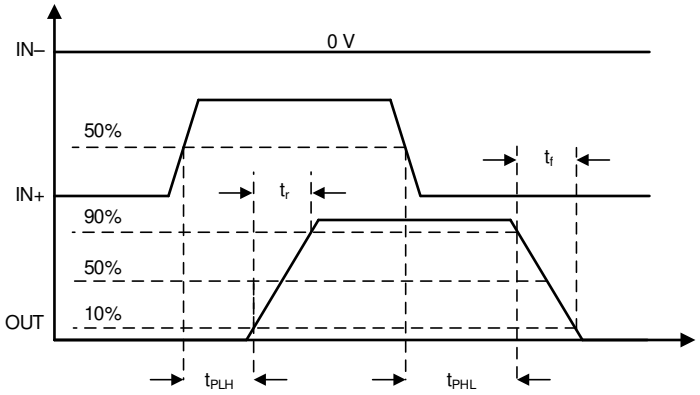


图 18. Propagation Delay, Noninverting Configuration

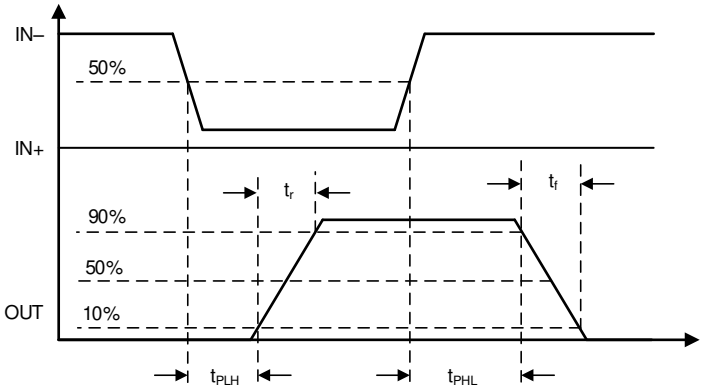


图 19. Propagation Delay, Inverting Configuration

Propagation Delay, Inverting, and Noninverting Configuration (接下页)

8.1.1 CMTI Testing

图 20 is a simplified diagram of the CMTI testing configuration.

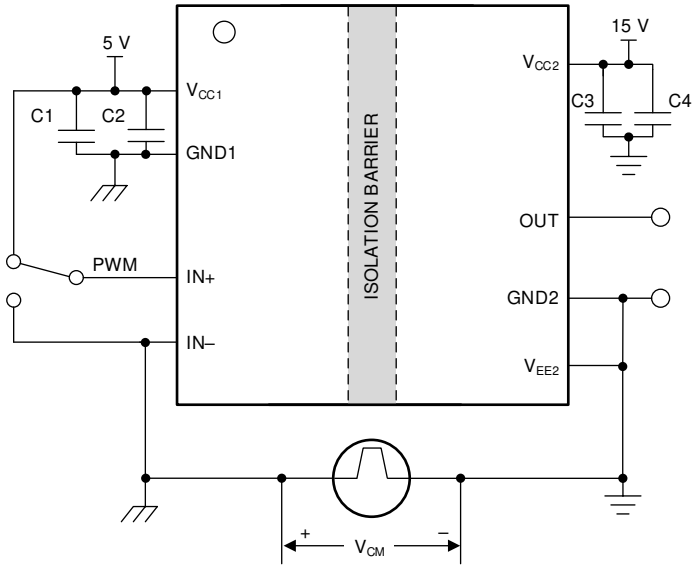


图 20. CMTI Test Circuit for UCC5390-Q1

9 Detailed Description

9.1 Overview

The isolation inside the UCC5390-Q1 is implemented with high-voltage SiO_2-based capacitors. The signal across the isolation has an on-off keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier (see 图 22). The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The UCC5390-Q1 also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, 图 21, shows a functional block diagram of a typical channel. 图 22 shows a conceptual detail of how the OOK scheme works.

图 21 shows how the input signal passes through the capacitive isolation barrier through modulation (OOK) and signal conditioning.

9.2 Functional Block Diagram

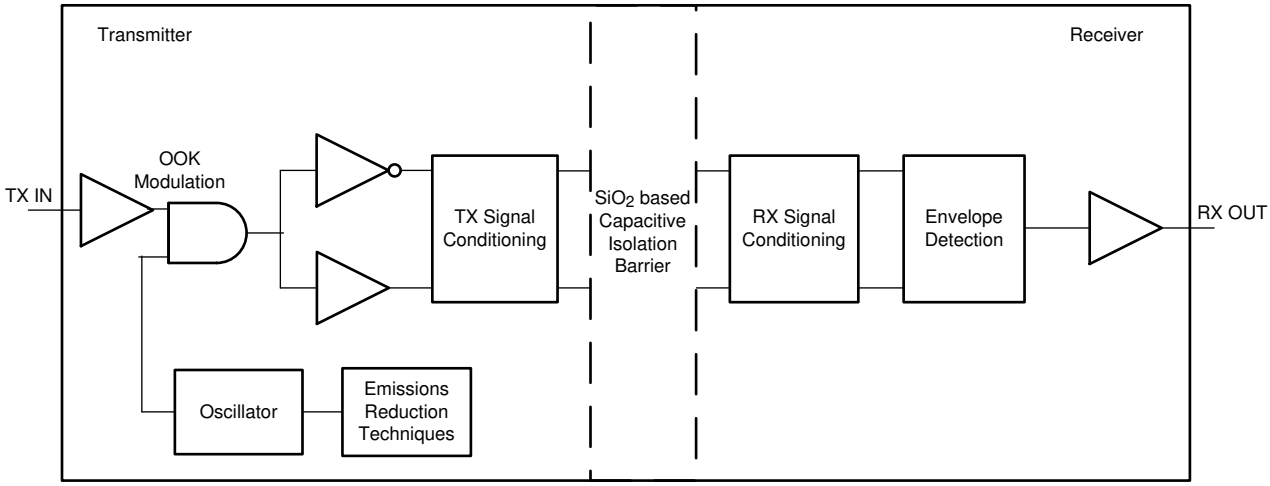


图 21. Conceptual Block Diagram of a Capacitive Data Channel

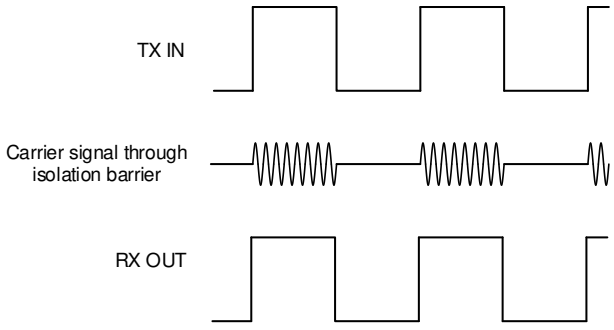


图 22. On-Off Keying (OOK) Based Modulation Scheme

Functional Block Diagram (接下页)

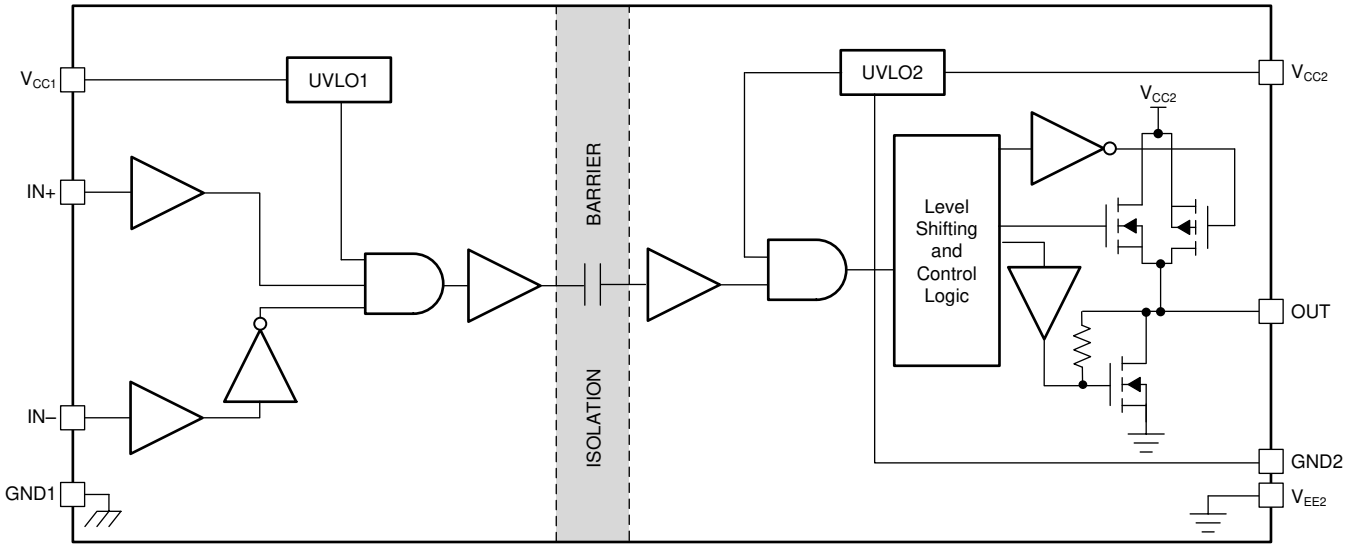


图 23. Functional Block Diagram — UVLO With Respect to GND2 (UCC5390-Q1)

9.3 Feature Description

9.3.1 Power Supply

The V_{CC1} input power supply supports a wide voltage range from 3 V to 15 V and the V_{CC2} output supply supports a voltage range from 9.5 V to 33 V. For operation with bipolar supplies, the power device is turned off with a negative voltage on the gate with respect to the emitter or source. This configuration prevents the power device from unintentionally turning on because of current induced from the Miller effect. The typical values of the V_{CC2} and V_{EE2} output supplies for bipolar operation are 15 V and –8 V with respect to GND2 for IGBTs and 20 V and –5 V for SiC MOSFETs.

For operation with unipolar supply, the V_{CC2} supply is connected to 15 V with respect to VEE2 for IGBTs, and 20 V for SiC MOSFETs. The V_{EE2} supply is connected to 0 V.

9.3.2 Input Stage

The input pins (IN+ and IN–) of the UCC5390-Q1 are based on CMOS-compatible input-threshold logic that is completely isolated from the V_{CC2} supply voltage. The input pins are easy to drive with logic-level control signals (such as those from 3.3-V microcontrollers), because the UCC5390-Q1 has a typical high threshold ($V_{IT+(IN)}$) of 0.55 × V_{CC1} and a typical low threshold of 0.45 × V_{CC1}. A wide hysteresis ($V_{hys(IN)}$) of 0.1 × V_{CC1} makes for good noise immunity and stable operation. If any of the inputs are left open, 128 kΩ of internal pulldown resistance forces the IN+ pin low and 128 kΩ of internal resistance pulls IN– high. However, TI still recommends grounding an input or tying to VCC1 if it is not being used for improved noise immunity.

Because the input side of the UCC5390-Q1 is isolated from the output driver, the input signal amplitude can be larger or smaller than V_{CC2} provided that it does not exceed the recommended limit. This feature allows greater flexibility when integrating the gate-driver with control signal sources and allows the user to choose the most efficient V_{CC2} for any gate. However, the amplitude of any signal applied to IN+ or IN– must never be at a voltage higher than V_{CC1}.

Feature Description (接下页)

9.3.3 Output Stage

The output stage of the UCC5390-Q1 features a pullup structure that delivers the highest peak-source current when it is most needed which is during the Miller plateau region of the power-switch turnon transition (when the power-switch drain or collector voltage experiences dV/dt). The output stage pullup structure features a P-channel MOSFET and an additional pullup N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a brief boost in the peak-sourcing current, which enables fast turn-on. Fast turn-on is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high. 表 1 lists the typical internal resistance values of the pullup and pulldown structure.

表 1. UCC5390-Q1 On-Resistance

DEVICE OPTION	R_{NMOS}	R_{OH}	R_{OL}	UNIT
UCC5390-Q1	0.76	12	0.13	Ω

The R_{OH} parameter is a DC measurement and is representative of the on-resistance of the P-channel device only. This parameter is only for the P-channel device, because the pullup N-channel device is held in the OFF state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore, the effective resistance of the UCC5390-Q1 pullup stage during this brief turnon phase is much lower than what is represented by the R_{OH} parameter, which yields a faster turnon. The turnon-phase output resistance is the parallel combination R_{OH} || R_{NMOS}.

The pulldown structure in the UCC5390-Q1 is simply composed of an N-channel MOSFET. The output of the UCC5390-Q1 is capable of delivering, or sinking, 10-A peak current pulses. The output voltage swing between V_{CC2} and V_{EE2} provides rail-to-rail operation because of the MOS-out stage which delivers very low dropout.

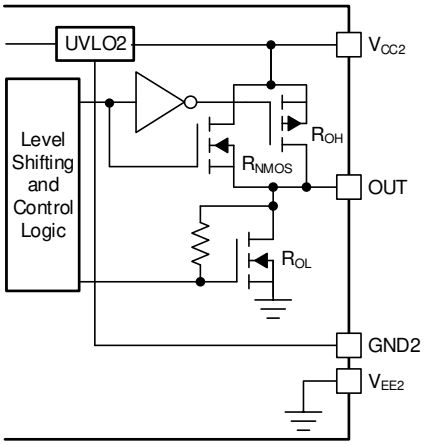


图 24. Output Stage

9.3.4 Protection Features

9.3.4.1 Undervoltage Lockout (UVLO)

UVLO functions are implemented for both the V_{CC1} and V_{CC2} supplies between the V_{CC1} and GND1, and V_{CC2} and V_{EE2} pins to prevent an underdriven condition on IGBTs and MOSFETs. When V_{CC} is lower than $V_{IT+\ (UVLO)}$ at device start-up or lower than $V_{IT-(UVLO)}$ after start-up, the voltage-supply UVLO feature holds the effected output low, regardless of the input pins (IN+ and IN–) as shown in 表 2. The V_{CC} UVLO protection has a hysteresis feature ($V_{hys(UVLO)}$). This hysteresis prevents chatter when the power supply produces ground noise; this allows the device to permit small drops in bias voltage, which occurs when the device starts switching and operating current consumption increases suddenly. 图 25 shows the UVLO functions.

表 2. UCC5390-Q1 V_{CC1} UVLO Logic

CONDITION	INPUTS		OUTPUT
	IN+	IN–	OUT
V_{CC1} – GND1 < $V_{IT+(UVLO1)}$ during device start-up	H	L	L
	L	H	L
	H	H	L
	L	L	L
V_{CC1} – GND1 < $V_{IT–(UVLO1)}$ after device start-up	H	L	L
	L	H	L
	H	H	L
	L	L	L

表 3. UCC5390-Q1 V_{CC2} UVLO Logic

CONDITION	INPUTS		OUTPUT
	IN+	IN–	OUT
V_{CC2} – V_{EE2} < $V_{IT+(UVLO2)}$ during device start-up	H	L	L
	L	H	L
	H	H	L
	L	L	L
V_{CC2} – V_{EE2} < $V_{IT–(UVLO2)}$ after device start-up	H	L	L
	L	H	L
	H	H	L
	L	L	L

When V_{CC1} or V_{CC2} drops below the UVLO1 or UVLO2 threshold, a delay, t_{UVLO1_rec} or t_{UVLO2_rec}, occurs on the output when the supply voltage rises above $V_{IT+(UVLO)}$ or $V_{IT+(UVLO2)}$ again. 图 25 shows this delay.

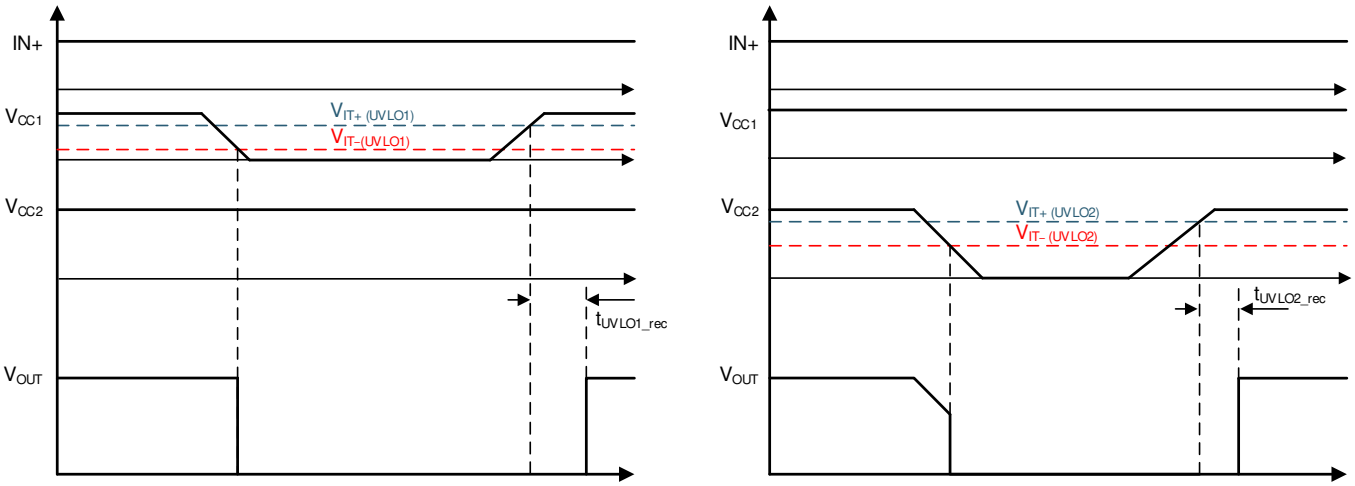


图 25. UVLO Functions

9.3.4.2 Active Pulldown

The active pulldown function is used to pull the IGBT or MOSFET gate to the low state when no power is connected to the V_{CC2} supply. This feature prevents false IGBT and MOSFET turnon on the OUT pin by clamping the output to approximately 2 V.

When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs. In this condition, the upper PMOS is resistively held off by a pullup resistor while the lower NMOS gate is tied to the driver output through a 500-kΩ resistor. In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device, which is approximately 1.5 V when no bias power is available.

9.3.4.3 Short-Circuit Clamping

The short-circuit clamping function is used to clamp voltages at the driver output slightly higher than the V_{CC2} voltage during short-circuit conditions. The short-circuit clamping function helps protect the IGBT or MOSFET gate from overvoltage breakdown or degradation. The short-circuit clamping function is implemented by adding a diode connection between the dedicated pins and the V_{CC2} pin inside the driver. The internal diodes can conduct up to 500-mA current for a duration of 10 µs and a continuous current of 20 mA. Use external Schottky diodes to improve current conduction capability as needed.

9.4 Device Functional Modes

lists the functional modes for the UCC5390-Q1 assuming V_{CC1} and V_{CC2} are in the recommended range.

表 4. Function Table

IN+	IN–	OUT
Low	X	Low
X	High	Low
High	Low	High

9.4.1 ESD Structure

图 26 shows the multiple diodes involved in the ESD protection components of the UCC5390-Q1. This provides pictorial representation of the absolute maximum rating for the device.

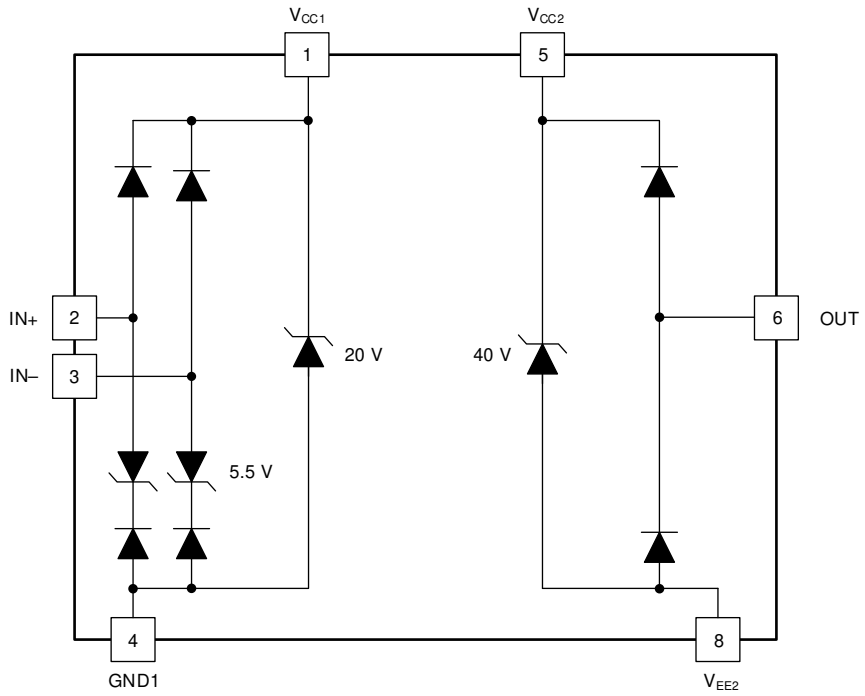


图 26. ESD Structure

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The UCC5390-Q1 is a simple, isolated gate driver for power semiconductor devices, such as MOSFETs, IGBTs, or SiC MOSFETs. The family of devices is intended for use in applications such as motor control, solar inverters, switched-mode power supplies, and industrial inverters.

10.2 Typical Application

The circuit in 图 27 show a typical application for driving IGBTs.

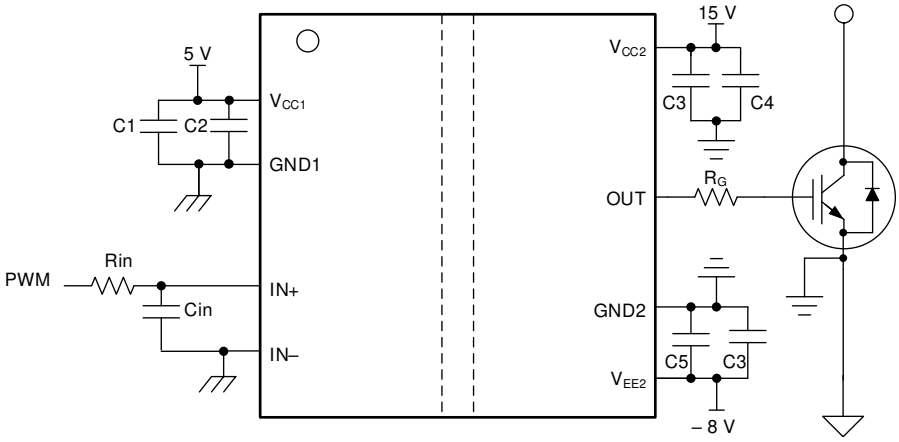


图 27. Typical Application Circuit for UCC5390-Q1 to Drive IGBT

10.2.1 Design Requirements

表 5 lists the recommended conditions to observe the input and output of the UCC5390-Q1 gate driver with the IN– pin tied to the GND1 pin.

表 5. UCC5390-Q1 Design Requirements

PARAMETER	VALUE	UNIT
V_{CC1}	3.3	V
V_{CC2}	18	V
V_{EE2}	-3	V
IN+	3.3	V
IN–	GND1	-
Switching frequency	300	kHz
Gate Charge of Power Device	126	nC

10.2.2 Detailed Design Procedure

10.2.2.1 Designing IN+ and IN– Input Filter

TI recommends that users avoid shaping the signals to the gate driver in an attempt to slow down (or delay) the signal at the output. However, a small input filter, R_{IN}-C_{IN}, can be used to filter out the ringing introduced by nonideal layout or long PCB traces.

Such a filter should use an R_{IN} resistor with a value from 0 Ω to 100 Ω and a C_{IN} capacitor with a value from 10 pF to 1000 pF. In the example, the selected value for R_{IN} is 51 Ω and C_{IN} is 33 pF, with a corner frequency of approximately 100 MHz.

When selecting these components, pay attention to the trade-off between good noise immunity and propagation delay.

10.2.2.2 Gate-Driver Output Resistor

The external gate-driver resistors, $R_{G(ON)}$ and $R_{G(OFF)}$ are used to:

1. Limit ringing caused by parasitic inductances and capacitances
2. Limit ringing caused by high voltage or high current switching dv/dt, di/dt, and body-diode reverse recovery
3. Fine-tune gate drive strength, specifically peak sink and source current to optimize the switching loss
4. Reduce electromagnetic interference (EMI)

The output stage has a pullup structure consisting of a P-channel MOSFET and an N-channel MOSFET in parallel. The combined peak source current is 17 A for UCC5390-Q1 . Use 公式 1 to estimate the peak source current.

$$I_{OH} = \min\left(17\,A, \frac{V_{CC2} - V_{EE2}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}}\right)$$

where

- R_{ON} is the external turnon resistance, which is 2.2 Ω in this example.
- R_{GFET_Int} is the power transistor internal gate resistance, found in the power transistor data sheet. We will assume 1.8Ω for our example.
- I_{OH} is the peak source current which is the minimum value between 17 A, the gate-driver peak source current, and the calculated value based on the gate-drive loop resistance. (1)

In this example, the peak source current is approximately 4.45 A as calculated in 公式 2.

$$I_{OH} = \frac{V_{CC2} - V_{EE2}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}} = \frac{21\,V}{0.76\,\Omega \,||\, 12\,\Omega + 2.2\,\Omega + 1.8\,\Omega} \approx 4.45\,A \quad (2)$$

Similarly, use 公式 3 to calculate the peak sink current.

$$I_{OL} = \min\left(17\,A, \frac{V_{CC2} - V_{EE2}}{R_{OL} + R_{OFF} + R_{GFET\_Int}}\right)$$

where

- R_{OFF} is the external turnoff resistance, which is 2.2 Ω in this example.
- I_{OL} is the peak sink current which is the minimum value between 17 A, the gate-driver peak sink current, and the calculated value based on the gate-drive loop resistance. (3)

In this example, the peak sink current is the minimum of 公式 4 and 17 A.

$$I_{OL} = \frac{V_{CC2} - V_{EE2}}{R_{OL} + R_{OFF} + R_{GFET\_Int}} = \frac{21\,V}{0.13\,\Omega + 2.2\,\Omega + 1.8\,\Omega} \approx 5.08\,A \quad (4)$$

注

The estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate-driver loop can slow down the peak gate-drive current and introduce overshoot and undershoot. Therefore, TI strongly recommends that the gate-driver loop should be minimized. Conversely, the peak source and sink current is dominated by loop parasitics when the load capacitance (C_{ISS}) of the power transistor is very small (typically less than 1 nF) because the rising and falling time is too small and close to the parasitic ringing period.

10.2.2.3 Estimate Gate-Driver Power Loss

The total loss, P_G, in the gate-driver subsystem includes the power losses (P_{GD}) of the UCC5390-Q1 device and the power losses in the peripheral circuitry, such as the external gate-drive resistor.

The P_{GD} value is the key power loss which determines the thermal safety-related limits of the UCC5390-Q1 device, and it can be estimated by calculating losses from several components.

The first component is the static power loss, P_{GDQ}, which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. The P_{GDQ} parameter is measured on the bench with no load connected to the OUT pins at a given V_{CC1}, V_{CC2}, switching frequency, and ambient temperature. In this example, V_{CC1} is 3.3V, V_{CC2} is 18 V and V_{EE2} is -3 V. The current on each power supply, with PWM switching from 0 V to 3.3 V at 300 kHz, is measured to be I_{CC1} = 1.67 mA and I_{CC2} = 1.28 mA. Therefore, use 公式 5 to calculate P_{GDQ}.

$$P_{GDQ} = V_{CC1} \times I_{VCC1} + (V_{CC2} - V_{EE2}) \times I_{CC2} \approx 32.4\text{mW} \tag{5}$$

The second component is the switching operation loss, P_{GDO}, with a given load capacitance which the driver charges and discharges the load during each switching cycle. Use 公式 6 to calculate the total dynamic loss from load switching, P_{GSW}.

$$P_{GSW} = (V_{CC2} - V_{EE2}) \times Q_G \times f_{SW}$$

where

- Q_G is the gate charge of the power transistor at V_{CC2}. (6)

So, for this example application the total dynamic loss from load switching is approximately 793.8 mW as calculated in 公式 7.

$$P_{GSW} = 21\text{ V} \times 126\text{ nC} \times 300\text{ kHz} = 793.8\text{ mW} \tag{7}$$

Q_G represents the total gate charge of the power transistor, and is subject to change with different testing conditions. The UCC5390-Q1 gate-driver loss on the output stage, P_{GDO}, is part of P_{GSW}. P_{GDO} is equal to P_{GSW} if the external gate-driver resistance and power-transistor internal resistance are 0 Ω, and all the gate driver-loss will be dissipated inside the UCC5390-Q1. If an external turn-on and turn-off resistance exists, the total loss is distributed between the gate driver pull-up/down resistance, external gate resistance, and power-transistor internal resistance. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 17 A, however, it will be non-linear if the source/sink current is saturated. Therefore, P_{GDO} is different in these two scenarios.

Case 1 - Linear Pull-Up/Down Resistor:

$$P_{GDO} = \frac{P_{GSW}}{2}\left(\frac{R_{OH} \,||\, R_{NMOS}}{R_{OH} \,||\, R_{NMOS} + R_{ON} + R_{GFET\_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} + R_{GFET\_Int}}\right) \tag{8}$$

In this design example, all the predicted source and sink currents are less than 17 A, therefore, use 公式 9 to estimate the UCC5390-Q1 gate-driver loss.

$$P_{GDO} = \frac{793.8\text{ mW}}{2}\left(\frac{12\ \Omega \,||\, 0.76\ \Omega}{12\ \Omega \,||\, 0.76\ \Omega + 2.2\ \Omega + 1.8\ \Omega} + \frac{0.13\ \Omega}{0.13\ \Omega + 2.2\ \Omega + 1.8\ \Omega}\right) \approx 72.66\text{ mW} \tag{9}$$

Case 2 - Nonlinear Pull-Up/Down Resistor:

$$P_{GDO} = f_{SW} \times \left[17\text{ A} \times \int_0^{T_{R\_Sys}} (V_{CC2} - V_{OUTH}(t))dt + 17\text{ A} \times \int_0^{T_{F\_Sys}} (V_{OUTL}(t) - V_{EE2})dt\right]$$

where

- $V_{OUTH/L(t)}$ is the gate-driver OUT pin voltage during the turnon and turnoff period. In cases where the output is saturated for some time, this value can be simplified as a constant-current source (17 A at turnon and turnoff) charging or discharging a load capacitor. Then, the $V_{OUTH/L(t)}$ waveform will be linear and the T_{R_Sys} and T_{F_Sys} can be easily predicted. (10)

For some scenarios, if only one of the pullup or pulldown circuits is saturated and another one is not, the P_{GDO} is a combination of case 1 and case 2, and the equations can be easily identified for the pullup and pulldown based on this discussion.

Use 公式 11 to calculate the total gate-driver loss dissipated in the UCC5390-Q1 gate driver, P_{GD}.

$$P_{GD} = P_{GDQ} + P_{GDO} = 32.4\text{mW} + 72.66\text{mW} = 105.06\text{mW} \quad (11)$$

10.2.2.4 Estimating Junction Temperature

Use 公式 12 to estimate the junction temperature (T_J) of the UCC5390-Q1 family.

$$T_J = T_C + \Psi_{JT} \times P_{GD}$$

where

- T_C is the UCC5390-Q1 case-top temperature measured with a thermocouple or some other instrument.
- Ψ_{JT} is the junction-to-top characterization parameter from the table. (12)

Using the junction-to-top characterization parameter (Ψ_{JT}) instead of the junction-to-case thermal resistance ($R_{\theta JC}$) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted). The $R_{\theta JC}$ resistance can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or when a heat sink is applied to an IC package. In all other cases, use of $R_{\theta JC}$ will inaccurately estimate the true junction temperature. The Ψ_{JT} parameter is experimentally derived by assuming that the dominant energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimations can be made accurately to within a few degrees Celsius.

10.2.3 Selecting V_{CC1} and V_{CC2} Capacitors

Bypass capacitors for the V_{CC1} and V_{CC2} supplies are essential for achieving reliable performance. TI recommends choosing low-ESR and low-ESL, surface-mount, multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients, and capacitance tolerances.

注

DC bias on some MLCCs will impact the actual capacitance value. For example, a 25-V, 1-μF X7R capacitor is measured to be only 500 nF when a DC bias of 15-V_{DC} is applied.

10.2.3.1 Selecting a V_{CC1} Capacitor

A bypass capacitor connected to the V_{CC1} pin supports the transient current required for the primary logic and the total current consumption, which is only a few milliamperes. Therefore, a 50-V MLCC with over 100 nF is recommended for this application. If the bias power-supply output is located a relatively long distance from the V_{CC1} pin, a tantalum or electrolytic capacitor with a value greater than 1 μF should be placed in parallel with the MLCC.

10.2.3.2 Selecting a V_{CC2} Capacitor

A 50-V, 10-μF MLCC and a 50-V, 0.22-μF MLCC are selected for the C_{VCC2} capacitor. If the bias power supply output is located a relatively long distance from the V_{CC2} pin, a tantalum or electrolytic capacitor with a value greater than 10 μF should be used in parallel with C_{VCC2}.

10.2.3.3 Application Circuits With Output Stage Negative Bias

When parasitic inductances are introduced by nonideal PCB layout and long package leads (such as TO-220 and TO-247 type packages), ringing in the gate-source drive voltage of the power transistor could occur during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, unintended turnon and shoot-through could occur. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. A few examples of implementing negative gate-drive bias follow.

图 28 shows another example which uses two supplies (or single-input, double-output power supply). The power supply across V_{CC2} and GND2 determines the positive drive output voltage and the power supply across V_{EE2} and GND2 determines the negative turnoff voltage. This solution requires more power supplies than the first example, however, it provides more flexibility when setting the positive and negative rail voltages.

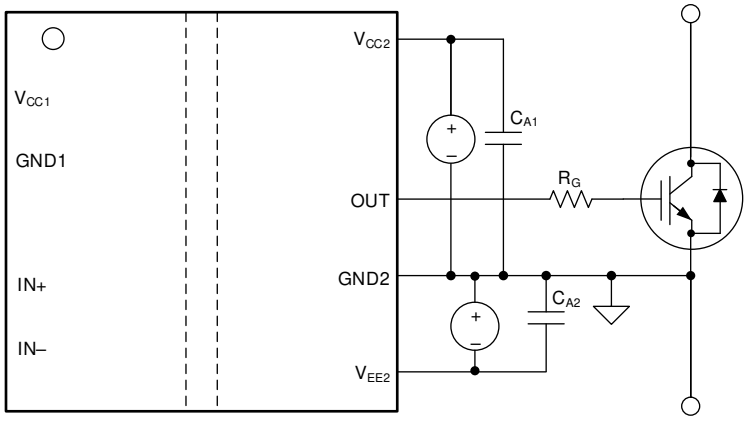
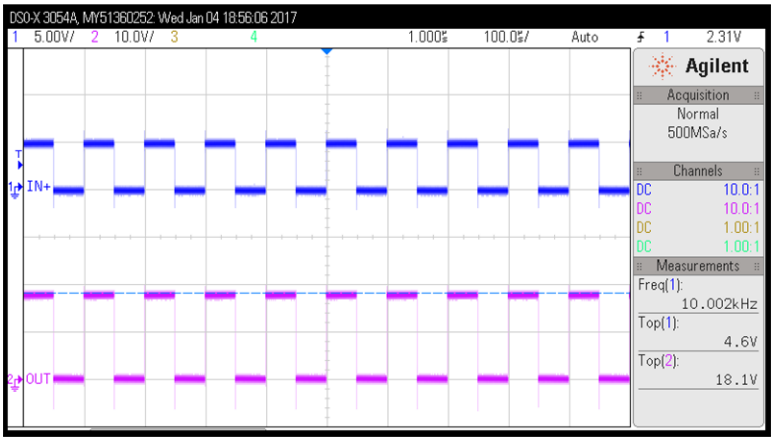


图 28. Negative Bias With Two Iso-Bias Power Supplies

10.2.4 Application Curve



V_{CC2} = 20 V V_{EE2} = GND f_{SW} = 10 kHz

图 29. PWM Input And Gate Voltage Waveform

11 Power Supply Recommendations

The recommended input supply voltage (V_{CC1}) for the UCC5390-Q1 device is from 3 V to 15 V. The lower limit of the range of output bias-supply voltage (V_{CC2}) is determined by the internal UVLO protection feature of the device. The V_{CC1} and V_{CC2} voltages should not fall below their respective UVLO thresholds for normal operation, or else the gate-driver outputs can become clamped low for more than 50 µs by the UVLO protection feature. For more information on UVLO, see the *Undervoltage Lockout (UVLO)* section. The higher limit of the V_{CC2} range depends on the maximum gate voltage of the power device that is driven by the UCC5390-Q1 device, and should not exceed the recommended maximum V_{CC2} of 33 V. A local bypass capacitor should be placed between the V_{CC2} and V_{EE2} pins, with a value of 220-nF to 10-µF for device biasing. TI recommends placing an additional 100-nF capacitor in parallel with the device biasing capacitor for high frequency filtering. Both capacitors should be positioned as close to the device as possible. Low-ESR, ceramic surface-mount capacitors are recommended. Similarly, a bypass capacitor should also be placed between the V_{CC1} and GND1 pins. Given the small amount of current drawn by the logic circuitry within the input side of the UCC5390-Q1 device, this bypass capacitor has a minimum recommended value of 100 nF.

If only a single, primary-side power supply is available in an application, isolated power can be generated for the secondary side with the help of a transformer driver such as Texas Instruments' SN6501 or SN6505A. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501 Transformer Driver for Isolated Power Supplies* data sheet and *SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet.

12 Layout

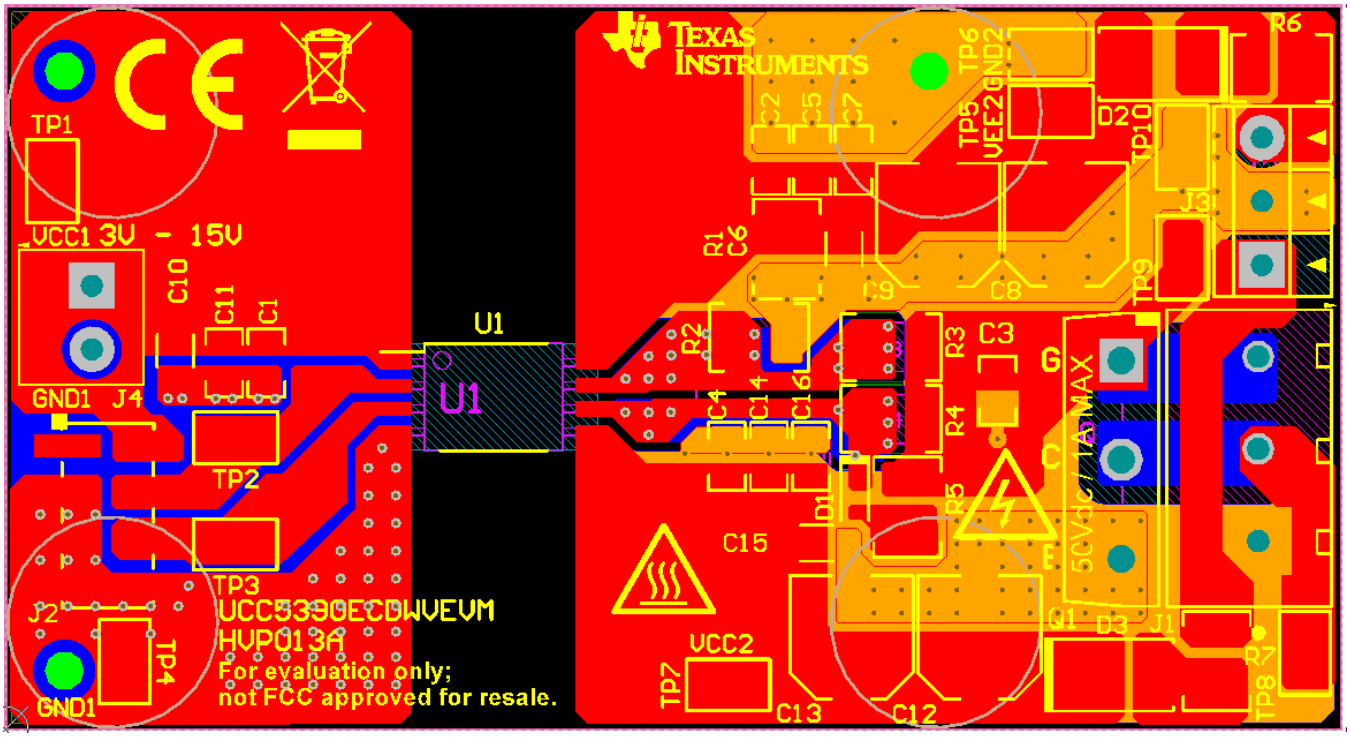
12.1 Layout Guidelines

Designers must pay close attention to PCB layout to achieve optimum performance for the UCC5390-Q1. Some key guidelines are:

- Component placement:
  - Low-ESR and low-ESL capacitors must be connected close to the device between the V_{CC1} and GND1 pins and between the V_{CC2} and V_{EE2} pins to bypass noise and to support high peak currents when turning on the external power transistor.
  - To avoid large negative transients on the V_{EE2} pins connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- Grounding considerations:
  - Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- High-voltage considerations:
  - To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended in order to prevent contamination that may compromise the isolation performance.
- Thermal considerations:
  - A large amount of power may be dissipated by the UCC5390-Q1 if the driving voltage is high, the load is heavy, or the switching frequency is high (for more information, see the *Estimate Gate-Driver Power Loss* section). Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction-to-board thermal impedance (θ_{JB}).
  - Increasing the PCB copper connecting to the V_{CC2} and V_{EE2} pins is recommended, with priority on maximizing the connection to V_{EE2}. However, the previously mentioned high-voltage PCB considerations must be maintained.
  - If the system has multiple layers, TI also recommends connecting the V_{CC2} and V_{EE2} pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity. However, keep in mind that no traces or coppers from different high voltage planes are overlapping.

12.2 Layout Example

图 30 shows a PCB layout example with the signals and key components labeled.



(1) No PCB traces or copper are located between the primary and secondary side, which ensures isolation performance.

图 30. Layout Example

Layout Example (接下页)

图 31 and 图 32 show the top and bottom layer traces and copper.

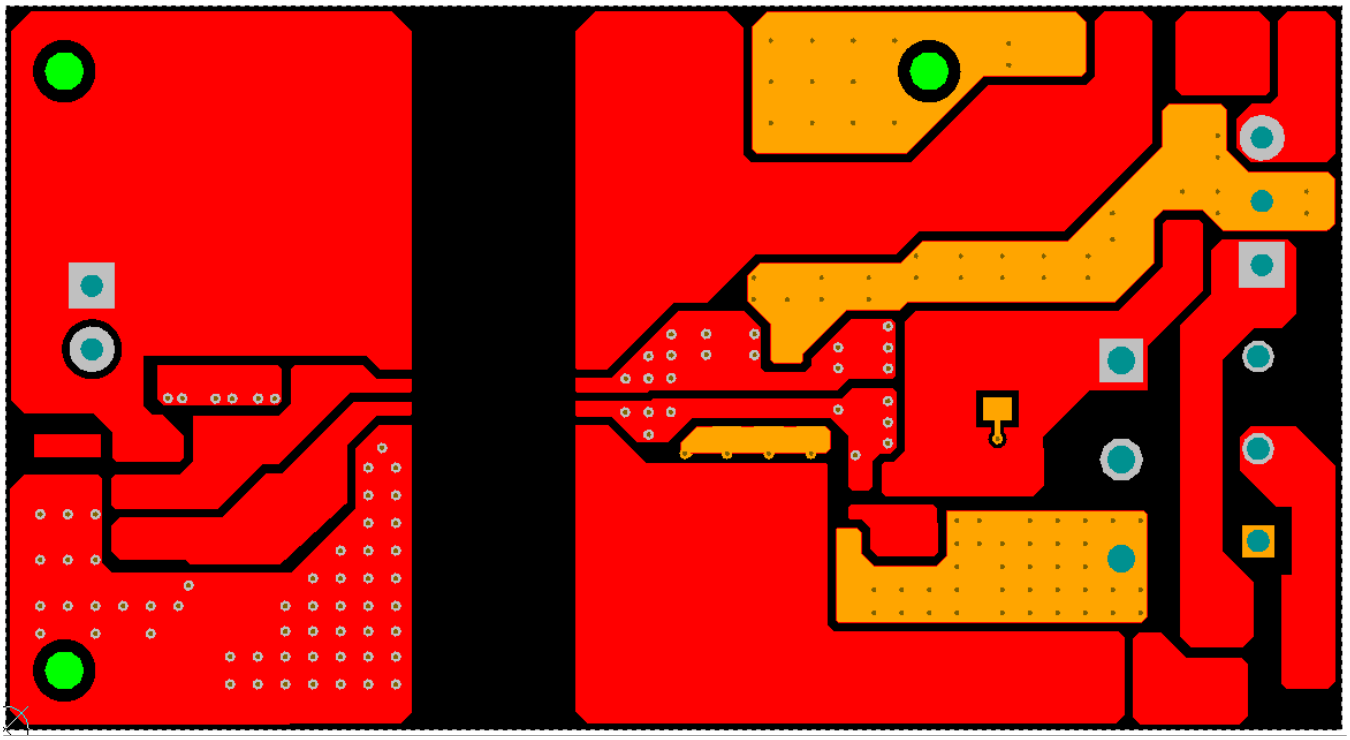


图 31. Top-Layer Traces and Copper

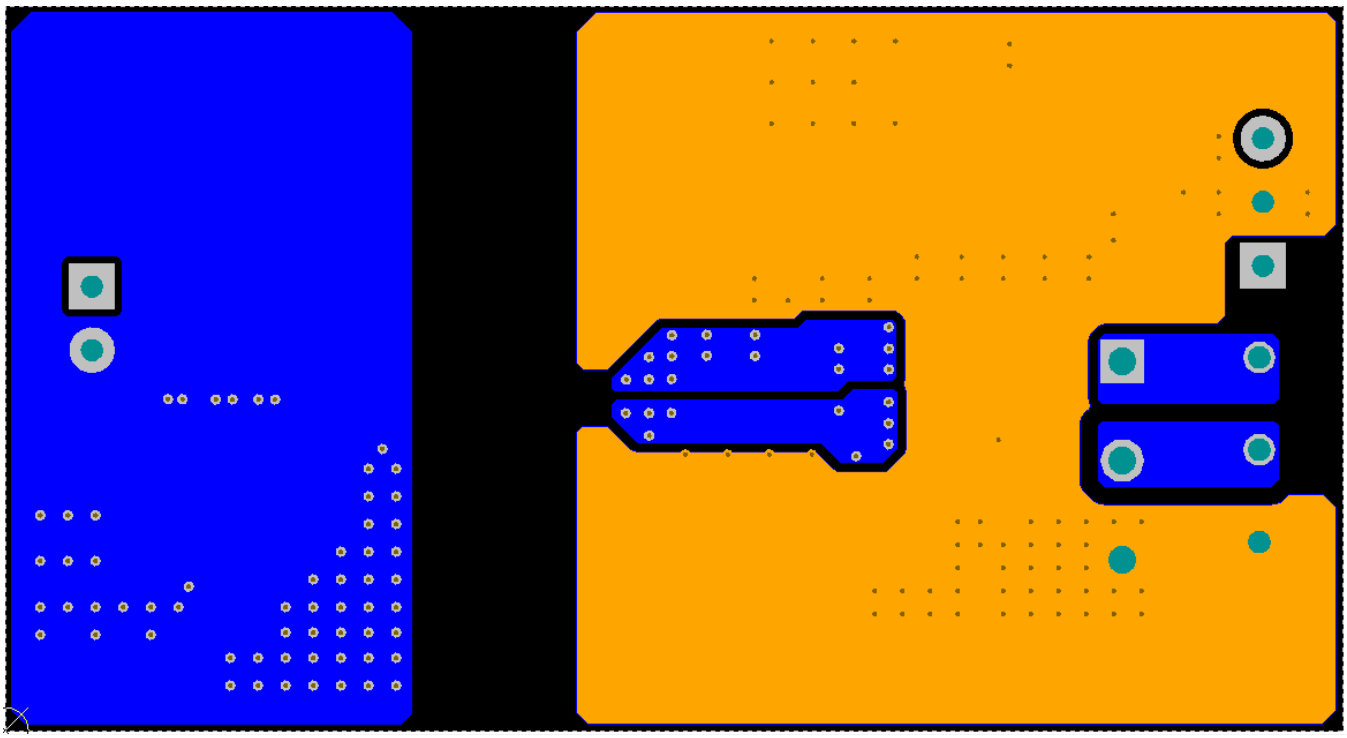


图 32. Bottom-Layer Traces and Copper (Flipped)

Layout Example (接下页)

图 33 shows the 3D layout of the top view of the PCB.

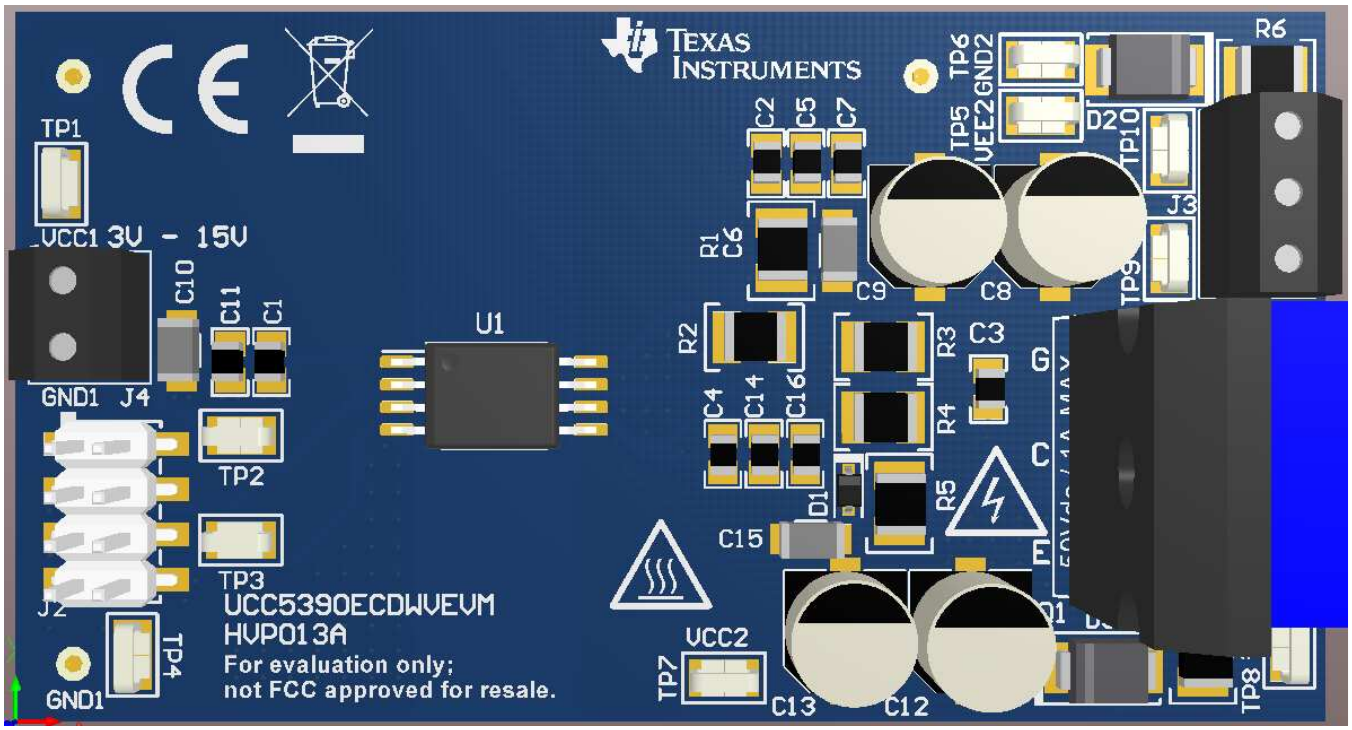


图 33. 3-D PCB View

12.3 PCB Material

Use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

图 34 shows the recommended layer stack.

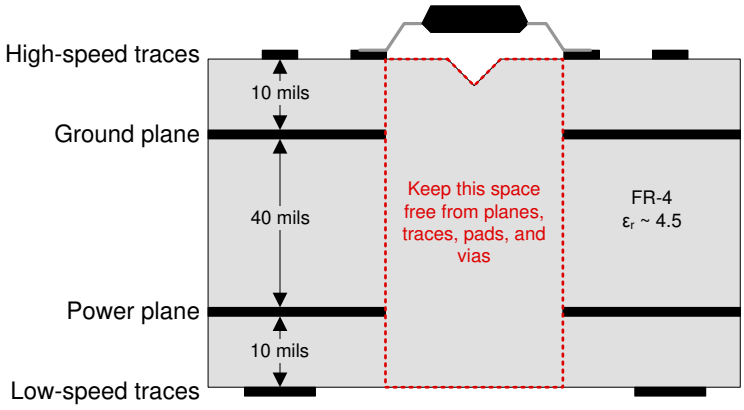


图 34. Recommended Layer Stack

13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《数字隔离器设计指南》*
- 德州仪器 (TI)，*隔离相关术语*
- 德州仪器 (TI)，*《SN6501 用于隔离式电源的变压器驱动器》数据表*
- 德州仪器 (TI)，*《SN6505A 用于隔离式电源的低噪声 1A 变压器驱动器》数据表*
- 德州仪器 (TI)，*UCC53x0xD 评估模块用户指南*

13.2 认证

UL 在线认证目录，*"FPPT2.E181974 非光学隔离器件 - 组件"*证书编号：20170718-E181974，

13.3 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

13.4 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.5 社区资源

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC5390ECQDWVQ1	ACTIVE	SOIC	DWV	8	64	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	5390ECQ	Samples
UCC5390ECQDWVRQ1	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	5390ECQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

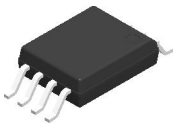
(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

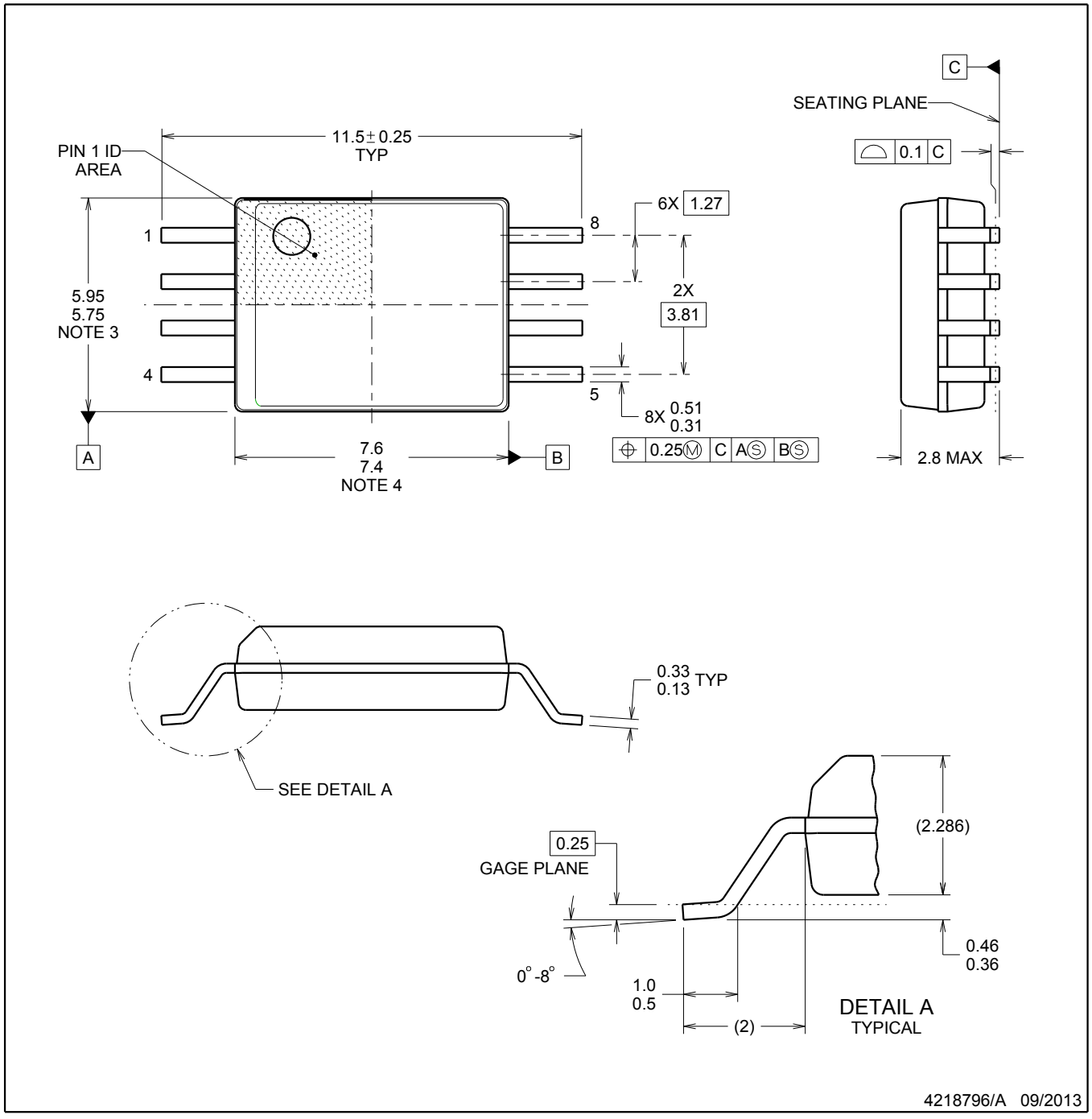
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



DWV0008A

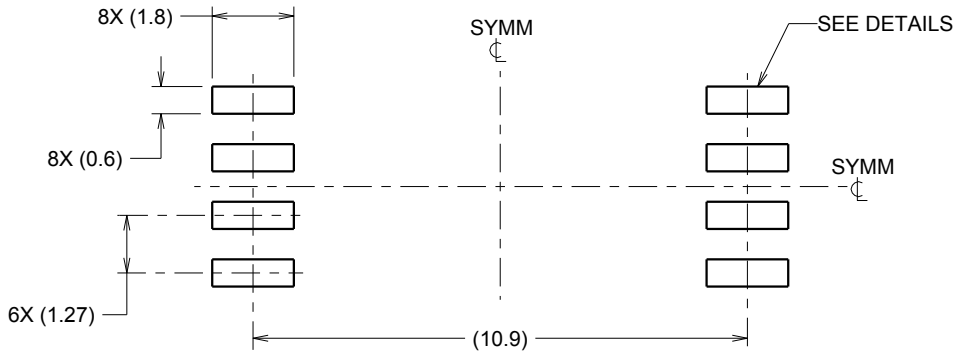
SOIC - 2.8 mm max height

SOIC

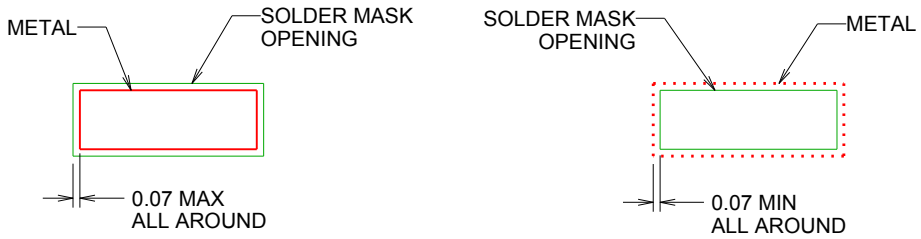


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

4218796/A 09/2013

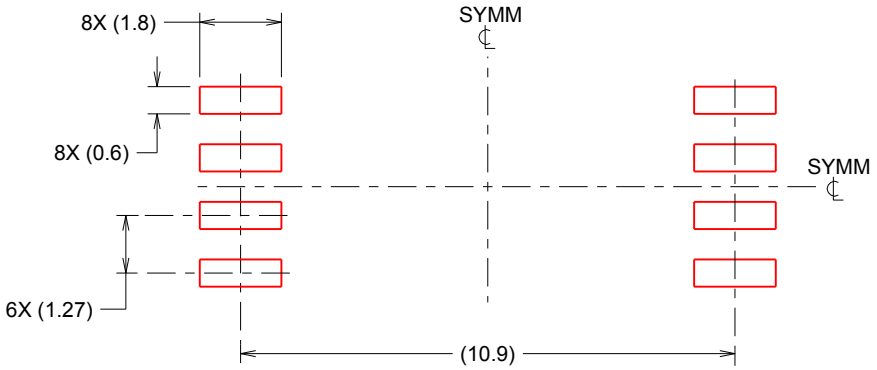
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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