Precision Micropower ΔΣ RMS-to-DC Converter

FEATURES

- **Simple to Use, Requires One Capacitor**
- **True RMS DC Conversion Using ΔΣ Technology**
- **High Accuracy:**
  0.1% Gain Accuracy from 50Hz to 1kHz
  0.25% Total Error from 50Hz to 1kHz
- **High Linearity:**
  0.02% Linearity Allows Simple System Calibration
- **Low Supply Current:**
  155µA Typ, 170µA Max
- **Ultralow Shutdown Current:**
  0.1µA
- **Constant Bandwidth:**
  Independent of Input Voltage
  800kHz –3dB, 6kHz ±1%
- **Flexible Supplies:**
  2.7V to 5.5V Single Supply
  Up to ±5.5V Dual Supply
- **Flexible Inputs:**
  Differential or Single-Ended
  Rail-to-Rail Common Mode Voltage Range
  Up to $1V_{PEAK}$ Differential Voltage
- **Flexible Output:**
  Rail-to-Rail Output
  Separate Output Reference Pin Allows Level Shifting
- **Wide Temperature Range:**
  –55°C to 125°C
- **Small Size:**
  Space Saving 8-Pin MSOP Package

DESCRIPTION

The LTC®1966 is a true RMS-to-DC converter that utilizes an innovative patented ΔΣ computational technique. The internal delta sigma circuitry of the LTC1966 makes it simpler to use, more accurate, lower power and dramatically more flexible than conventional log antilog RMS-to-DC converters.

The LTC1966 accepts single-ended or differential input signals (for EMI/RFI rejection) and supports crest factors up to 4. Common mode input range is rail-to-rail. Differential input range is $1V_{PEAK}$, and offers unprecedented linearity. Unlike previously available RMS-to-DC converters, the superior linearity of the LTC1966 allows hassle free system calibration at any input voltage.

The LTC1966 also has a rail-to-rail output with a separate output reference pin providing flexible level shifting. The LTC1966 operates on a single power supply from 2.7V to 5.5V or dual supplies up to ±5.5V. A low power shutdown mode reduces supply current to 0.5µA.

The LTC1966 is insensitive to PC board soldering and stresses, as well as operating temperature. The LTC1966 is packaged in the space saving MSOP package which is ideal for portable applications.

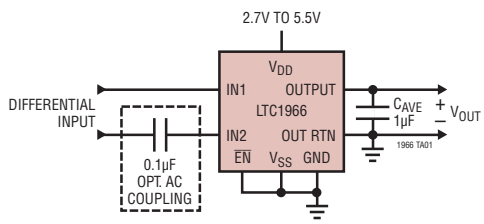
APPLICATIONS

- True RMS Digital Multimeters and Panel Meters
- True RMS AC + DC Measurements

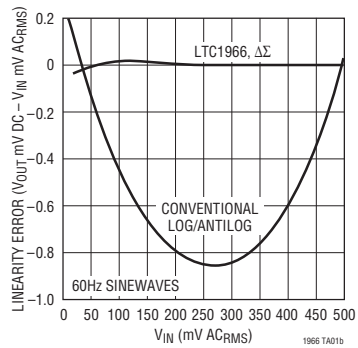
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TYPICAL APPLICATION

Single Supply RMS-to-DC Converter



Quantum Leap in Linearity Performance



ABSOLUTE MAXIMUM RATINGS

(Note 1)

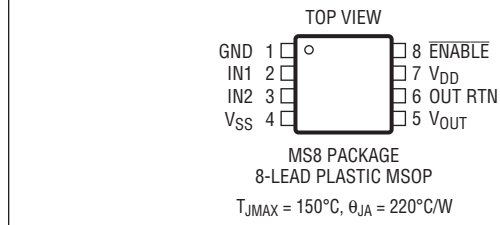
Supply Voltage
- V_{DD} to GND ..... –0.3V to 7V
- V_{DD} to V_{SS} ..... –0.3V to 12V
- V_{SS} to GND ..... –7V to 0.3V

Input Currents (Note 2) ..... ±10mA
Output Current (Note 3) ..... ±10mA
$\overline{ENABLE}$ Voltage ..... V_{SS} – 0.3V to V_{SS} + 12V
OUT RTN Voltage ..... V_{SS} – 0.3V to V_{DD}
Operating Temperature Range (Note 4)
- LTC1966C/LTC1966I ..... –40°C to 85°C
- LTC1966H ..... –40°C to 125°C
- LTC1966MP ..... –55°C to 125°C

Specified Temperature Range (Note 5)
- LTC1966C/LTC1966I ..... –40°C to 85°C
- LTC1966H ..... –40°C to 125°C
- LTC1966MP ..... –55°C to 125°C

Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PIN CONFIGURATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 220°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1966CMS8#PBF	LTC1966CMS8#TRPBF	LTTG	8-Lead Plastic MSOP	0°C to 70°C
LTC1966IMS8#PBF	LTC1966IMS8#TRPBF	LTTH	8-Lead Plastic MSOP	–40°C to 85°C
LTC1966HMS8#PBF	LTC1966HMS8#TRPBF	LTTG	8-Lead Plastic MSOP	–40°C to 125°C
LTC1966MPMS8#PBF	LTC1966MPMS8#TRPBF	LTTG	8-Lead Plastic MSOP	–55°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 5V, V_{SS} = –5V, V_{OUTRTN} = 0V, C_{AVE} = 10µF, V_{IN} = 200mV_{RMS}, $V_{\overline{ENABLE}}$ = 0.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Conversion Accuracy							
G_{ERR}	Conversion Gain Error	50Hz to 1kHz Input (Notes 6, 7)			±0.1	±0.3	%
		LTC1966C, LTC1966I	●			±0.4	%
		LTC1966H, LTC1966MP	●			±0.7	%
V_{OOS}	Output Offset Voltage	(Notes 6, 7)			0.1	0.2	mV
		LTC1966C, LTC1966I	●			0.4	mV
		LTC1966H, LTC1966MP	●			0.6	mV
LIN_{ERR}	Linearity Error	50mV to 350mV (Notes 7, 8)	●		0.02	0.15	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 5V, V_{SS} = –5V, V_{OUTRTN} = 0V, C_{AVE} = 10µF, V_{IN} = 200mV_{RMS}, $V_{\overline{ENABLE}}$ = 0.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PSRR	Power Supply Rejection	(Note 9) LTC1966C, LTC1966I LTC1966H, LTC1966MP	 ● ●		0.02	0.15 0.20 0.3	%V %V %V
V_{IOS}	Input Offset Voltage	(Notes 6, 7, 10)	 ●		0.02	0.8 1.0	mV mV
Accuracy vs Crest Factor (CF)							
	CF = 4	60Hz Fundamental, 200mV_{RMS} (Note 11)	●	–1		2	mV
	CF = 5	60Hz Fundamental, 200mV_{RMS} (Note 11)	●	–20		30	mV
Input Characteristics							
I_{VR}	Input Voltage Range	(Note 14)	●	V_{SS}		V_{DD}	V
Z_{IN}	Input Impedance	Average, Differential (Note 12) Average, Common Mode (Note 12)			8 100		MΩ MΩ
CMRRI	Input Common Mode Rejection	(Note 13)	●		7	200	µV/V
V_{IMAX}	Maximum Input Swing	Accuracy = 1% (Note 14)	●	1	1.05		V
V_{IMIN}	Minimum RMS Input		●			5	mV
PSRRI	Power Supply Rejection	V_{DD} Supply (Note 9) V_{SS} Supply (Note 9)	● ●		250 120	600 300	µV/V µV/V
Output Characteristics							
OVR	Output Voltage Range		●	V_{SS}		V_{DD}	V
Z_{OUT}	Output Impedance	$V_{\overline{ENABLE}}$ = 0.5V (Note 12) $V_{\overline{ENABLE}}$ = 4.5V	●	75	85 30	95	kΩ kΩ
CMRRO	Output Common Mode Rejection	(Note 13)	●		16	200	µV/V
V_{OMAX}	Maximum Differential Output Swing	Accuracy = 2%, DC Input (Note 14)	 ●	1.0 0.9	1.05		V V
PSRRO	Power Supply Rejection	V_{DD} Supply (Note 9) V_{SS} Supply (Note 9)	● ●		250 50	1000 500	µV/V µV/V
Frequency Response							
f_{1P}	1% Additional Error (Note 15)	C_{AVE} = 10µF			6		kHz
f_{10P}	10% Additional Error (Note 15)	C_{AVE} = 10µF			20		kHz
$f_{–3dB}$	±3dB Frequency (Note 15)				800		kHz
Power Supplies							
V_{DD}	Positive Supply Voltage		●	2.7		5.5	V
V_{SS}	Negative Supply Voltage	(Note 16)	●	–5.5		0	V
I_{DD}	Positive Supply Current	IN1 = 20mV, IN2 = 0V IN1 = 200mV, IN2 = 0V	●		155 158	170	µA µA
I_{SS}	Negative Supply Current	IN1 = 20mV, IN2 = 0V	●		12	20	µA
Shutdown Characteristics							
I_{DDS}	Supply Currents	$V_{\overline{ENABLE}}$ = 4.5V	●		0.5	10	µA
I_{SSS}	Supply Currents	$V_{\overline{ENABLE}}$ = 4.5V LTC1966H, LTC1966MP	● ●	–1 –2	–0.1		µA µA
I_{IH}	$\overline{ENABLE}$ Pin Current High	$V_{\overline{ENABLE}}$ = 4.5V	●	–0.3	–0.05		µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 5V, V_{SS} = –5V, V_{OUTRTN} = 0V, C_{AVE} = 10µF, V_{IN} = 200mV_{RMS}, V_{ENABLE} = 0.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{IL}	$\overline{ENABLE}$ Pin Current Low	$V_{\overline{ENABLE}}$ = 0.5V LTC1966H, LTC1966MP	● ●	–2 –10	–1	–0.1	µA µA
V_{TH}	$\overline{ENABLE}$ Threshold Voltage	V_{DD} = 5V, V_{SS} = –5V V_{DD} = 5V, V_{SS} = GND V_{DD} = 2.7V, V_{SS} = GND			2.4 2.1 1.3		V V V
V_{HYS}	$\overline{ENABLE}$ Threshold Hysteresis				0.1		V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs (IN1, IN2) are protected by shunt diodes to V_{SS} and V_{DD}. If the inputs are driven beyond the rails, the current should be limited to less than 10mA.

Note 3: The LTC1966 output (V_{OUT}) is high impedance and can be overdriven, either sinking or sourcing current, to the limits stated.

Note 4: The LTC1966C/LTC1966I are guaranteed functional over the operating temperature range of –40°C to 85°C. The LTC1966H/LTC1966MP are guaranteed functional over the operating temperature range of –55°C to 125°C.

Note 5: The LTC1966C is guaranteed to meet specified performance from 0°C to 70°C. The LTC1966C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested nor QA sampled at these temperatures. The LTC1966I is guaranteed to meet specified performance from –40°C to 85°C. The LTC1966H is guaranteed to meet specified performance from –40°C to 125°C. The LTC1966MP is guaranteed to meet specified performance from –55°C to 125°C.

Note 6: High speed automatic testing cannot be performed with C_{AVE} = 10µF. The LTC1966 is 100% tested with C_{AVE} = 22nF. Correlation tests have shown that the performance limits above can be guaranteed with the additional testing being performed to guarantee proper operation of all the internal circuitry.

Note 7: High speed automatic testing cannot be performed with 60Hz inputs. The LTC1966 is 100% tested with DC and 10kHz input signals. Measurements with DC inputs from 50mV to 350mV are used to calculate the four parameters: G_{ERR}, V_{OOS}, V_{IOS} and linearity error. Correlation tests have shown that the performance limits above can be guaranteed with the additional testing being performed to guarantee proper operation of all internal circuitry.

Note 8: The LTC1966 is inherently very linear. Unlike older log/antilog circuits, its behavior is the same with DC and AC inputs, and DC inputs are used for high speed testing.

Note 9: The power supply rejections of the LTC1966 are measured with DC inputs from 50mV to 350mV. The change in accuracy from V_{DD} = 2.7V to V_{DD} = 5.5V with V_{SS} = 0V is divided by 2.8V. The change in accuracy from V_{SS} = 0V to V_{SS} = –5.5V with V_{DD} = 5.5V is divided by 5.5V.

Note 10: Previous generation RMS-to-DC converters required nonlinear input stages as well as a nonlinear core. Some parts specify a DC reversal error, combining the effects of input nonlinearity and input offset voltage. The LTC1966 behavior is simpler to characterize and the input offset voltage is the only significant source of DC reversal error.

Note 11: High speed automatic testing cannot be performed with 60Hz inputs. The LTC1966 is 100% tested with DC stimulus. Correlation tests have shown that the performance limits above can be guaranteed with the additional testing being performed to verify proper operation of all internal circuitry.

Note 12: The LTC1966 is a switched capacitor device and the input/output impedance is an average impedance over many clock cycles. The input impedance will not necessarily lead to an attenuation of the input signal measured. Refer to the Applications Information section titled Input Impedance for more information.

Note 13: The common mode rejection ratios of the LTC1966 are measured with DC inputs from 50mV to 350mV. The input CMRR is defined as the change in V_{IOS} measured between input levels of V_{SS} to V_{SS} + 350mV and input levels of V_{DD} – 350mV to V_{DD} divided by V_{DD} – V_{SS} – 350mV. The output CMRR is defined as the change in V_{OOS} measured with OUT RTN = V_{SS} and OUT RTN = V_{DD} – 350mV divided by V_{DD} – V_{SS} – 350mV.

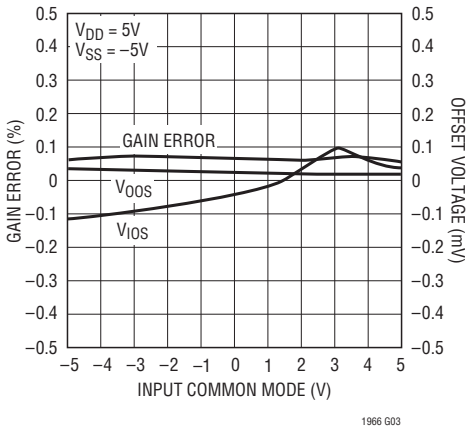
Note 14: Each input of the LTC1966 can withstand any voltage within the supply range. These inputs are protected with ESD diodes, so going beyond the supply voltages can damage the part if the absolute maximum current ratings are exceeded. Likewise for the output pins. The LTC1966 input and output voltage swings are limited by internal clipping. The maximum differential input of the LTC1966 (referred to as maximum input swing) is 1V. This applies to either input polarity, so it can be thought of as ±1V. Because the differential input voltage gets processed by the LTC1966 with gain, it is subject to internal clipping. Exceeding the 1V maximum can, depending on the input crest factor, impact the accuracy of the output voltage, but does not damage the part. Fortunately, the LTC1966's ΔΣ topology is relatively tolerant of momentary internal clipping. The input clipping is tested with a crest factor of 2, while the output clipping is tested with a DC input.

Note 15: The LTC1966 exploits oversampling and noise shaping to reduce the quantization noise of internal 1-bit analog-to-digital conversions. At higher input frequencies, increasingly large portions of this noise are aliased down to DC. Because the noise is shifted in frequency, it becomes a low frequency rumble and is only filtered at the expense of increasingly long settling times. The LTC1966 is inherently wideband, but the output accuracy is degraded by this aliased noise. These specifications apply with C_{AVE} = 10µF and constitute a 3-sigma variation of the output rumble.

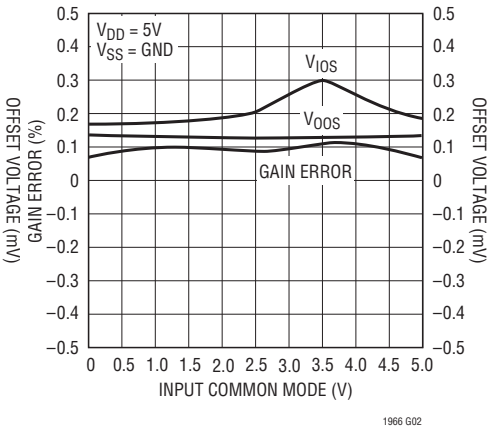
Note 16: The LTC1966 can operate down to 2.7V single supply but cannot operate at ±2.7V. This additional constraint on V_{SS} can be expressed mathematically as $-3 \bullet (V_{DD} - 2.7V) \leq V_{SS} \leq$ Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

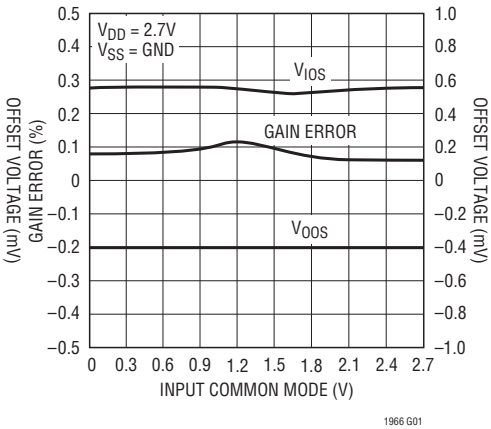
Gain and Offsets vs Input Common Mode



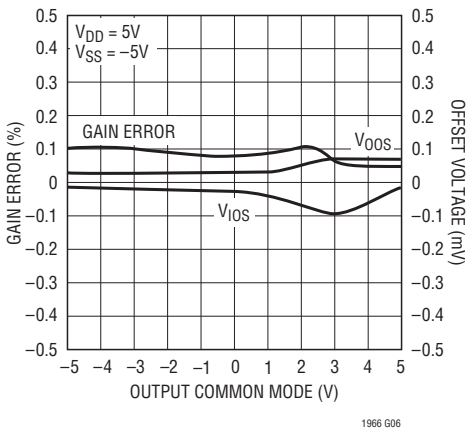
Gain and Offsets vs Input Common Mode



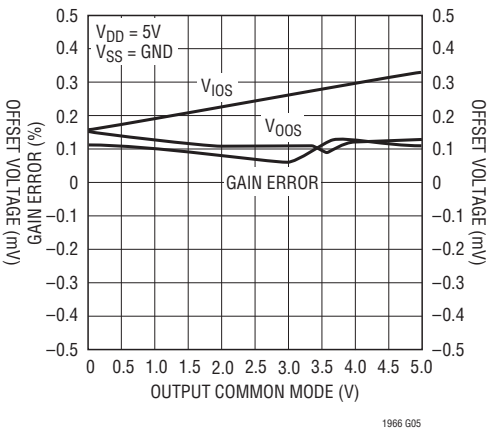
Gain and Offsets vs Input Common Mode



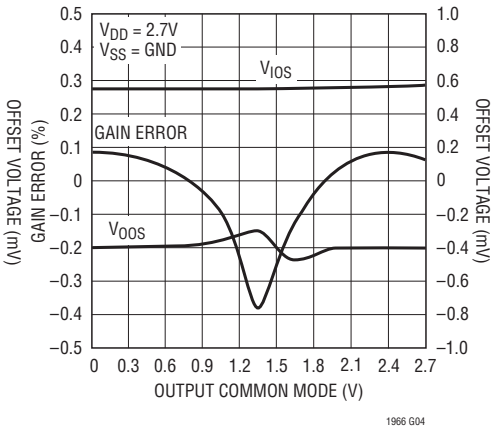
Gain and Offsets vs Output Common Mode



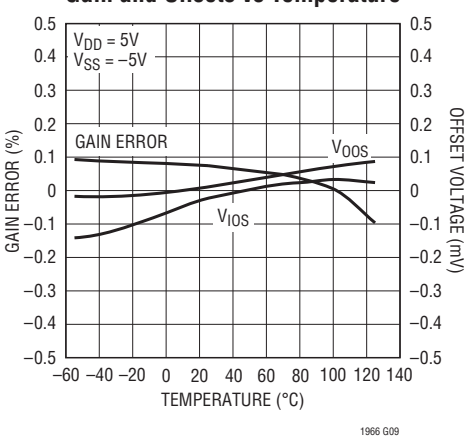
Gain and Offsets vs Output Common Mode



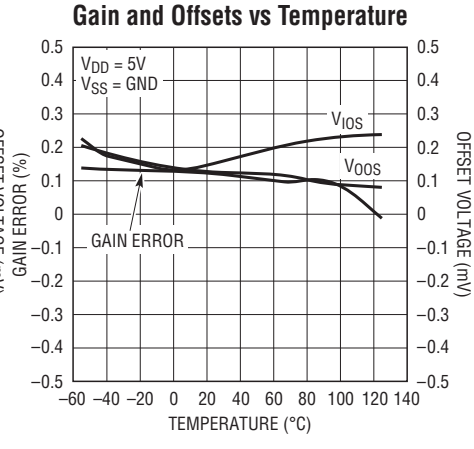
Gain and Offsets vs Output Common Mode



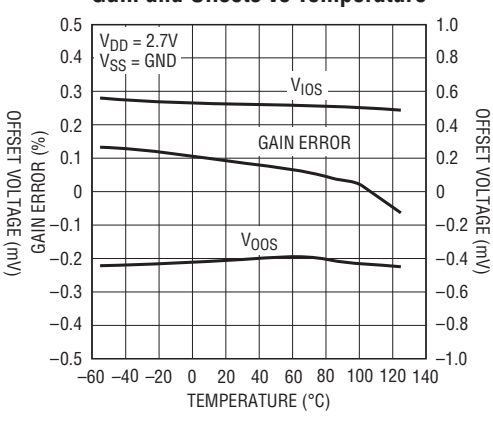
Gain and Offsets vs Temperature



Gain and Offsets vs Temperature

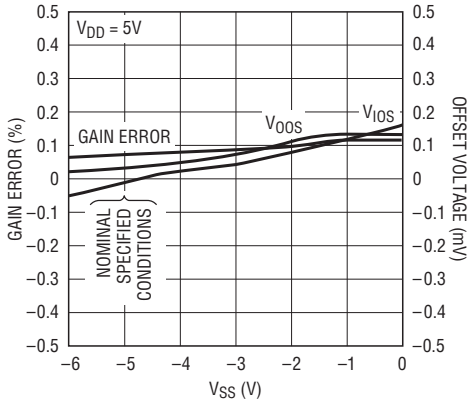


Gain and Offsets vs Temperature

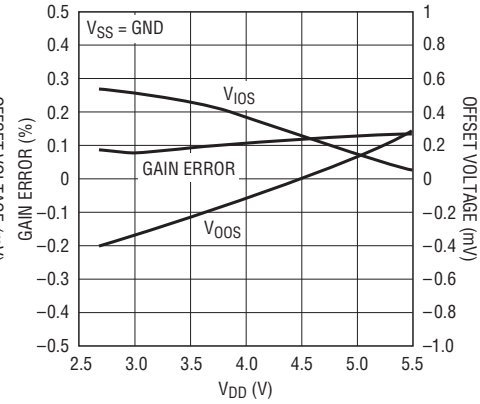


TYPICAL PERFORMANCE CHARACTERISTICS

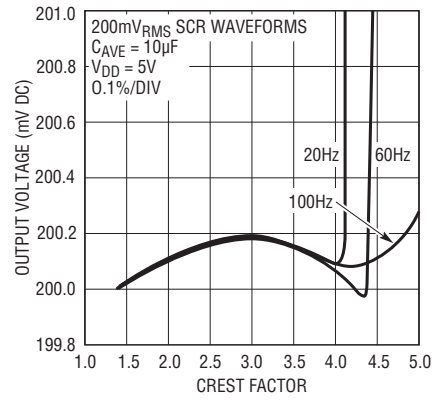
Gain and Offsets vs V_{SS} Supply



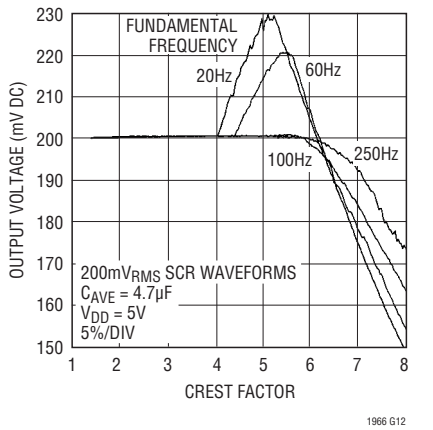
Gain and Offsets vs V_{DD} Supply



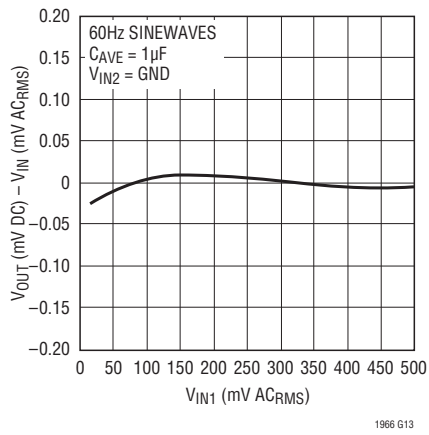
Performance vs Crest Factor



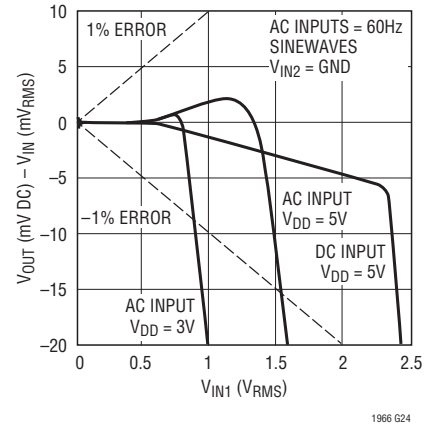
Performance vs Large Crest Factors



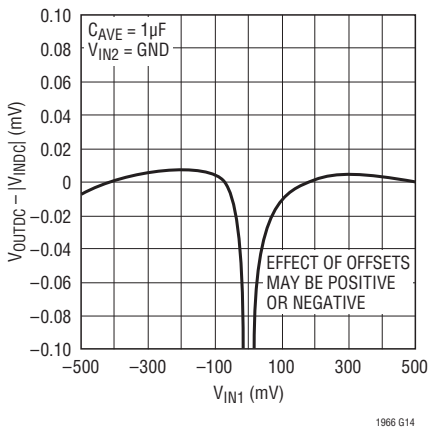
AC Linearity



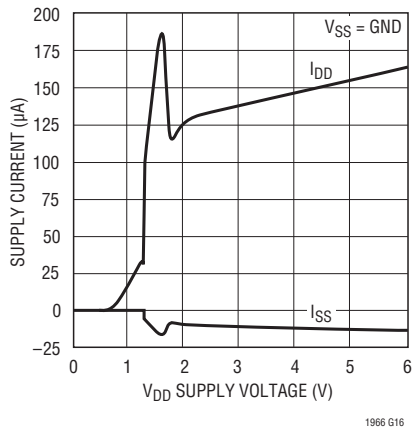
Output Accuracy vs Signal Amplitude



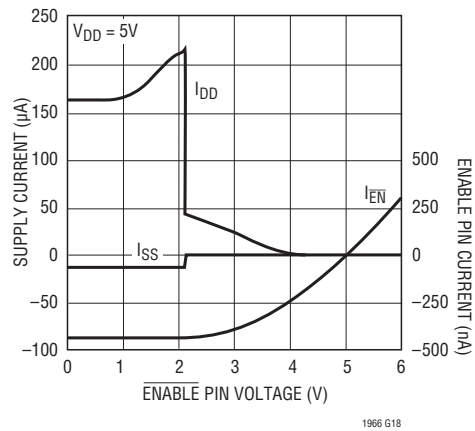
DC Linearity



Quiescent Supply Currents vs Supply Voltage

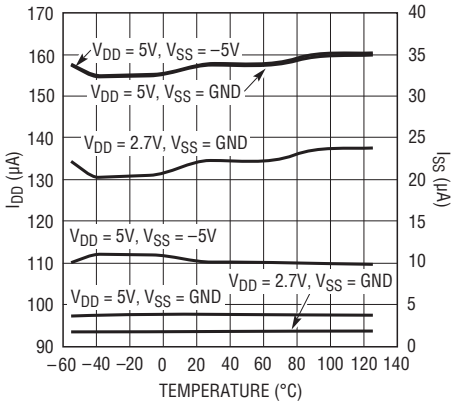


Shutdown Currents vs $\overline{\text{ENABLE}}$ Voltage

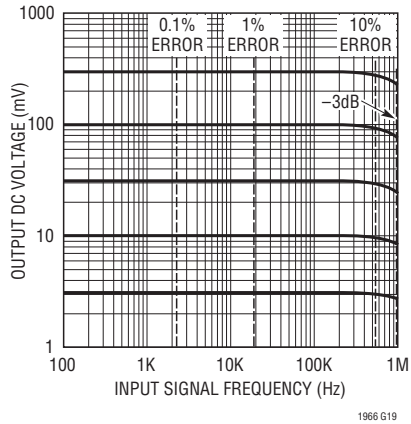


TYPICAL PERFORMANCE CHARACTERISTICS

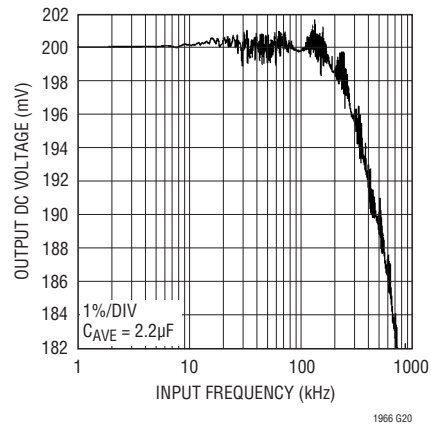
Quiescent Supply Currents vs Temperature



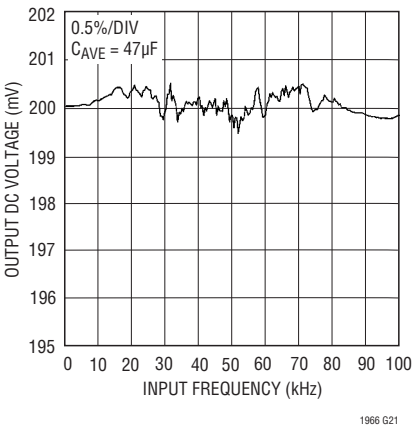
Input Signal Bandwidth



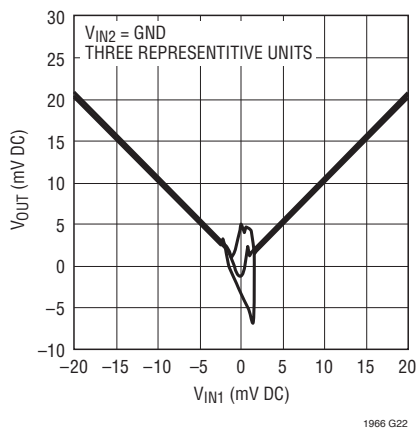
Input Signal Bandwidth



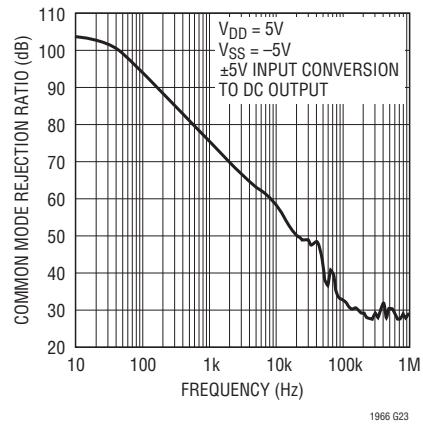
Bandwidth to 100kHz



DC Transfer Function Near Zero



Common Mode Rejection Ratio vs Frequency



PIN FUNCTIONS

GND (Pin 1): Ground. A power return pin.

IN1 (Pin 2): Differential Input. DC coupled (polarity is irrelevant).

IN2 (Pin 3): Differential Input. DC coupled (polarity is irrelevant).

V_{SS} (Pin 4): Negative Voltage Supply. GND to –5.5V.

V_{OUT} (Pin 5): Output Voltage. This is high impedance. The RMS averaging is accomplished with a single shunt capacitor from this node to OUT RTN. The transfer function is given by:

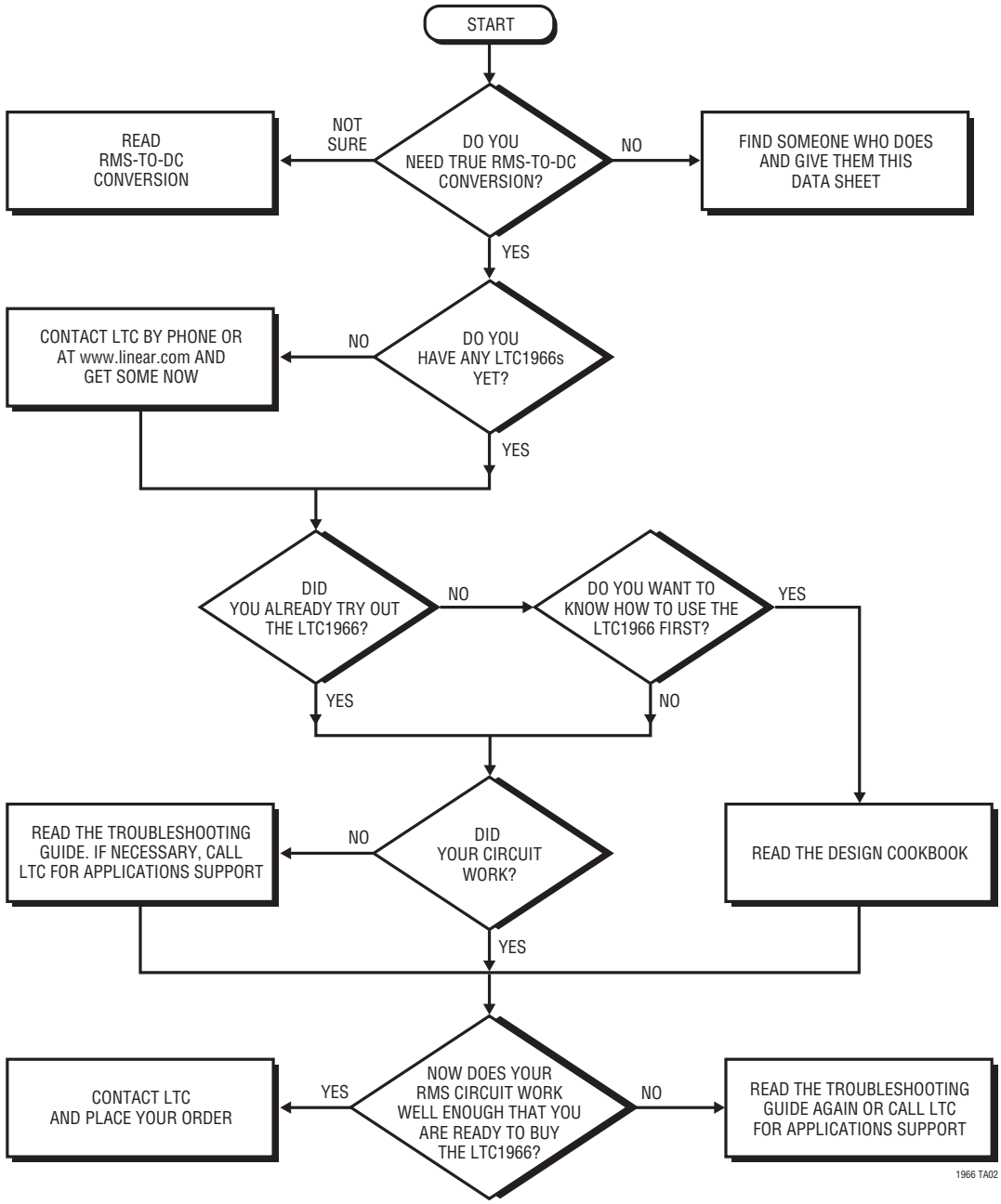
$$\left(V_{OUT} - \text{OUT RTN}\right) = \sqrt{\text{Average}\left[\left(\text{IN2} - \text{IN1}\right)^2\right]}$$

OUT RTN (Pin 6): Output Return. The output voltage is created relative to this pin. The V_{OUT} and OUT RTN pins are not balanced and this pin should be tied to a low impedance, both AC and DC. Although it is typically tied to GND, it can be tied to any arbitrary voltage, V_{SS} < OUT RTN < (V_{DD} – Max Output). Best results are obtained when OUT RTN = GND.

V_{DD} (Pin 7): Positive Voltage Supply. 2.7V to 5.5V.

$\overline{\text{ENABLE}}$ (Pin 8): An Active Low Enable Input. LTC1966 is debiased if open circuited or driven to V_{DD}. For normal operation, pull to GND, a logic low or even V_{SS}.

APPLICATIONS INFORMATION



APPLICATIONS INFORMATION

RMS-TO-DC CONVERSION

Definition of RMS

RMS amplitude is the consistent, fair and standard way to measure and compare dynamic signals of all shapes and sizes. Simply stated, the RMS amplitude is the heating potential of a dynamic waveform. A $1V_{RMS}$ AC waveform will generate the same heat in a resistive load as will 1V DC.

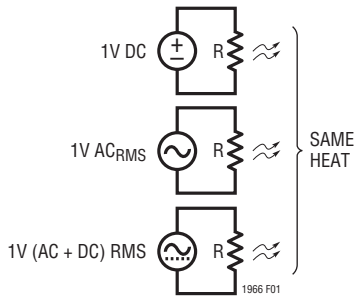


Figure 1

Mathematically, RMS is the root of the mean of the square:

$$V_{RMS} = \sqrt{\overline{V^2}}$$

Alternatives to RMS

Other ways to quantify dynamic waveforms include peak detection and average rectification. In both cases, an average (DC) value results, but the value is only accurate at the one chosen waveform type for which it is calibrated, typically sine waves. The errors with average rectification are shown in Table 1. Peak detection is worse in all cases and is rarely used.

Table 1. Errors with Average Rectification vs True RMS

WAVEFORM	V_{RMS}	AVERAGE RECTIFIED (V)	ERROR*
Square Wave	1.000	1.000	11%
Sine Wave	1.000	0.900	*Calibrate for 0% Error
Triangle Wave	1.000	0.866	–3.8%
SCR at 1/2 Power, Θ = 90°	1.000	0.637	–29.3%
SCR at 1/4 Power, Θ = 114°	1.000	0.536	–40.4%

The last two entries of Table 1 are chopped sine waves as is commonly created with thyristors such as SCRs and Triacs. Figure 2a shows a typical circuit and Figure 2b shows the resulting load voltage, switch voltage and load currents. The power delivered to the load depends on the firing angle, as well as any parasitic losses such as switch ON voltage drop. Real circuit waveforms will also typically have significant ringing at the switching transition, dependent on exact circuit parasitics. For the purposes of this data sheet, SCR waveforms refers to the ideal chopped sine wave, though the LTC1966 will do faithful RMS-to-DC conversion with real SCR waveforms as well.

The case shown is for Θ = 90°, which corresponds to 50% of available power being delivered to the load. As noted in Table 1, when Θ = 114°, only 25% of the available power is being delivered to the load and the power drops quickly as Θ approaches 180°.

With an average rectification scheme and the typical calibration to compensate for errors with sine waves, the RMS level of an input sine wave is properly reported; it is only with a nonsinusoidal waveform that errors occur. Because of this calibration, and the output reading in V_{RMS}, the term true RMS got coined to denote the use of an actual RMS-to-DC converter as opposed to a calibrated average rectifier.

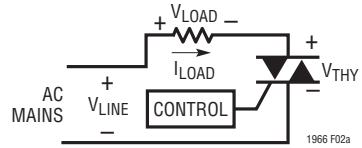


Figure 2a

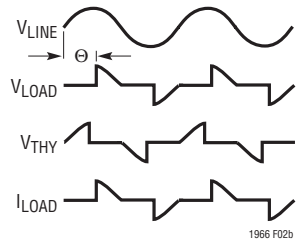


Figure 2b

APPLICATIONS INFORMATION

How an RMS-to-DC Converter Works

Monolithic RMS-to-DC converters use an implicit computation to calculate the RMS value of an input signal. The fundamental building block is an analog multiply/divide used as shown in Figure 3. Analysis of this topology is easy and starts by identifying the inputs and the output of the lowpass filter. The input to the LPF is the calculation from the multiplier/divider; $(V_{IN})^2/V_{OUT}$. The lowpass filter will take the average of this to create the output, mathematically:

$$V_{OUT} = \overline{\left(\frac{(V_{IN})^2}{V_{OUT}}\right)},$$

Because V_{OUT} is DC,

$$\overline{\left(\frac{(V_{IN})^2}{V_{OUT}}\right)} = \frac{\overline{(V_{IN})^2}}{V_{OUT}}, \text{ so}$$

$$V_{OUT} = \frac{\overline{(V_{IN})^2}}{V_{OUT}}, \text{ and}$$

$$(V_{OUT})^2 = \overline{(V_{IN})^2}, \text{ or}$$

$$V_{OUT} = \sqrt{\overline{(V_{IN})^2}} = RMS(V_{IN})$$

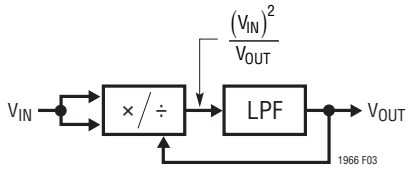


Figure 3. RMS-to-DC Converter with Implicit Computation

Unlike the prior generation RMS-to-DC converters, the LTC1966 computation does NOT use log/antilog circuits, which have all the same problems, and more, of log/antilog multipliers/dividers, i.e., linearity is poor, the bandwidth changes with the signal amplitude and the gain drifts with temperature.

How the LTC1966 RMS-to-DC Converter Works

The LTC1966 uses a completely new topology for RMS-to-DC conversion, in which a ΔΣ modulator acts as the divider, and a simple polarity switch is used as the multiplier as shown in Figure 4.

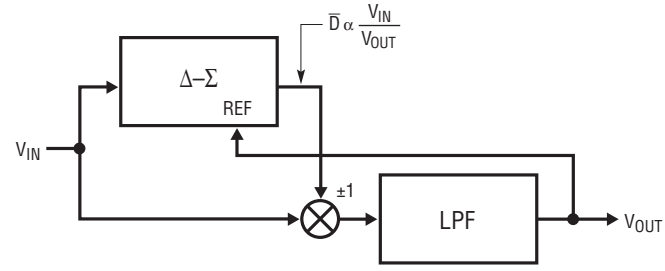


Figure 4. Topology of LTC1966

The ΔΣ modulator has a single-bit output whose average duty cycle ($\overline{D}$) will be proportional to the ratio of the input signal divided by the output. The ΔΣ is a 2nd order modulator with excellent linearity. The single bit output is used to selectively buffer or invert the input signal. Again, this is a circuit with excellent linearity, because it operates at only two points: ±1 gain; the average effective multiplication over time will be on the straight line between these two points. The combination of these two elements again creates a lowpass filter input signal proportional to $(V_{IN})^2/V_{OUT}$, which, as shown above, results in RMS-to-DC conversion.

The lowpass filter performs the averaging of the RMS function and must be a lower corner frequency than the lowest frequency of interest. For line frequency measurements, this filter is simply too large to implement on-chip, but the LTC1966 needs only one capacitor on the output to implement the lowpass filter. The user can select this capacitor depending on frequency range and settling time requirements, as will be covered in the Design Cookbook section to follow.

This topology is inherently more stable and linear than log/antilog implementations primarily because all of the signal processing occurs in circuits with high gain op amps operating closed loop.

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More detail of the LTC1966 inner workings is shown in the Simplified Schematic towards the end of this data sheet. Note that the internal scalings are such that the ΔΣ output duty cycle is limited to 0% or 100% only when V_{IN} exceeds ± 4 • V_{OUT}.

Linearity of an RMS-to-DC Converter

Linearity may seem like an odd property for a device that implements a function that includes two very nonlinear processes: squaring and square rooting.

However, an RMS-to-DC converter has a transfer function, RMS volts in to DC volts out, that should ideally have a 1:1 transfer function. To the extent that the input to output transfer function does not lie on a straight line, the part is nonlinear.

A more complete look at linearity uses the simple model shown in Figure 5. Here an ideal RMS core is corrupted by both input circuitry and output circuitry that have imperfect transfer functions. As noted, input offset is introduced in the input circuitry, while output offset is introduced in the output circuitry.

Any nonlinearity that occurs in the output circuity will corrupt the RMS in to DC out transfer function. A nonlinearity in the input circuitry will typically corrupt that transfer function far less, simply because with an AC input, the RMS-to-DC conversion will average the nonlinearity from a whole range of input values together.

But the input nonlinearity will still cause problems in an RMS-to-DC converter because it will corrupt the accuracy as the input signal shape changes. Although an RMS-to-DC converter will convert any input waveform to a DC output, the accuracy is not necessarily as good for all waveforms as it is with sine waves. A common way to describe dynamic signal wave shapes is crest factor. The crest factor is the ratio of the peak value relative to the RMS value of a waveform. A signal with a crest factor of 4, for instance, has a peak that is four times its RMS value. Because this peak has energy (proportional to voltage squared) that is 16 times (4^2) the energy of the RMS value, the peak is necessarily present for at most 6.25% (1/16) of the time.

The LTC1966 performs very well with crest factors of 4 or less and will respond with reduced accuracy to signals with higher crest factors. The high performance with crest factors less than 4 is directly attributable to the high linearity throughout the LTC1966.

The LTC1966 does not require an input rectifier, as is common with traditional log/antilog RMS-to-DC converters. Thus, the LTC1966 has none of the nonlinearities that are introduced by rectification.

The excellent linearity of the LTC1966 allows calibration to be highly effective at reducing system errors. See System Calibration section following the Design Cookbook.



Figure 5. Linearity Model of an RMS-to-DC Converter

APPLICATIONS INFORMATION

DESIGN COOKBOOK

The LTC1966 RMS-to-DC converter makes it easy to implement a rather quirky function. For many applications all that will be needed is a single capacitor for averaging, appropriate selection of the I/O connections and power supply bypassing. Of course, the LTC1966 also requires power. A wide variety of power supply configurations are shown in the Typical Applications section towards the end of this data sheet.

Capacitor Value Selection

The RMS or root-mean-squared value of a signal, *the root of the mean of the square*, cannot be computed without some averaging to obtain the *mean* function. The LTC1966 true RMS-to-DC converter utilizes a single capacitor on the output to do the low frequency averaging required for RMS-to-DC conversion. To give an accurate measure of a dynamic waveform, the averaging must take place over a sufficiently long interval to average, rather than track, the lowest frequency signals of interest. For a single averaging capacitor, the accuracy at low frequencies is depicted in Figure 6.

Figure 6 depicts the so-called DC error that results at a given combination of input frequency and filter capacitor values[1]. It is appropriate for most applications, in which the output is fed to a circuit with an inherently band limited frequency response, such as a dual slope/integrating A/D converter, a ΔΣ A/D converter or even a mechanical analog meter.

However, if the output is examined on an oscilloscope with a very low frequency input, the incomplete averaging will be seen, and this ripple will be larger than the error depicted in Figure 6. Such an output is depicted in Figure 7. The ripple is at twice the frequency of the input because of the computation of the square of the input. The typical values shown, 5% peak ripple with 0.05% DC error, occur with C_{AVE} = 1µF and f_{INPUT} = 10Hz.

If the application calls for the output of the LTC1966 to feed a sampling or Nyquist A/D converter (or other circuitry that will not average out this double frequency ripple) a larger averaging capacitor can be used. This trade-off is depicted in Figure 8. The peak ripple error can also be reduced by additional lowpass filtering after the LTC1966, but the simplest solution is to use a larger averaging capacitor.

[1]This frequency dependent error is in addition to the static errors that affect all readings and are therefore easy to trim or calibrate out. The Error Analyses section to follow discusses the effect of static error terms.

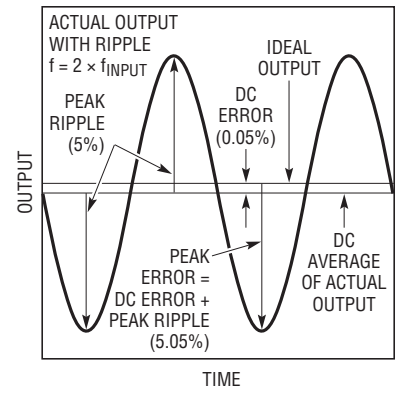


Figure 7. Output Ripple Exceeds DC Error

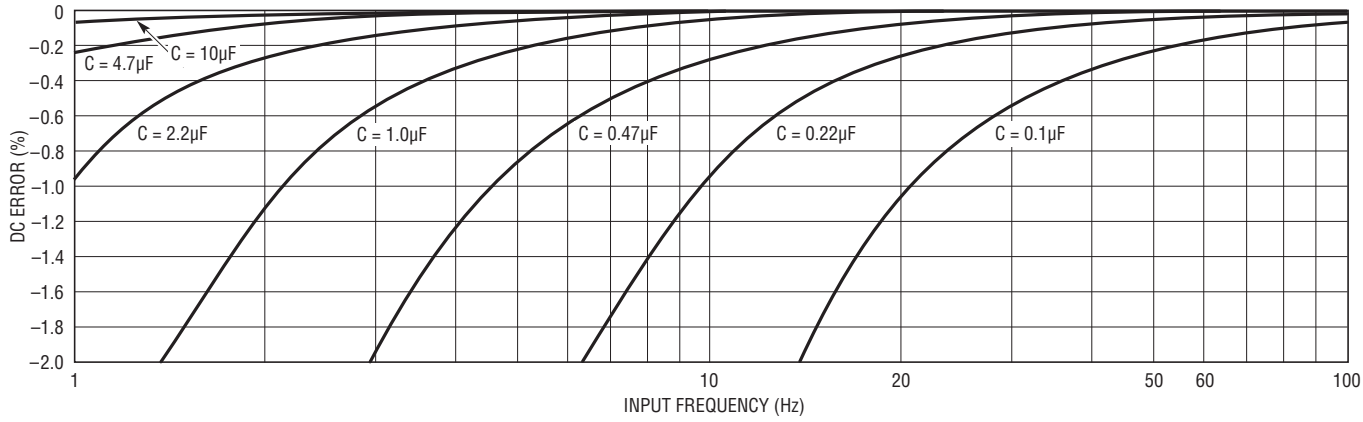


Figure 6. DC Error vs Input Frequency

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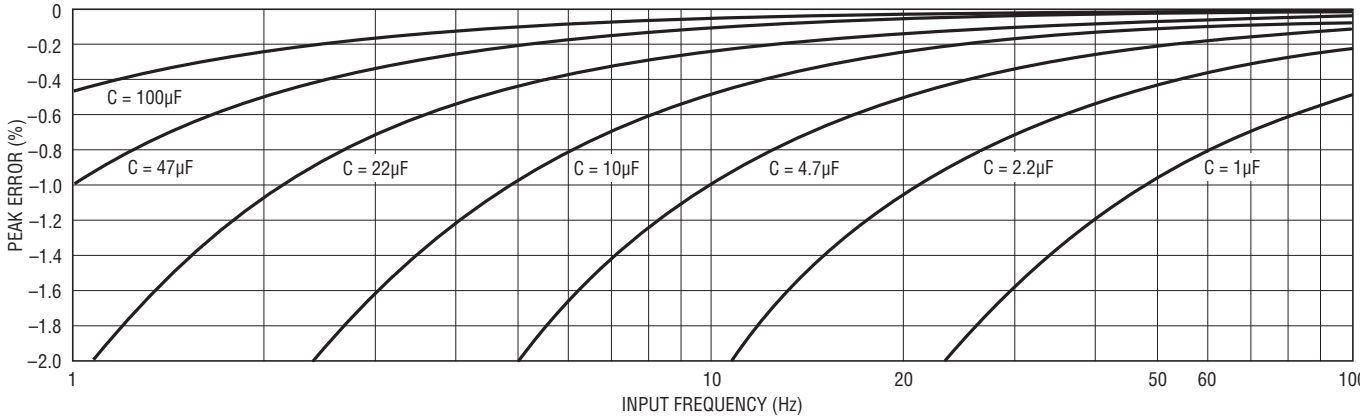


Figure 8. Peak Error vs Input Frequency with One Cap Averaging

A 1µF capacitor is a good choice for many applications. The peak error at 50Hz/60Hz will be <1% and the DC error will be <0.1% with frequencies of 10Hz or more.

Note that both Figure 6 and Figure 8 assume AC-coupled waveforms with a crest factor less than 2, such as sine waves or triangle waves. For higher crest factors and/or AC + DC waveforms, a larger C_{AVE} will generally be required. See Crest Factor and AC + DC Waveforms.

Capacitor Type Selection

The LTC1966 can operate with many types of capacitors. The various types offer a wide array of sizes, tolerances, parasitics, package styles and costs.

Ceramic chip capacitors offer low cost and small size, but are not recommended for critical applications. The value stability over voltage and temperature is poor with many types of ceramic dielectrics. This will not cause an RMS-to-DC accuracy problem except at low frequencies, where it can aggravate the effects discussed in the previous section. If a ceramic capacitor is used, it may be necessary to use a much higher nominal value in order to assure the low frequency accuracy desired.

Another parasitic of ceramic capacitors is leakage, which is again dependent on voltage and particularly temperature. If the leakage is a constant current leak, the I • R drop of the leak multiplied by the output impedance of the LTC1966 will create a constant offset of the output voltage. If the leak is Ohmic, the resistor divider formed with the LTC1966 output impedance will cause a gain error. For <0.1% gain accuracy degradation, the parallel impedance of the capacitor leakage will need to be >1000 times the LTC1966 output impedance. Accuracy at this level can be hard to achieve with a ceramic capacitor, particularly with a large value of capacitance and at high temperature.

For critical applications, a film capacitor, such as metalized polyester, will be a much better choice. Although more expensive, and larger for a given value, the value stability and low leakage make metal film capacitors a trouble free choice.

With any type of capacitor, the self resonance of the capacitor can be an issue with the switched capacitor LTC1966. If the self resonant frequency of the averaging capacitor is 1MHz or less, a second smaller capacitor should be added in parallel to reduce the impedance seen by the LTC1966 output stage at high frequencies. A capacitor 100 times smaller than the averaging capacitor will typically be small enough to be a low cost ceramic with a high quality dielectric such as X7R or NPO/COG.

Input Connections

The LTC1966 input is differential and DC coupled. The LTC1966 responds to the RMS value of the differential voltage between Pin 2 and Pin 3, including the DC portion of that difference. However, there is no DC-coupled path from the inputs to ground. Therefore, at least one of the two inputs must be connected with a DC return path to ground.

Both inputs must be connected to something. If either input is left floating, a zero volt output will result.

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For single-ended DC-coupled applications, simply connect one of the two inputs (they are interchangeable) to the signal, and the other to ground. This will work well for dual supply configurations, but for single supply configurations it will only work well for unipolar input signals. The LTC1966 input voltage range is from rail-to-rail, and when the input is driven above V_{DD} or below V_{SS} (ground for single supply operation) the gain and offset errors will increase substantially after just a few hundred millivolts of overdrive. Fortunately, most single supply circuits measuring a DC-coupled RMS value will include some reference voltage other than ground, and the second LTC1966 input can be connected to that point.

For single-ended AC-coupled applications, Figure 9 shows three alternate topologies. The first one, shown in Figure 9a uses a coupling capacitor to one input while the other is grounded. This will remove the DC voltage difference from the input to the LTC1966, and it will therefore not be part of the resulting output voltage. Again, this connection will work well with dual supply configurations, but in single supply configurations it will be necessary to raise the voltage on the grounded input to assure that the signal at the active input stays within the range of V_{SS} to V_{DD}. If there is already a suitable voltage reference available, connect the second input to that point. If not, a midsupply voltage can be created with two resistors as shown in Figure 9b.

Finally, if the input voltage is known to be between V_{SS} and V_{DD}, it can be AC-coupled by using the configuration shown in Figure 9c. Whereas the DC return path was provided through Pin 3 in Figures 9a and 9b, in this case, the return path is provided on Pin 2, through the input signal voltages. The switched capacitor action between the two input pins of the LTC1966 will cause the voltage on the coupling capacitor connected to the second input to follow the DC average of the input voltage.

For differential input applications, connect the two inputs to the differential signal. If AC coupling is desired, one of the two inputs can be connected through a series capacitor.

In all of these connections, to choose the input coupling capacitor, C_C, calculate the low frequency coupling time constant desired, and divide by the LTC1966 differential input impedance. Because the LTC1966 input impedance is about 100 times its output impedance, this capacitor is typically much smaller than the output averaging capacitor. Its requirements are also much less stringent, and a ceramic chip capacitor will usually suffice.

Output Connections

The LTC1966 output is differentially, but not symmetrically, generated. That is to say, the RMS value that the LTC1966 computes will be generated on the output (Pin 5) relative to the output return (Pin 6), but these two pins are not interchangeable. For most applications, Pin 6 will be tied to ground (Pin 1), and this will result in the best accuracy. However, Pin 6 can be tied to any voltage between V_{SS} (Pin 4) and V_{DD} (Pin 7) less the maximum output voltage swing desired. This last restriction keeps V_{OUT} itself (Pin 5) within the range of V_{SS} to V_{DD}. If a reference level other than ground is used, it should be a low impedance, both AC and DC, for proper operation of the LTC1966.

Use of a voltage in the range of $V_{DD} - 1V$ to $V_{DD} - 1.3V$ can lead to errors due to the switch dynamics as the NMOS transistor is cut off. For this reason, it is recommended that OUT RTN = 0V if V_{DD} is $\leq 3V$.

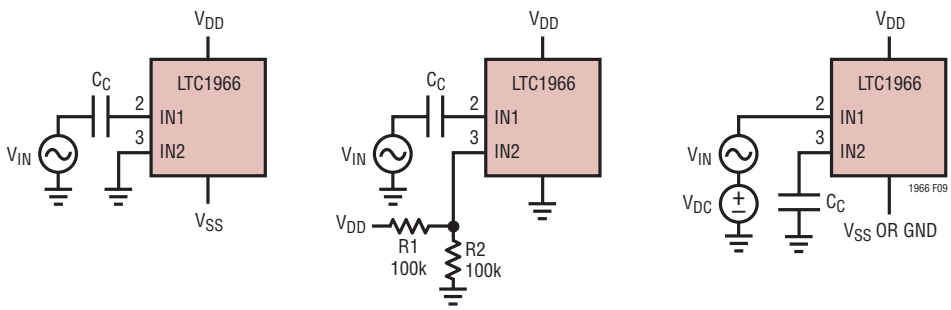


Figure 9. Single-Ended AC-Coupled Input Connection Alternatives

APPLICATIONS INFORMATION

In any configuration, the averaging capacitor should be connected between Pins 5 and 6. The LTC1966 RMS DC output will be a positive voltage created at V_{OUT} (Pin 5) with respect to OUT RTN (Pin 6).

Power Supply Bypassing

The LTC1966 is a switched capacitor device, and large transient power supply currents will be drawn as the switching occurs. For reliable operation, standard power supply bypassing must be included. For single supply operation, a 0.01µF capacitor from V_{DD} (Pin 7) to GND (Pin 1) located close to the device will suffice. For dual supplies, add a second 0.01µF capacitor from V_{SS} (Pin 4) to GND (Pin 1), located close to the device. If there is a good quality ground plane available, the capacitors can go directly to that instead. Power supply bypass capacitors can, of course, be inexpensive ceramic types.

The sampling clock of the LTC1966 operates at approximately 200kHz, and most operations repeat at a rate of 100kHz. If this internal clock becomes synchronized to a multiple or submultiple of the input frequency, significant conversion error could occur. This is particularly important when frequencies exceeding 10kHz can be injected into the LTC1966 via supply or ground bounce. To minimize this possibility, capacitive bypassing is recommended on both supplies with capacitors placed immediately adjacent to the LTC1966. For best results, the bypass capacitors should be separately routed from Pin 7 to Pin 1, and from Pin 4 to Pin 1.

The LTC1966 needs at least 2.7V for its power supply, more for dual supply configurations. The range of allowable negative supply voltages (V_{SS}) vs positive supply voltages (V_{DD}) is shown in Figure 10. Mathematically, the V_{SS} constraint is:

$$-3 \bullet (V_{DD} - 2.7V) \leq V_{SS} \leq GND$$

The LTC1966 has internal ESD absorption devices, which are referenced to the V_{DD} and V_{SS} supplies. For effective in-circuit ESD immunity, the V_{DD} and V_{SS} pins must be connected to a low external impedance. This can be accomplished with low impedance power planes or simply with the recommended 0.01µF decoupling to ground on each supply.

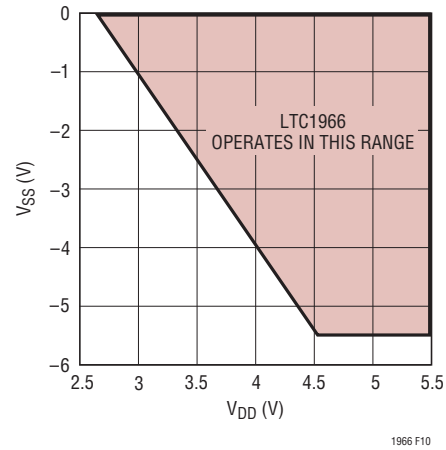


Figure 10. V_{SS} Limits vs V_{DD}

Up and Running!

If you have followed along this far, you should have the LTC1966 up and running by now! Don't forget to enable the device by grounding Pin 8, or driving it with a logic low.

Keep in mind that the LTC1966 output impedance is fairly high, and that even the standard 10MΩ input impedance of a digital multimeter (DMM) or a 10× scope probe will load down the output enough to degrade its typical gain error of 0.1%. In the end application circuit, either a buffer or another component with an extremely high input impedance (such as a dual slope integrating ADC) should be used. For laboratory evaluation, it may suffice to use a bench top DMM with the ability to disconnect the 10MΩ shunt.

If you are still having trouble, it may be helpful to skip ahead a few pages and review the Troubleshooting Guide.

What About Response Time?

With a large value averaging capacitor, the LTC1966 can easily perform RMS-to-DC conversion on low frequency signals. It compares quite favorably in this regard to prior generation products because nothing about the ΔΣ circuitry is temperature sensitive. So the RMS result doesn't get distorted by signal driven thermal fluctuations like a log/antilog circuit output does.

However, using large value capacitors results in a slow response time. Figure 11 shows the rising and falling step responses with a 1µF averaging capacitor. Although they both appear at first glance to be standard exponential

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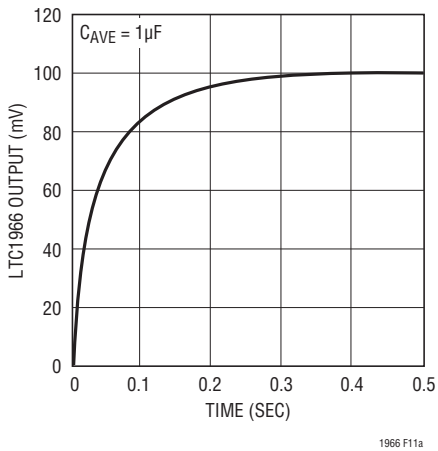


Figure 11a. LTC1966 Rising Edge with C_{AVE} = 1µF

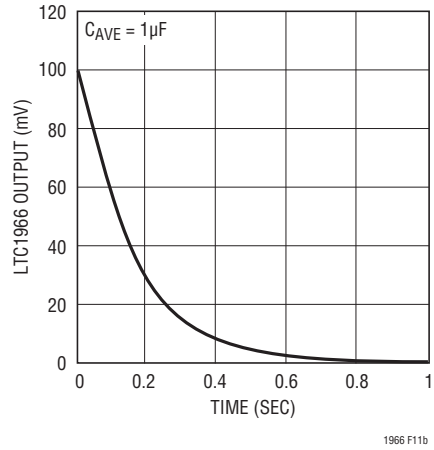


Figure 11b. LTC1966 Falling Edge with C_{AVE} = 1µF

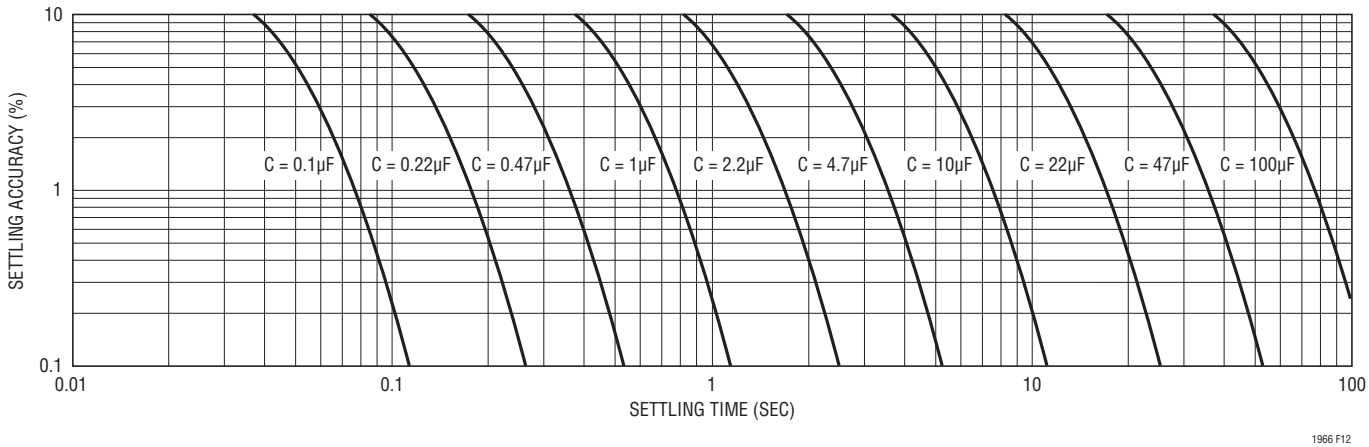


Figure 12. LTC1966 Settling Time with One Cap Averaging

decay type settling, they are not. This is due to the nonlinear nature of an RMS-to-DC calculation. Also note the change in the time scale between the two; the rising edge is more than twice as fast to settle to a given accuracy. Again this is a necessary consequence of RMS-to-DC calculation.[2]

Although shown with a step change between 0mV and 100mV, the same response shapes will occur with the LTC1966 for ANY step size. This is in marked contrast to prior generation log/antilog RMS-to-DC converters, whose averaging time constants are dependent on the signal level, resulting in excruciatingly long waits for the output to go to zero.

The shape of the rising and falling edges will be dependent on the total percent change in the step, but for less than the 100% changes shown in Figure 11, the responses will be less distorted and more like a standard exponential decay. For example, when the input amplitude is changed from 100mV to 110mV (+10%) and back (–10%), the step responses are essentially the same as a standard exponential rise and decay between those two levels. In such cases, the time constant of the decay will be in between that of the rising edge and falling edge cases of Figure 11. Therefore, the worst case is the falling edge response as it goes to zero, and it can be used as a design guide.

Figure 12 shows the settling accuracy vs settling time for a variety of averaging capacitor values. If the capacitor value previously selected (based on error requirements) gives an acceptable settling time, your design is done.

[2]To convince oneself of this necessity, consider a pulse train of 50% duty cycle between 0mV and 100mV. At very low frequencies, the LTC1966 will essentially track the input. But as the input frequency is increased, the average result will converge to the RMS value of the input. If the rise and fall characteristics were symmetrical, the output would converge to 50mV. In fact though, the RMS value of a 100mV DC-coupled 50% duty cycle pulse train is 70.71mV, which the asymmetrical rise and fall characteristics will converge to as the input frequency is increased.

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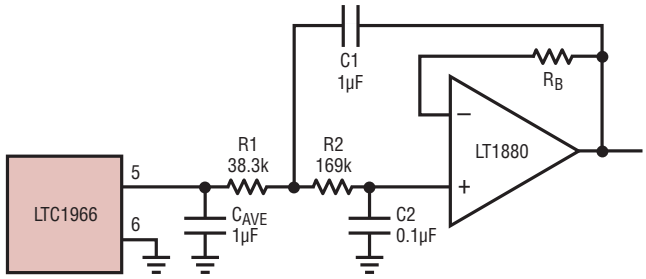
But with 100µF, the settling time to even 10% is a full 38 seconds, which is a long time to wait. What can be done about such a design? If the reason for choosing 100µF is to keep the DC error with a 75mHz input less than 0.1%, the answer is: not much. The settling time to 1% of 76 seconds is just 5.7 cycles of this extremely low frequency. Averaging very low frequency signals takes a long time.

However, if the reason for choosing 100µF is to keep the peak error with a 10Hz input less than 0.05%, there is another way to achieve that result with a much improved settling time.

Reducing Ripple with a Post Filter

The output ripple is always much larger than the DC error, so filtering out the ripple can reduce the peak error substantially, without the large settling time penalty of simply increasing the averaging capacitor.

Figure 13 shows a basic 2nd order post filter, for a net 3rd order filtering of the LTC1966 RMS calculation. It uses the 85kΩ output impedance of the LTC1966 as the first resistor of a 3rd order Sallen-Key active RC filter. This topology features a buffered output, which can be desirable depending on the application. However, there are disadvantages to this topology, the first of which is that the op amp input voltage and current errors directly degrade the effective LTC1966 V_{OOS}. The table inset in Figure 13 shows these errors for four of Linear Technology's op amps.



OP AMP	LT1494	LT1880	LT1077	LT2050
LTC1966 V_{OOS}	±200µV			
V_{IOS}	±375µV	±150µV	±60µV	±3µV
$I_{B/OS}$ • R	±73µV	±329µV	±329µV	±27µV
TOTAL OFFSET	±648µV	±679µV	±589µV	±230µV
R_B VALUE	294k	SHORT	294k	SHORT
I_{SQ}	1µA	1.2mA	48µA	750µA

Figure 13. Buffered Post Filter

A second disadvantage is that the op amp output has to operate over the same range as the LTC1966 output, including ground, which in single supply applications is the negative supply. Although the LTC1966 output will function fine just millivolts from the rail, most op amp output stages (and even some input stages) will not. There are at least two ways to address this. First of all, the op amp can be operated split supply if a negative supply is available. Just the op amp would need to do so; the LTC1966 can remain single supply. A second way to address this issue is to create a signal reference voltage a half volt or so above ground. This is most attractive when the circuitry that follows has a differential input, so that the tolerance of the signal reference is not a concern. To do this, tie all three ground symbols shown in Figure 13 to the signal reference, as well as to the differential return for the circuitry that follows.

Figure 14 shows an alternative 2nd order post filter, for a net 3rd order filtering of the LTC1966 RMS calculation. It also uses the 85kΩ output impedance of the LTC1966 as the first resistor of a 3rd order active RC filter, but this topology filters without buffering so that the op amp DC error characteristics do not affect the output. Although the output impedance of the LTC1966 is increased from 85kΩ to 285kΩ, this is not an issue with an extremely high input impedance load, such as a dual slope integrating ADC like the ICL7106. And it allows a generic op amp to be used, such as the SOT-23 one shown. Furthermore, it easily works on a single supply rail by tying the noninverting input of the op amp to a low noise reference as optionally shown. This reference will not change the DC voltage at the circuit output, although it does become the AC ground for the filter, thus the (relatively) low noise requirement.

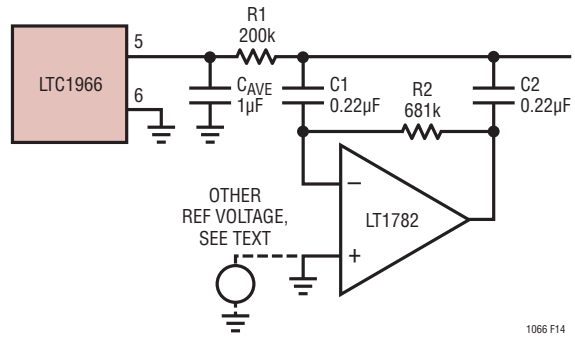


Figure 14. DC Accurate Post Filter

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Step Responses with a Post Filter

Both of the post filters, shown in Figures 13 and 14, are optimized for additional filtering with clean step responses. The 85kΩ output impedance of the LTC1966 working into a 1µF capacitor forms a 1st order LPF with a –3dB frequency of ~1.8Hz. The two filters have 1µF at the LTC1966 output for easy comparison with a 1µF only case, and both have the same relative (Bessel-like) shape. However, because of the topological differences of pole placements between the various components within the two filters, the net effective bandwidth for Figure 13 is slightly higher (≈1.2 • 1.8 ≈ 2.1Hz) than with 1µF alone, while the bandwidth for Figure 14 is somewhat lower (≈0.7 • 1.8 ≈ 1.3Hz) than with 1µF alone. To adjust the bandwidth of either of them, simply scale all the capacitors by a common multiple, and leave the resistors unchanged.

The step responses of the LTC1966 with 1µF only and with the two post filters are shown in Figure 15. This is the rising edge RMS output response to a 10Hz input starting at t = 0. Although the falling edge response is the worst case for settling, the rising edge illustrates the ripple that these post filters are designed to address, so the rising edge makes for a better intuitive comparison.

The initial rise of the LTC1966 will have enhanced slew rates with DC and very low frequency inputs due to saturation effects in the ΔΣ modulator. This is seen in Figure 15 in two ways. First, the 1µF only output is seen to rise very quickly in the first 40ms. The second way this effect shows up is that the post filter outputs have a modest overshoot, on the order of 3mV to 4mV, or 3% to 4%. This is only an issue with input frequency bursts at 50Hz or less, and even with the overshoot, the settling to a given level of accuracy improves due to the initial speedup.

As predicted by Figure 6, the DC error with 1µF is well under 1mV and is not noticeable at this scale. However, as predicted by Figure 8, the peak error with the ripple from a 10Hz input is much larger, in this case about 5mV. As can be clearly seen, the post filters reduce this ripple. Even the wider bandwidth of Figure 13's filter is seen to cut the ripple down substantially (to <1mV) while the settling to 1% happens faster. With the narrower bandwidth of Figure 14's filter, the step response is somewhat slower, but the double frequency output ripple is just 180µV.

Figure 16 shows the step response of the same three cases with a burst of 60Hz rather than 10Hz. With 60Hz, the initial portion of the step response is free of the boost seen in Figure 15 and the two post filter responses have less than 1% overshoot. The 1µF only case still has noticeable 120Hz ripple, but both filters have removed all detectable ripple on this scale. This is to be expected; the first order filter will reduce the ripple about 6:1 for a 6:1 change in frequency, while the third order filters will reduce the ripple about 6^3:1 or 216:1 for a 6:1 change in frequency.

Again, the two filter topologies have the same relative shape, so the step response and ripple filtering trade-offs of the two are the same, with the same performance of each possible with the other by scaling it accordingly. Figures 17 and 18 show the peak error vs. frequency for a selection of capacitors for the two different filter topologies. To keep the clean step response, scale all three capacitors

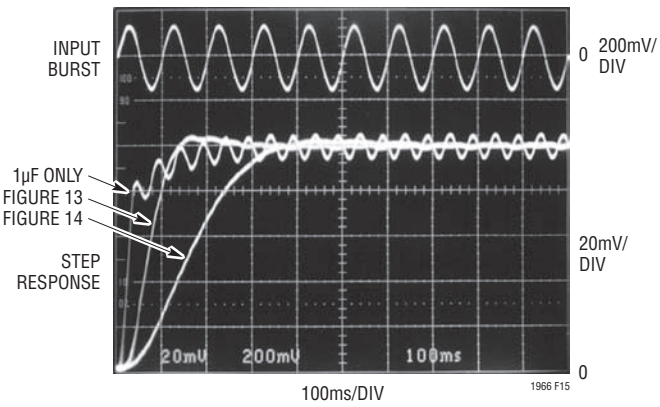


Figure 15. Step Responses with 10Hz Burst

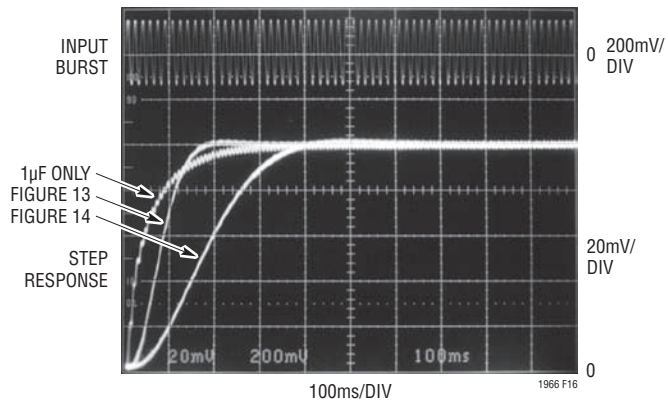


Figure 16. Step Responses with 60Hz Burst

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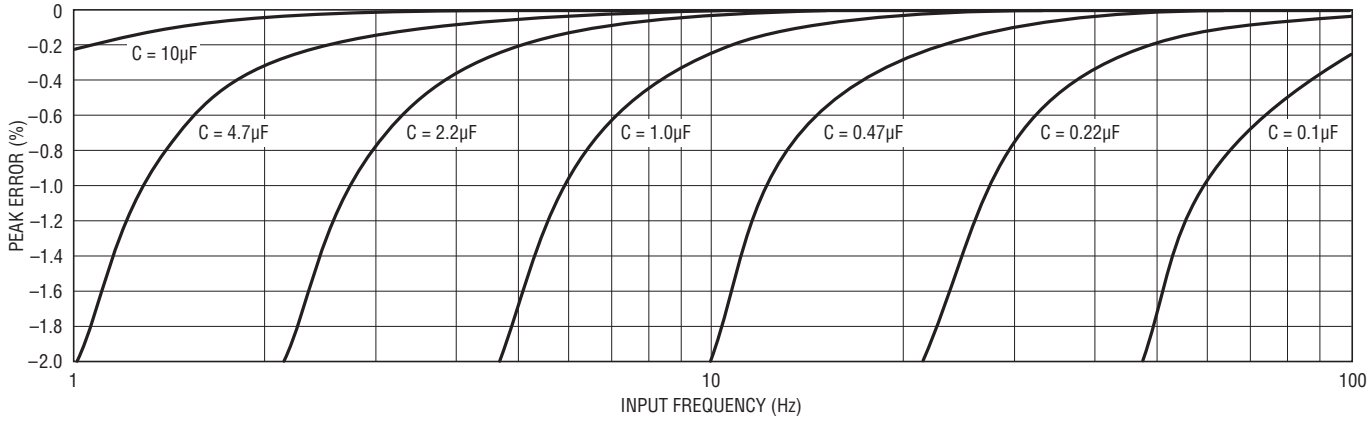


Figure 17. Peak Error vs Input Frequency with Buffered Post Filter

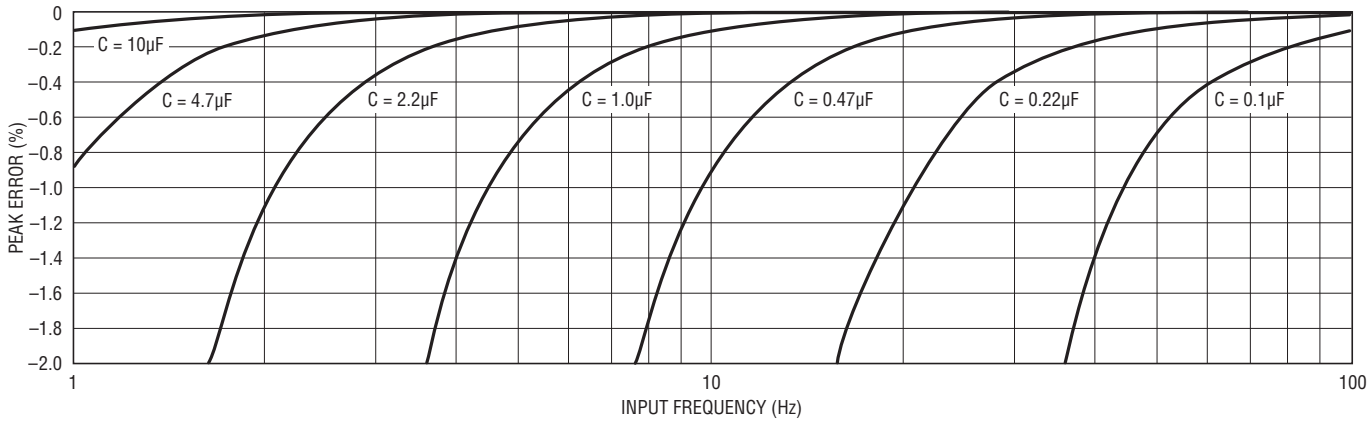


Figure 18. Peak Error vs Input Frequency with DC Accurate Post Filter

within the filter. Scaling the buffered topology of Figure 13 is simple because the capacitors are in a 10:1:10 ratio. Scaling the DC accurate topology of Figure 14 can be done with standard value capacitors; one decade of scaling is shown in Table 2.

Table 2. One Decade of Capacitor Scaling for Figure 14 with EIA Standard Values

C_{AVE}	$C_1 = C_2 =$
1µF	0.22µF
1.5µF	0.33µF
2.2µF	0.47µF
3.3µF	0.68µF
4.7µF	1µF
6.8µF	1.5µF

Figures 19 and 20 show the settling time versus settling accuracy for the buffered and DC accurate post filters, respectively. The different curves represent different scalings of the filters, as indicated by the C_{AVE} value. These are comparable to the curves in Figure 12 (single capacitor case), with somewhat less settling time for the buffered post filter, and somewhat more settling time for the DC accurate post filter. These differences are due to the change in overall bandwidth as mentioned earlier.

The other difference is the settling behavior of the filters below the 1% level. Unlike the case of a 1st order filter, any 3rd order filter can have overshoot and ringing. The filter designs presented here have minimal overshoot and ringing, but are somewhat sensitive to component mismatches. Even the ±12% tolerance of the LTC1966 output impedance can be enough to cause some ringing. The dashed lines indicate what can happen when ±5% capacitors and ±1% resistors are used.

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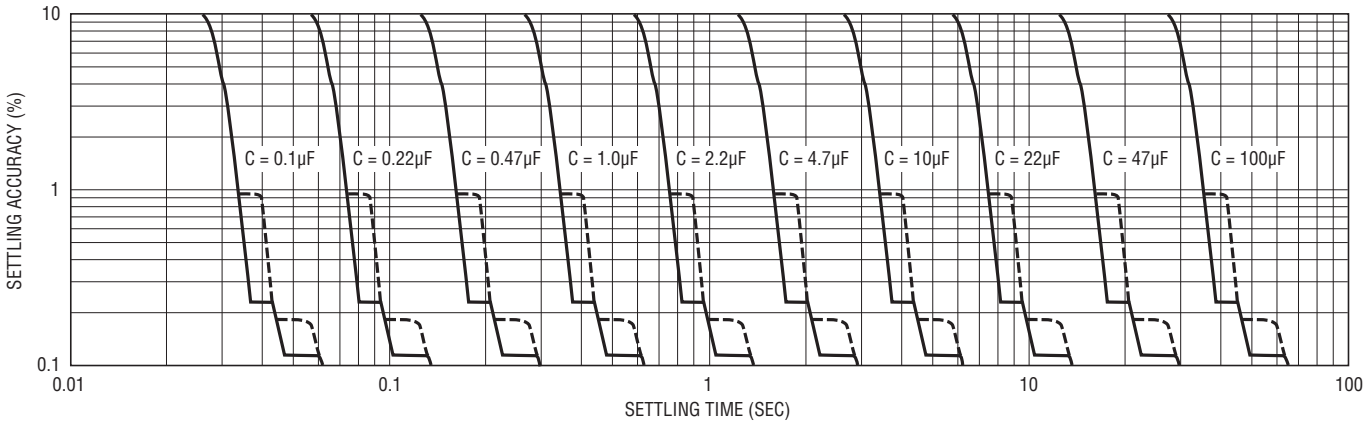


Figure 19. Settling Time with Buffered Post Filter

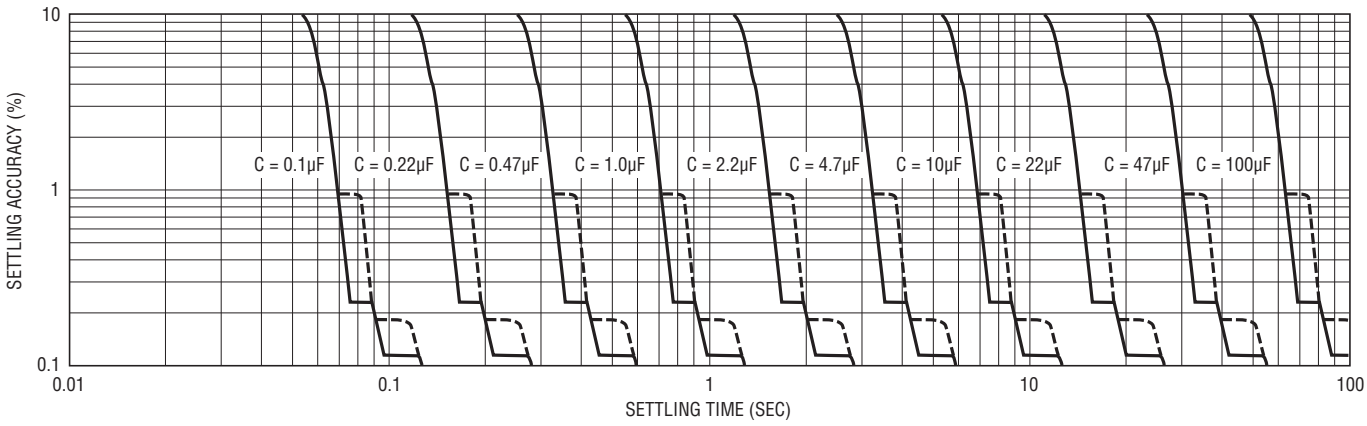


Figure 20. Settling Time with DC Accurate Post Filter

Although the settling times for the post filtered configurations shown on Figures 19 and 20 are not that much different from those with a single capacitor, the point of using a post filter is that the settling times are far better for a given level peak error. The filters dramatically reduce the low frequency averaging ripple with far less impact on settling time.

Crest Factor and AC + DC Waveforms

In the preceding discussion, the waveform was assumed to be AC-coupled, with a modest crest factor. Both assumptions ease the requirements for the averaging capacitor. With an AC-coupled sine wave, the calculation engine squares the input, so the averaging filter that follows is required to filter twice the input frequency, making its job easier. But with a sinewave that includes DC offset, the square of the input has frequency content at the input frequency and the filter must average out that lower frequency. So with AC + DC waveforms, the required value for C_{AVE} should be based on half of the lowest input frequency, using the same design curves presented in Figures 6, 8, 17 and 18.

Crest factor, which is the peak to RMS ratio of a dynamic signal, also effects the required C_{AVE} value. With a higher crest factor, more of the energy in the signal is concentrated into a smaller portion of the waveform, and the averaging has to ride out the long lull in signal activity. For busy waveforms, such as a sum of sine waves, ECG traces or SCR chopped sine waves, the required value for C_{AVE} should be based on the lowest fundamental input frequency divided as such:

$$f_{DESIGN} = \frac{f_{INPUT(MIN)}}{3 \bullet \sqrt{CF - \sqrt{2}}}$$

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using the same design curves presented in Figures 6, 8, 17 and 18. For the worst-case of square top pulse trains, that are always either zero volts or the peak voltage, base the selection on the lowest fundamental input frequency divided by twice as much:

$$f_{DESIGN} = \frac{f_{INPUT(MIN)}}{6 \bullet \sqrt{CF - \sqrt{2}}}$$

The effects of crest factor and DC offsets are cumulative. So for example, a 10% duty cycle pulse train from $0V_{PEAK}$ to $1V_{PEAK}$ (CF = $\sqrt{10}$ = 3.16) repeating at 16.67ms (60Hz) input is effectively only 30Hz due to the DC asymmetry and is effectively only:

$$f_{DESIGN} = \frac{30}{6 \bullet \sqrt{3.16 - \sqrt{2}}} = 3.78Hz$$

for the purposes of Figures 6, 8, 17 and 18.

Obviously, the effect of crest factor is somewhat simplified above given the factor of 2 difference based on a subjective description of the waveform type. The results will vary somewhat based on actual crest factor and waveform dynamics and the type of filtering used. The above method is conservative for some cases and about right for others.

The LTC1966 works well with signals whose crest factor is 4 or less. At higher crest factors, the internal ΔΣ modulator will saturate, and results will vary depending on the exact frequency, shape and (to a lesser extent) amplitude of the input waveform. The output voltage could be higher or lower than the actual RMS of the input signal.

The ΔΣ modulator may also saturate when signals with crest factors less than 4 are used with insufficient averaging. This will only occur when the output droops to less than 1/4 of the input voltage peak. For instance, a DC-coupled pulse train with a crest factor of 4 has a duty cycle of 6.25% and a $1V_{PEAK}$ input is $250mV_{RMS}$. If this input is 50Hz, repeating every 20ms, and C_{AVE} = 1μF, the output will droop during the inactive 93.75% of the waveform. This droop is calculated as:

$$V_{MIN} = \frac{V_{RMS}}{2}\left(1 - e^{-\left(\frac{\text{INACTIVE TIME}}{2 \bullet Z_{OUT} \bullet C_{AVE}}\right)}\right)$$

For the LTC1966, whose output impedance (Z_{OUT}) is 85kΩ, this droop works out to –5.22%, so the output would be reduced to 237mV at the end of the inactive portion of the input. When the input signal again climbs to $1V_{PEAK}$, the peak/output ratio is 4.22.

With C_{AVE} = 10μF, the droop is only –0.548% to 248.6mV and the peak/output ratio is just 4.022, which the LTC1966 has enough margin to handle without error.

For crest factors less than 3.5, the selection of C_{AVE} as previously described should be sufficient to avoid this droop and modulator saturation effect. But with crest factors above 3.5, the droop should also be checked for each design.

Error Analyses

Once the RMS-to-DC conversion circuit is working, it is time to take a step back and do an analysis of the accuracy of that conversion. The LTC1966 specifications include three basic static error terms, V_{OOS}, V_{IOS} and GAIN. The output offset is an error that simply adds to (or subtracts from) the voltage at the output. The conversion gain of the LTC1966 is nominally 1.000 V_{DCOUT}/V_{RMSIN} and the gain error reflects the extent to which this conversion gain is not perfectly unity. Both of these affect the results in a fairly obvious way.

Input offset on the other hand, despite its conceptual simplicity, effects the output in a nonobvious way. As its name implies, it is a constant error voltage that adds directly with the input. And it is the sum of the input and V_{IOS} that is RMS converted.

This means that the effect of V_{IOS} is warped by the nonlinear RMS conversion. With 0.2mV (typ) V_{IOS}, and a $200mV_{RMS}$ AC input, the RMS calculation will add the DC and AC terms in an RMS fashion and the effect is negligible:

$$V_{OUT} = \sqrt{(200mV\ AC)^2 + (0.2mV\ DC)^2}$$
$$= 200.0001mV$$
$$= 200mV + 1/2ppm$$

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But with 10× less AC input, the error caused by V_{IOS} is 100× larger:

$$V_{OUT} = \sqrt{(20mV\ AC)^2 + (0.2mV\ DC)^2}$$
$$= 20.001mV$$
$$= 20mV + 50ppm$$

This phenomena, although small, is one source of the LTC1966's residual nonlinearity.

On the other hand, if the input is DC-coupled, the input offset voltage adds directly. With +200mV and a +0.2mV V_{IOS}, a 200.2mV output will result, an error of 0.1% or 1000ppm. With DC inputs, the error caused by V_{IOS} can be positive or negative depending if the two have the same or opposing polarity.

The total conversion error with a sine wave input using the typical values of the LTC1966 static errors is computed as follows:

$$V_{OUT} = (\sqrt{(500mV\ AC)^2 + (0.2mV\ DC)^2}) \bullet 1.001 + 0.1mV$$
$$= 500.600mV$$
$$= 500mV + 0.120\%$$

$$V_{OUT} = (\sqrt{(50mV\ AC)^2 + (0.2mV\ DC)^2}) \bullet 1.001 + 0.1mV$$
$$= 50.150mV$$
$$= 50mV + 0.301\%$$

$$V_{OUT} = (\sqrt{(5mV\ AC)^2 + (0.2mV\ DC)^2}) \bullet 1.001 + 0.1mV$$
$$= 5.109mV$$
$$= 5mV + 2.18\%$$

As can be seen, the gain term dominates with large inputs, while the offset terms become significant with smaller inputs. In fact, 5mV is the minimum RMS level needed to keep the LTC1966 calculation core functioning normally, so this represents the worst-case of usable input levels.

Using the worst-case values of the LTC1966 static errors, the total conversion error is:

$$V_{OUT} = (\sqrt{(500mV\ AC)^2 + (0.8mV\ DC)^2}) \bullet 1.003 + 0.2mV$$
$$= 501.70mV$$
$$= 500mV + 0.340\%$$

$$V_{OUT} = (\sqrt{(50mV\ AC)^2 + (0.8mV\ DC)^2}) \bullet 1.003 + 0.2mV$$
$$= 50.356mV$$
$$= 50mV + 0.713\%$$

$$V_{OUT} = (\sqrt{(5mV\ AC)^2 + (0.8mV\ DC)^2}) \bullet 1.003 + 0.2mV$$
$$= 5.279mV$$
$$= 5mV + 5.57\%$$

These static error terms are in addition to dynamic error terms that depend on the input signal. See the Design Cookbook for a discussion of the DC conversion error with low frequency AC inputs. The LTC1966 bandwidth limitations cause additional errors with high frequency inputs. Another dynamic error is due to crest factor. The LTC1966 performance versus crest factor is shown in the Typical Performance Characteristics.

Monotonicity and Linearity

The LTC1966, like all implicit RMS-to-DC convertors (Figure 3), has a division with the output in the denominator. This works fine most of the time, but when the output is zero or near zero this becomes problematic. The LTC1966 has multiple switched capacitor amplifier stages, and depending on the different offsets and their polarity, the DC transfer curve near zero input can take a few different forms, as shown in the Typical Performance Characteristics graph titled DC Transfer Function Near Zero.

Some units (about 1 of every 16) will even be well behaved with a transfer function that is the upper half of a unit rectangular hyperbola with a focal point on the y-axis of a few millivolts.[3] For AC inputs, these units will have a monotonic transfer function all the way down to zero input.

The LTC1966 is trimmed for offsets as small as practical, and the resulting behavior is the best statistical linearity provided the zero region troubles are avoided.

It is possible, and even easy, to force the zero region to be well behaved at the price of additional (though predictable) V_{OOS} and some linearity error. For large enough input signals, this linearity error may be negligible.

[3]In general, every LTC1966 will have a DC transfer function that is essentially a unit rectangular hyperbola (the gain is not always exactly unity, but the gain error is small) with an X- and Y- offset equal to V_{IOS} and V_{OOS}, respectively, until the inputs are small enough that the delta sigma section gets confused. While some units will be the north half of a north south pair, other units will have two upper halfs of the conjugate, east west, hyperbolas. The circuit of Figure 23 will assure a continuous transfer function.

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To do this, inject current into the output. As shown in Figure 21, the charge pump output impedance is 170kΩ, with the computational feedback cutting the closed loop output impedance to the 85kΩ specification. By injecting 30nA of current into this 170Ω, with zero input, a 5mV offset

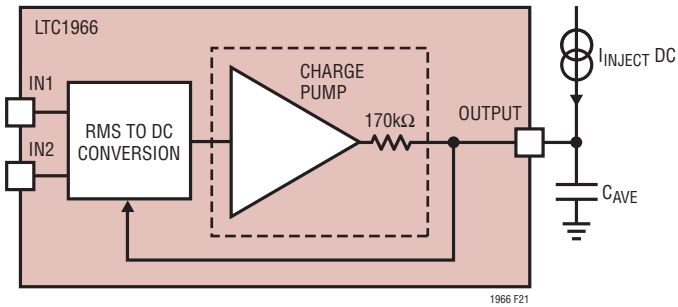


Figure 21. Behavioral Block Diagram of LTC1966

is created at the output feedback point, which is sufficient to overcome the 5mV minimum signal level. With large enough input signals, the computational feedback cuts the output impedance to 85kΩ so the transfer function asymptotes will have an output offset of 2.5mV, as shown in Figure 22. This is the additional, predictable, V_{OOS} that is added, and should be subtracted from the RMS results, either digitally, or by an analog means.

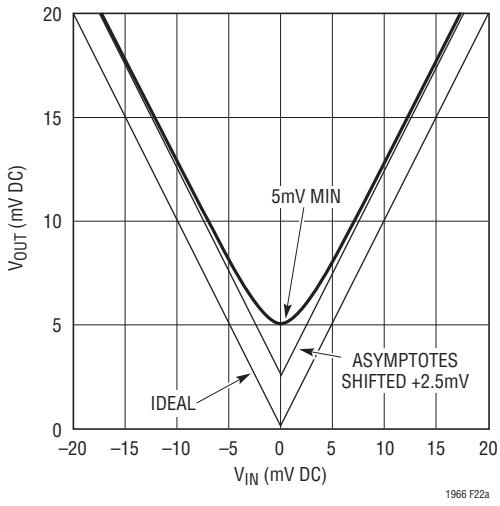


Figure 22a. DC Transfer Function with I_{INJECT} = 30nA

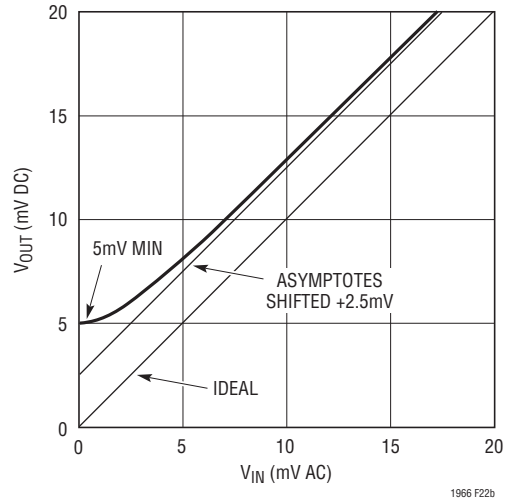


Figure 22b. AC Transfer Function with I_{INJECT} = 30nA

Figure 23 shows an analog implementation of this with the offset and gain errors corrected; only the slight, but necessary, degradation in nonlinearity remains. The circuit works by creating approximately 300mV of bias at the junction of the 10MΩ resistors when the LTC1966's input/output are zero. The 10MΩ resistor to the LTC1966 output therefore feeds in 30nA. The loading of this resistor causes a slight reduction in gain which is corrected, as is the nominal 2.5mV offset, by the LT1494 op amp.

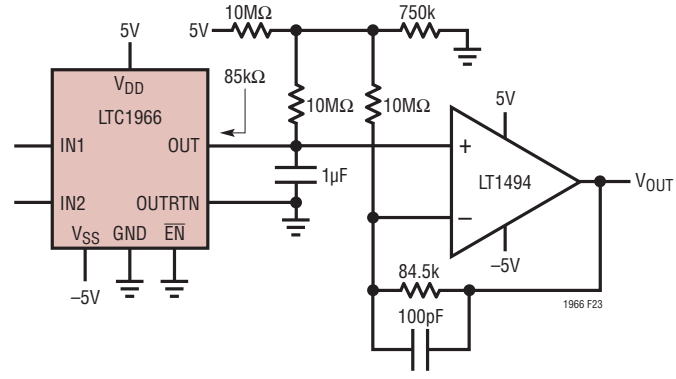


Figure 23. Monotonic AC Response with Offset and Gain Corrected

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The two 10MΩ resistors not connected to the supply can be any value as long as they match and the feed voltage is changed for 30nA injection. The op amp gain is only 1.00845, so the output is dominated by the LTC1966 RMS results, which keeps errors low. With the values shown, the resistors can be ±2% and only introduce ±170ppm of gain error. The 84.5k resistor is the closest match in the 1% EIA values but if the 2% EIA value of 82k were used instead, the gain would only be reduced by 248ppm.

This low error sensitivity is important because the LTC1966 output impedance is 85kΩ ±11.8%, which can create a gain error of ±0.1%; enough to degrade the overall gain accuracy somewhat. This gain variation term is increased with lower value feed resistors, and decreased with higher value feed resistors.

A bigger error caused by the variation of the LTC1966 output impedance is imperfect cancelation of the output offset introduced by the injected current. The offset correction provided by the LT1494 will be based on a consistent 84.5kΩ times the injected current, while the LTC1966 output impedance will vary enough that the output offset will have a ±300µV range about the nominal 2.5mV. If this level of output offset is not acceptable, either system calibration or a potentiometer in the LT1494 feedback may be needed.

If the two 10MΩ feed resistors to the LT1494 have significant mismatch, cancellation of the 2.5mV offset would be further impacted, so it is probably worth paying an extra penny or so for 1% resistors or even the better temperature stability of thin film devices. The 300mV feed voltage is not particularly critical because it is nominally cancelled, but the offset errors due to these resistance mismatches is scaled by that voltage.

Note that the input bias current of the op amp used in Figure 23 is also nominally cancelled, but it will add or subtract to the total current injected into the LTC1966 output. With the 1nA I_{BIAS} of the LT1494 this is negligible. While it is possible to eliminate the feed resistors by using an op amp with a PNP input stage whose I_{BIAS} is 30nA or more, I_{BIAS} is usually only specified for maximum and this circuit needs a minimum of 30nA, therefore such an approach may not always work.

Because the circuit of Figure 23 subtracts the offset created by the injected current, the LT1494 output with zero LTC1966 input will rest at +2.5mV, nominal before offsets, rather then the 5mV seen in Figure 22.

Output Errors Versus Frequency

As mentioned in the Design Cookbook, the LTC1966 performs very well with low frequency and very low frequency inputs, provided a large enough averaging capacitor is used.

However, the LTC1966 will have additional dynamic errors as the input frequency is increased. The LTC1966 is designed for high accuracy RMS-to-DC conversion of signals into the audible range. The input sampling amplifiers have a –3dB frequency of 800kHz or so. However, the switched capacitor circuitry samples the inputs at a modest 100kHz nominal. The response versus frequency is depicted in the Typical Performance Characteristics titled Input Signal Bandwidth. Although there is a pattern to the response versus frequency that repeats every sample frequency, the errors are not overwhelming. This is because LTC1966 RMS calculation is inherently wideband, operating properly with minimal oversampling, or even undersampling, using several proprietary techniques to exploit the fact that the RMS value of an aliased signal is the same as the RMS value of the original signal. However, a fundamental feature of the ΔΣ modulator is that sample estimation noise is shaped such that minimal noise occurs with input frequencies much less than the sampling frequency, but such noise peaks when input frequency reaches half the sampling frequency. Fortunately the LTC1966 output averaging filter greatly reduces this error, but the RMS-to-DC topology frequency shifts the noise to low (baseband) frequencies. So with input frequencies above 5kHz to 10kHz, the output will slowly wander around ±a few percent.

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Input Impedance

The LTC1966 true RMS-to-DC converter utilizes a 2.5pF capacitor to sample the input at a nominal 100kHz sample frequency. This accounts for the 8MΩ input impedance. See Figure 24 for the equivalent analog input circuit. Note however, that the 8MΩ input impedance does not directly affect the input sampling accuracy. For instance, if a 100k source resistance is used to drive the LTC1966, the sampling action of the input stage will drag down the voltage seen at the input pins with small spikes at every sample clock edge as the sample capacitor is connected to be charged. The time constant of this combination is small, 2.5pF • 100kΩ = 250ns, and during the 2.5µs period devoted to sampling, ten time constants elapse. This allows each sample to settle to within 46ppm and it is these samples that are used to compute the RMS value.

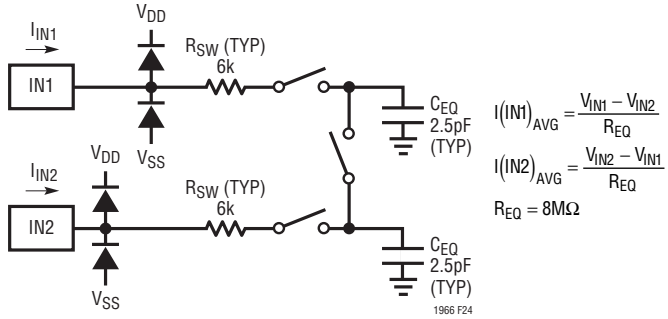


Figure 24. LTC1966 Equivalent Analog Input Circuit

This is a much higher accuracy than the LTC1966 conversion limits, and far better than the accuracy computed via the simplistic resistive divider model:

$$V_{IN} = V_{SOURCE}\frac{R_{IN}}{R_{IN} + R_{SOURCE}}$$

$$= V_{SOURCE}\frac{8M\Omega}{8M\Omega + 100k\Omega}$$

$$= V_{SOURCE} - 1.25\%$$

This resistive divider calculation does give the correct model of what voltage is seen at the input terminals by a parallel load averaged over a several clock cycles, which is what a large shunt capacitor will do—average the current spikes over several clock cycles.

When high source impedances are used, care must be taken to minimize shunt capacitance at the LTC1966 input so as not to increase the settling time. Shunt capacitance of just 2.5pF will double the input settling time constant and the error in the above example grows from 46ppm to 0.67% (6700ppm). A 13pF scope probe will increase the error to almost 20%. As a consequence, it is important to *not* try to filter the input with large input capacitances unless driven by a low impedance. Keep time constant ≪2.5µs.

When the LTC1966 is driven by op amp outputs, whose low DC impedance can be compromised by sharp capacitive load switching, a small series resistor may be added. A 10k resistor will easily settle with the 2.5pF input sampling capacitor to within 1ppm.

These are important points to consider both during design and debug. During lab debug, and even production testing, a high value series resistor to any test point is advisable.

Output Impedance

The LTC1966 output impedance during operation is similarly due to a switched capacitor action. In this case, 59pF of on-chip capacitance operating at 100kHz translates into 170kΩ. The closed loop RMS-to-DC calculation cuts that in half to the nominal 85kΩ specified.

In order to create a DC result, a large averaging capacitor is required. Capacitive loading and time constants are not an issue on the output.

APPLICATIONS INFORMATION

However, resistive loading is an issue and the 10MΩ impedance of a DMM or 10× scope probe will drag the output down by –0.85% typ.

During shutdown, the switching action is halted and a fixed 30k resistor shunts V_{OUT} to OUT RTN so that C_{AVE} is discharged.

Guard Ringing the Output

The LTC1966's combination of precision and high output impedance can present challenges that make the use of a guard ring around the output a good idea for many applications.

As mentioned above, a 10M resistive loading to ground will drag down the gain far more than the specificed gain tolerance. On a printed circuit board, contaminants from solder flux residue to finger grime can create parasitic resistances, which may be very high impedance, but can have deleterious effects on the realized accuracy. As an example, if the output (Pin 5) is routed near V_{SS} (Pin 4) in a ±5V application, a parasitic resistance of 1G (1,000M) is enough to introduce a –425µV output offset error, more than the specified limit of the LTC1966 itself.

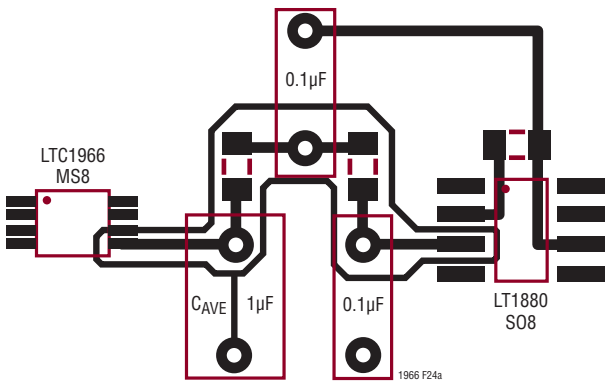


Figure 24a. PCB Layout of Figure 13 with Guard Ring

Use of a guard ring, wherein the LTC1966 output node is completely surrounded by a low impedance voltage, can reduce leakage related errors substantially. The ground ring can be tied to OUTRTN (Pin 6) and should encircle the output (Pin 5), the averaging capacitor terminal, and the destination terminal at the ADC, filter op amp, or whatever else may be next.

Figure 24a shows a sample PCB layout for the circuit of Figure 13, wherein the guard ring trace encloses R1, R2, and the terminals of C1, C2, and the op amp input connected to the high impedance LTC1966 Output. For the circuit of figure 14, the guard ring should enclose R1 and the terminals of C1 and C2, as well as the terminal at the ultimate destination.

Figure 24b shows a sample PCB layout for the circuit of Figure 23. The summing node of the LT1494 has the same high impedance and high accuracy as the LTC1966 output, so here the guard ring encircles both of them. Any leakage between them is benign because the LT1494 forces them to the same nominal voltage.

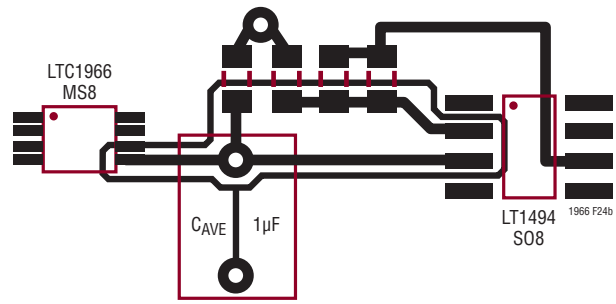


Figure 24b. PCB Layout of Figure 23 with Guard Ring

APPLICATIONS INFORMATION

Interfacing with an ADC

The LTC1966 output impedance and the RMS averaging ripple need to be considered when using an analog-to-digital converter (ADC) to digitize the LTC1966 RMS result.

The simplest configuration is to connect the LTC1966 directly to the input of a type 7106/7136 ADC as shown in Figure 25a. These devices are designed specifically for DVM/DPM use and include display drivers for a 3 1/2 digit LCD segmented display. Using a dual slope conversion, the input is sampled over a long integration window, which results in rejection of line frequency ripple when integration time is an integer number of line cycles. Finally, these parts have an input impedance in the GΩ range, with specified input leakage of 10pA to 20pA. Such a leakage, combined with the LTC1966 output impedance, results in just 1µV to 2µV of additional output offset voltage.

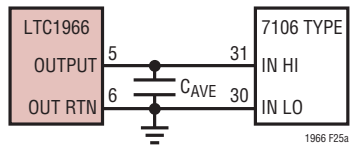


Figure 25a. Interfacing to DVM/DPM ADC

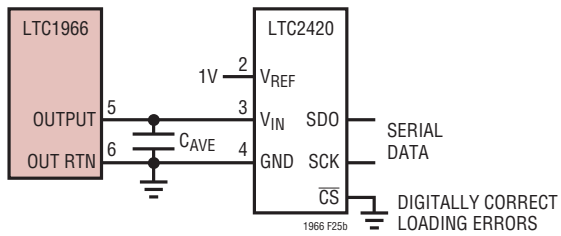


Figure 25b. Interfacing to LTC2420

Another type of ADC that has inherent rejection of RMS averaging ripple is an oversampling ΔΣ. With most, but not all, of these devices, it is possible to connect the LTC1966 output directly to the converter input. Issues to look out for are the input impedance, and any input sampling currents. The input sampling currents drawn by ΔΣ ADCs often have large spikes of current with short durations that can confuse some op amps, but with the large C_{AVE} needed by the LTC1966 these are not an issue.

The average current is important, as it can create LTC1966 errors; if it is constant it will create an offset, while average currents that change with the voltage level create gain errors. Some converters run continuously, others only sample upon demand, and this will change the results in ways that need to be understood. The LTC1966 output impedance has a loose tolerance relative to the usual resistors and the same can be true for the input impedance of ΔΣ ADC, resulting in gain errors from part-to-part. The system calibration techniques described in the following section should be used in applications that demand tight tolerances.

One example of driving an oversampling ΔΣ ADC is shown in Figure 25b. In this circuit, the LTC2420 is used with a 1V V_{REF}. Since the LTC1966 output voltage range is about 1V, and the LTC2420 has a ±12.5% extended input range, this configuration matches the two ranges with room to spare. The LTC2420 has an input impedance of 16.6MΩ, resulting in a gain error of –0.4% to –0.6%. In fact, the LTC2420 DC input current is not zero at 0V, but rather at one half its reference, so both an output offset and a gain error will result. These errors will vary from part to part, but with a specific LTC1966 and LTC2420 combination, the errors will be fixed, varying less than ±0.05% over temperature. So a system that has digital calibration can be quite accurate despite the nominal gain and offset error. With 20 bits of resolution, this part is more accurate than the LTC1966, but the extra resolution is helpful because it reduces nonlinearity at the LSB transitions as a digital gain correction is made. Furthermore, its small size and ease of use make it attractive.

APPLICATIONS INFORMATION

As is shown in Figure 25b, where the LTC2420 is set to continuously convert by grounding the CS pin. The gain error will be less if CS is driven at a slower rate, however, the rate should either be consistent or at a rate low enough that the LTC1966 and its output capacitor have fully settled by the beginning of each conversion, so that the loading errors are consistent.

Note that in this circuit, the input current of the LTC2420 is being used to assure monotonicity. The LTC2420 Z_{IN} of 16.6MΩ is effectively connected to half the reference voltage, so when the LTC1966 has zero signal, 500mV/16.6MΩ = 30nA is provided.

Alternatively, a 5V V_{REF} can be used, but in this case the LTC1966 output span will only use 20% of the LTC2420's input voltage range. Furthermore, if the OUTRTN remains grounded, the injected current with zero signal will be 150nA, resulting in 5× the offset error and nonlinearity shown in Figure 22.

In both of the circuits of Figure 25, a guard ring only has to encircle three terminals, the LTC1966 output, the top of the averaging capacitor, and the ADC input. Figure 26 shows the top copper patterns for example PCB layouts of each.

The low power consumption of the LTC1966 makes it well suited for battery powered applications, and its slow output (DC) makes it an ideal candidate for a micropower ADC.

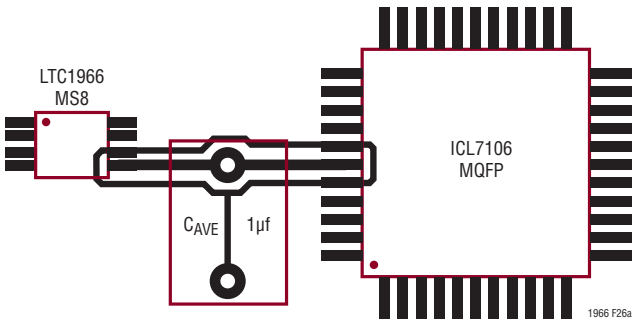


Figure 26a. PCB Layout of Figure 25a with Guard Ring

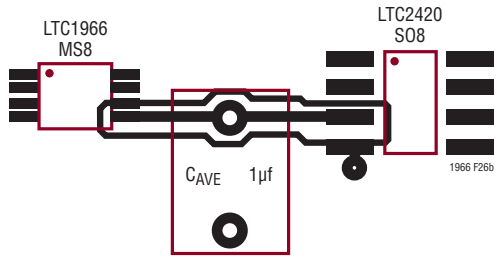


Figure 26b. PCB Layout of Figure 25b with Guard Ring

Figure 10 in Application Note 75, for instance, details a 10-bit ADC with a 35ms conversion time that uses just 29µA of supply current. Such an ADC may also be of use within a 4mA to 20mA loop.

Other types of ADCs sample the input signal once and perform a conversion on that one sample. With these ADCs (Nyquist ADCs), a post filter will be needed in most cases to reduce the peak error with low input frequencies. The DC accurate filter of Figure 14 is attractive from an error standpoint, but it increases the impedance at the ADC input. In most cases, the buffered post filter of Figure 13 will be more appropriate for use with Nyquist analog-to-digital converters.

SYSTEM CALIBRATION

The LTC1966 static accuracy can be improved with end system calibration. Traditionally, calibration has been done at the factory, or at a service depot only, typically using manually adjusted potentiometers. Increasingly, systems are being designed for electronic calibration where the accuracy corrections are implemented in digital code wherever possible, and with calibration DACs where necessary. Additionally, many systems are now designed for self calibration, in which the calibration occurs inside the machine, automatically without user intervention.

APPLICATIONS INFORMATION

Whatever calibration scheme is used, the linearity of the LTC1966 will improve the calibrated accuracy over that achievable with older log/antilog RMS-to-DC converters. Additionally, calibration using DC reference voltages are essentially as accurate with the LTC1966 as those using AC reference voltages. Older log/antilog RMS-to-DC converters required nonlinear input stages (rectifiers) whose linearity would typically render DC based calibration unworkable.

The following are four suggested calibration methods. Implementations of the suggested adjustments are dependent on the system design, but in many cases, gain and output offset can be corrected in the digital domain, and will include the effect of all gains and offsets from the LTC1966 output through the ADC. Input offset voltage, on the other hand, will have to be corrected with adjustment to the actual analog input to the LTC1966.

The methods below assume the unaltered linearity of the LTC1966, i.e. without the monotonicity fix of Figure 21. If this is present, the V_{OOS} shift it introduces should be taken out before using either method for which V_{OOS} is not calibrated. Also, the nonlinearity it introduces will increase the 20mV readings discussed below by 0.78% but increase the 200mV readings only 78ppm. There are a variety of ways to deal with these errors, including possibly ignoring them, but the specifics will depend on system requirements. Designers are cautioned to avoid the temptation to digitally take out the hyperbolic transfer function introduced because if the offsets are not exactly the nominals assumed, the system will end up right back where it began with a potential discontinuity with zero input, either from a divide by zero or from a square root of a negative number in the calculations to undo the hyperobic transfer function. An adaptive algorithm would most likely be necessary to safely take out more than half of the introduced nonlinearity.

If a 5V reference is used in the connection of Figure 25b, the V_{OOS} and nonlinearity created would be even larger, and will no doubt be more tempting to correct for. Designers are likewise cautioned against correcting for all of the nonlinearity.

AC-Only, 1 Point

The dominant error at full-scale will be caused by the gain error, and by applying a full-scale sine wave input, this error can be measured and corrected for. Unlike older log/antilog RMS-to-DC converters, the correction should be made for zero error at full scale to minimize errors throughout the dynamic range.

The best frequency for the calibration signal is roughly ten times the –0.1% DC error frequency. For 1µF, –0.1% DC error occurs at 8Hz, so 80Hz is a good calibration frequency, although anywhere from 60Hz to 100Hz should suffice.

The trade-off here is that on the one hand, the DC error is input frequency dependent, so a calibration signal frequency high enough to make the DC error negligible should be used. On the other hand, as low a frequency as can be used is best to avoid attenuation of the calibrated AC signal, either from parasitic RC loading or insufficient op amp gain. For instance, with a 1kHz calibration signal, a 1MHz op amp will typically only have 60dB of open loop gain, so it could attenuate the calibration signal a full 0.1%.

AC-Only, 2 Point

The next most significant error for AC-coupled applications will be the effect of output offset voltage, noticeable at the bottom end of the input scale. This too can be calibrated out if two measurements are made, one with a full-scale sine wave input and a second with a sine wave input (of the same frequency) at 10% of full-scale. The trade-off in selecting this second level is that it should be small enough that the gain error effect becomes small compared to the gain error effect at full-scale, while on the other hand, not using so small an input that the input offset voltage becomes an issue.

APPLICATIONS INFORMATION

The calculations of the error terms for a 200mV full-scale case are:

$$\text{Gain} = \frac{\text{Reading at 200mV} - \text{Reading at 20mV}}{180\text{mV}}$$

$$\text{Output Offset} = \frac{\text{Reading at 20mV}}{\text{Gain}} - 20\text{mV}$$

DC, 2 Point

DC based calibration is preferable in many cases because a DC voltage of known, good accuracy is easier to generate than such an AC calibration voltage. The only down side is that the LTC1966 input offset voltage plays a role. It is therefore suggested that a DC based calibration scheme check at least two points: ±full-scale. Applying the –full-scale input can be done by physically inverting the voltage or by applying the same +full-scale input to the opposite LTC1966 input.

For an otherwise AC-coupled application, only the gain term may be worth correcting for, but for DC-coupled applications, the input offset voltage can also be calculated and corrected for.

The calculations of the error terms for a 200mV full-scale case are:

$$\text{Gain} = \frac{\text{Reading at 200mV} + \text{Reading at} - 200\text{mV}}{400\text{mV}}$$

$$\text{Input Offset} = \frac{\text{Reading at} - 200\text{mV} - \text{Reading at 200mV}}{2 \bullet \text{Gain}}$$

Note: Calculation of and correction for input offset voltage are the only way in which the two LTC1966 inputs (IN1, IN2) are distinguishable from each other. The calculation above assumes the standard definition of offset; that a positive offset is the case of a positive voltage error inside the device that must be corrected by applying a like negative voltage outside. The offset is referred to whichever pin is driven positive for the +full-scale reading.

DC, 3 Point

One more point is needed with a DC calibration scheme to determine output offset voltage: +10% of full scale.

The calculation of the input offset is the same as for the 2-point calibration above, while the gain and output offset are calculated for a 200mV full-scale case as:

$$\text{Gain} = \frac{\text{Reading at 200mV} - \text{Reading at 20mV}}{180\text{mV}}$$

$$\text{Output Offset} = \frac{\text{Reading at 200mV} + \text{Reading at} - 200\text{mV} - 400\text{mV} \bullet \text{Gain}}{2}$$

APPLICATIONS INFORMATION

TROUBLESHOOTING GUIDE

Top Ten LTC1966 Application Mistakes

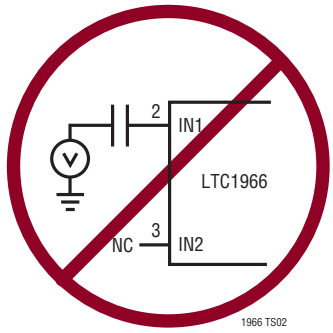
1. Circuit won't work–Dead On Arrival–no power drawn.
   – Probably forgot to enable the LTC1966 by pulling Pin 8 low.

   Solution: Tie Pin 8 to Pin 1.

2. Circuit won't work, but draws power. Zero or very little output, single-ended input application.
   – Probably didn't connect both input pins.

   Solution: Tie both inputs to something. See Input Connections in the Design Cookbook.

CONNECT PIN 3

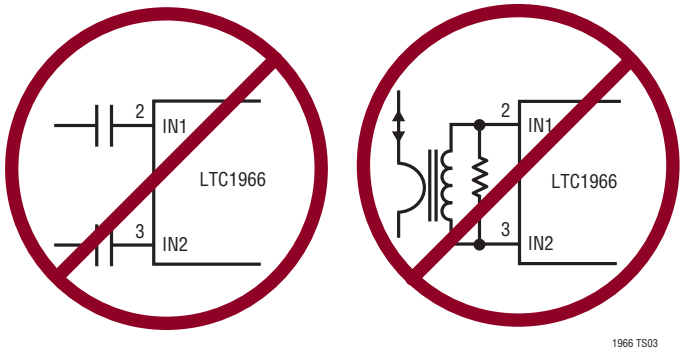


3. Screwy results, particularly with respect to linearity or high crest factors; differential input application.
   – Probably AC-coupled both input pins.

   Solution: Make at least one input DC-coupled. See Input Connections in the Design Cookbook.

DC CONNECT ONE INPUT

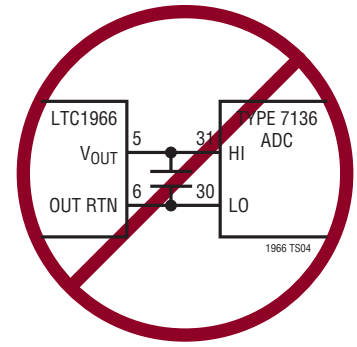
DC CONNECT ONE INPUT



4. Gain is low by a few percent, along with other screwy results.
   – Probably tried to use output in a floating, differential manner.

   Solution: Tie Pin 6 to a low impedance. See Output Connections in the Design Cookbook.

GROUND PIN 6



5. Offsets perceived to be out of specification because 0V in ≠ 0V out.
   – The offsets are not specified at 0V in. No RMS-to-DC converter works well at 0 due to a divide-by-zero calculation.

   Solution: Measure V_{IOS}/V_{OOS} by extrapolating readings > $\pm 5mV_{DC}$.

6. Linearity perceived to be out of specification particularly with small input signals.
   – This could again be due to using 0V in as one of the measurement points.

   Solution: Check Linearity from $5mV_{RMS}$ to $500mV_{RMS}$.

   – The input offset voltage can cause small AC linearity errors at low input amplitudes as well. See Error Analyses section.

   Possible Solution: Include a trim for input offset.

APPLICATIONS INFORMATION

7. Output is noisy with >10kHz inputs.
   – This is a fundamental characteristic of this topology. The LTC1966 is designed to work very well with inputs of 1kHz or less. It works okay as high as 1MHz, but it is limited by aliased ΔΣ noise.

     Solution: Bandwidth limit the input or digitally filter the resulting output.

8. Large errors occur at crest factors approaching, but less than 4.
   – Insufficient averaging.

     Solution: Increase C_{AVE}. See Crest Factor and AC + DC Waveforms section for discussion of output droop.

9. Screwy results, errors > spec limits, typically 1% to 5%.
   – High impedance (85kΩ) and high accuracy (0.1%) require clean boards! Flux residue, finger grime, etc. all wreak havoc at this level.

     Solution: Wash the board.

     Helpful Hint: Sensitivity to leakages can be reduced significantly through the use of guard traces.

KEEP BOARD CLEAN



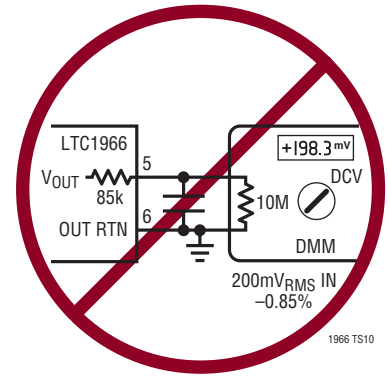
10. Gain is low by ≅1% or more, no other problems.
   – Probably due to circuit loading. With a DMM or a 10× scope probe, Z_{IN} = 10MΩ. The LTC1966 output is 85kΩ, resulting in –0.85% gain error. Output impedance is higher with the DC accurate post filter.

     Solution: Remove the shunt loading or buffer the output.

   – Loading can also be caused by cheap averaging capacitors.

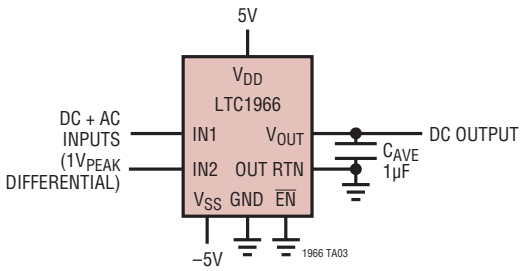
     Solution: Use a high quality metal film capacitor for C_{AVE}.

LOADING DRAGS DOWN GAIN

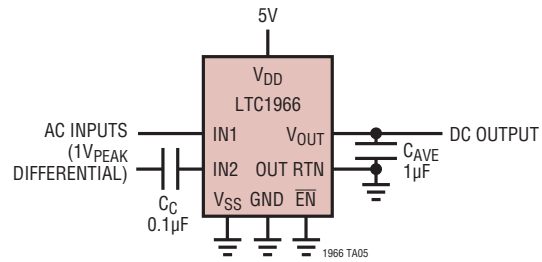


TYPICAL APPLICATIONS

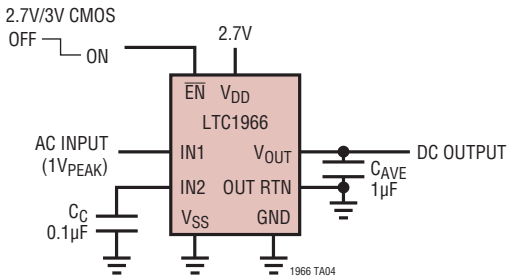
±5V Supplies, Differential, DC-Coupled RMS-to-DC Converter



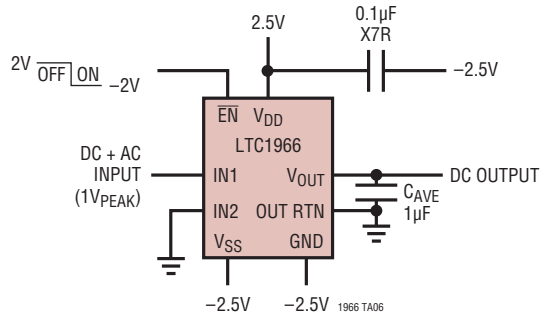
5V Single Supply, Differential, AC-Coupled RMS-to-DC Converter



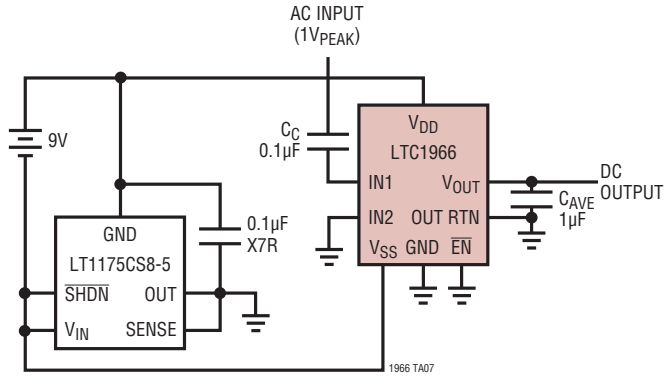
2.7V Single Supply, Single Ended, AC-Coupled RMS-to-DC Converter with Shutdown



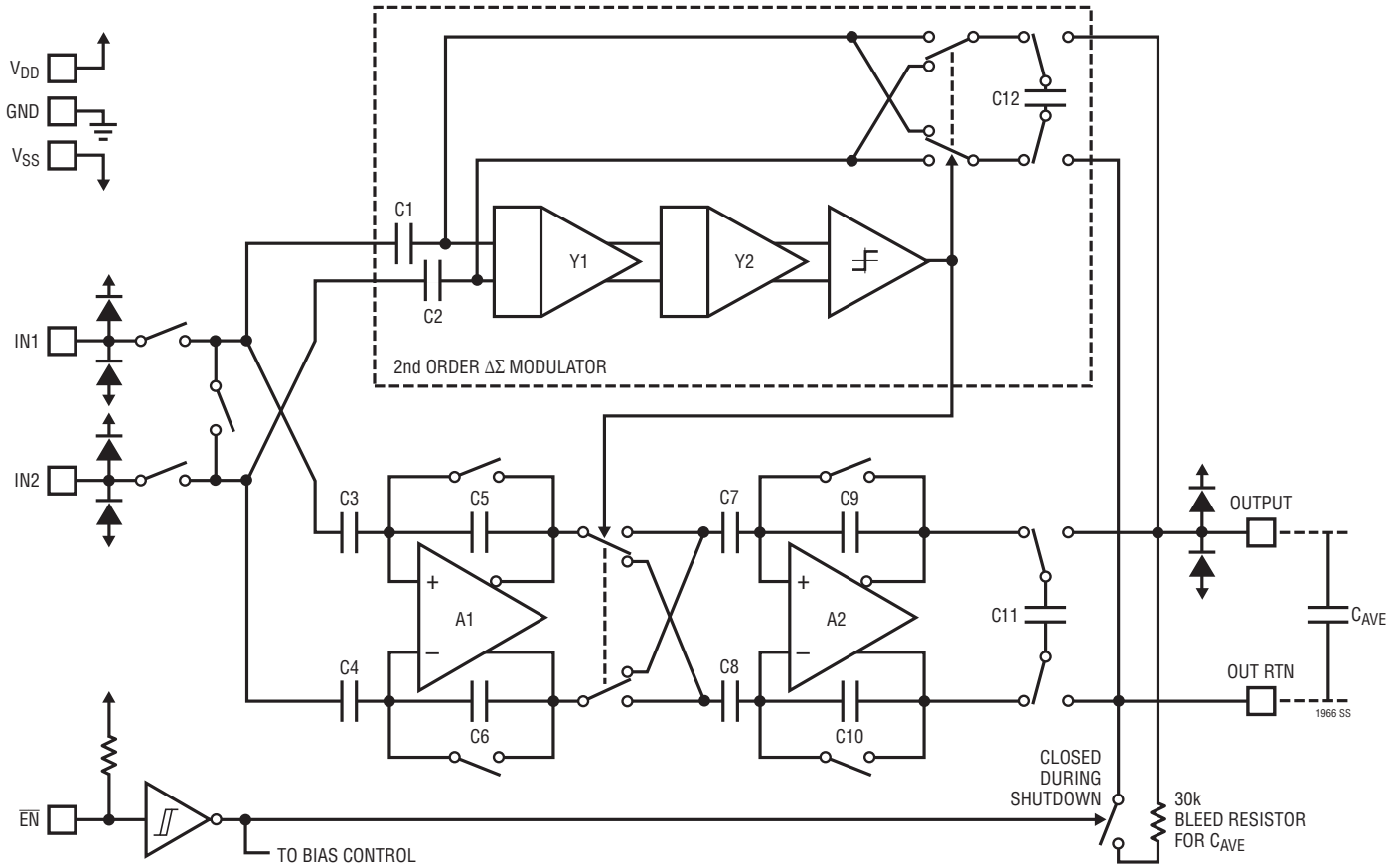
±2.5V Supplies, Single Ended, DC-Coupled RMS-to-DC Converter with Shutdown



Battery Powered Single-Ended AC-Coupled RMS-to-DC Converter

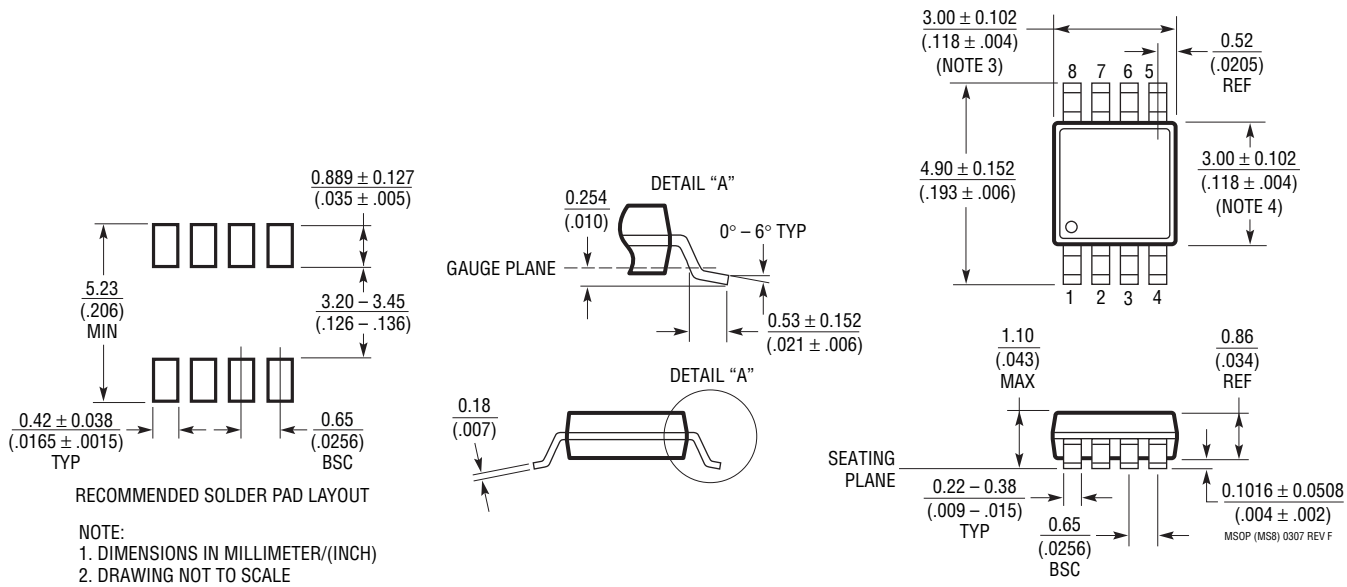


SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

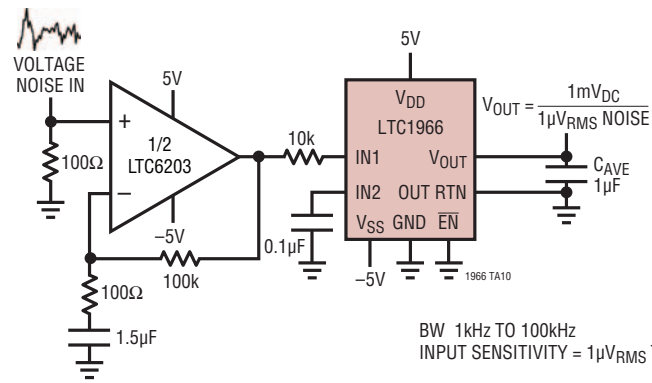
REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	5/11	Revised entire data sheet to add H- and MP- grades	1 to 38

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

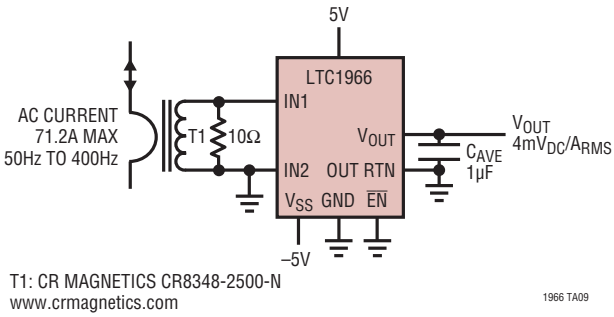
TYPICAL APPLICATION

RMS Noise Measurement



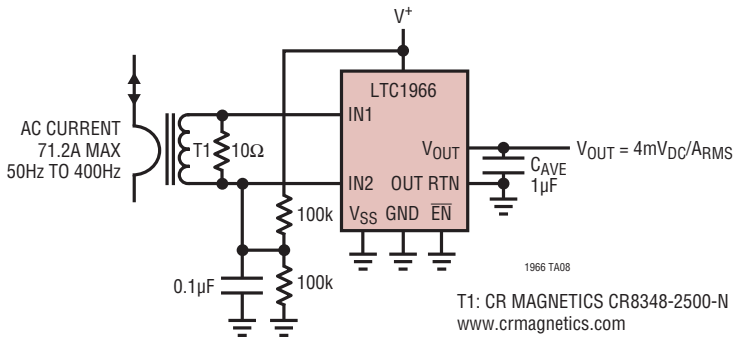
BW 1kHz TO 100kHz
INPUT SENSITIVITY = $1\mu V_{RMS}$ TYP

70A Current Measurement



T1: CR MAGNETICS CR8348-2500-N
www.crmagnetics.com

Single Supply RMS Current Measurement



T1: CR MAGNETICS CR8348-2500-N
www.crmagnetics.com

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1077	Micropower, Single Supply Precision Op Amp	48μA I_{SY}, 60μV $V_{OS(MAX)}$, 450pA $I_{OS(MAX)}$
LT1175-5	Negative, –5V Fixed, Micropower LDO Regulator	45μA I_Q, Available in SO-8 or SOT-223
LT1494	1.5μA Max, Precision Rail-to-Rail I/O Op Amp	375μV $V_{OS(MAX)}$, 100pA $I_{OS(MAX)}$
LT1782	General Purpose SOT-23 Rail-to-Rail Op Amp	40μA I_{SY}, 800μV $V_{OS(MAX)}$, 2nA $I_{OS(MAX)}$
LT1880	SOT-23 Rail-to-Rail Output Precision Op Amp	1.2mA I_{SY}, 150μV $V_{OS(MAX)}$, 900pA $I_{OS(MAX)}$
LTC1967	Precision, Extended Bandwidth RMS to DC Converter	330μA I_{SY}, ΔΣ RMS Conversion to 4MHz
LTC1968	Precision, Wide Bandwidth RMS to DC Converter	2.3mA I_{SY}, ΔΣ RMS Conversion to 15MHz
LTC2050	Zero Drift Op Amp in SOT-23	750μA I_{SY}, 3μV $V_{OS(MAX)}$, 75pA $I_{B(MAX)}$
LT2178/LT2178A	17μA Max, Single Supply Precision Dual Op Amp	14μA I_{SY}, 120μV $V_{OS(MAX)}$, 350pA $I_{OS(MAX)}$
LTC2402	2-Channel, 24-bit, Micropower, No Latency ΔΣ™ ADC	200μA I_{SY}, 4ppm INL, 10ppm TUE
LTC2420	20-bit, Micropower, No Latency ΔΣ ADC in SO-8	200μA I_{SY}, 8ppm INL, 16ppm TUE
LTC2422	2-Channel, 20-bit, Micropower, No Latency ΔΣ ADC	Dual Channel Version of LTC2420

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LT 0511 REV B • PRINTED IN USA

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