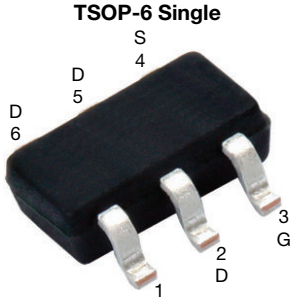
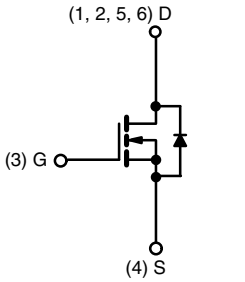
Automotive N-Channel 60 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	60
$R_{DS(on)}$ (Ω) at V_{GS} = 10 V	0.042
$R_{DS(on)}$ (Ω) at V_{GS} = 4.5 V	0.063
I_D (A)	7
Configuration	Single

TSOP-6 Single



Top View



N-Channel MOSFET

Marking Code: 8Q

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

Pb-free

RoHS COMPLIANT

HALOGEN FREE

ORDERING INFORMATION	
Package	TSOP-6
Lead (Pb)-free and Halogen-free	SQ3426EV-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25 °C	I_D	7	A
	T_C = 125 °C		4	
Continuous Source Current (Diode Conduction)		I_S	6	
Pulsed Drain Current [a]		I_{DM}	29	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	10	
Single Pulse Avalanche Energy		E_{AS}	5	mJ
Maximum Power Dissipation [a]	T_C = 25 °C	P_D	5	W
	T_C = 125 °C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to +175	°C

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount [b]	R_{thJA}	110	°C/W
Junction-to-Foot (Drain)		R_{thJF}	30	

Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. When mounted on 1" square PCB (FR4 material).

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SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0, I_D = 250 µA		60	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		1.5	2	2.5	
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V		-	-	± 100	nA
		V_{DS} = 0 V, V_{GS} = ± 20 V		-	-	± 300	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 60 V	-	-	1	µA
		V_{GS} = 0 V	V_{DS} = 60 V, T_J = 125 °C	-	-	50	
		V_{GS} = 0 V	V_{DS} = 60 V, T_J = 175 °C	-	-	150	
On-State Drain Current [a]	$I_{D(on)}$	V_{GS} = 10 V	V_{DS} ≥ 5 V	10	-	-	A
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 5 A	-	0.032	0.042	Ω
		V_{GS} = 10 V	I_D = 5 A, T_J = 125 °C	-	0.056	-	
		V_{GS} = 10 V	I_D = 5 A, T_J = 175 °C	-	0.071	-	
		V_{GS} = 4.5 V	I_D = 4 A	-	0.035	0.063	
Forward Transconductance [a]	g_{fs}	V_{DS} = 15 V, I_D = 4 A		-	21	-	S
Dynamic [b]							
Input Capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = 30 V, f = 1 MHz	-	560	720	pF
Output Capacitance	C_{oss}			-	85	110	
Reverse Transfer Capacitance	C_{rss}			-	55	70	
Total Gate Charge [c]	Q_g	V_{GS} = 4.5 V	V_{DS} = 30 V, I_D = 4 A	-	6.3	12	nC
Gate-Source Charge [c]	Q_{gs}			-	2.1	-	
Gate-Drain Charge [c]	Q_{gd}			-	4.1	-	
Gate Resistance	R_g	f = 1 MHz		1.9	3.8	5.7	Ω
Turn-On Delay Time [c]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 7.5 Ω I_D ≅ 4 A, V_{GEN} = 10 V, R_g = 1 Ω		-	9	14	ns
Rise Time [c]	t_r			-	12	18	
Turn-Off Delay Time [c]	$t_{d(off)}$			-	19	29	
Fall Time [c]	t_f			-	7	11	
Source-Drain Diode Ratings and Characteristics [b]							
Pulsed Current [a]	I_{SM}			-	-	29	A
Forward Voltage	V_{SD}	I_F = 1.6 A, V_{GS} = 0		-	0.75	1.2	V

Notes

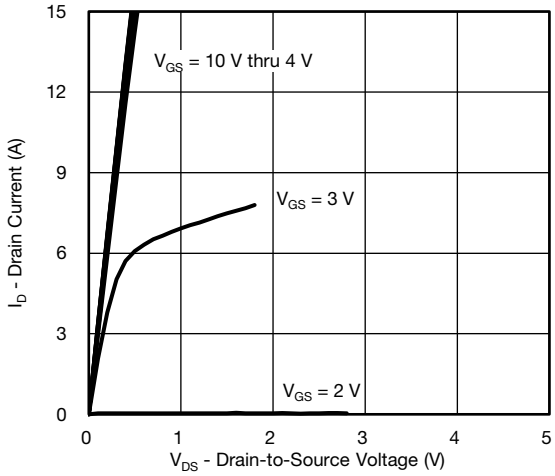
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

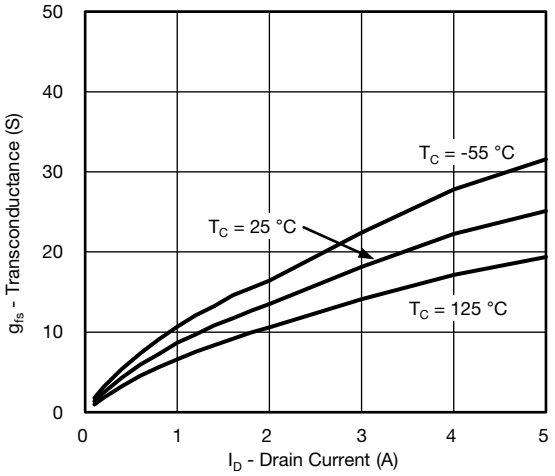
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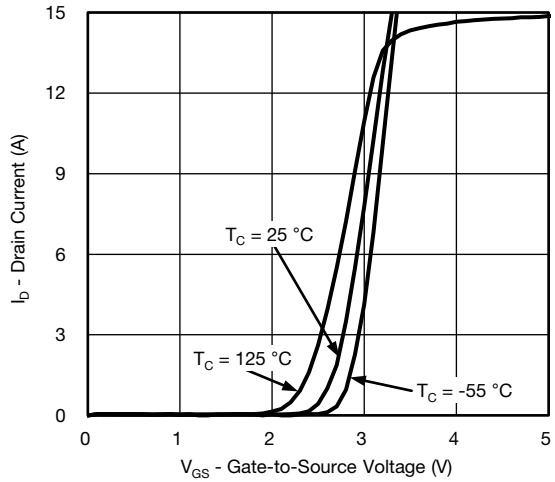
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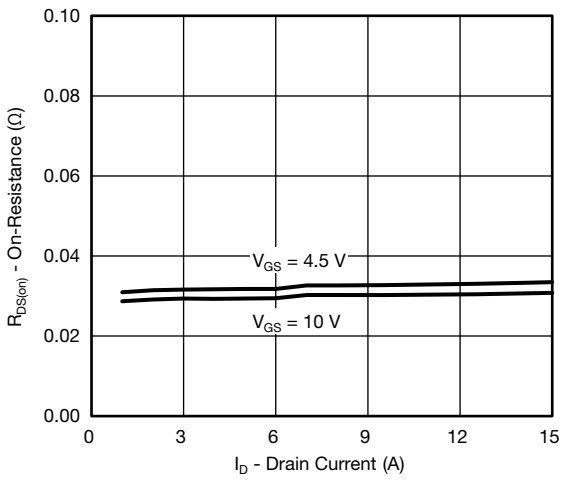
Output Characteristics



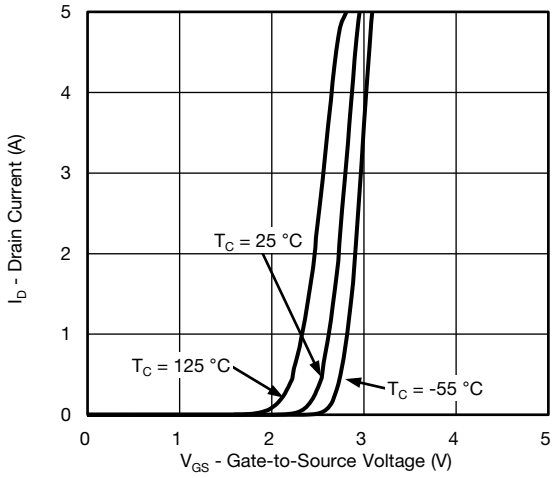
Transconductance



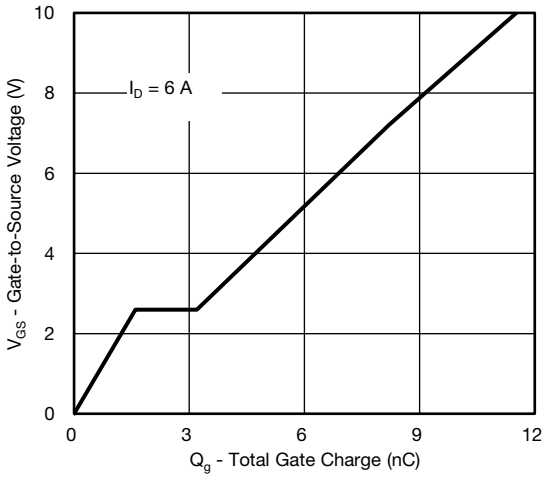
Transfer Characteristics



On-Resistance vs. Drain Current



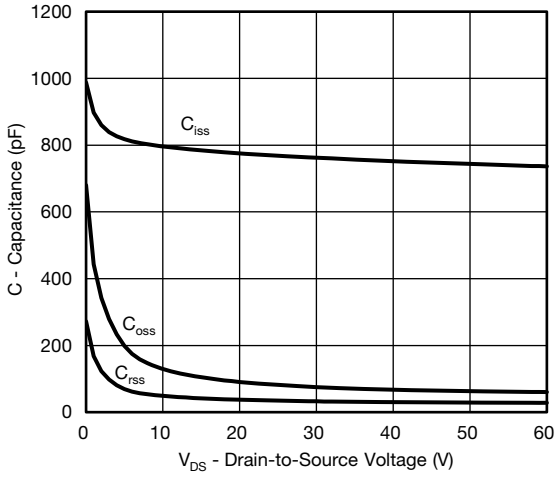
Transfer Characteristics



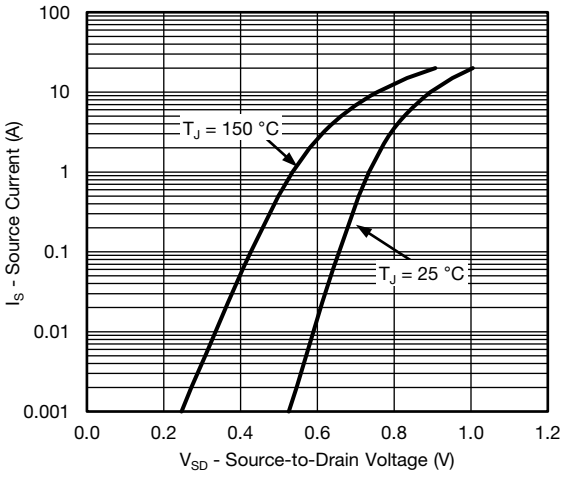
Gate Charge

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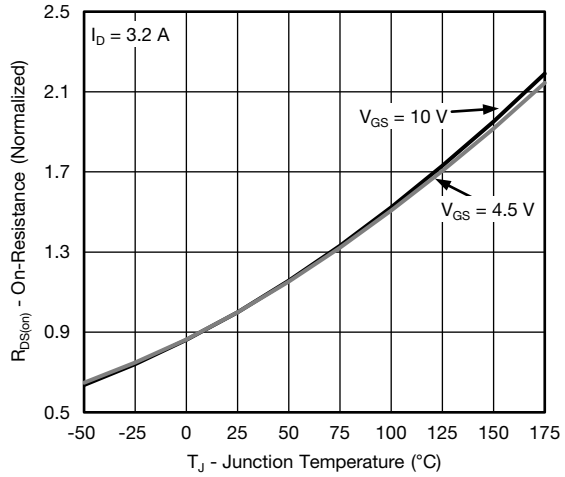
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



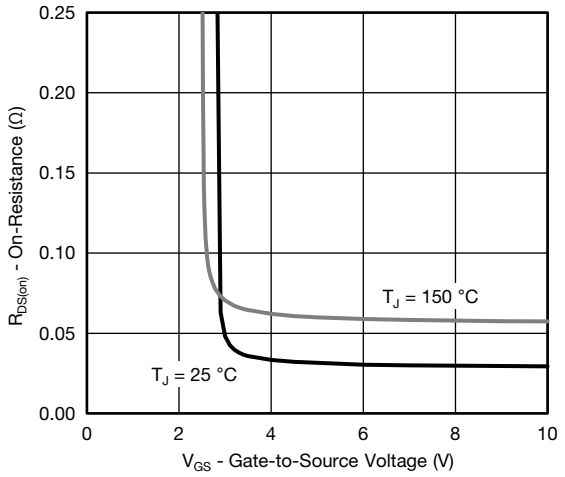
Capacitance



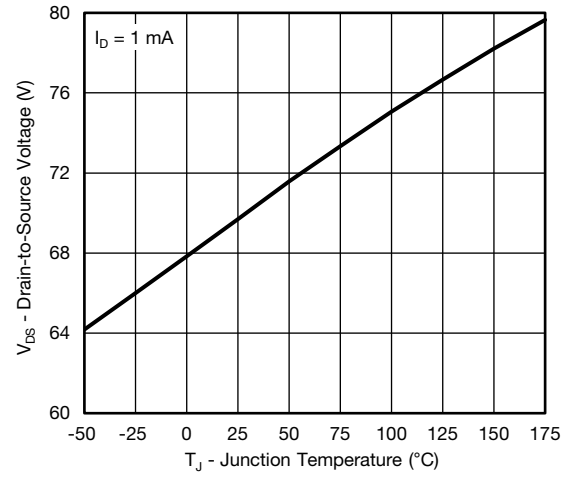
Source Drain Diode Forward Voltage



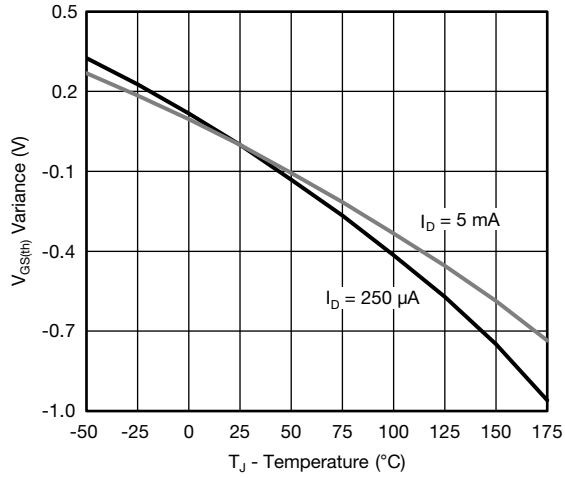
On-Resistance vs. Junction Temperature



On-Resistance vs. Gate-Source Voltage



Drain Source Breakdown vs. Junction Temperature

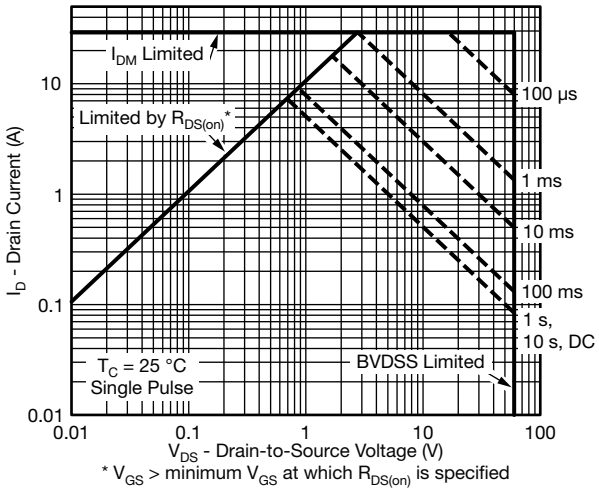


Threshold Voltage

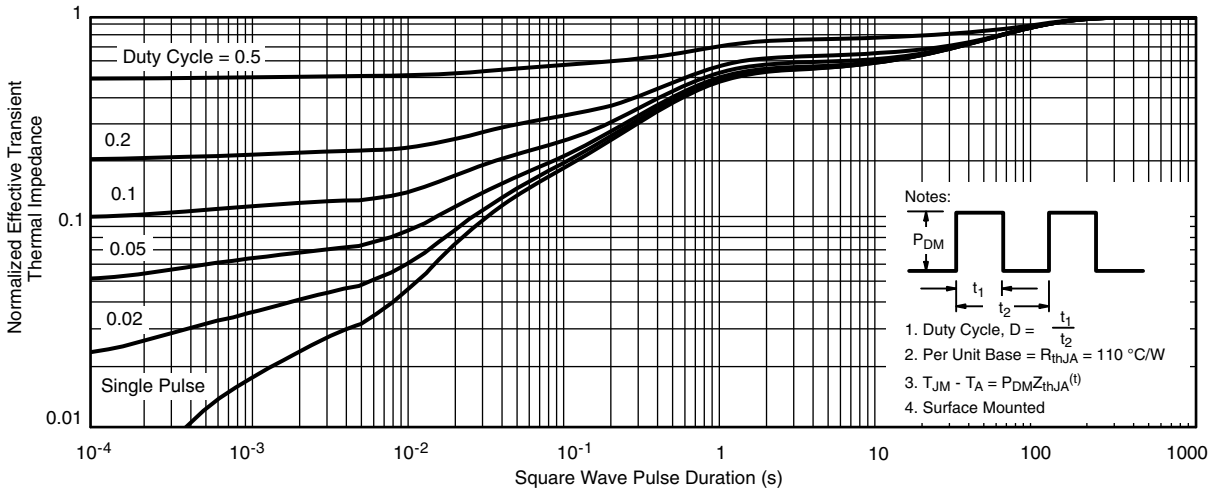
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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



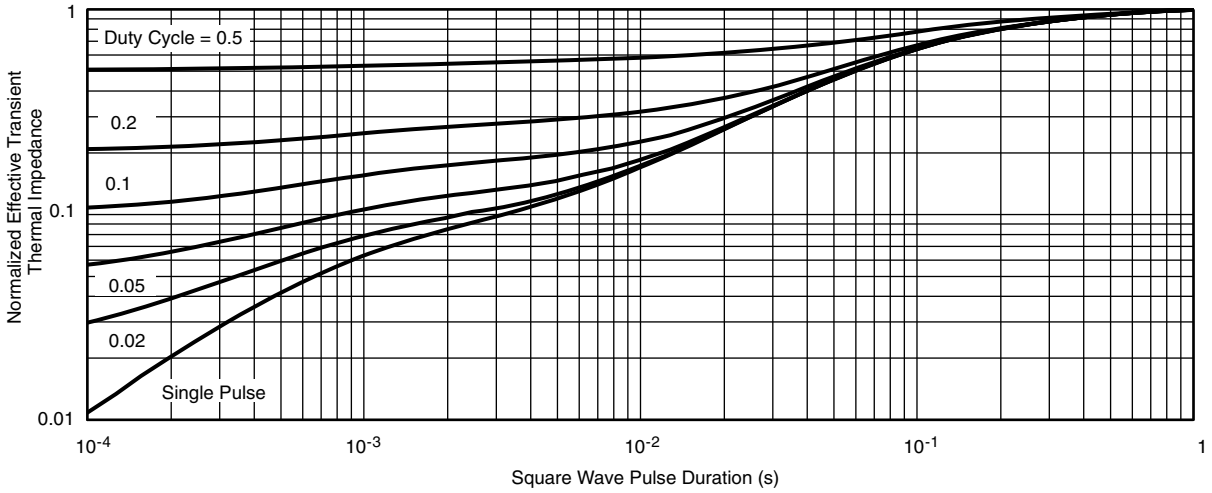
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized thermal Transient Impedance, Junction-to-Foot

Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction to Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction to Foot (25 °C)

  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65107.

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TSOP-6

Ordering codes for the SQ rugged series power MOSFETs in the TSOP-6 package:

DATASHEET PART NUMBER	OLD ORDERING CODE [a]	NEW ORDERING CODE
SQ3410EV	SQ3410EV-T1-GE3	**SQ3410EV-T1_GE3**
SQ3418AEEV	-	**SQ3418AEEV-T1_GE3**
SQ3418EV	-	**SQ3418EV-T1_GE3**
SQ3419AEEV	-	**SQ3419AEEV-T1_GE3**
SQ3419EV	-	**SQ3419EV-T1_GE3**
SQ3425EV	-	**SQ3425EV-T1_GE3**
SQ3426AEEV	-	**SQ3426AEEV-T1_GE3**
SQ3426EV	-	**SQ3426EV-T1_GE3**
SQ3427AEEV	-	**SQ3427AEEV-T1_GE3**
SQ3427EV	-	**SQ3427EV-T1_GE3**
SQ3456BEV	SQ3456BEV-T1-GE3	**SQ3456BEV-T1_GE3**
SQ3457EV	SQ3457EV-T1-GE3	**SQ3457EV-T1_GE3**
SQ3460EV	SQ3460EV-T1-GE3	**SQ3460EV-T1_GE3**
SQ3461EV	-	**SQ3461EV-T1_GE3**
SQ3469EV	SQ3469EV-T1-GE3	**SQ3469EV-T1_GE3**
SQ3481EV	SQ3481EV-T1-GE3	**SQ3481EV-T1_GE3**
SQ3985EV	-	**SQ3985EV-T1_GE3**

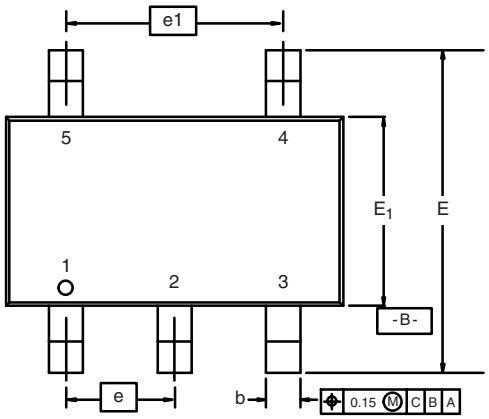
Note

a. Old ordering code is obsolete and no longer valid for new orders

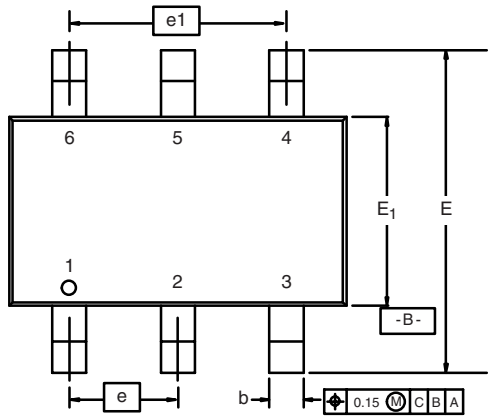
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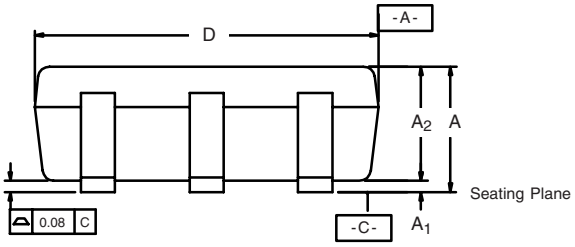
TSOP: 5/6–LEAD
JEDEC Part Number: MO-193C

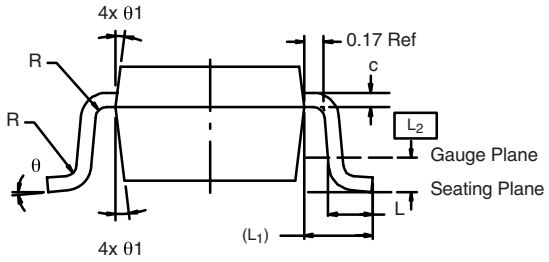


5-LEAD TSOP



6-LEAD TSOP





Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A_1	0.01	-	0.10	0.0004	-	0.004
A_2	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E_1	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e_1	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L_1	0.60 Ref			0.024 Ref		
L_2	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ_1	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540						

Mounting LITTLE FOOT® TSOP-6 Power MOSFETs

Surface mounted power MOSFET packaging has been based on integrated circuit and small signal packages. Those packages have been modified to provide the improvements in heat transfer required by power MOSFETs. Leadframe materials and design, molding compounds, and die attach materials have been changed. What has remained the same is the footprint of the packages.

The basis of the pad design for surface mounted power MOSFET is the basic footprint for the package. For the TSOP-6 package outline drawing see http://www.vishay.com/doc?71200 and see http://www.vishay.com/doc?72610 for the minimum pad footprint. In converting the footprint to the pad set for a power MOSFET, you must remember that not only do you want to make electrical connection to the package, but you must made thermal connection and provide a means to draw heat from the package, and move it away from the package.

In the case of the TSOP-6 package, the electrical connections are very simple. Pins 1, 2, 5, and 6 are the drain of the MOSFET and are connected together. For a small signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.

Figure 1 shows the copper spreading recommended footprint for the TSOP-6 package. This pattern shows the starting point for utilizing the board area available for the heat spreading copper. To create this pattern, a plane of copper overlays the basic pattern on pins 1,2,5, and 6. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. Notice that the planar copper is shaped like a “T” to move heat away from the drain leads in all directions. This pattern uses all the available area underneath the body for this purpose.

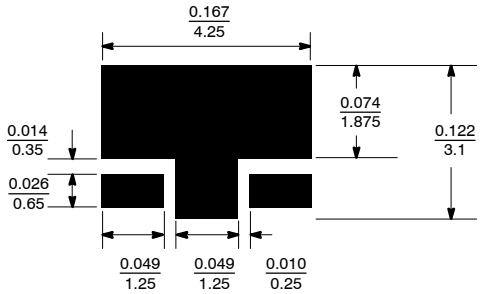


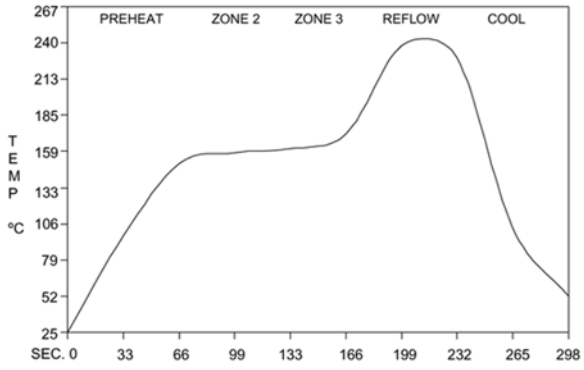
FIGURE 1. Recommended Copper Spreading Footprint

Since surface mounted packages are small, and reflow soldering is the most common form of soldering for surface mount components, “thermal” connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.

REFLOW SOLDERING

Vishay Siliconix surface-mount packages meet solder reflow reliability requirements. Devices are subjected to solder reflow as a test preconditioning and are then reliability-tested using temperature cycle, bias humidity, HAST, or pressure pot. The solder reflow temperature profile used, and the temperatures and time duration, are shown in Figures 2 and 3.



Ramp-Up Rate	+6°C/Second Maximum
Temperature @ 155 ± 15°C	120 Seconds Maximum
Temperature Above 180°C	70 – 180 Seconds
Maximum Temperature	240 +5/–0°C
Time at Maximum Temperature	20 – 40 Seconds
Ramp-Down Rate	+6°C/Second Maximum

FIGURE 2. Solder Reflow Temperature Profile

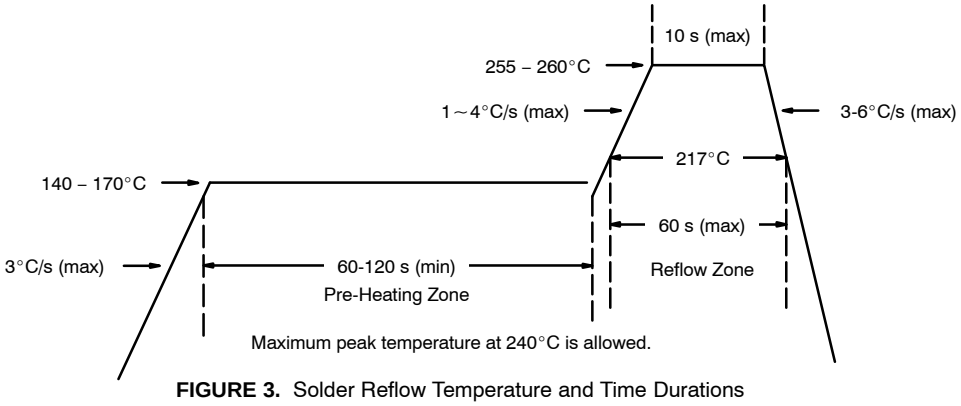


FIGURE 3. Solder Reflow Temperature and Time Durations

THERMAL PERFORMANCE

A basic measure of a device's thermal performance is the junction-to-case thermal resistance, $R\theta_{jc}$, or the junction-to-foot thermal resistance, $R\theta_{jf}$. This parameter is measured for the device mounted to an infinite heat sink and is therefore a characterization of the device only, in other words, independent of the properties of the object to which the device is mounted. Table 1 shows the thermal performance of the TSOP-6.

TABLE 1.

Equivalent Steady State Performance—TSOP-6	
Thermal Resistance $R\theta_{jf}$	30°C/W

SYSTEM AND ELECTRICAL IMPACT OF TSOP-6

In any design, one must take into account the change in MOSFET $r_{DS(on)}$ with temperature (Figure 4).

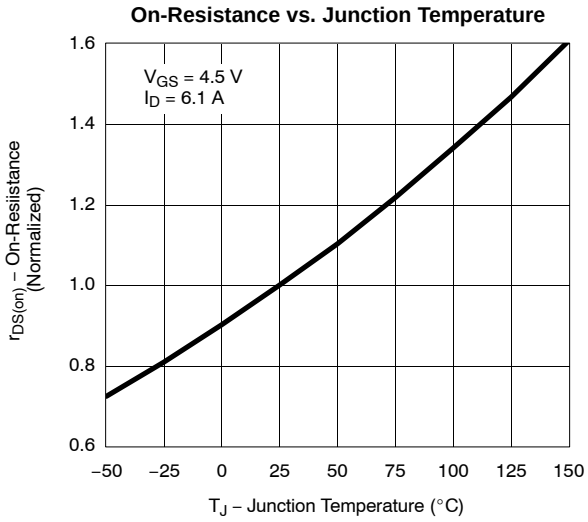
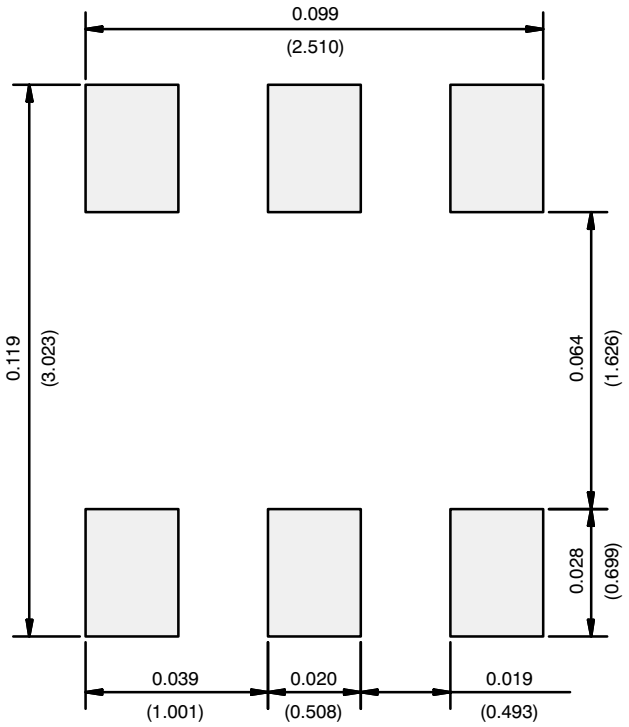


FIGURE 4. Si3434DV

RECOMMENDED MINIMUM PADS FOR TSOP-6



Recommended Minimum Pads
Dimensions in Inches/(mm)

Return to Index

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