National Semiconductor

August 1998

# 54ACT399
# Quad 2-Port Register

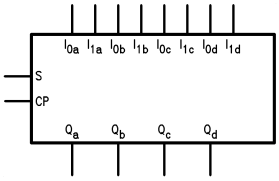
## General Description

The 'AC/ACT399 is the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flop on the rising edge of the clock.

## Features

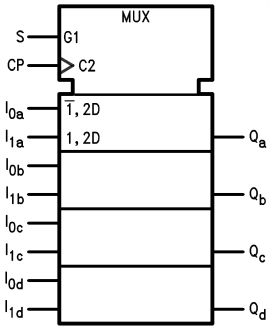
- $I_{CC}$ reduced by 50%
- Select inputs from two data sources
- Fully positive edge-triggered operation
- Outputs source/sink 24 mA
- ACT399 has TTL-compatible inputs

## Logic Symbols




DS100356-1

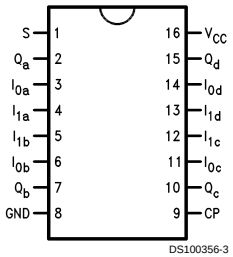
**IEEE/IEC**




DS100356-5

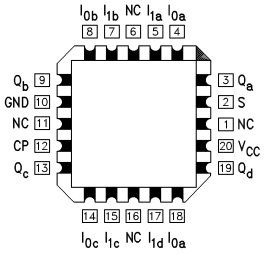
## Connection Diagrams

**Pin Assignment for DIP and Flatpak**




DS100356-3

**Pin Assignment for LCC**




DS100356-2

| Pin Names | Description |
|---|---|
| S | Common Select Input |
| CP | Clock Pulse Input |
| $I_{0a}$–$I_{0d}$ | Data Inputs from Source 0 |
| $I_{1a}$–$I_{1d}$ | Data Inputs from Source 1 |
| $Q_a$–$Q_d$ | Register True Outputs |

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## Functional Description

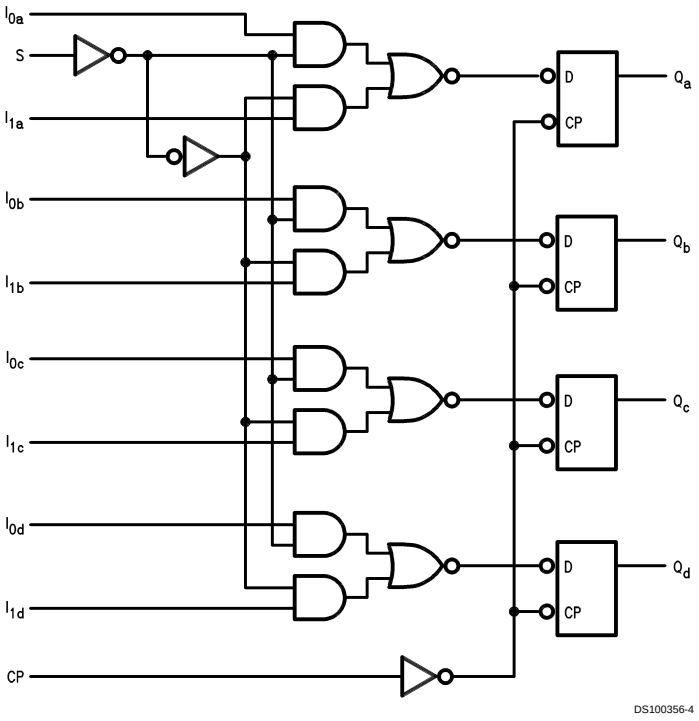
The 'AC/ACT399 is a high-speed quad 2-port register. It selects four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs ($I_{0x}$, $I_{1x}$) and Select input (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation.

## Function Table

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| **S** | **$I_0$** | **$I_1$** | **CP** | **Q** | **$\overline{Q}$** |
| L | L | X | ⌐ | L | H |
| L | H | X | ⌐ | H | L |
| H | X | L | ⌐ | L | H |
| H | X | H | ⌐ | H | L |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

## Logic Diagram




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ = −0.5V | −20 mA |
| $V_I$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Input Voltage ($V_I$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ = −0.5V | −20 mA |
| $V_O$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Output Voltage ($V_O$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Source or Sink Current ($I_O$) | ±50 mA |
| DC $V_{CC}$ or Ground Current per Output Pin ($I_{CC}$ or $I_{GND}$ ) | ±50 mA |
| Storage Temperature ($T_{STG}$) | −65˚C to +150˚C |
| Junction Temperature ($T_J$) | |
| CDIP | +175˚C |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | |
| 'ACT | 4.5V to 5.5V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | |
| 54ACT | −55˚C to +125˚C |
| Minimum Input Edge Rate ($\Delta V/\Delta t$) | |
| 'ACT Devices | |
| $V_{IN}$ from 0.8V to 2.0V | |
| $V_{CC}$ @ 4.5V, 5.5V | 125 mV/ns |

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

## DC Electrical Characteristics for 'ACT Family Devices

| Symbol | Parameter | $V_{CC}$ (V) | 54ACT $T_A$ = −55˚C to +125˚C Guaranteed Limits | Units | Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High Level Input Voltage | 4.5 | 2.0 | V | $V_{OUT}$ = 0.1V |
| | | 5.5 | 2.0 | | or $V_{CC}$ −0.1V |
| $V_{IL}$ | Maximum Low Level Input Voltage | 4.5 | 0.8 | V | $V_{OUT}$ = 0.1V |
| | | 5.5 | 0.8 | | or $V_{CC}$ − 0.1V |
| $V_{OH}$ | Minimum High Level | 4.5 | 4.4 | V | $I_{OUT}$ = −50 µA |
| | | 5.5 | 5.4 | | |
| | | | | | (Note 2) $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 4.5 | 3.70 | V | $I_{OH}$ = −24 mA |
| | | 5.5 | 4.70 | | $I_{OH}$ = −24 mA |
| $V_{OL}$ | Maximum Low Level Output Voltage | 4.5 | 0.1 | V | $I_{OUT}$ = 50 µA |
| | | 5.5 | 0.1 | | |
| | | | | | (Note 2) $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 4.5 | 0.50 | V | $I_{OL}$ = 24 mA |
| | | 5.5 | 0.50 | | $I_{OL}$ = 24 mA |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | ±1.0 | µA | $V_I$ = $V_{CC}$, GND |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | 5.5 | 1.6 | mA | $V_I$ = $V_{CC}$ −2.1V |
| $I_{OLD}$ | Minimum Dynamic (Note 3) | 5.5 | 50 | mA | $V_{OLD}$ = 1.65V Max |
| $I_{OHD}$ | Output Current | 5.5 | −50 | mA | $V_{OHD}$ = 3.85V Min |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | 80.0 | µA | $V_{IN}$ = $V_{CC}$ or Ground |

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

## AC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) (Note 4) | 54ACT $T_A$, $V_{CC}$ = Mil $C_L$ = 50 pF | | Units | Fig. No. |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| $f_{max}$ | Input Clock Frequency | 5.0 | 90 | | MHz | |
| $t_{PLH}$ | Propagation Delay CP to Q | 5.0 | 1.5 | 10.0 | ns | |
| $t_{PHL}$ | Propagation Delay CP to Q | 5.0 | 1.5 | 10.0 | ns | |

**Note 4:** Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements

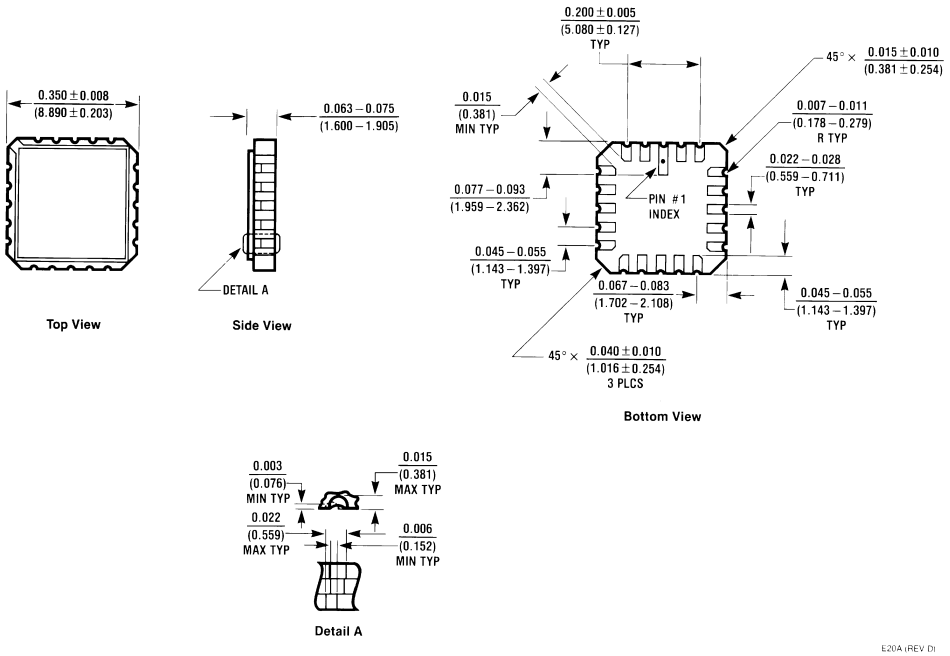
| Symbol | Parameter | $V_{CC}$ (V) (Note 5) | 54ACT $T_A$ = −55°C to +125°C $C_L$ = 50 pF Guaranteed Minimum | Units | Fig. No. |
|---|---|---|---|---|---|
| $t_s$ | Setup Time, HIGH or LOW $I_n$ to CP | 5.0 | 3.5 | ns | |
| $t_h$ | Hold Time, HIGH or LOW $I_n$ to CP | 5.0 | 3.0 | ns | |
| $t_s$ | Setup Time, HIGH or LOW S to CP | 5.0 | 6.0 | ns | |
| $t_h$ | Hold Time, HIGH or LOW S to CP | 5.0 | 2.5 | ns | |
| $t_w$ | CP Pulse Width, HIGH or LOW | 5.0 | 5.0 | ns | |

**Note 5:** Voltage Range 5.0 is 5.0V ±0.5V

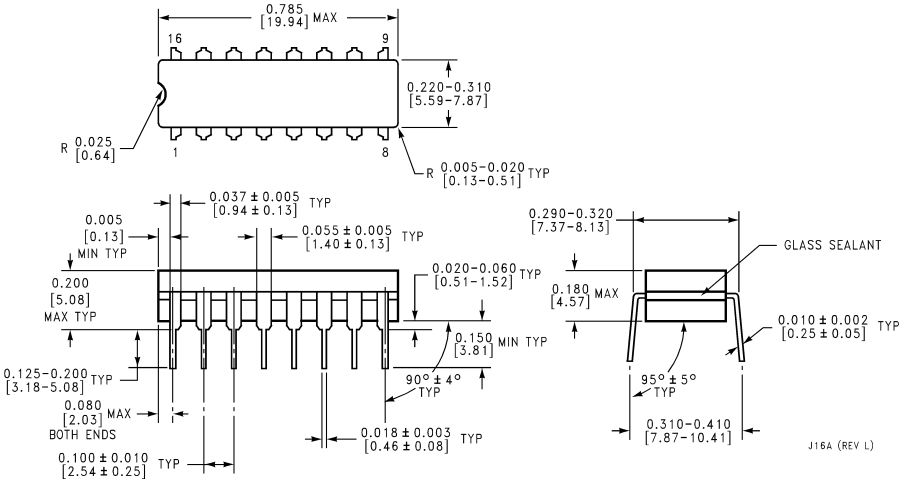
## Capacitance

| Symbol | Parameter | Typ | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = OPEN |
| $C_{PD}$ | Power Dissipation Capacitance | 30 | pF | $V_{CC}$ = 5.0V |

## Physical Dimensions inches (millimeters) unless otherwise noted

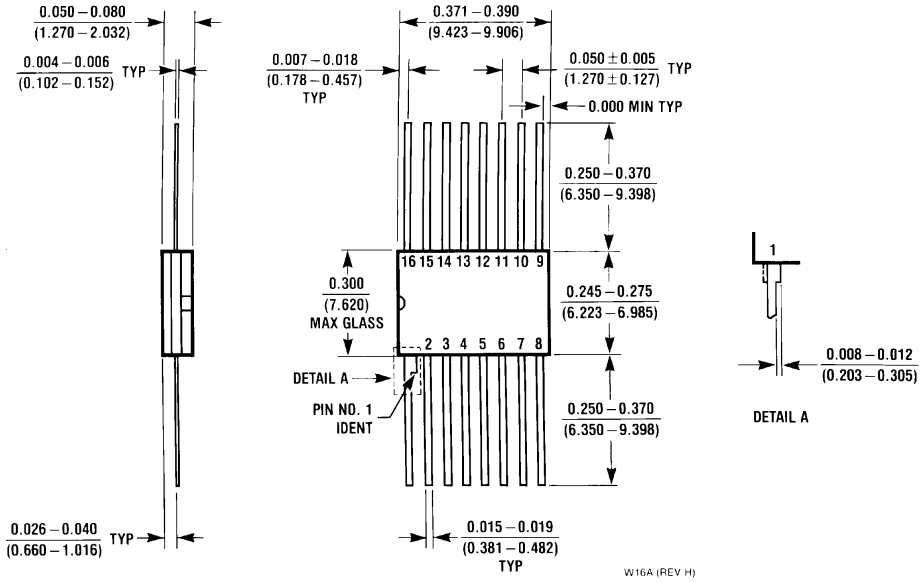



**20 Terminal Ceramic Leadless Chip Carrier (L)**
**NS Package Number E20A**




**16-Lead Ceramic Dual-In-Line Package (D)**
**NS Package Number J16A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**16-Lead Ceramic Flatpak (IF)**
**NS Package Number W16A**

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