AP4400AEC

Ultra Low Power Voltage Detector

1. General Description

The AP4400AEC product family is a voltage detector CMOS IC for monitoring battery, power supply and system voltage. The AP4400AEC offers ultra-low power consumption that is 20nA typical.

2. Features

- Detection voltage “High” (VDETH) 2.7～4.2V (Options)
- Detection voltage “Low”(VDETL) 2.5～VDETH-0.2V (Options)
- Hysteresis voltage of detector 0.2 ～ 1.7 V
- Operating Power VDDIN = 1.2 ～ 5.5V
- Power consumption 20nA typical (@VDDIN=3.4V)
- Operation temperature Ta = -15 ～ 85 °C
- Package WLCSP 4- pin

3. Table of Contents

4. Block Diagram

■ Block Diagram

AP4400AEC：CMOS output (Active “High”)

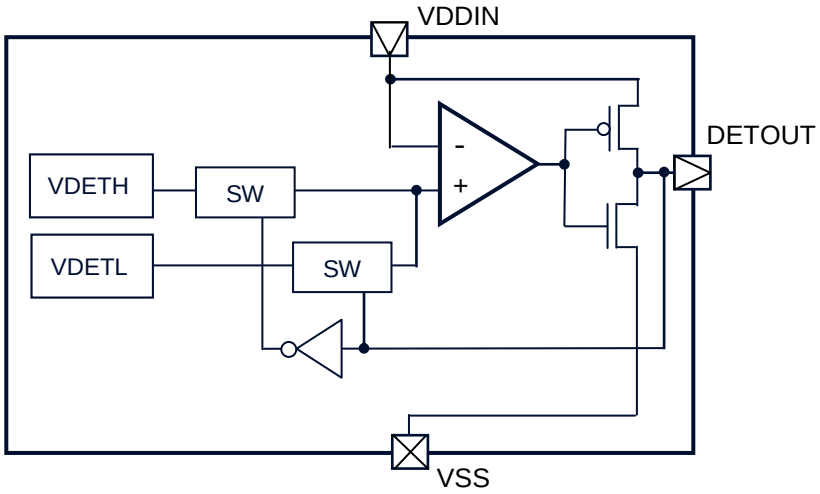
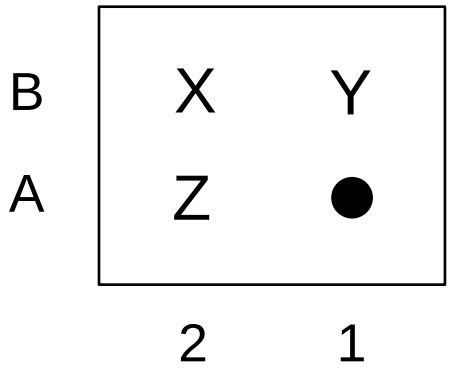


Figure 1. Block Diagram

5. Pin Configuration and Function

■ Pin Configuration

WLCSP 4-pin



Top View

■ Function

Pin No	Pin Name	I/O (Note1)	Function
A1	VSS	Ground	Ground
A2	DETOUT	Output	Dectction voltage output(CMOS Output)
B1	NC	-	Non connect
B2	VDDIN	Power	Power supply

Note 1. Power：Power supply pin (VDDIN)

6. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Power Supply Volgtage (Note 2)	VDDIN	-0.3	6.5	V
Output Voltage(Note 2)	V_{out}	VSS-0.3	VDDIN + 0.3	V
Outut Current	I_{out}	-10	+10	mA
Storage Temperature	T_{stg}	-55	150	°C

Note 2. All voltages are with reference to VSS = 0 V

WARNING: Stresses exceeding Maximum Ratings may damage the device. Normal operation is not guarantee if the condition exceeds the maximum rating.

7. Recommended Operating Conditions

Parameter	Symbol	min	typ	max	Unit	Condition
Operation Temperature	Ta	-15	-	85	°C	
Power Supply Volgtage (Note 3)	VDDIN	1.2		5.5	V	

Note 3. The output voltage is indefinite if the power supply voltage is less than the minimum value.

8. Electrical Characteristics

Ta= -15 to 85°C, DETOUT=open unless otherwise specified.

Parameter	Symbol	min	typ	max	Unit	Condition
Detection Voltage (Note 4)						
Detection Voltage "High" (VDETH) Detection Voltage "Low" (VDETL)	VDETH VDETL	2.9 2.4	3.0 2.5	3.1 2.6	V V	Ta=25°C VDDIN= "L"→"H" VDDIN= "H"→"L"
Detection voltage temperature coefficient	$\Delta V_{DET}/\Delta Ta$	-	0.75	-	mV/°C	Design guarantee value (Note 5)
Power Consumption (Note 6)						
Upper threshold detection Lower threshold detection	IDDH IDDL	-	20 20	50 50	nA nA	Ta=25°C VDDIN=VDETH+0.1V VDDIN=VDETL-0.1V
Power Consumption (Note 6)						
Upper threshold detection Lower threshold detection	IDDH IDDL	-	20 20	200 200	nA nA	VDDIN=VDETH+0.1V VDDIN=VDETL-0.1V
IOL (Note 7)	I_{OL}	0.2	-	-	mA	VDDIN=VDETL-0.1V, VDDIN-VDETOUT=0.5V
IOH (Note 7)	I_{OH}	0.15	-	-	mA	VDDIN=VDETH+0.1V, VDETOUT-VSS=0.5V
Response Time 1 (Note 4)	tPLH tPHL	- -	0.5 4.0	1.0 10	ms ms	No-load condition Ta=25°C VDDIN= VDETH-0.1V→VDETH+0.1V VDDIN= VDETL+0.1V→VDETL-0.1V
Response Time 2 (Note 4)	tPLH tPHL	- -		1.0 30	ms ms	No-load condition VDDIN= VDETH-0.1V→VDETH+0.1V VDDIN= VDETL+0.1V→VDETL-0.1V

Note 4. This specification is for VDETH＝3.0V and VDETL＝2.5V.
Note 5. Not tested
Note 6. Output drive is not included.
Note 7. Output current depends on VDDIN.
IOL shows N-Channel pull current when AP4400AEC DETOUT outputs low.
IOH shows P-Channel push current when AP4400AEC DETOUT outputs high.

9. Function Description

・**Input voltage VDDIN becomes greater than the detection voltage "High"(VDETH)**

The DETOUT will be in an undefined state when VDDIN voltage is from VSS to AP4400AEC minimum operating voltage. The DETOUT outputs VSS when VDDIN volgate exceeds minimum operating voltage. The DETOUT outputs VDDIN when VDDIN voltage is larger than detection voltage "High"(VDETH).

・**Input voltage VDDIN falls smaller than the detection voltage "Low"(VDETL)**

The DETOUT outputs VDDIN when VDDIN voltage is larger than detection voltage "High"(VDETH). The DETOUT outputs VSS when VDDIN voltage falls smaller than detection voltage "Low"(VDETL). The DETOUT will be in an undefined state when VDDIN voltage is below AP4400AEC minimum operating voltage.

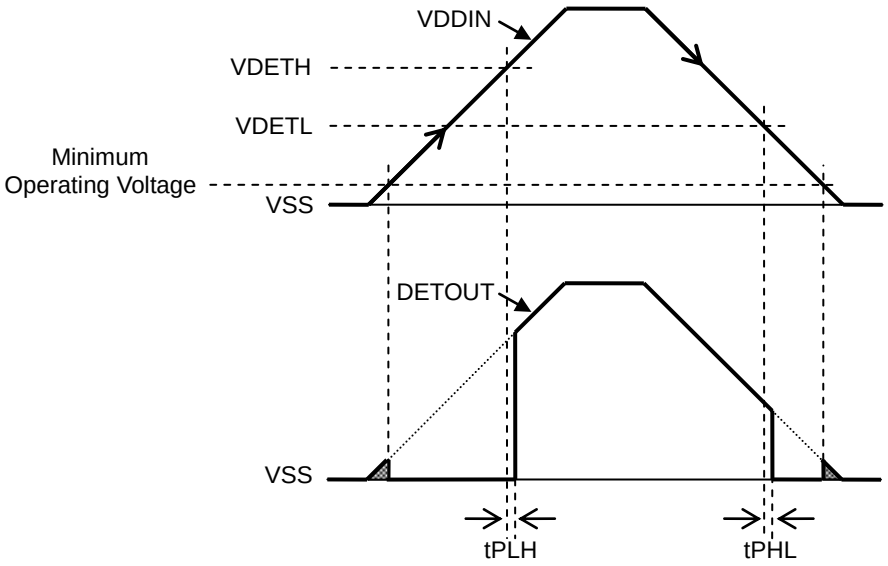


Figure 2. Operation

10. Example Application

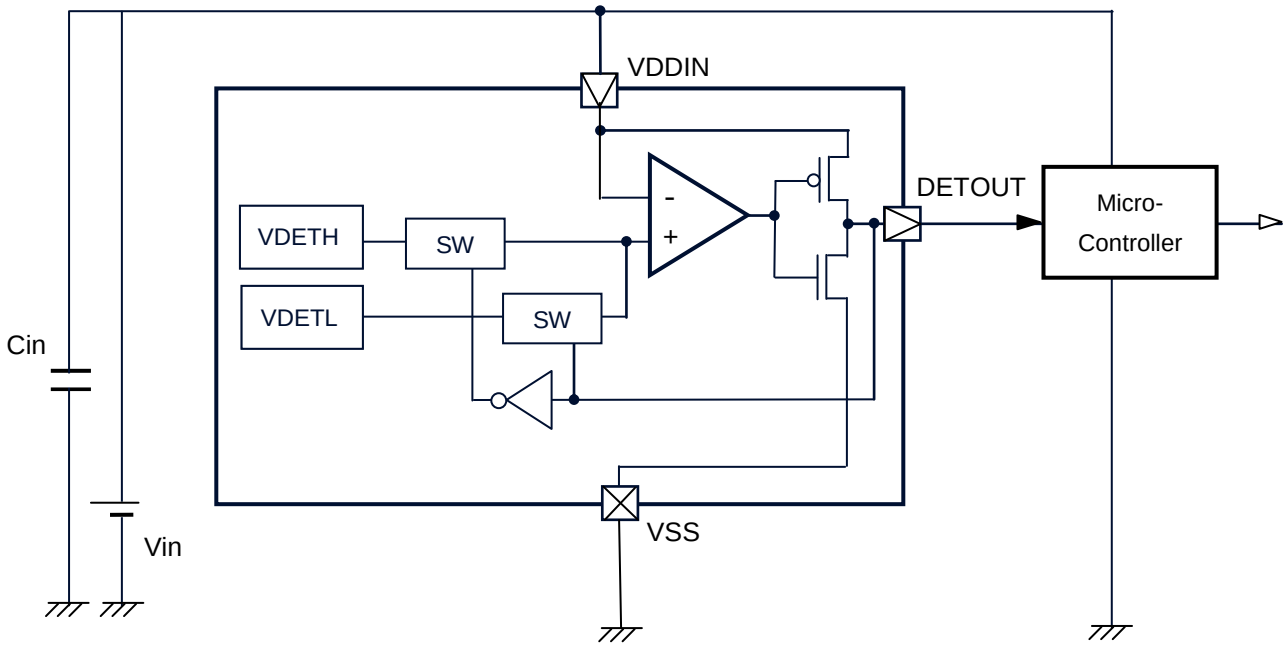


Figure 3. Microprocessor Reset Circuit

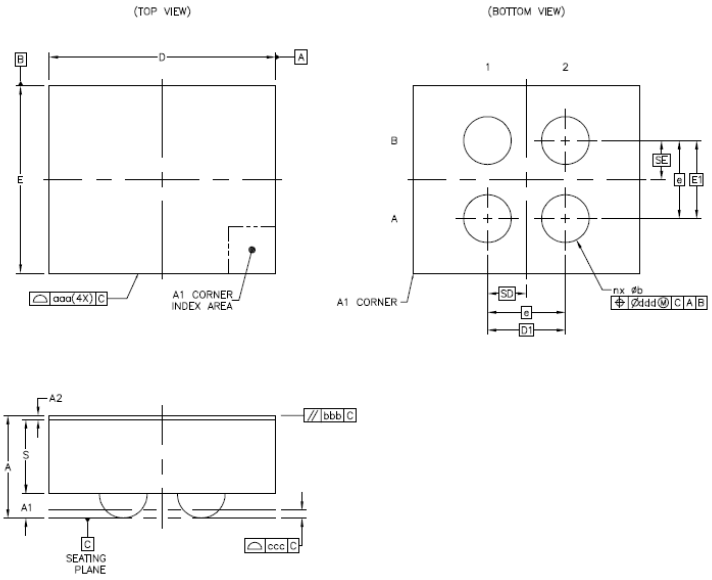
Note 8. When a user control VDDIN falling voltage using DETOUT turnover timing, please add Cin near VDDIN pin and VSS pin depends on load condition.

11. Package

■Outline Dimensions

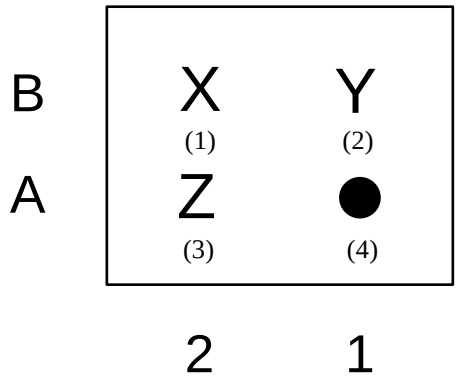
WLCSP 4-pin (Unit : mm)

When the IC is exposed to light, it might affect the electrical characteristics of the IC due to the light sensitivity of WLCSP package structures.



		SYMBOL	COMMON DIMENSIONS
TOTAL THICKNESS		A	0.525 ± 0.031
WAFER THICKNESS		S	0.378 ± 0.012
STAND OFF		A1	0.11 ~ 0.14
FILM THICKNESS		A2	0.022 ± 0.004
BODY SIZE	X	D	1.16
	Y	E	0.96
BALL/BUMP PITCH	X	SD	0.2 BSC
	Y	SE	0.2 BSC
EDGE BALL CENTER TO CENTER	X	D1	0.4 BSC
	Y	E1	0.4 BSC
PITCH		e	0.4 BSC
BALL DIAMETER (SIZE)			0.2
BALL/BUMP WIDTH		b	0.215 ~ 0.275
BALL/BUMP COUNT		n	4
PACKAGE EDGE TOLERANCE		aaa	0.05
WAFER FLATNESS		bbb	0.1
COPLANARITY		ccc	0.04
BALL/BUMP OFFSET (PACKAGE)		ddd	0.15

■Marking



Top View

(1) X: Year code (last 1 digit)
*If (2) LOT number is occupied, 1 to 9 and 0, and then A to K and L to U and V will be numbered

(2) Y: LOT number
*numbered 1 to 9 by LOT and then A to Z

(3) Z: Part number code

(4) 1 pin Indication

12. Revision History

Date (YY/MM/DD)	Revision	Page	Contents
2016/07/21	00	-	First Edition

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