AAT2511

Dual 600mA, 1MHz Step-Down DC/DC Converter

SystemPower™

General Description

The AAT2511 is a member of AnalogicTech's Total Power Management IC™ (TPMIC™) product family. It is comprised of two 1MHz step-down converters designed to minimize external component size and cost. The input voltage ranges from 2.7V to 5.5V. The output voltage ranges from 0.6V to the maximum applied input voltage and is externally adjustable.

Peak current mode control with internal compensation provides a stable converter with low ESR ceramic output capacitors for extremely low output ripple. Each channel has a low 25µA quiescent operating current, which is critical for maintaining high efficiency at light load.

For maximum battery life, each converter's high-side P-channel MOSFET conducts continuously when the input voltage approaches dropout (100% duty cycle operation).

Both regulators have independent input and enable inputs.

The AAT2511 is available in a Pb-free, thermally-enhanced 12-pin TDFN33 package, and is rated over the -40°C to +85°C temperature range.

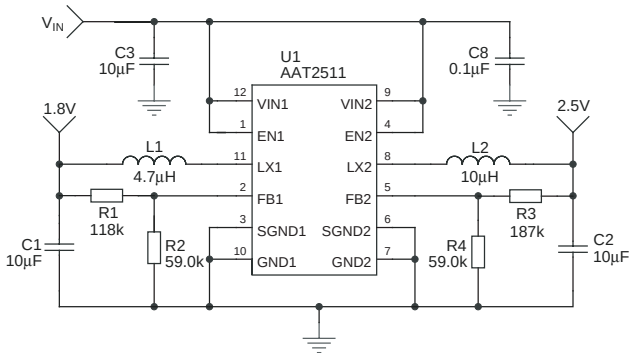
Features

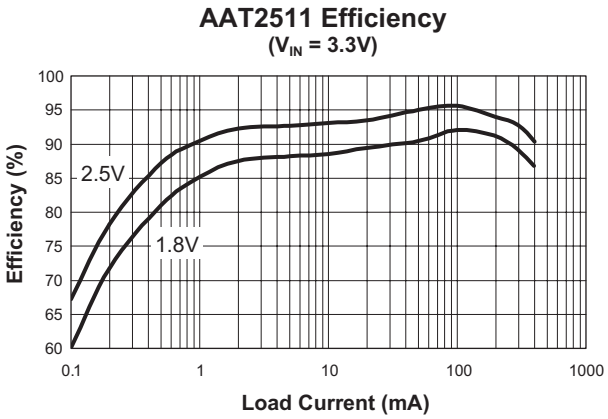
- Up to 97% Efficiency
- 25µA Quiescent Current Per Channel
- V_{IN} Range: 2.7V to 5.5V
- V_{OUT} Range: 0.6V to V_{IN}
- Output Current: 600mA
- Low $R_{DS(ON)}$ 0.4Ω Integrated Power Switches
- Low Drop Out 100% Duty Cycle
- 1.0MHz Switching Frequency
- Shutdown Current <1µA
- Current Mode Operation
- Internal Reference Soft Start
- Short-Circuit Protection
- Fast Turn-On (100µs Typical)
- Over-Temperature Protection
- 3mm x 3mm, < 1mm high
- TDFN33-12 Package
- -40°C to +85°C Temperature Range

Applications

- Cellular Phones
- Digital Cameras
- Handheld Instruments
- Microprocessor/DSP Core/IO Power
- PDAs and Handheld Computers
- Portable Media Players

Typical Application



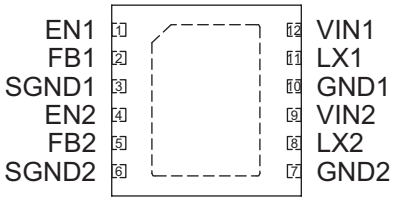


Pin Descriptions

Pin #	Symbol	Function
1, 4	EN1, EN2	Converter enable input. A logic high enables the converter channel. A logic low forces the channel into shutdown mode, reducing the channel supply current to less than 1µA. This pin should not be left floating. When not actively controlled, this pin can be tied directly to the source voltage (VIN1, VIN2).
2, 5	FB1, FB2	Feedback input pin. An external resistive divider ties to this point and programs the output voltage to the desired value.
3, 6	SGND1, SGND2	Signal ground. Return the feedback resistive divider to this ground. See section on PCB layout guidelines and evaluation board layout diagram.
7, 10	GND2, GND1	Main power ground return. Connect to the input and output capacitor return. See section on PCB layout guidelines and evaluation board layout diagram.
8, 11	LX2, LX1	Output switching node that connects to the respective output inductor.
9, 12	VIN2, VIN1	Input supply voltage. Must be closely decoupled to the respective power gnd.
EP		Exposed paddle (bottom). Use properly sized vias for thermal coupling to the ground plane. See section on PCB layout guidelines.

Pin Configuration

TDFN33-12
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{IN}	VIN1, VIN2 to SGND1, SGND2, GND1, and GND2	6.0	V
V_{LX}	LX1, LX2 to GND1, GND2	-0.3 to V_P + 0.3	V
V_{FB}	FB1 and FB2 to SGND1, SGND2, GND1, and GND2	-0.3 to V_P + 0.3	V
V_{EN}	EN1 and EN2 to SGND1, SGND2, GND1, and GND2	-0.3 to 6.0	V
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C

Thermal Information

Symbol	Description	Value	Units
P_D	Maximum Power Dissipation	2	W
θ_{JA}	Thermal Resistance[2]	50	°C/W

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on an FR4 board with exposed paddle connected to ground plane.

Electrical Characteristics[1]

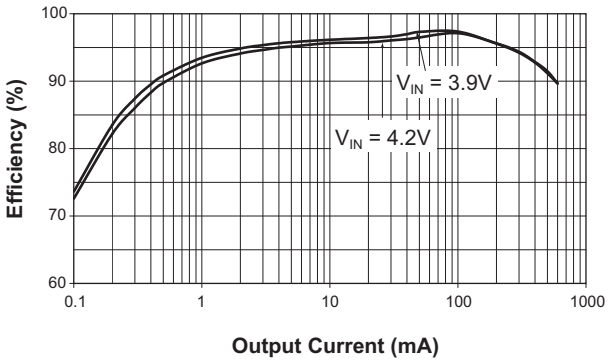
T_A = -40°C to 85°C, unless otherwise noted. Typical values are T_A = 25°C, V_{IN} = 3.6V.

Symbol	Description	Conditions	Min	Typ	Max	Units
Step-Down Converter Channels						
V_{IN}	Input Voltage		2.7		5.5	V
V_{UVLO}	UVLO Threshold	V_{IN} Rising			2.6	V
		Hysteresis		100		mV
		V_{IN} Falling	1.8			V
V_{OUT}	Output Voltage Tolerance	I_{OUT} = 0 to 400mA, V_{IN} = 2.7 - 5.5V	-3.0		+3.0	%
V_{OUT}	Output Voltage Range		0.6		4.0	V
I_Q	Quiescent Current	No Load, 0.6V Adjustable Version, Per Channel		25	50	µA
I_{SHDN}	Shutdown Current	EN = SGND = GND			1.0	µA
I_{LIM}	P-Channel Current Limit		600			mA
$R_{DS(ON)H}$	High Side Switch On Resistance			0.45		Ω
$R_{DS(ON)L}$	Low Side Switch On Resistance			0.4		Ω
I_{LXLK}	LX Leakage Current	V_{IN} = 5.5V, V_{LX} = 0 to V_{IN}, EN = SGND = GND			1	µA
$\Delta V_{Linereg}$	Line Regulation	V_{IN} = 2.7V to 5.5V			0.2	%/V
V_{FB}	FB Threshold Voltage Accuracy	0.6V Output, No Load, T_A = 25°C	597	600	615	mV
T_S	Start-Up Time	From Enable to Output Regulation		100		µs
F_{OSC}	Oscillator Frequency	T_A = 25°C	0.7	1.0	1.5	MHz
T_{SD}	Over-Temperature Shutdown Threshold			140		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			15		°C
EN						
$V_{EN(L)}$	Enable Threshold Low				0.6	V
$V_{EN(H)}$	Enable Threshold High		1.4			V
I_{EN}	Input Low Current	V_{IN} = V_{FB} = 5.5V	-1.0		1.0	µA

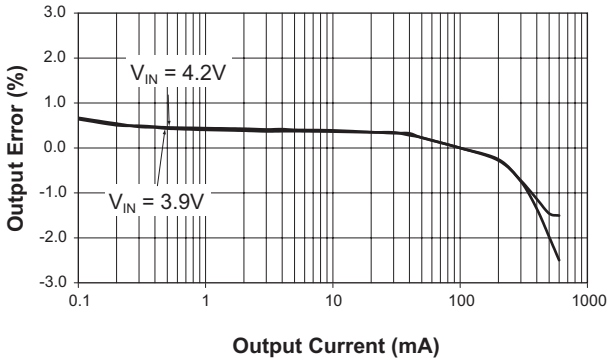
1. The AAT2511 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.
2. For adjustable version with higher than 2.5V output, please consult your AnalogicTech representative.

Typical Channel Characteristics

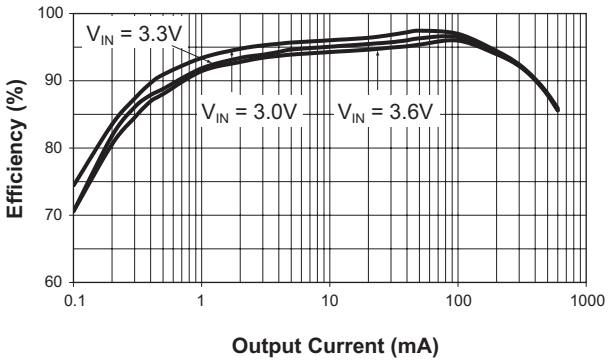
Efficiency vs. Load
(V_{OUT} = 3.3V; L = 10µH)



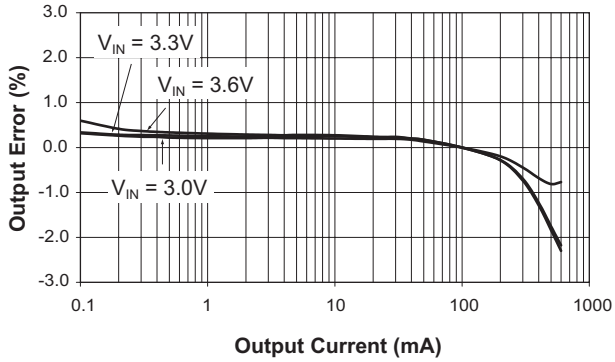
DC Regulation
(V_{OUT} = 3.3V; L = 10µH)



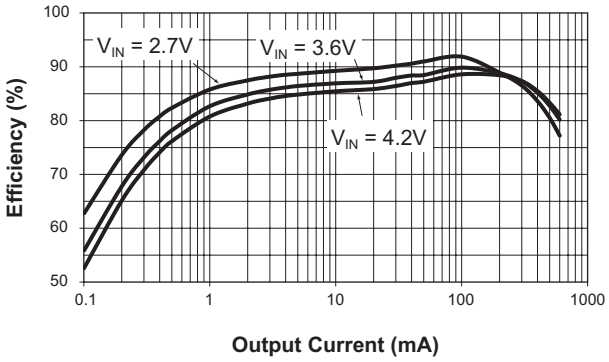
Efficiency vs. Load
(V_{OUT} = 2.5V; L = 10µH)



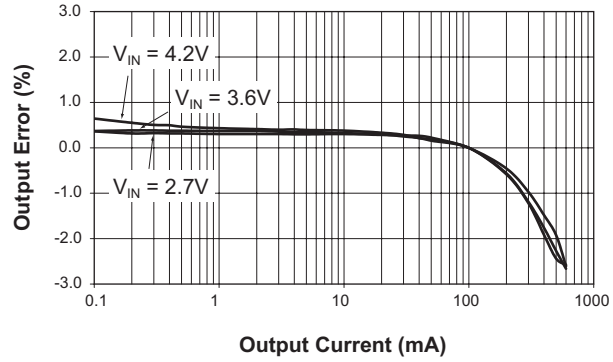
DC Regulation
(V_{OUT} = 2.5V; L = 10µH)



Efficiency vs. Load
(V_{OUT} = 1.5V; L = 4.7µH)

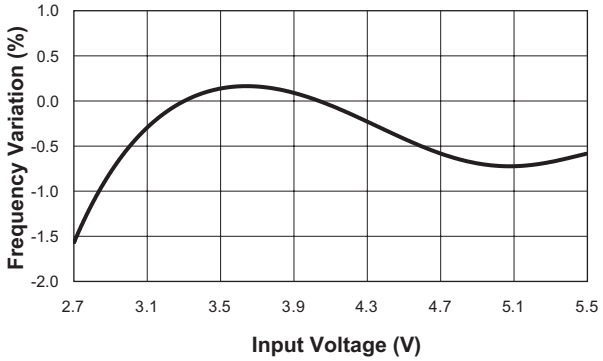


DC Regulation
(V_{OUT} = 1.5V; L = 4.7µH)

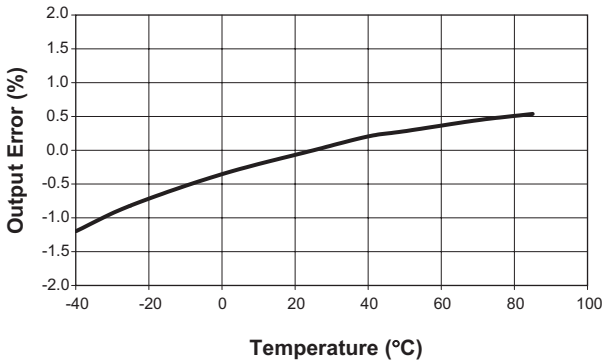


Typical Channel Characteristics

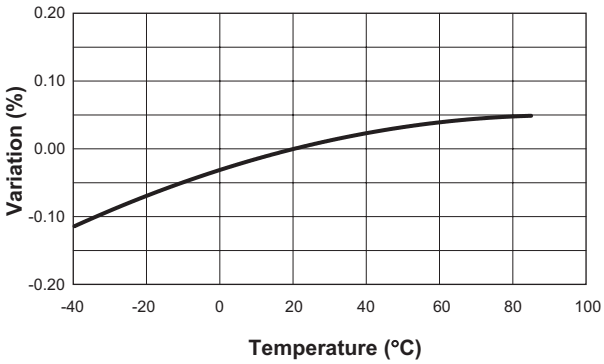
Frequency vs. Input Voltage
(V_{OUT} = 1.8V)



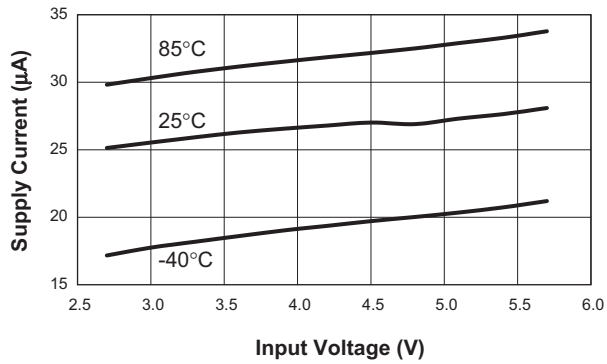
Output Voltage Error vs. Temperature
(V_{IN} = 3.6V; V_O = 2.5V)



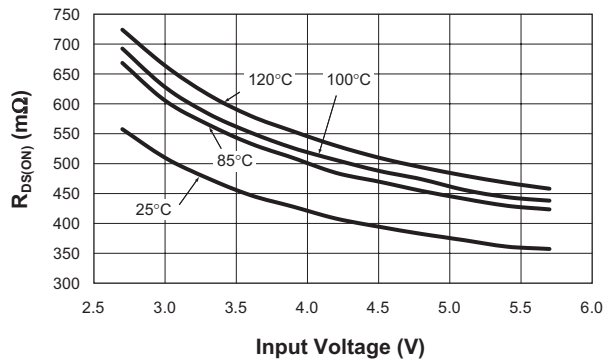
Switching Frequency vs. Temperature
(V_{IN} = 3.6V; V_O = 1.5V)



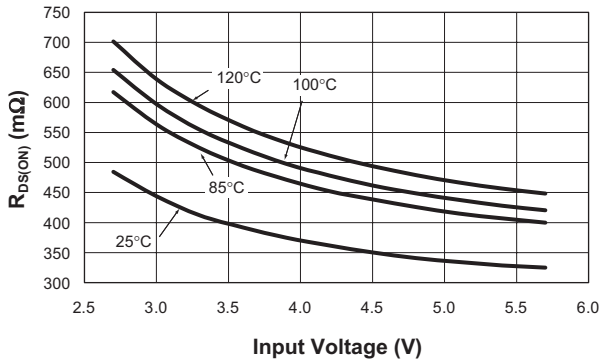
Quiescent Current vs. Input Voltage
(V_O = 1.8V)



P-Channel $R_{DS(ON)}$ vs. Input Voltage

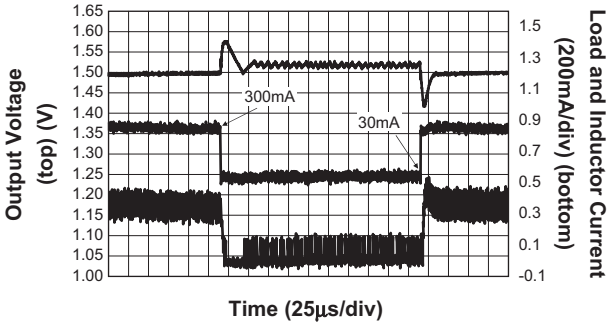


N-Channel $R_{DS(ON)}$ vs. Input Voltage

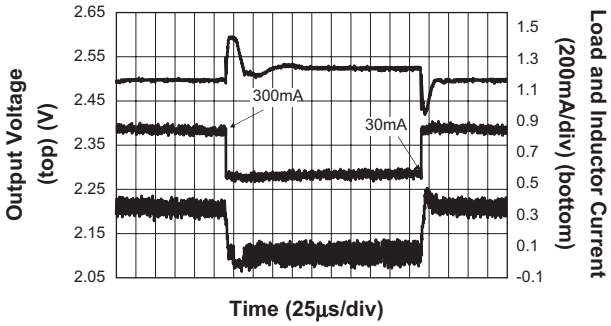


Typical Channel Characteristics

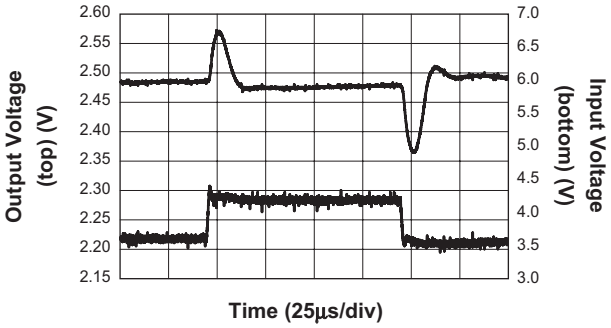
Load Transient Response
($30mA - 300mA; V_{IN} = 3.6V; V_{OUT} = 1.5V; C1 = 22\mu F$)



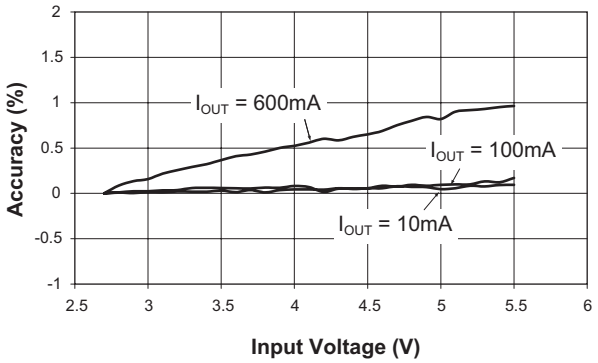
Load Transient Response
($30mA - 300mA; V_{IN} = 3.6V; V_{OUT} = 2.5V; C1 = 22\mu F$)



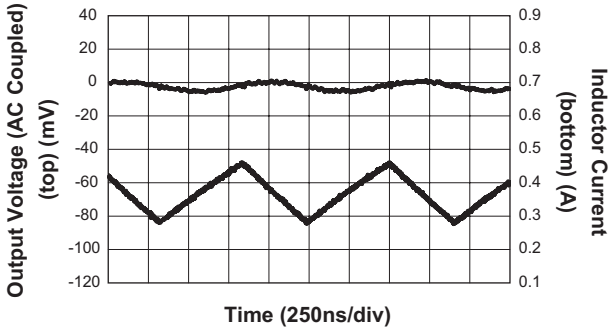
Line Transient
($V_{OUT} = 2.5V$ @ 500mA)



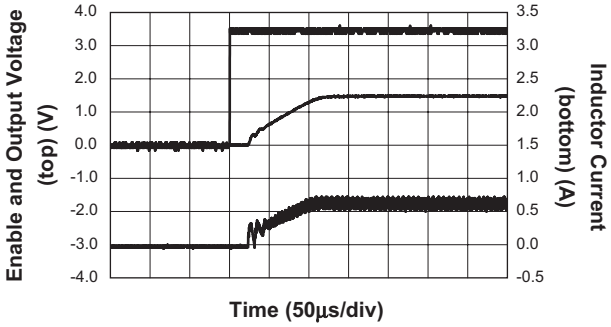
Line Regulation
($V_{OUT} = 1.5V$)



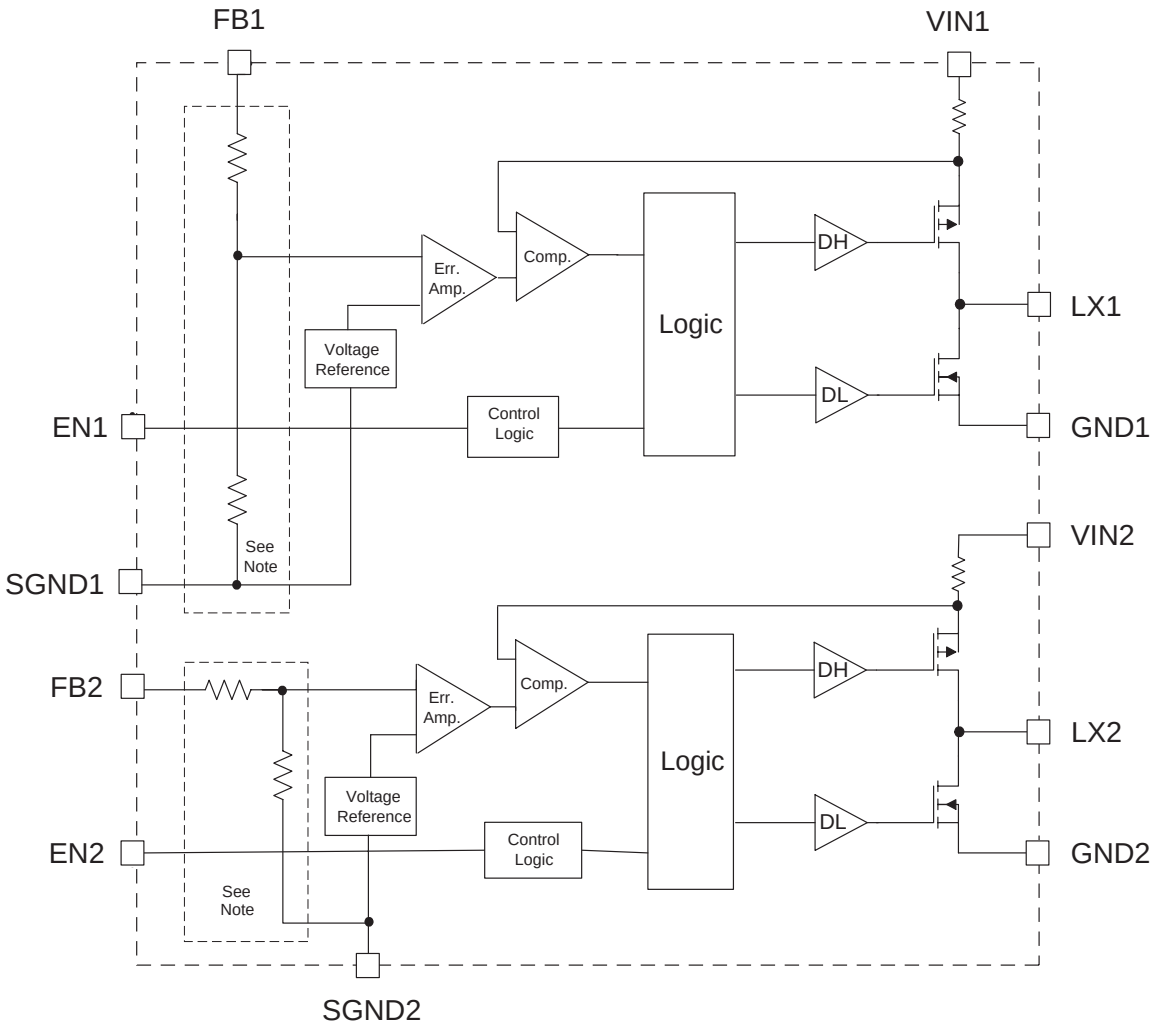
Output Ripple
($V_{IN} = 3.6V; V_{OUT} = 1.8V; 400mA$)



Soft Start
($V_{IN} = 3.6V; V_{OUT} = 1.5V; L = 4.7\mu H$)



Functional Block Diagram



Note: Internal resistor divider included for ≥1.2V versions. For low voltage versions, the feedback pin is tied directly to the error amplifier input.

Operation

Device Summary

The AAT2511 is a constant frequency peak current mode PWM converter with internal compensation. Each channel has independent input, enable, feedback, and ground pins with non-synchronized 1MHz clocks.

Both converters are designed to operate with an input voltage range of 2.7V to 5.5V. The output voltage ranges from 0.6V to the input voltage. The 0.6V fixed model shown in Figure 1 is also the adjustable version and is externally programmable with a resistive divider as shown in Figure 2. The converter MOSFET power stage is sized for 600mA load capability with up to 97% efficiency. Light load efficiency exceeds 80% at a 500µA load.

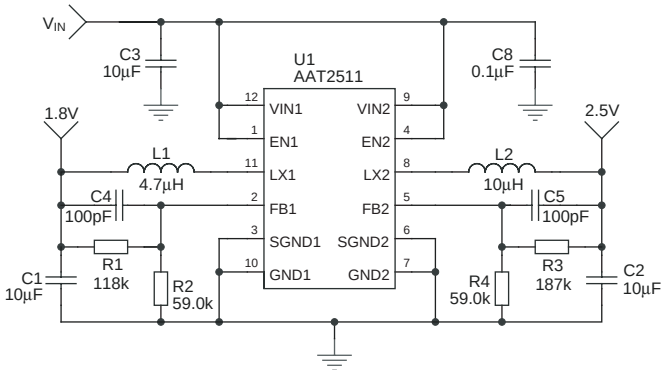


Figure 1: AAT2511 Adjustable Output with Enhanced Transient Response.

Soft Start

The AAT2511 soft-start control prevents output voltage overshoot and limits inrush current when either the input power or the enable input is applied. When pulled low, the enable input forces the converter into a low-power, non-switching state with a bias current of less than 1µA.

Low Dropout Operation

For conditions where the input voltage drops to the output voltage level, the converter duty cycle increases to 100%. As 100% duty cycle is approached, the minimum off-time initially forces the high side on-time to exceed the 1MHz clock cycle and reduce the effective switching frequency. Once the input drops below the level where the output can be regulated, the high side P-channel MOSFET is turned on continuously for 100% duty cycle. At 100% duty cycle, the output voltage tracks the input voltage minus the I*R drop of the high side P-channel MOSFET $R_{DS(ON)}$.

Low Supply

The under-voltage lockout (UVLO) feature guarantees sufficient V_{IN} bias and proper operation of all internal circuitry prior to activation.

Fault Protection

For overload conditions, the peak inductor current is limited. Thermal protection disables switching when the internal dissipation or ambient temperature becomes excessive. The junction over-temperature threshold is 140°C with 15°C of hysteresis.

Applications Information

Inductor Selection

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. The internal slope compensation for the adjustable and low-voltage fixed versions of the AAT2511 is 0.24A/µsec. This equates to a slope compensation that is 75% of the inductor current down slope for a 1.5V output and 4.7µH inductor.

$$m = \frac{0.75 \cdot V_O}{L} = \frac{0.75 \cdot 1.5V}{4.7\mu H} = 0.24 \frac{A}{\mu sec}$$

This is the internal slope compensation for the adjustable (0.6V) version or low-voltage fixed version. When externally programming the 0.6V version to a 2.5V output, the calculated inductance would be 7.5µH.

$$L = \frac{0.75 \cdot V_O}{m} = \frac{0.75V}{0.24A/\mu sec} \approx 3\frac{\mu sec}{A} \cdot V_O$$

$$= 3\frac{\mu sec}{A} \cdot 2.5V = 7.5\mu H$$

In this case, a standard 10µH value is selected.

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

The 4.7µH CDRH3D16 series inductor selected from Sumida has a 105mΩ DCR and a 900mA DC current rating. At full load, the inductor DC loss is 38mW for a 600mA 1.5V output.

Input Capacitor

Select a 4.7µF to 10µF X7R or X5R ceramic capacitor for the input. To estimate the required input capacitor size, determine the acceptable input ripple level (V_{PP}) and solve for C. The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot F_S}$$

This equation provides an estimate for the input capacitor required for a single channel.

Configuration	Output Voltage	Inductor	Slope Compensation
0.6V Adjustable With External Resistive Divider	0.6V to 2.0V	4.7µH	0.24A/µsec
	2.5V	10µH	0.24A/µsec

Table 1: Inductor Values.

The equation below solves for input capacitor size for both channels. It makes the worst-case assumptions that both converters are operating at 50% duty cycle and are synchronized.

$$C_{IN} = \frac{1}{\left(\frac{V_{PP}}{I_{O1} + I_{O2}} - ESR\right) \cdot 4 \cdot F_S}$$

Because the AAT2511 channels will generally operate at different duty cycles and are not synchronized, the actual ripple will vary and be less than the ripple (V_{PP}) used to solve for the input capacitor in the equation above.

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10µF 6.3V X5R ceramic capacitor with 5V DC applied is actually about 6µF.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_{O1} \cdot \left(\sqrt{\frac{V_{O1}}{V_{IN}} \cdot \left(1 - \frac{V_{O1}}{V_{IN}}\right)}\right) + I_{O2} \cdot \left(\sqrt{\frac{V_{O2}}{V_{IN}} \cdot \left(1 - \frac{V_{O2}}{V_{IN}}\right)}\right)$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current of both converters combined.

$$I_{RMS(MAX)} = \frac{I_{O1(MAX)} + I_{O2(MAX)}}{2}$$

This equation also makes the worst-case assumption that both converters are operating at 50% duty cycle and are synchronized. Since the converters are not synchronized and are not both operating at 50% duty cycle, the actual RMS current will always be less than this. Losses associated with the input ceramic capacitor are typically minimal.

The term $\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)$ appears in both the input voltage ripple and input capacitor RMS current equations. It is a maximum when V_O is twice V_{IN}. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT2511. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize the stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple.

The proper placement of the input capacitor (C3 and C8) can be seen in the evaluation board layout in Figure 4. Since decoupling must be as close to the input pins as possible, it is necessary to use two decoupling capacitors. C3 provides the bulk capacitance required for both converters, while C8 is a high frequency bypass capacitor for the second channel (see C3 and C8 placement in Figure 4).

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low ESR ceramic input capacitor, can create a high Q network that may affect converter performance.

This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result.

Since the inductance of a short printed circuit board trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect converter performance, a high ESR tantalum or aluminum electrolytic capacitor should be placed in parallel with the low ESR, ESL bypass ceramic capacitor. This dampens the high Q network and stabilizes the system.

Output Capacitor

The output capacitor limits the output ripple and provides holdup during large load transitions. A 4.7µF to 10µF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabi-

lize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple.

The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current the ceramic output capacitor alone supplies the load current until the loop responds. As the loop responds, the inductor current increases to match the load current demand. This typically takes two to three switching cycles and can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

The internal voltage loop compensation also limits the minimum output capacitor value to 4.7µF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

The maximum output capacitor RMS ripple current is given by:

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F \cdot V_{IN(MAX)}}$$

Dissipation due to the RMS current in the ceramic output capacitor ESR is typically minimal, resulting in less than a few degrees rise in hot spot temperature.

Adjustable Output Resistor Selection

For applications requiring an adjustable output voltage, the 0.6V version can be programmed externally. Resistors R1 through R4 of Figure 1 program the output to regulate at a voltage higher than 0.6V. To limit the bias current required for the external feedback resistor string, the minimum suggested value for R2 and R4 is 59kΩ. Although a larger value will reduce the quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Table 2 summarizes the resistor values for various output voltages with R2 and R4 set to either 59kΩ for good noise immunity or 221kΩ for reduced no load input current.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \cdot R2 = \left(\frac{1.5V}{0.6V} - 1\right) \cdot 59k\Omega = 88.5k\Omega$$

The adjustable version of the AAT2511 in combination with an external feedforward capacitor (C4 and C5 of Figure 1) delivers enhanced transient response for extreme pulsed load applications. The addition of the feedforward capacitor typically requires a larger output capacitor (C1 and C2) for stability.

	R2, R4 = 59kΩ	R2, R4 = 221kΩ
V_{OUT} (V)	R1, R3 (kΩ)	R1, R3 (kΩ)
0.8	19.6	75
0.9	29.4	113
1.0	39.2	150
1.1	49.9	187
1.2	59.0	221
1.3	68.1	261
1.4	78.7	301
1.5	88.7	332
1.8	118	442
1.85	124	464
2.0	137	523
2.5	187	715

Table 2: Adjustable Resistor Values For Use With 0.6V Version.

Thermal Calculations

There are three types of losses associated with the AAT2511 converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the dual converter losses is given by:

$$P_{TOTAL} = \frac{I_{O1}^2 \cdot (R_{DSON(HS)} \cdot V_{O1} + R_{DSON(LS)} \cdot [V_{IN} - V_{O1}])}{V_{IN}}$$

$$+ \frac{I_{O2}^2 \cdot (R_{DSON(HS)} \cdot V_{O2} + R_{DSON(LS)} \cdot [V_{IN} - V_{O2}])}{V_{IN}}$$

$$+ (t_{sw} \cdot F \cdot [I_{O1} + I_{O2}] + 2 \cdot I_Q) \cdot V_{IN}$$

I_Q is the AAT2511 quiescent current for one channel and t_{sw} is used to estimate the full load switching losses.

For the condition where channel one is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_{TOTAL} = I_{O1}^2 \cdot R_{DSON(HS)}$$

$$+ \frac{I_{O2}^2 \cdot (R_{DSON(HS)} \cdot V_{O2} + R_{DSON(LS)} \cdot [V_{IN} - V_{O2}])}{V_{IN}}$$

$$+ (t_{sw} \cdot F \cdot I_{O2} + 2 \cdot I_Q) \cdot V_{IN}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the TDFN33-12 package which is 50°C/W.

$$T_{J(MAX)} = P_{TOTAL} \cdot \Theta_{JA} + T_{AMB}$$

PCB Layout

The following guidelines should be used to insure a proper layout.

1. Due to the pin placement of V_{IN} for both converters, proper decoupling is not possible with just one input capacitor. The large input capacitor C3 should connect as closely as possible to V_P and GND, as shown in Figure 3. The additional input bypass capacitor C8 is necessary for proper high frequency decoupling of the second converter.
2. The output capacitor and inductor should be connected as closely as possible. The connection of the inductor to the LX pin should also be as short as possible.
3. The feedback trace should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation. If external feedback resistors are used, they should be placed as closely as possible to the FB pin. This prevents noise from being coupled into the high impedance feedback node.
4. The resistance of the trace from the load return to GND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. For good thermal coupling, PCB vias are required from the pad for the TDFN paddle to the ground plane. The via diameter should be 0.3mm to 0.33mm and positioned on a 1.2 mm grid.

Design Example

Specifications

V_{O1} = 2.5V @ 600mA (adjustable using 0.6V version), pulsed load ΔI_{LOAD} = 300mA

V_{O2} = 1.8V @ 600mA (adjustable using 0.6V version), pulsed load ΔI_{LOAD} = 300mA

V_{IN} = 2.7V to 4.2V (3.6V nominal)

F_S = 1.0 MHz

T_{AMB} = 85°C

2.5V V_{O1} Output Inductor

$$L1 = 3\frac{\mu sec}{A} \cdot V_{O1} = 3\frac{\mu sec}{A} \cdot 2.5V = 7.5\mu H$$ (see Table 1)

For Sumida inductor CDRH3D16, 10µH, DCR = 210mΩ.

$$\Delta I1 = \frac{V_O}{L1 \cdot F} \cdot \left(1 - \frac{V_{O1}}{V_{IN}}\right) = \frac{2.5V}{10\mu H \cdot 1.0MHz} \cdot \left(1 - \frac{2.5V}{4.2V}\right) = 100mA$$

$$I_{PK1} = I_{O1} + \frac{\Delta I1}{2} = 0.6A + 0.05A = 0.65A$$

$$P_{L1} = I_{O1}^2 \cdot DCR = (0.4A)^2 \cdot 210m\Omega = 76mW$$

1.8V V_{O2} Output Inductor

$$L2 = 3\frac{\mu sec}{A} \cdot V_{O2} = 3\frac{\mu sec}{A} \cdot 1.8V = 5.4\mu H$$ (see Table 1)

For Sumida inductor CDRH3D16, 4.7µH, DCR = 105mΩ.

$$\Delta I2 = \frac{V_{O2}}{L \cdot F} \cdot \left(1 - \frac{V_{O2}}{V_{IN}}\right) = \frac{1.8V}{4.7\mu H \cdot 1.0MHz} \cdot \left(1 - \frac{1.8V}{4.2V}\right) = 218mA$$

$$I_{PK2} = I_{O2} + \frac{\Delta I2}{2} = 0.6A + 0.11A = 0.71A$$

$$P_{L2} = I_{O2}^2 \cdot DCR = (0.6A)^2 \cdot 105m\Omega = 38mW$$

2.5V Output Capacitor

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S} = \frac{3 \cdot 0.6A}{0.2V \cdot 1MHz} = 9\mu F$$

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{(V_{OUT}) \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F \cdot V_{IN(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{2.5V \cdot (4.2V - 2.5V)}{10\mu H \cdot 1MHz \cdot 4.2V} = 29mArms$$

$$P_{esr} = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (29mA)^2 = 4.2\mu W$$

1.8V Output Capacitor

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S} = \frac{3 \cdot 0.6A}{0.2V \cdot 1MHz} = 9\mu F$$

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{(V_{OUT}) \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F \cdot V_{IN(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{1.8V \cdot (4.2V - 1.8V)}{4.7\mu H \cdot 1.0MHz \cdot 4.2V} = 63mArms$$

$$P_{esr} = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (63mA)^2 = 20\mu W$$

Input Capacitor

Input Ripple V_{PP} = 25mV.

$$C_{IN} = \frac{1}{\left(\frac{V_{PP}}{I_{O1} + I_{O2}} - ESR\right) \cdot 4 \cdot F_S} = \frac{1}{\left(\frac{25mV}{1.2A} - 5m\Omega\right) \cdot 4 \cdot 1MHz} = 15.78\mu F$$

$$I_{RMS(MAX)} = \frac{I_{O1} + I_{O2}}{2} = 6Arms$$

$$P = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (0.6A)^2 = 1.8mW$$

AAT2511 Losses

The maximum dissipation occurs at dropout where V_{IN} = 2.7V. All values assume an ambient temperature of 85°C and a junction temperature of 120°C.

$$P_{TOTAL} = \frac{I_{O1}^2 \cdot (R_{DSON(HS)} \cdot V_{O1} + R_{DSON(LS)} \cdot (V_{IN} - V_{O1})) + I_{O2}^2 \cdot (R_{DSON(HS)} \cdot V_{O2} + R_{DSON(LS)} \cdot (V_{IN} - V_{O2}))}{V_{IN}}$$

$$+ (t_{sw} \cdot F \cdot I_{O2} + 2 \cdot I_Q) \cdot V_{IN}$$

$$= \frac{0.6^2 \cdot (0.725\Omega \cdot 2.5V + 0.7\Omega \cdot (2.7V - 2.5V)) + 0.6^2 \cdot (0.725\Omega \cdot 1.8V + 0.7\Omega \cdot (2.7V - 1.8V))}{2.7V}$$

$$+ 5ns \cdot 1MHz \cdot 0.6A + 60\mu A) \cdot 2.7V = 527mW$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P_{LOSS} = 85°C + (50°C/W) \cdot 527mW = 111°C$$

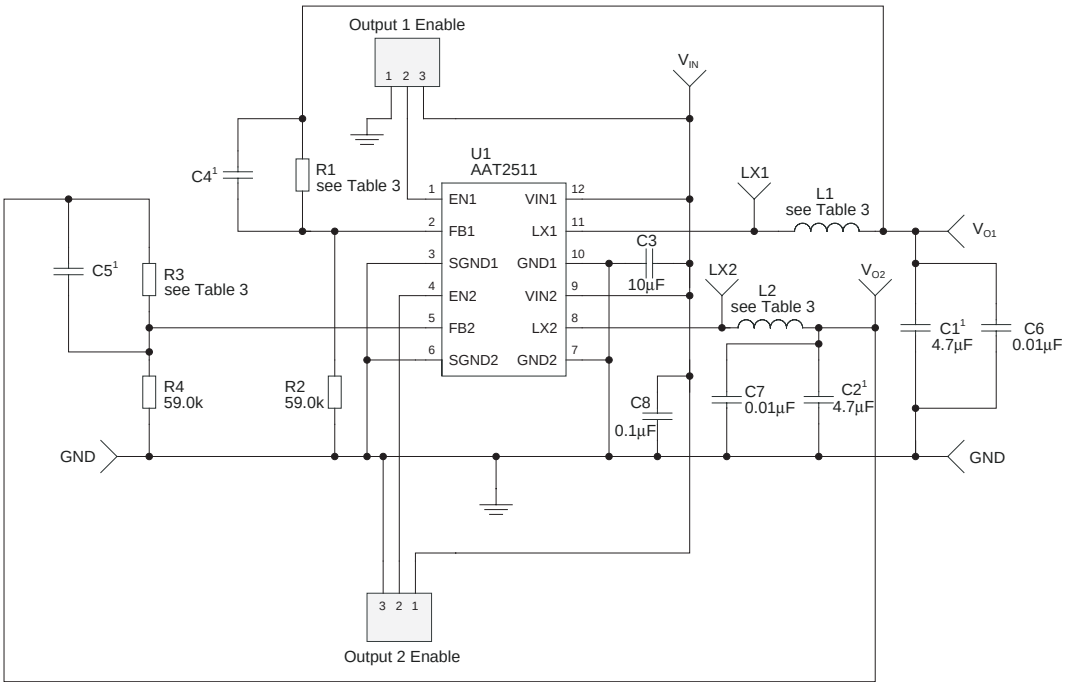


Figure 2: AAT2511 Evaluation Board Schematic.

1. For enhanced transient configuration C5, C4 = 100pF and C1, C2 = 10µF.

Adjustable Version (0.6V device)	R2, R4 = 59kΩ	R2, R4 = 221kΩ[1]	
V_{OUT} (V)	R1, R3 (kΩ)	R1, R3 (kΩ)	L1, L2 (µH)
0.8	19.6	75.0	4.7
0.9	29.4	113	4.7
1.0	39.2	150	4.7
1.1	49.9	187	4.7
1.2	59.0	221	4.7
1.3	68.1	261	4.7
1.4	78.7	301	4.7
1.5	88.7	332	4.7
1.8	118	442	4.7
1.85	124	464	4.7
2.0	137	523	4.7 or 6.8
2.5	187	715	10

Table 3: Evaluation Board Component Values.

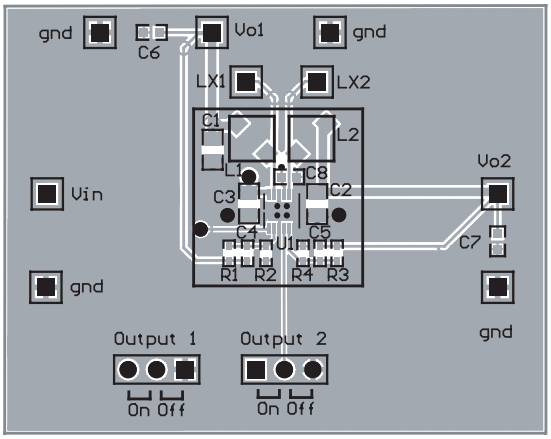


Figure 3: AAT2511 Evaluation Board Top Side.

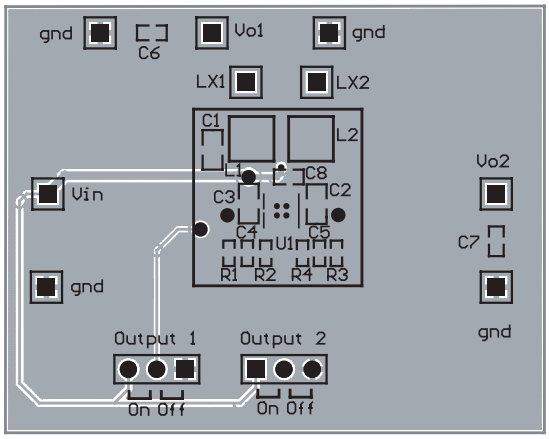


Figure 4: AAT2511 Evaluation Board Bottom Side.

1. For reduced quiescent current, R2 and R4 = 221kΩ.

Manufacturer	Part Number	Inductance (µH)	Max DC Current (A)	DCR (Ω)	Size (mm) LxWxH	Type
Sumida	CDRH3D16-4R7	4.7	0.90	0.11	3.8x3.8x1.8	Shielded
Sumida	CDRH3D16-100	10	0.55	0.21	3.8x3.8x1.8	Shielded
MuRata	LQH32CN4R7M23	4.7	0.45	0.20	2.5x3.2x2.0	Non-Shielded
MuRata	LQH32CN4R7M33	4.7	0.65	0.15	2.5x3.2x2.0	Non-Shielded
MuRata	LQH32CN4R7M53	4.7	0.65	0.15	2.5x3.2x1.55	Non-Shielded
Coilcraft	LPO6610-472	4.7	1.10	0.20	5.5x6.6x1.0	1mm
Coilcraft	LPO3310-472	4.7	0.80	0.27	3.3x3.3x1.0	1mm
Coiltronics	SDRC10-4R7	4.7	1.53	0.117	4.5x3.6x1.0	1mm Shielded
Coiltronics	SDR10-4R7	4.7	1.30	0.122	5.7x4.4x1.0	1mm Shielded
Coiltronics	SD3118-4R7	4.7	0.98	0.122	3.1x3.1x1.85	Shielded
Coiltronics	SD18-4R7	4.7	1.77	0.082	5.2x5.2x1.8	Shielded

Table 4: Typical Surface Mount Inductors.

Manufacturer	Part Number	Value	Voltage	Temp. Co.	Case
MuRata	GRM219R61A475KE19	4.7µF	10V	X5R	0805
MuRata	GRM21BR60J106KE19	10uF	6.3V	X5R	0805
MuRata	GRM21BR60J226ME39	22uF	6.3V	X5R	0805

Table 5: Surface Mount Capacitors.

Ordering Information

Package	Voltage		Marking[1]	Part Number (Tape and Reel)[2]
	Channel 1	Channel 2		
TDFN33-12	0.6V	0.6V	QRXYY	**AAT2511IWP-AA-T1**

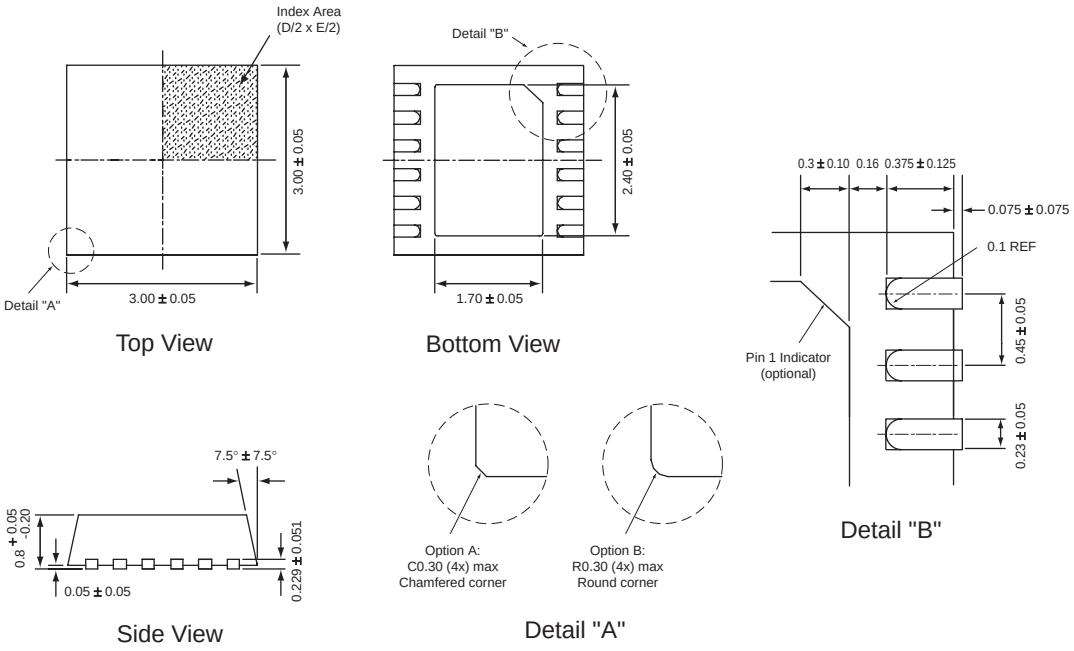
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Legend	
Voltage	**Code**
Adjustable (0.6V)	A
1.2	E
1.5	G
1.6	H
1.8	I
1.9	Y
2.5	N
2.6	O
2.7	P
2.8	Q
2.85	R
2.9	S
3.0	T
3.3	W

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

Package Information

TDFN33-12



All dimensions in millimeters.

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Advanced Analogic Technologies, Inc.
830 E. Arques Avenue, Sunnyvale, CA 94085
Phone (408) 737-4600
Fax (408) 737-4611