NEC

MOS INTEGRATED CIRCUIT

μPD75P316A

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD75P316A is a product of the μPD75316 with on-chip ROM having been replaced with the one-time PROM or EPROM.

It is most suitable for test production during system development and for production in small amounts since it can operate under the same supply voltage as mask products.

The one-time PROM product is capable of writing only once and is effective for production of many kinds of sets in small quantities and early startup. The EPROM product allows program writing and rewriting, and is therefore suitable for system evaluation. The on-chip RAM has twice the capacity of the μPD75316/75P316, enabling large amounts of data to be processed.

Details of functions are described in the User's Manual shown below. Be sure to read in design.
μPD75308 User's Manual : IEM-5016

FEATURES

- Compatible (excluding mask option) with the mask products
- Memory capacity
  - Program memory (PROM) : 16256 × 8 bits
  - Data memory (RAM) : 1024 × 4 bits
- Low-voltage operation capability: 2.7 to 6.0 V

ORDERING INFORMATION

Ordering Code	Package	On-Chip ROM
μPD75P316AGF-3B9	80-pin plastic QFP (14 × 20 mm)	One-time PROM
μPD75P316AK	80-pin ceramic WQFN (LCC with window)	EPROM

QUALITY GRADE

Ordering Code	Package	Quality Grade
μPD75P316AGF-3B9	80-pin plastic QFP (14 × 20 mm)	Standard
μPD75P316AK	80-pin ceramic WQFN (LCC with window)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

In descriptions common to one-time PROM products and EPROM products in this document, the term "PROM" is used.

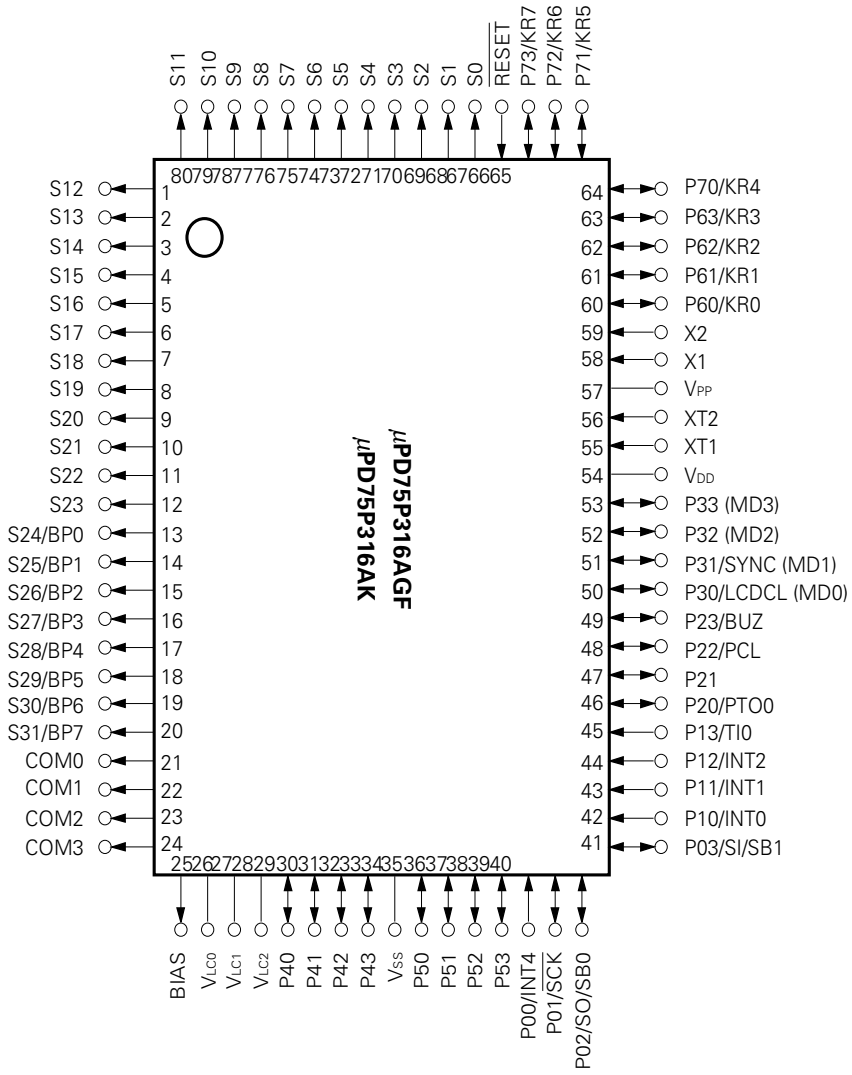
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Date Published October 1993 P
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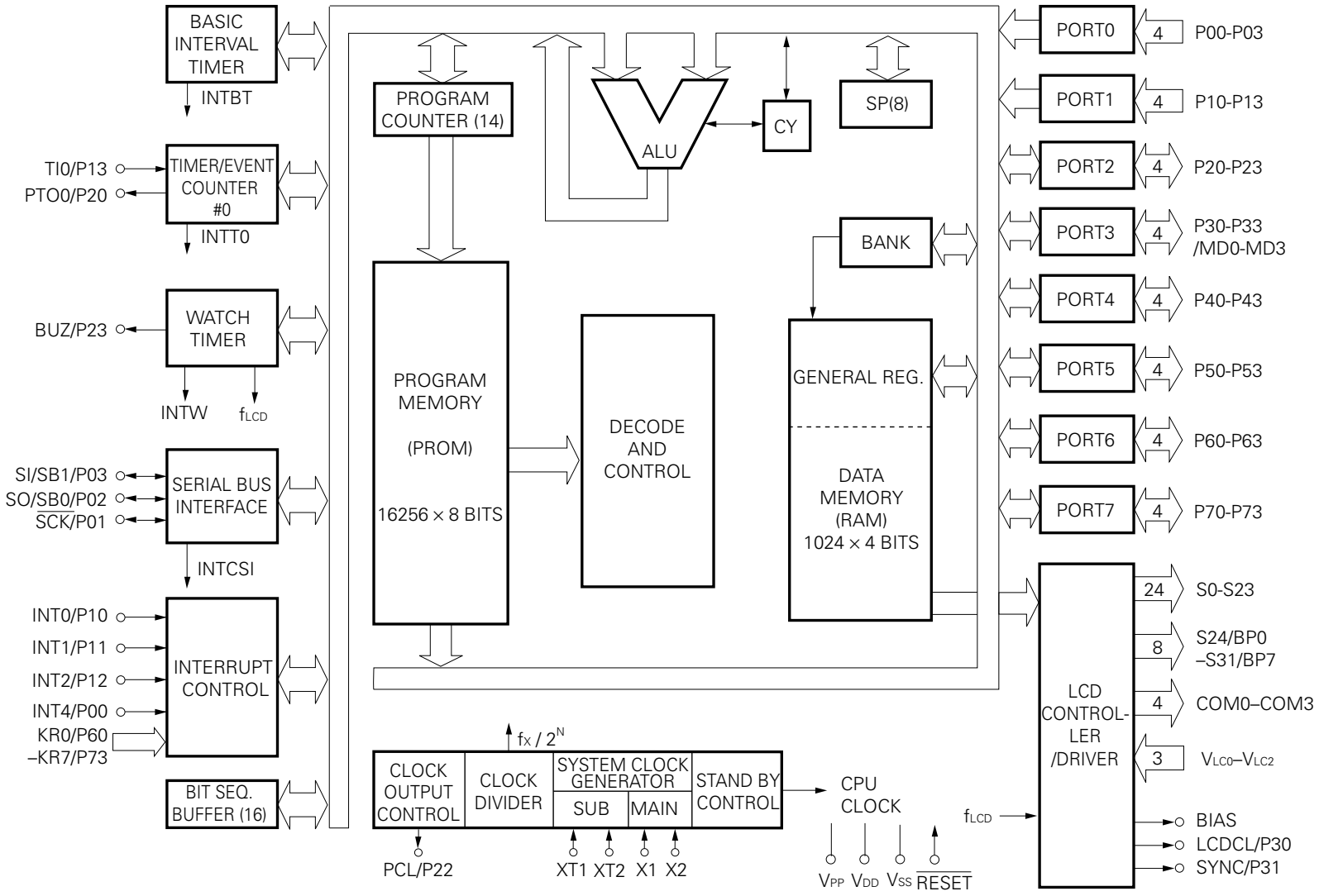
The mark ★ shows major revised points.

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PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



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1. PIN FUNCTIONS

1.1 PORT PINS (1/2)

Pin Name	Input/Output	Dual-Function Pin	Function	8-Bit I/O	Afer Reset	I/O Circuit Type*1
P00	Input	INT4	4-bit input port (PORT0) Internal pull-up resistor specification by software is possible for P01 to P03 as a 3-bit unit.	×	Input	Ⓑ
P01	Input/output	$\overline{SCK}$				Ⓕ - A
P02	Input/output	SO/SB0				Ⓕ - B
P03	Input/output	SI/SB1				Ⓜ - C
P10	Input	INT0	With noise elimination circuit	×	Input	Ⓑ - C
P11		INT1	4-bit input port (PORT1) Internal pull-up resistor specification by software is possible as a 4-bit unit.			
P12		INT2				
P13		TI0				
P20	Input/output	PTO0	4-bit input/output port (PORT2) Internal pull-up resistor specification by software is possible as a 4-bit unit.	×	Input	E - B
P21		—				
P22		PCL				
P23		BUZ				
P30 *2	Input/output	LCDCL / MD0	Programmable 4-bit input/output port (PORT3) Input/output settable bit-wise. Internal pull-up resistor specification by software is possible as a 4-bit unit.	×	Input	E - B
P31 *2		SYNC / MD1				
P32 *2		MD2				
P33 *2		MD3				
P40 to P43*2	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 4). Data input/output pins for program memory (PROM) write/verify (low-order 4 bits).	○	High impedance	M - A
P50 to P53 *2	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 5) Data input/output pins for program memory (PROM) write/verify (high-order 4 bits).		High impedance	M - A
P60	Input/output	KR0	Programmable 4-bit input/output port (PORT6). Input/output settable bit-wise. Internal pull-up resistor specification by software is possible as a 4-bit unit.	○	Input	Ⓕ - A
P61		KR1				
P62		KR2				
P63		KR3				
P70	Input/output	KR4	4-bit input/output port (PORT7). Internal pull-up resistor specification by software is possible as a 4-bit unit.		Input	Ⓕ - A
P71		KR5				
P72		KR6				
P73		KR7				

* **1.** ◯ : Indicates a Schmitt-triggered input.
2 . Direct LED drive capability.

1.1 PORT PINS (2/2)

Pin Name	Input/Output	Dual-Function Pin	Function	8-Bit I/O	After Reset	I/O Circuit TYPE
BP0	Output	S24	1-bit output port (BIT PORT) Dual-function as segment output pins.	×	*	G - C
BP1		S25				
BP2		S26				
BP3		S27				
BP4	Output	S28				
BP5		S29				
BP6		S30				
BP7		S31				

* For BP0 to BP7, V_{LC1} is selected as the input source. The output level depends on BP0 to BP7 and the V_{LC1} external circuit, however.

1.2 OTHER PINS

Pin Name	Input/Output	Dual-Function Pin	Function	After Reset	I/O Circuit Type *1
TI0	Input	P13	External event pulse input pin for timer/event counter.	—	Ⓑ - C
PTO0	output	P20	Timer/event counter output pin	Input	E - B
PCL	Input/output	P22	Clock output pin	Input	E - B
BUZ	Input/output	P23	Fixed frequency output pin (for buzzer or system clock trimming)	Input	E - B
$\overline{SCK}$	Input/output	P01	Serial clock input/output pin	Input	Ⓕ - A
SO/SB0	Input/output	P02	Serial data output pin Serial bus input/output pin	Input	Ⓕ - B
SI/SB1	Input/output	P03	Serial data input pin Serial bus input/output pin	Input	Ⓜ - C
INT4	Input	P00	Edge-detected vectored interrupt input pin (rising or falling edge detection).	—	Ⓑ
INT0	Input	P10	Edge-detected vectored interrupt input pin (detection edge selectable)	—	Ⓑ - C
INT1		P11			
INT2	Input	P12	Edge-detected testable input pin (rising edge detection)	—	Ⓑ - C
KR0 to KR3	Input/output	P60 to P63	Testable Input/output pins (parallel falling edge detection)	Input	Ⓕ - A
KR4 to KR7	Input/output	P70 to P73	Testable Input/output pins (parallel falling edge detection)	Input	Ⓕ - A
S0 to S23	Output	—	Segment signal output pins	*3	G - A
S24 to S31	Output	BP0 to 7	Segment signal output pins	*3	G - C
COM0 to COM3	Output	—	Common signal output pins	*3	G - B
V_{LC0} to V_{LC2}	—	—	LCD drive power supply pins	—	—
BIAS	—	—	External split cutting output pin	High impedance	—
LCDCL*2	Input/output	P30	External extension driver drive clock output pin	Input	E - B
SYNC*2	Input/output	P31	External extension driver synchronization clock output pin	Input	E - B
X1, X2	Input	—	Main system clock oscillation crystal/ceramic connection pins. When an external clock is used, the clock is input to X1 and the inverted clock to X2.	—	—
XT1, XT2	Input	—	Subsystem clock oscillation crystal connection pins When an external clock is used, the clock is input to XT1 and the inverted clock to XT2. XT1 can be used as a 1-bit input (test) pin.	—	—
$\overline{RESET}$	Input	—	System reset input pin (low-level active).	—	Ⓑ
MD0 to MD3	Input/output	P30 to P33	Mode selection pin for program memory (PROM) write/verify.	Input	E - B
V_{PP}	—	—	Program voltage application pin for program memory (PROM) write/verify . Connected to V_{DD} in normal operation. Applies +12.5 V in program memory write/verify.	—	—
V_{DD}	—	—	Positive power supply pin	—	—
V_{SS}	—	—	GND potential pin	—	—

* **1.** ◯ : Indicates a Schmitt-triggered input.

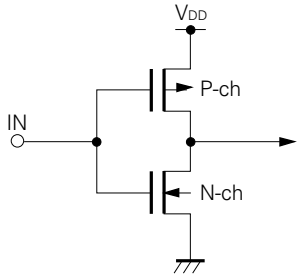
2. Pins provided for future system expansion. Currently used only as pins 30 and 31.

3. V_{LCX} shown below can be selected for display outputs.
S0 to S31: V_{LC1}, COM0 to COM2: V_{LC2} , COM3: V_{LC0}
However, display output levels depend on the display output and V_{LCX} external circuit.

1.3 PIN INPUT/OUTPUT CIRCUITS

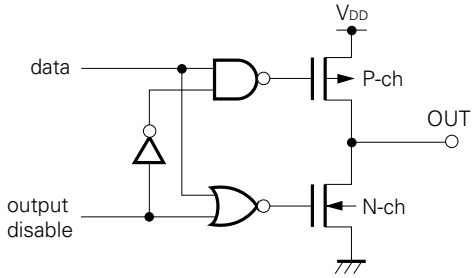
The input/output circuits of each pin of the μPD75P316A are shown by in abbreviated form.

TYPE A (For TYPE E-B)



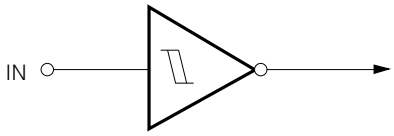
CMOS standard input buffer

TYPE D (For TYPE E-B, F-A)



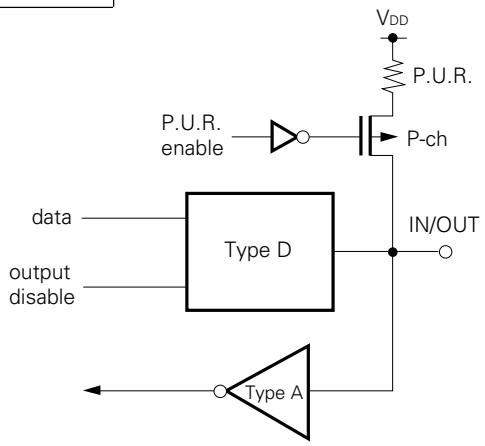
Push-pull output that can be made high-impedance output (P-ch and N-ch OFF)

TYPE B



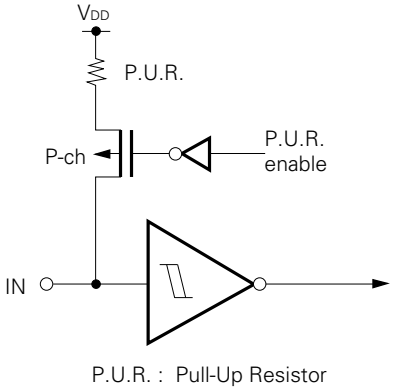
Schmitt trigger input with hysteresis characteristic

TYPE E-B



P.U.R.:Pull-Up Resistor

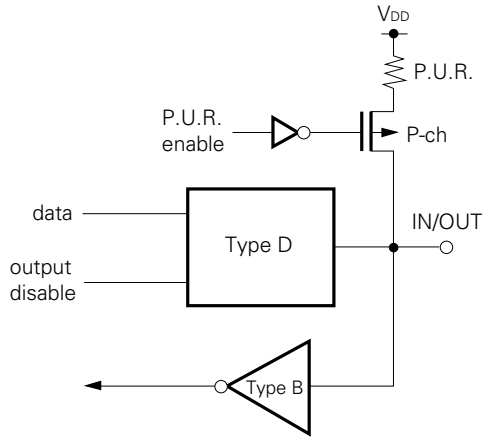
TYPE B-C



P.U.R. : Pull-Up Resistor

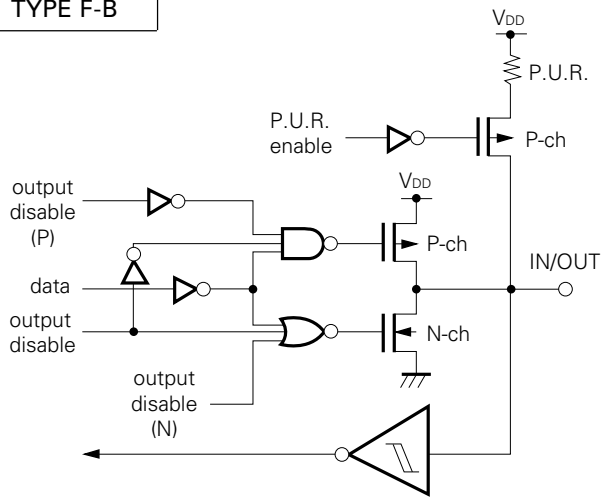
Schmitt trigger input with hysteresis characteristic

TYPE F-A



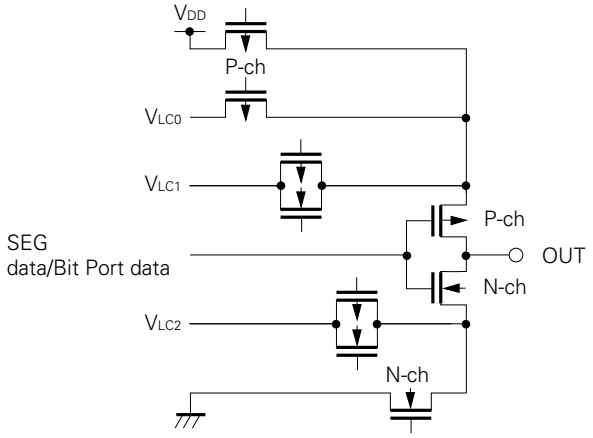
P.U.R.:Pull-Up Resistor

TYPE F-B

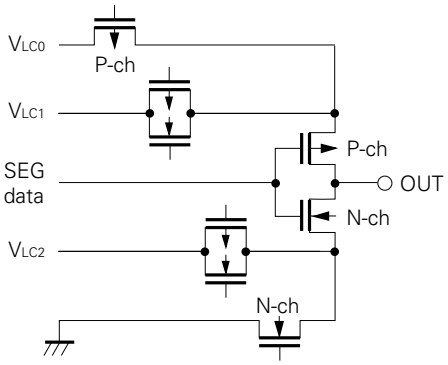


P.U.R.:Pull-Up Resistor

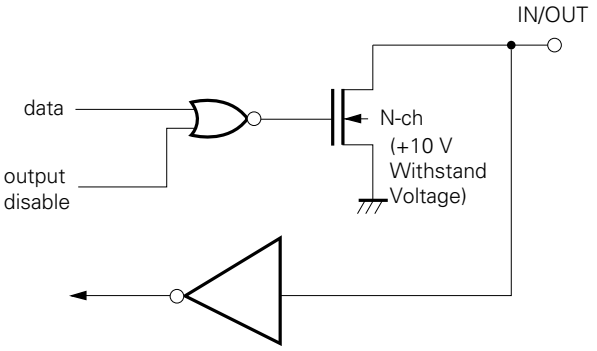
TYPE G-C



TYPE G-A

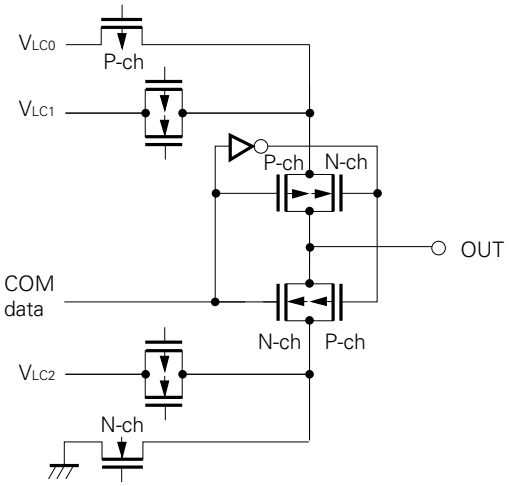


TYPE M-A

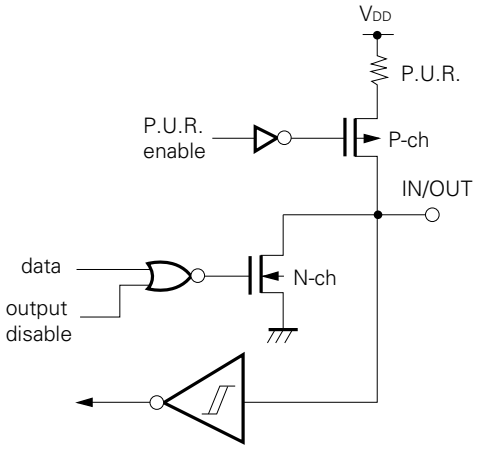


Middle-High Voltage Input Buffer
(+10 V Withstand Voltage)

TYPE G-B



TYPE M-C



P.U.R.:Pull-Up Resistor

1.4 CAUTION ON USING P00/INT4 PIN AND RESET PIN ★

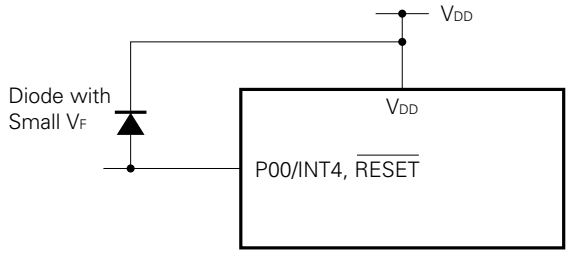
The P00/INT4 and $\overline{\text{RESET}}$ pins have a test mode setting function (IC test only) which tests internal operations of the μPD75P316A in addition to those functions given in 1.1 and 1.2.

The test mode is set when voltage greater than V_{DD} is applied to either pin. Therefore, even during normal operation, the test mode is engaged when noise greater than V_{DD} is added, thus causing interference with normal operation.

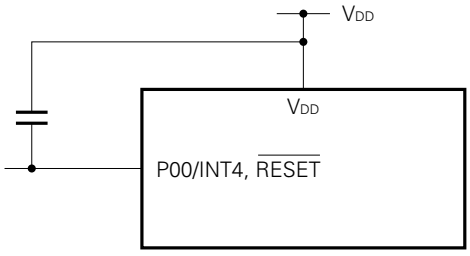
For example, this problem may occure if the P00/INT4 and $\overline{\text{RESET}}$ pins wiring is too long, causing line noise.

To avoid this, try to suppress line noise in wiring. If line noise is still high, try elimminating the noise using the exterior add-on components shown in the Figures below.

- **Connect a diode with low V_F between the V_{DD} and the pin.**



- **Connect a condenser between the V_{DD} and the pin.**



2. DIFFERENCES BETWEEN PRODUCTS IN SERIES

The μPD75P316A is a product of the μPD75316 with on-chip mask ROM having been replaced with the one-time PROM or EPROM. If you use PROM for debugging the applied system or trial manufacturing, and proceed to use masked ROM products for mass production, do so only with a full understanding of their differences beforehand.

Also, μPD75P316A functions are an extension of those of the μPD75P316. Table 2-1 shows the differences between the series products. All products have the same functions except as indicated in this table.

For the details of the CPU functions and the built-in hardware, please refer to the **μPD75308 User's Manual (IEM-5016)**.

Table 2-1 Differences between Products in Series

Comparison Item \ Product Name		μPD75304/75306/75308	μPD75312/75316	μPD75304B/75306B/75308B	μPD75312B/75316B	μPD75P308	μPD75P316	μPD75P316A	μPD75P316B*1
ROM(× 8 bits)		Mask ROM 4K/6K/8K	Mask ROM 12K/16K	Mask ROM 4K/6K/8K	Mask ROM 12K/16K	One-time PROM,EPROM 8K	One-time PROM 16K	One-time PROM,EPROM 16K	One-time PROM 16K
RAM(× 4 bits)		512			1024	512		1024	
Mask option		Port 4, 5 pull-up resistor incorporated LCD driving power supplying split resistor				No			
Pin connection	No. 50 to 53	P30 to P33				P30/MD0 to P33/MD3			
	No. 57	NC			IC	V_{PP}			
★ Electrical specifications		Masked ROM products and PROM products have different current dissipation and operating temperature range ***2**. For details, refer to the electrical specifications of respective data sheet.							
Power supply voltage range		2.7 to 6.0 V		2.0 to 6.0 V	2.0 to 5.5 V	5 V ±5 %		2.7 to 6.0 V	2.0 to 5.5 V
Operating temperature range		−40 to +85 °C				−10 to +70 °C		−40 to +85 °C	Under investigation
Package		• 80-pin plastic QFP (14 × 20)		• 80-pin plastic QFP QFP (□14) • 80-pin plastic QFP (14 × 20) • 80-pin plastic TQFP (□12)	• 80-pin plastic QFP (□14) • 80-pin plastic TQFP (□12)	• 80-pin plastic QFP (14 × 20) • 80-pin ceramic WQFN (LCC with window)	• 80-pin plastic QFP (14 × 20)	• 80-pin plastic QFP (14 × 20) • 80-pin ceramic WQFN (LCC with window)	• 80 pin plastic QFP (□14) • 80 pin plastic TQFP (□12)
★ On-chip PROM product		μPD75P308	μPD75P316 μPD75P316A	μPD75P316A μPD75P316B	μPD75P316B	——			
★ Others		Masked ROM products and PROM products have different noise endurance limits and noise radiation due to differing circuit scales and mask layouts.							

* **1.** The μPD75P316B is under development.

2. The μPD75P316A is the same as the mask ROM products.

★ **Note PROM and masked ROM have different noise endurance limits and noise radiation. When considering replacement of masked ROM products after trial manufacturing with PROM products, sufficient evaluation of CS products (not ES products) with masked ROM products should be performed.**

3. DATA MEMORY (RAM)

Fig. 3-1 shows the data memory configuration. It consists of a data area and a peripheral hardware area. The data memory consists of memory banks 0 to 3 with each bank consisting of 256 words × 4 bits. Peripheral hardware has been assigned to the area of memory bank 15.

(1) Data area

The data area comprises a static RAM. It is used to store program data and as a subroutine, interrupt execution stack memory. Even if the CPU operation is stopped in the standby mode, it is possible to hold the memory content for a long time by battery backup, etc. The data area is operated by memory manipulation instructions.

The static RAM has been mapped to memory banks 0, 1, 2 and 3 by 256 × 4 bits each. Bank 0 has been mapped as a data area but is also available as a general register area (000H to 007H) and a stack area (000H to 0FFH) (banks 1, 2 and 3 are available only as a data area).

In the static RAM, 1 address consists of 4 bits. It can be operated in units of 8 bits by 8-bit memory manipulation instructions or in bits by bit manipulation instructions, however. In an 8-bit manipulation instruction, an even address should be specified.

(a) General register area

The general register area can be operated either by general register operation instructions or by memory manipulation instructions. Up to eight 4-bit registers are available. That part of the 8 general registers which is not used in the program is available as a data area or a stack area.

(b) Stack area

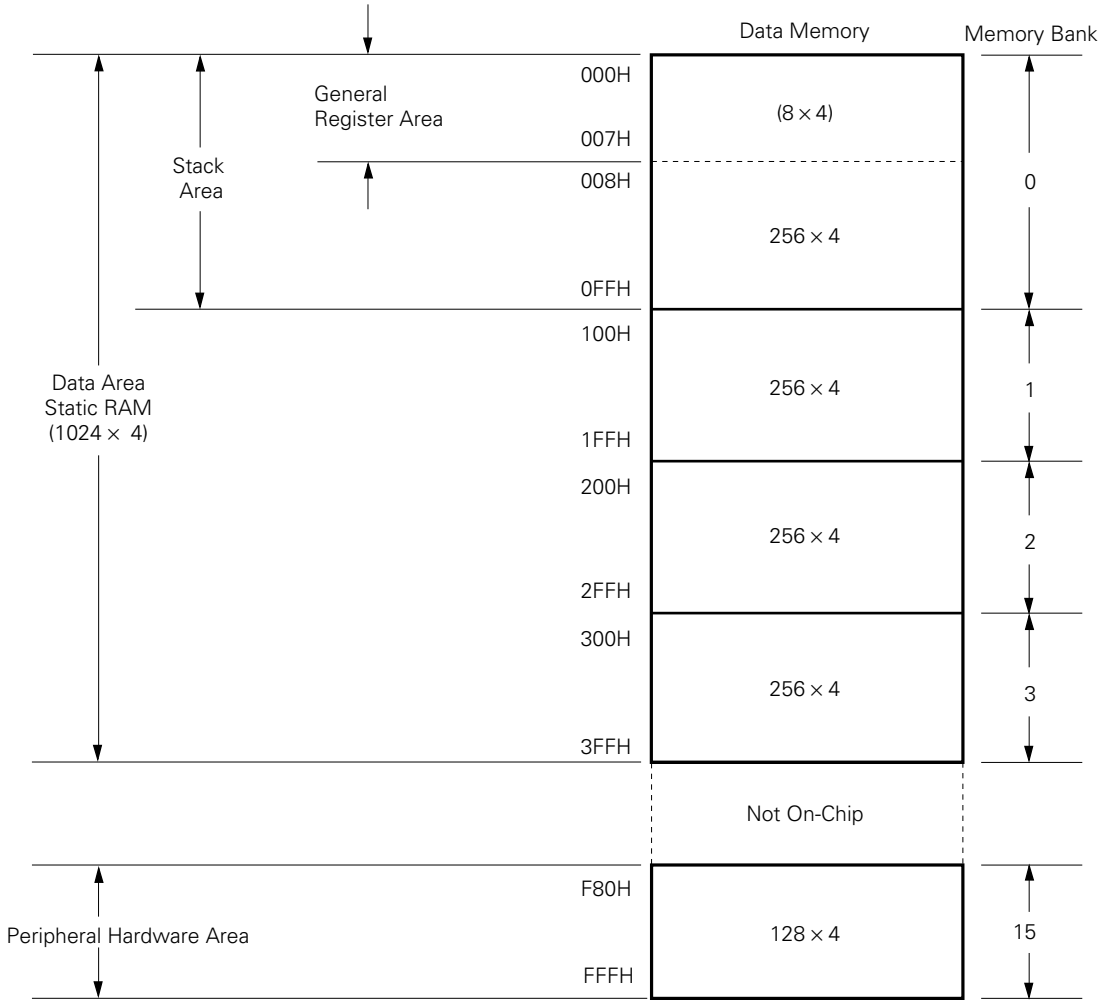
The stack area is set by an instruction. It is available as a subroutine execution or interrupt service execution save area.

(2) Peripheral hardware area

The peripheral hardware area has been mapped to F80H to FFFH of memory bank 15.

It is operated by memory manipulation instructions just as the static RAM. In the peripheral hardware, however, the operable bit unit differs from one address to another. An address to which peripheral hardware has not been assigned is inaccessible since no data memory is built in.

Fig. 3-1 Data Memory Map



4. PROGRAM MEMORY WRITE AND VERIFY

The ROM built into the μPD75P316A is a 16256×8-bit electrically writable one-time PROM. The table below shows the pins used to program this PROM. There is no address input; instead, a method to update the address by the clock input via the X1 pin is adopted.

Pin Name	Function
V_{PP}	Voltage applecation pin for program memory write/verify (normally V_{DD} potential).
X1, X2	Address update clock inputs for program memory write/ verify. Inverse of X1 pin signal is input to X2 pin.
MD0 to MD3	Operating mode selection pins for program memory write/ verify.
P40 to P43 (low-order 4 bits) P50 to P53 (high-order 4 bits)	8-bit data input/output pins for progrm memory write/ verify.
V_{DD}	Supply voltage application pin. Applies 2.7 to 6.0 V in normal operation, and 6 V for program memory write/verify.

Note 1. A lightshield cover film should be applied to the μPD75P316AK provided with an erasure window, except when erasing the EPROM.

2. The one-time PROM version of μPD75P316AGF is not provided with an erasure window, and therefore UV erasure is not possible.

4.1 PROGRAM MEMORY WRITE/VERIFY OPERATING MODES

The μPD75P316A assumes the program memory write/verify mode when +6 V and +12.5 V are applied respectively to the V_{DD} and V_{PP} pins. The table below shows the operating modes available by the MD0 to MD3 pin setting in this mode. All the remaining pins are at the V_{SS} potential by the pull-down resistor.

Operating Mode Setting						Operating Mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address zero-clear
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	×	H	H	Program inhibit mode

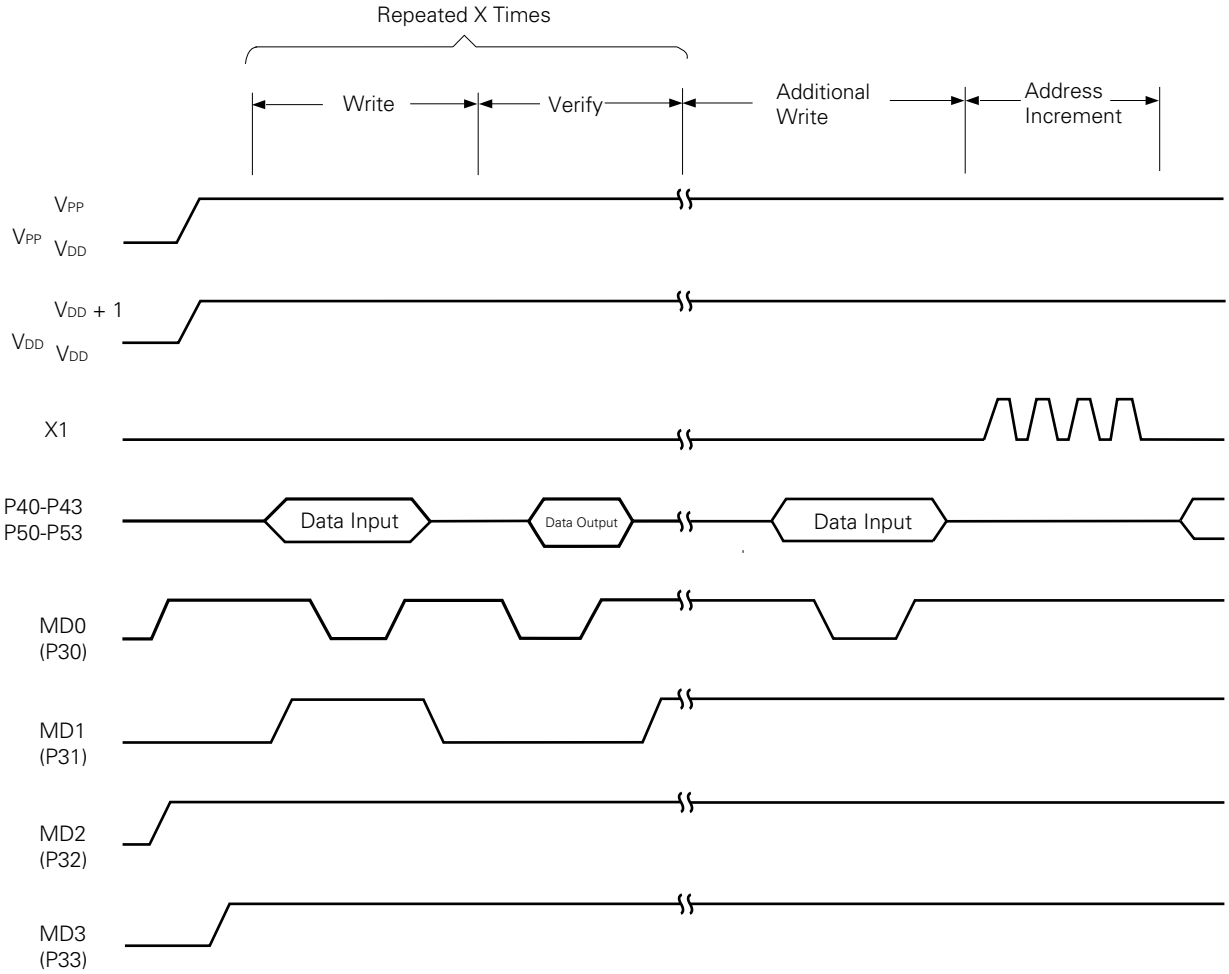
×: L or H

4.2 PROGRAM MEMORY WRITING PROCEDURE

The program memory writing procedure is shown below. High-speed write is possible.

(1) Pull down a pin which is not used to V_{SS} via the resistor. The X1 pin is at the low level.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) 10 μs wait.
(4) The program memory address 0 clear mode.
(5) Supply 6 V and 12.5 V respectively to V_{DD} and V_{PP}.
(6) The program inhibit mode.
(7) Write data in the 1-ms write mode.
(8) The program inhibit mode.
(9) The verify mode. If written, proceed to (10); if not written, repeat (7) to (9).
(10) (Number of times written in (7) to (9): X) × 1-ms additional write.
(11) The program inhibit mode.
(12) Update (+1) the program memory address by inputting 4 pulses to the X1 pin.
(13) Repeat (7) to (12) up to the last address.
(14) The program memory address 0 clear mode.
(15) Change the V_{DD} and V_{PP} pins voltage to 5 V.
(16) Power off.

The diagram below shows the procedure of the above (2) to (12).

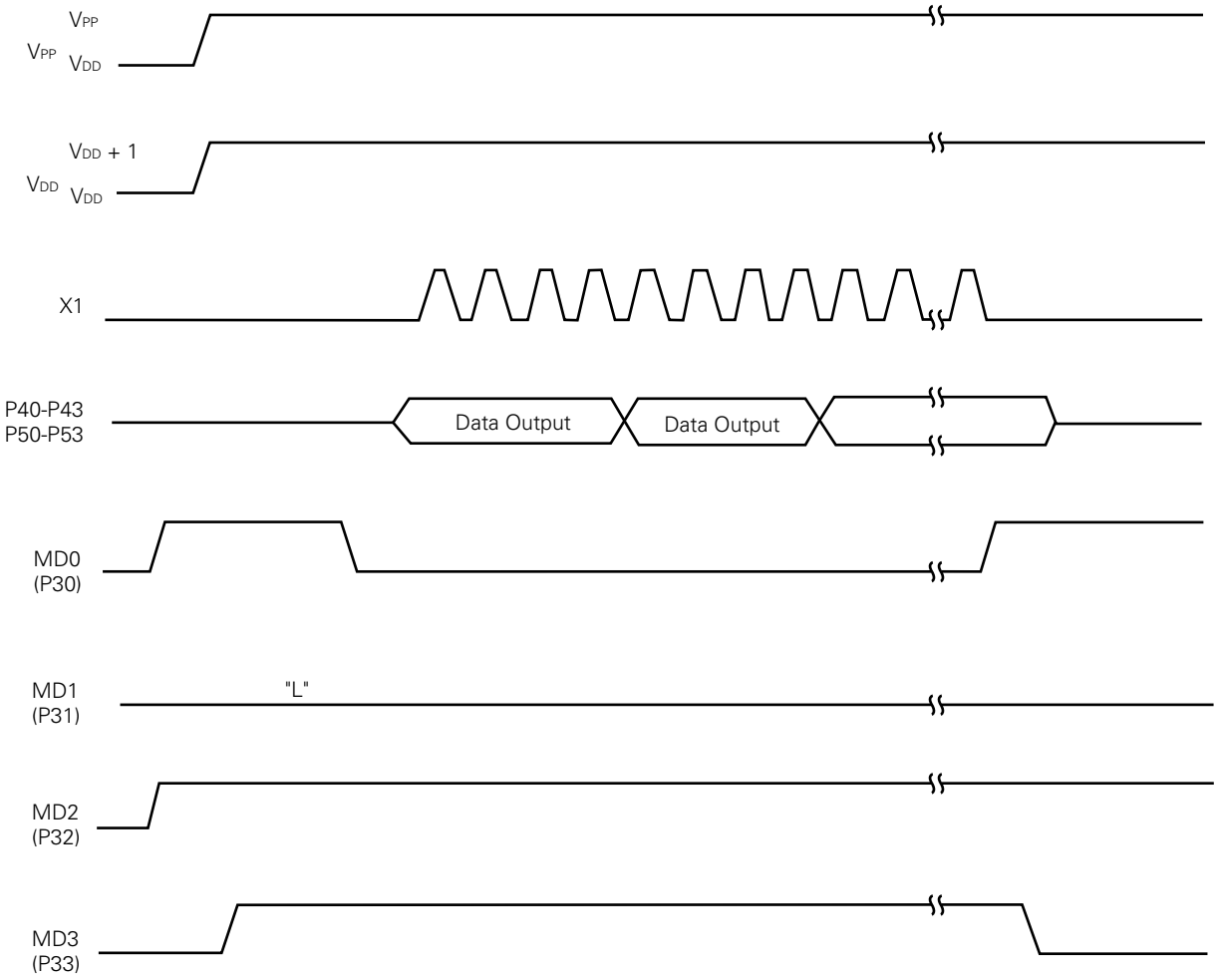


4.3 PROGRAM MEMORY READING PROCEDURE

The μPD75P316A can read the content of the program memory in the following procedure. It reads in the verify mode.

(1) Pull down a pin which is not used to V_{SS} via the resistor. The X1 pin is at the low level.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) 10 μs wait.
(4) The program memory address 0 clear mode.
(5) Supply 6 V and 12.5 V respectively to V_{DD} and V_{PP}.
(6) The program inhibit mode.
(7) The verify mode. If clock pulses are input to the X1 pin, data is output sequentially 1 address at a time at the period of inputting 4 pulses.
(8) The program inhibit mode.
(9) The program memory address 0 clear mode.
(10) Change the V_{DD} and V_{PP} pins voltage to 5 V.
(11) Power off.

The diagram below shows the procedure of the above (2) to (9).



4.4 ERASING METHOD (μPD75P316AK ONLY)

The content of the data programmed in the μPD75P316A is erased as ultraviolet rays are irradiated to the window in the upper part.

The erasable ultraviolet-ray wavelength is about 250 nm.

The dose required for complete erasure is 15 W•s/cm^2 (ultraviolet-ray intensity × erasure time). If a commercially available ultraviolet-ray lamp (wavelength 254 nm, intensity 12 mW/cm^2) is used, it takes about 15 to 20 minutes to erase.

Note 1. The content may be erased if exposed to direct sunlight or fluorescent lamp light for a long time. To protect the content, the window in the upper part should be masked with a lightshield cover film. NEC attaches such a lightshield cover film to each UV EPROM product.

2. When erasing, the distance between the ultraviolet-ray lamp and the μPD75P316A should be kept normally within 2.5 cm.

Remarks It may take longer to erase if the ultraviolet-ray lamp has deteriorated or if the package window is dirty and so on.

5. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

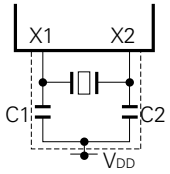
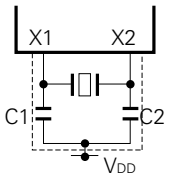
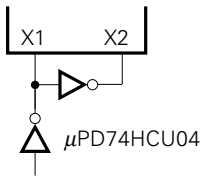
PARAMETER	SYMBOL	TEST CONDITIONS		RATING	UNIT
Power supply voltage	V_{DD}			–0.3 to +7.0	V
	V_{PP}			–0.3 to +13.5	V
Input voltage	V_{I1}	Except ports 4, 5		–0.3 to V_{DD} +0.3	V
	V_{I2}	Ports 4, 5	Open-drain	–0.3 to +11	V
Output voltage	V_O			–0.3 to V_{DD} +0.3	V
Output current high	I_{OH}	1 pin		–15	mA
		All pins		–30	mA
Output current low	I_{OL}*	1 pin	Peak value	30	mA
			Effective value	15	mA
		Total of ports 0, 2, 3, 5	Peak value	100	mA
			Effective value	60	mA
		Total of ports 4, 6, 7	Peak value	100	mA
			Effective value	60	mA
Operating temperature	T_{opt}			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

* Calculate the effective value with the formula [Effective value] = [Peak value] × $\sqrt{\text{duty}}$.

CAPACITANCE (Ta = 25 °C, V_{DD} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pin returned to 0 V			15	pF
Output capacitance	C_{OUT}				15	pF
Input /output capacitance	C_{IO}				15	pF

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

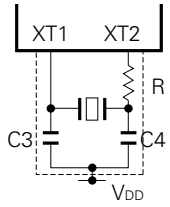
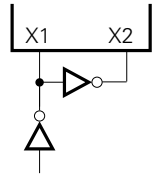
RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ceramic resonator		Oscillator frequency (f_X) ***1**		1.0		5.0***3**	MHz
		Oscillation stabilization time ***2**	After V_{DD} reaches the minimum value in the oscillation voltage range			4	ms
Crystal resonator		Oscillator frequency (f_X) ***1**		1.0	4.19	5.0***3**	MHz
		Oscillation stabilization time ***2**	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External clock		X1 input frequency (f_X) ***1**		1.0		5.0***3**	MHz
		X1 high and low level widths (t_{XH}, t_{XL})		100		500	ns

* **1.** Oscillator characteristics only. Refer to the description of AC characteristics for details of instruction execution time.

2. Time required for oscillation to become stabilized after V_{DD} reaches MIN. of the oscillation voltage range or after STOP mode release.

3. When the oscillator frequency is 4.19 MHz < f_X ≤ 5.0 MHz, do not select PPC = 0011 as instruction execution time. If PCC = 0011 is selected, 1 machine cycle becomes less than 0.95 μs, with the result that specified MIN. value 0.95 μs can not be observed.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal resonator		Oscillator frequency (f_{XT})		32	32.768	35	kHz
		Oscillation stabilization time*	V_{DD} = 4.5 to 6.0 V		1.0	2	s
						10	s
External clock		XT1 input frequency (f_{XT})		32		100	kHz
		XT1 high and low level widths (t_{XTH}, t_{XTL})		5		15	μs

* Time required for oscillation to become stabilized after V_{DD} reaches MIN. of the oscillation voltage range or after STOP made release.

Note When the main system clock and subsystem clock oscillation circuit are used, the area enclosed by dotted line in the figure should be wired as follows to prevent influence from the wiring capacitance, etc..

- **Wiring should be as short as possible.**
- **Do not cross other signal lines.**
  Do not place the circuit closed to a line in which varying high current flows.
- **The connecting point of oscillation circuit capacitor should always be the same potential as V_{DD}. Do not connect it to the power supply pattern in which high current flows.**
- **Do not pick up a signal from the oscillation circuit.**

The subsystem clock oscillation circuit is designed to be low amplification circuit for low dissipation current, thus misoperation due to noise occurs more often than with the main system clock oscillation circuit. Therefore, when the subsystem clock is used, care is needed especially for the wiring procedure.

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V) (1/2)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH1}	Ports 2 and 3		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7, $\overline{RESET}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4 and 5	Open-drain	0.7 V_{DD}		10	V
	V_{IH4}	X1, X2, XT1		V_{DD} –0.5		V_{DD}	V
Input voltage low	V_{IL1}	Ports 2, 3, 4 and 5		0		0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7, $\overline{RESET}$		0		0.2 V_{DD}	V
	V_{IL3}	X1, X2, XT1		0		0.4	V
Output voltage high	V_{OH1}	Ports 0, 2, 3, 6, 7, BIAS	V_{DD} = 4.5 to 6.0 V I_{OH} = –1 mA	V_{DD} –1.0			V
			I_{OH} = -100 μA	V_{DD} –0.5			V
	V_{0H2}	BP0 to BP7 (with 2 I_{OH} outputs)	V_{DD} = 4.5 to 6.0 V I_{OH} = –100 μA	V_{DD} –2.0			V
			I_{OH} = –30 μA	V_{DD} –1.0			V
Output voltage low	V_{OL1}	Ports 0, 2, 3, 4, 5, 6 and 7	Ports 3, 4 and 5 V_{DD} = 4.5 to 6.0 V I_{OL} = 15 mA		0.4	2.0	V
			V_{DD} = 4.5 to 6.0 V I_{OL} = 1.6 mA			0.4	V
			I_{OL} = 400 μA			0.5	V
		SB0, 1	Open-drain pull-up resistor ≥ 1 kΩ			0.2 V_{DD}	V
	V_{OL2}	BP0 to BP7 (with 2 I_{OL} outputs)	V_{DD} = 4.5 to 6.0 V I_{OL} = 100 μA			1.0	V
			I_{OL} = 50 μA			1.0	V
Input leakage current high	I_{LIH1}	V_{IN} = V_{DD}	Other than below			3	μA
	I_{LIH2}		X1, X2, XT1			20	μA
	I_{LIH3}	V_{IN} = 10 V	Ports 4 and 5 (when open-drain)			20	μA
Input leakage current low	I_{LIL1}	V_{IN} = 0 V	Other than below			-3	μA
	I_{LIL2}		X1, X2, XT1			-20	μA

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V) (1/2)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Output leakage current high	I_{LOH1}	V_{OUT} = V_{DD}	Other than below			3	μA
	I_{LOH2}	V_{OUT} = 10 V	Ports 4 and 5 (when open-drain)			20	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V				–3	μA
On-chip pull-up resistor	R_{L1}	Ports 0, 1, 2, 3, 6 and 7 (Except P00) V_{IN} = 0 V	V_{DD} = 5.0 V ±10%	15	40	80	kΩ
			V_{DD} = 3.0 V ±10%	30		300	kΩ
LCD drive voltage	V_{LCD}			2.5		V_{DD}	V
LCD output voltage deviation***1** (common)	V_{ODC}	Io = ±5 μA	V_{LCD0} = V_{LCD}, V_{LCD1} = V_{LCD} × 2/3, V_{LCD2} = V_{LCD} × 1/3, 2.7 V ≤ V_{LCD} ≤ V_{DD}	0		±0.2	V
LCD output voltage deviation***1** (segment)	V_{ODC}	Io = ±5μA		0		±0.2	V
Supply current***2**	I_{DD1}	4.19 MHz***3** crystal oscillation C1=C2 22 pF	V_{DD} = 5 V ±10%***4**		4.5	14	mA
			V_{DD} = 3 V ±10%***5**		0.9	3	mA
	I_{DD2}		HALT mode, V_{DD} = 5 V ±10%		700	2100	μA
			HALT mode, V_{DD} = 3 V ±10%		300	900	μA
	I_{DD3}	32 kHz***6** crystal oscillation	Operating mode, V_{DD} = 3 V ±10%		100	300	μA
	I_{DD4}		HALT mode, V_{DD} = 3 V ±10%		20	60	μA
	I_{DD5}	XT1 = 0 V STOP mode	V_{DD} = 5 V±10%		0.5	20	μA
			V_{DD} = 3 V±10%		0.1	10	μA
			V_{DD} = 3 V±10%, T_a = 25°C		0.1	5	μA
	I_{DD6}	32 kHz crystal oscillation STOP mode	V_{DD} = 3 V ±10%***7**		5	15	μA

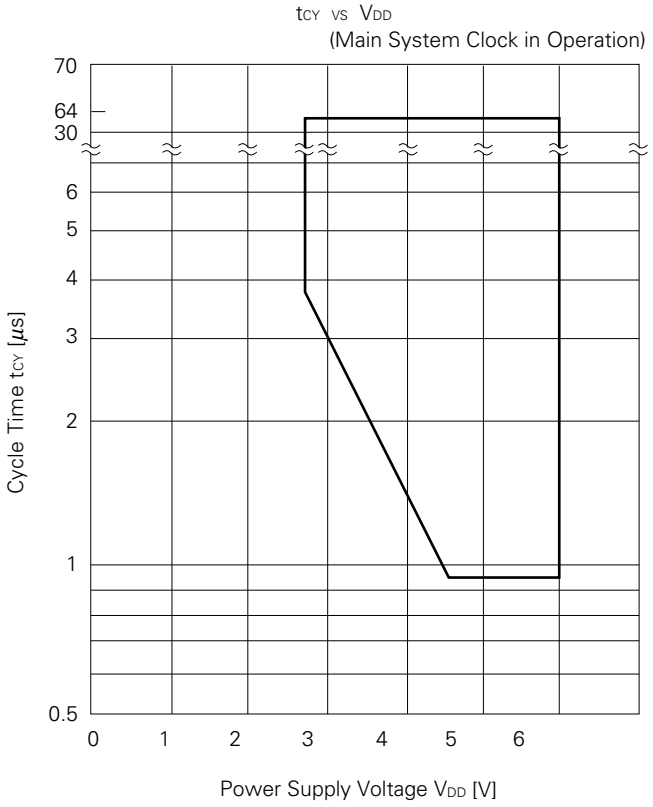
* **1.** The voltage deviation is a difference between the segment and common output ideal value (V_{LCDn}; n = 0, 1, 2) and output voltage.
  2. Current flowing in the internal pull-up resistor and LCD split resistor are not included.
  3. Includes when the subsystem clock is oscillated.
  4. When the processor clock control register (PCC) is set to 0011 and operated in high-speed mode.
  5. When the PCC is set to 0000 and operated in low-speed mode.
  6. When operated by the subsystem clock with the system clock control register (SCC) set to 1011 and the main system clock stops.
  7. When the STOP instruction is executed during the main system clock operation and the subsystem clock is oscillated.

AC CHARACTERISTICS (Ta = –40 to +85 °C , V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CPU clock cycle time (minimum instruction execution time = 1 machine cycle)***1**	t_{CY}	Operation with main system clock	V_{DD} = 4.5 to 6.0 V	0.95		64	μs
				3.8		64	μs
		Operation with subsystem clock		114	122	125	μs
TI0 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHZ
				0		275	kHz
TI0 input high and low-level widths	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
Interrupt input high and low-level widths	t_{INTH}, t_{INTL}	INT0		***2**			μs
		INT1, 2, 4		10			μs
		KR0–7		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

*** 1.** CPU clock (Φ) cycle time is determined by oscillator frequency of the connected resonator, system clock control register (SCC) and processor clock control register (PCC). Characteristics for power supply voltage V_{DD} vs • cycle time t_{CY} in main system clock operation is shown below.

2. It becomes $2t_{CY}$ or $128/f_X$ by interrupt mode register (IM0) setting.



Serial Transfer Operation

2-wire and 3-wire serial I/O mode ($\overline{SCK}$...Internal clock output)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high and low level widths	t_{KL1}	V_{DD} = 4.5 to 6.0 V		$t_{KCY1}/2-50$			ns
	t_{KH1}			$t_{KCY1}/2-150$			ns
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIK1}			150			ns
SI hold time (from $\overline{SCK}\uparrow$)	t_{KSI1}			400			ns
SO output delay time from $\overline{SCK}\downarrow$	t_{KSO1}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			250	ns
						1000	ns

* R_L and C_L are SO output line load resistance and load capacitance, respectively.

2-wire and 3-wire serial I/O mode ($\overline{SCK}$...External clock input)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high and low level widths	t_{KL2}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KH2}			1600			ns
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIK2}			100			ns
SI hold time (from $\overline{SCK}\uparrow$)	t_{KSI2}			400			ns
SO output delay time from $\overline{SCK}\downarrow$	t_{KSO2}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns

* R_L and C_L are SO output line load resistance and load capacitance, respectively.

SBI mode ($\overline{SCK}$...Internal clock output (master))

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high and low level widths	t_{KL3}	V_{DD} = 4.5 to 6.0 V		$t_{KCY3}/2-50$			ns
	t_{KH3}			$t_{KCY3}/2-150$			ns
SB0 and SB1 setup time (to $\overline{SCK}\uparrow$)	t_{SIK3}			150			ns
SB0 and SB1 hold time (from $\overline{SCK}\uparrow$)	t_{KSI3}			$t_{KCY3}/2$			ns
SB0 and SB1 output delay time from $\overline{SCK}\downarrow$	t_{KSO3}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK}\uparrow$	t_{KSB}			t_{KCY3}			ns
$\overline{SCK}$ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0 and SB1 low-level widths	t_{SBL}			t_{KCY3}			ns
SB0 and SB1 high-level widths	t_{SBH}			t_{KCY3}			ns

* R_L and C_L are SO output line load resistance and load capacitance, respectively.

SBI mode ($\overline{SCK}$...External clock input (slave))

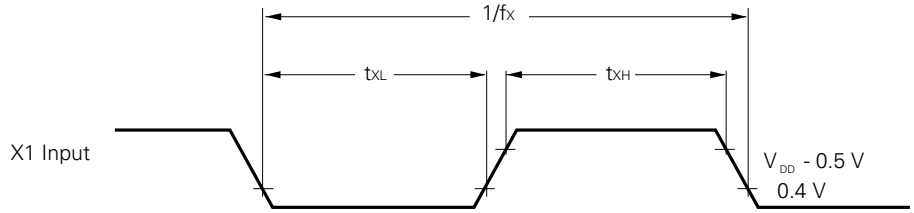
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high and low level widths	t_{KL4}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KH4}			1600			ns
SB0 and SB1 setup time (to $\overline{SCK}\uparrow$)	t_{SIK4}			100			ns
SB0 and SB1 hold time (from $\overline{SCK}\uparrow$)	t_{KSI4}			$t_{KCY3}/2$			ns
SB0 and SB1 output delay time from $\overline{SCK}\downarrow$	t_{KSO4}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK}\uparrow$	t_{KSB}			t_{KCY4}			ns
$\overline{SCK}$ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0 and SB1 low-level widths	t_{SBL}			t_{KCY4}			ns
SB0 and SB1 high-level widths	t_{SBH}			t_{KCY4}			ns

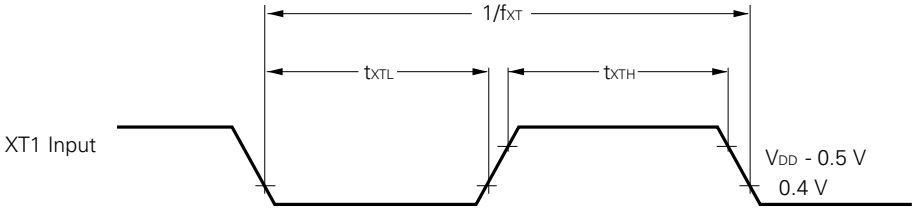
* R_L and C_L are SO output line load resistance and load capacitance, respectively.

AC Timing Test Points (Except X1 and XT1 Inputs)

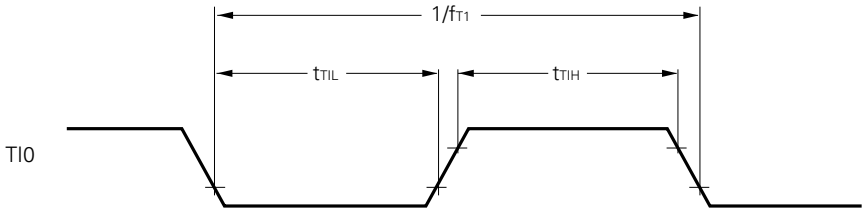


Clock Timing



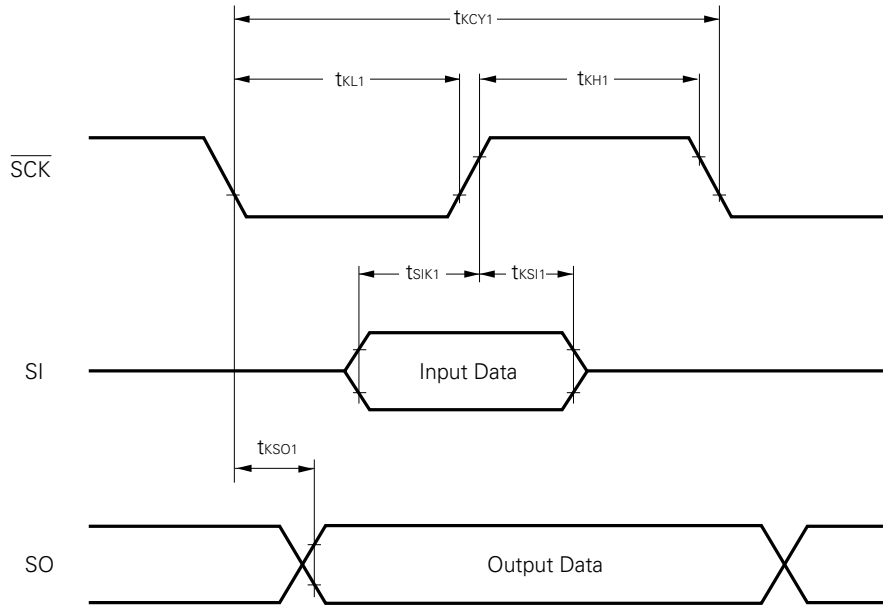


TI0 Timing

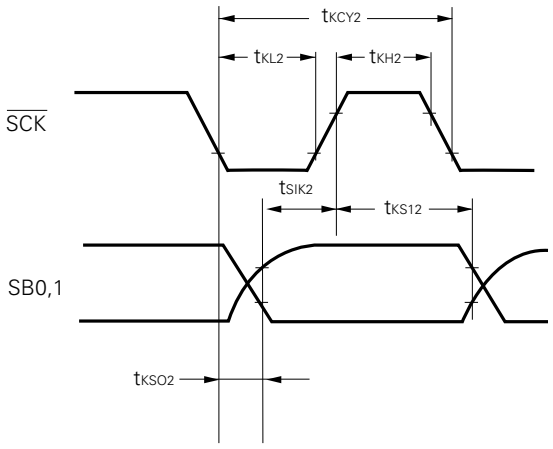


Serial Transfer Timing

3-wire serial I/O mode:

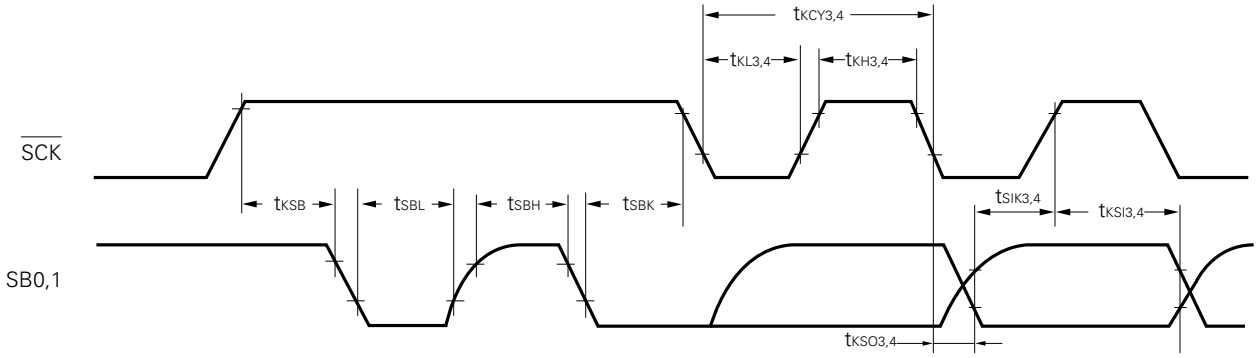


2-wire serial I/O mode:

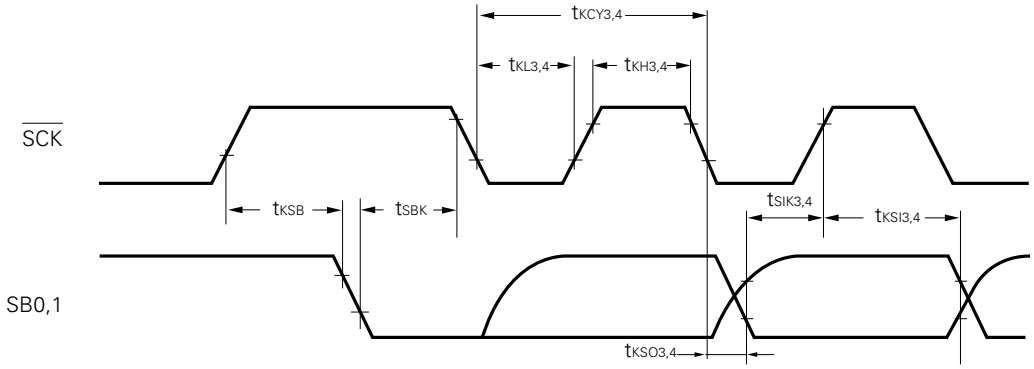


Serial Transfer Timing

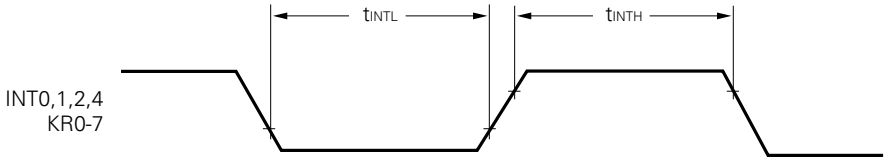
Bus release signal transfer:



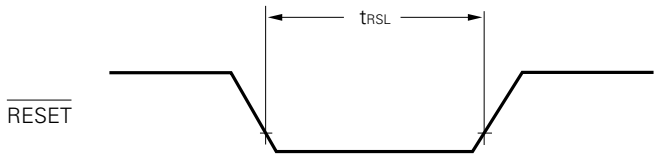
Command signal transfer:



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



DATA MEMORY STOP MODE LOW POWER SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (Ta = –40 to +85 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention power supply voltage	V_{DDDR}		2.0		6.0	V
Data retention power supply current *1	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time *2	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt request		*3		ms

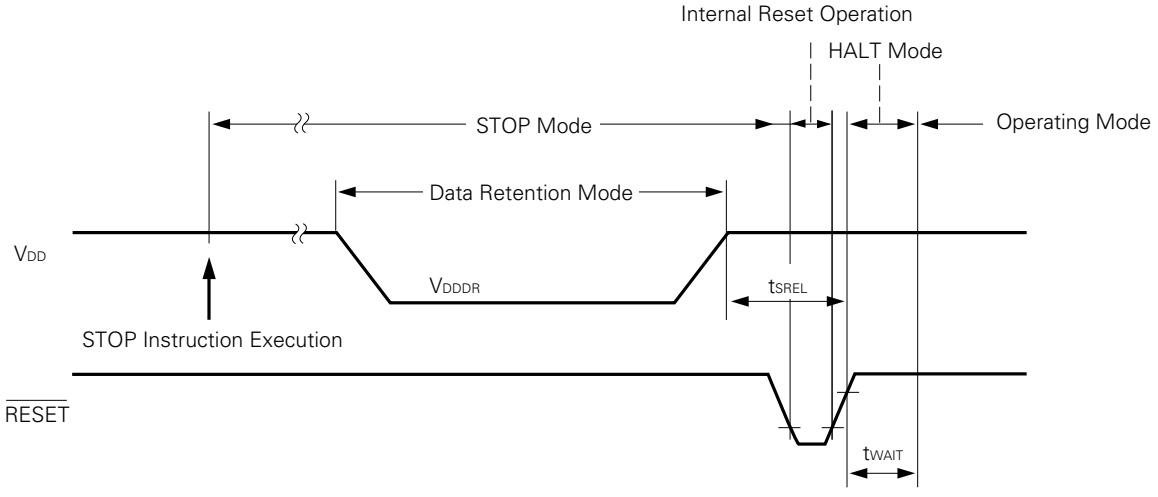
* **1.** Current to the internal pull-up resistor is not included.

2. Oscillation stabilization wait time is time to stop CPU operation to prevent unstable operation upon oscillation start.

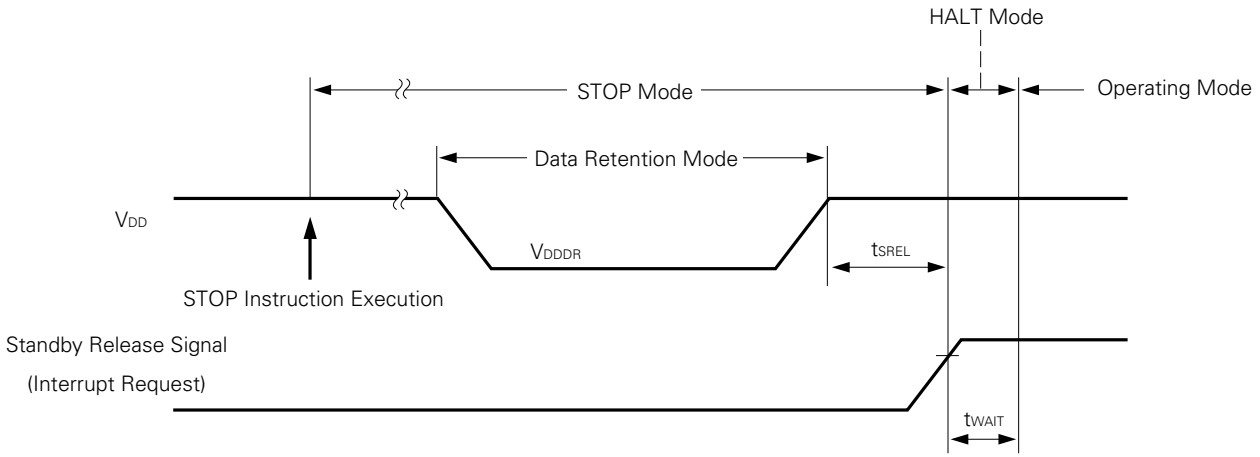
3. According to the setting of the basic interval timer mode register (BTM) (see below).

BTM3	BTM2	BTM1	BTM0	Wait Time (Values at f_{XX} = 4.19 MHz in parentheses)
—	0	0	0	$2^{20}/f_{XX}$ (approx. 250 ms)
—	0	1	1	$2^{17}/f_{XX}$ (approx. 31.3 ms)
—	1	0	1	$2^{15}/f_{XX}$ (approx. 7.82 ms)
—	1	1	1	$2^{13}/f_{XX}$ (approx. 1.95 ms)

Data Retention Timing (STOP Mode Release by $\overline{RESET}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



DC PROGRAMMING CHARACTERISTICS (Ta = –25 to ±5 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.3 V, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH1}	Except X1, X2	0.7 V_{DD}		V_{DD}	V
	V_{IH2}	X1, X2	V_{DD} –0.5		V_{DD}	V
Input voltage low	V_{IL1}	Except X1, X2	0		0.3 V_{DD}	V
	V_{IL2}	X1, X2	0		0.4	V
Input leakage current	I_{LI}	V_{IN} = V_{IL} or V_{IH}			10	μA
Output voltage high	V_{OH}	I_{OH} = –1mA	V_{DD} –1.0			V
Output voltage low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} power supply current	I_{DD}				30	mA
V_{PP} power supply current	I_{PP}	MD0 = V_{IL}, MD1 = V_{IH}			30	mA

Note 1. V_{PP} including overshoot should not exceed +13.5 V.
2. V_{DD} should be applied before V_{PP} and should be cut after V_{PP}.

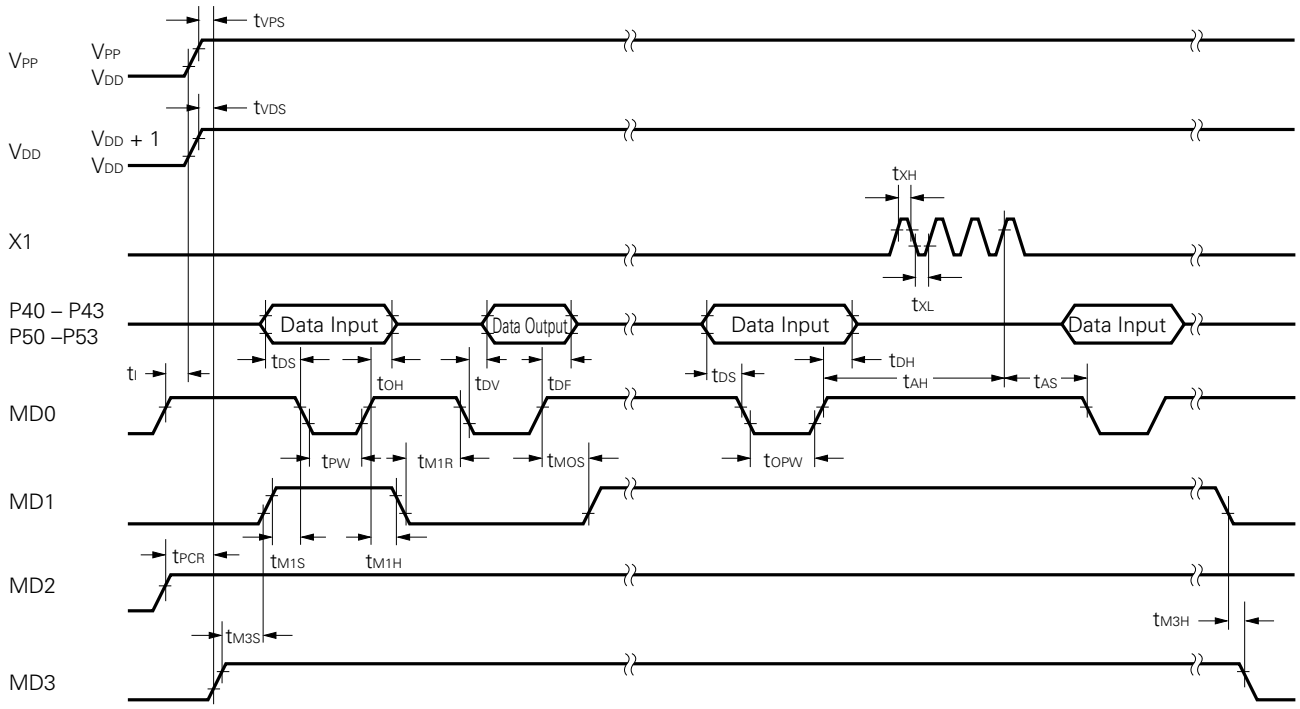
AC PROGRAMMING CHARACTERISTICS (Ta = 25 to ±5 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.3 V, V_{SS} = 0 V)

PARAMETER	SYMBOL	*1	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Address setup time*2 (to MD0 ↓)	t_{AS}	t_{AS}		2			μs
MD1 setup time (to MD0 ↓)	t_{M1S}	t_{OES}		2			μs
Data setup time (to MD0 ↓)	t_{DS}	t_{DS}		2			μs
Address hold time*2 (from MD0 ↑)	t_{AH}	t_{AH}		2			μs
Data hold time (to MD0 ↑)	t_{DH}	t_{DH}		2			μs
Data output float delay time from MD0 ↑	t_{DF}	t_{DF}		0		130	ns
V_{PP} setup time (to MD3 ↑)	t_{VPS}	t_{VPS}		2			μs
V_{DD} setup time (to MD3 ↑)	t_{VDS}	t_{VCS}		2			μs
Initial program pulse width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD1 setup time (to MD1 ↑)	t_{MOS}	t_{CES}		2			μs
Data output delay time from MD0 ↓	t_{DV}	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
MD1 hold time (from MD0 ↑)	t_{M1H}	t_{OEH}	$t_{M1H} + t_{M1R} \geq 50$ μs	2			μs
MD1 recovery time (from MD0 ↓)	t_{M1R}	t_{OR}		2			μs
Program counter reset time	t_{PCR}	–		10			μs
X1 input high/low level width	t_{XH}, t_{XL}	–		0.125			μs
X1 input frequency	f_X	–				4.19	MHz
Initial mode set time	t_I	–		2			μs
MD3 setup time (to MD1 ↑)	t_{M3S}	–		2			μs
MD3 hold time (from MD1 ↓)	t_{M3H}	–		2			μs
MD3 setup time (to MD0 ↓)	t_{M3SR}	–	When reading program memory	2			μs
Data output delay time from address*2	t_{DAD}	t_{ACC}	When reading program memory			2	μs
Data output hold time from address*2	t_{HAD}	t_{OH}	When reading program memory	0		130	ns
MD3 hold time (from MD0 ↑)	t_{M3HR}	–	When reading program memory	2			μs
Data output float delay time from MD3 ↓	t_{DFR}	–	When reading program memory			2	μs

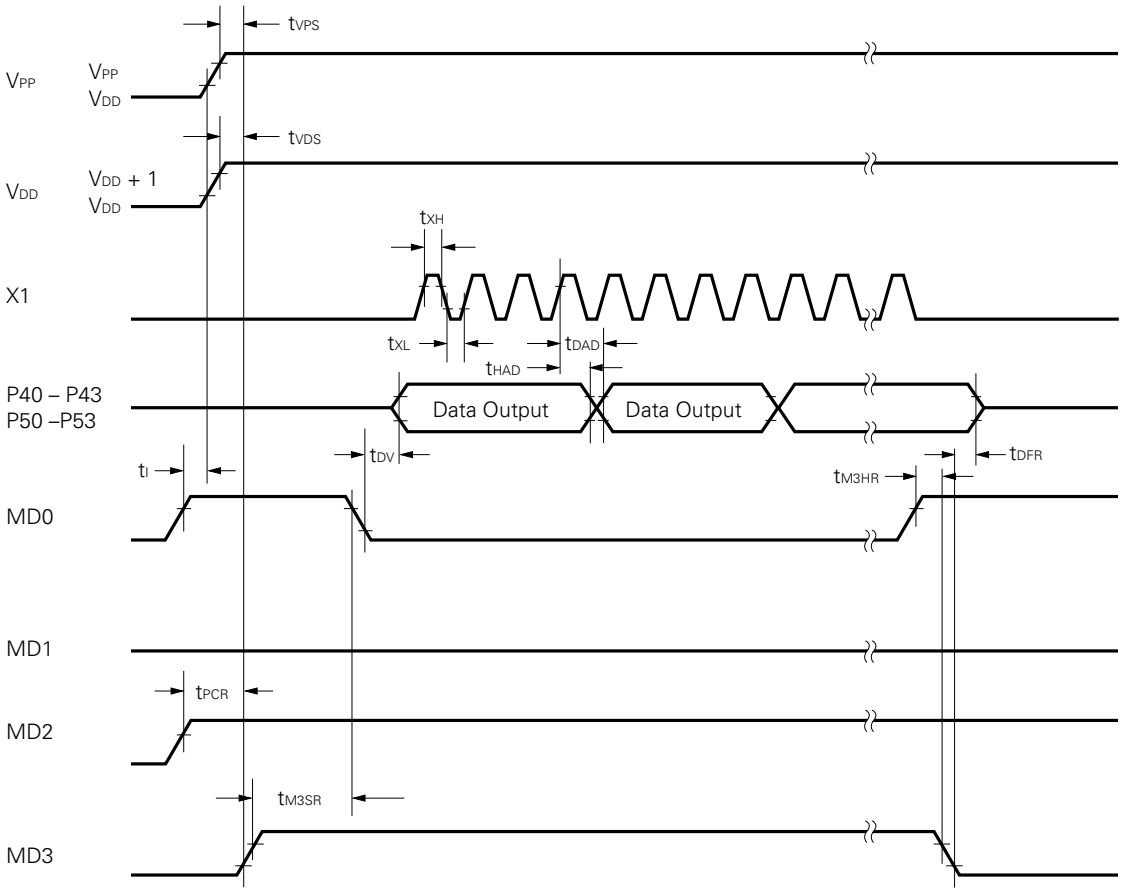
* **1.** Symbol of the corresponding μPD27C256A.

2. The internal address signal is incremented (+1) at the rising edge of the fourth X1 input. The signal is not connected to pins.

Program Memory Write Timing

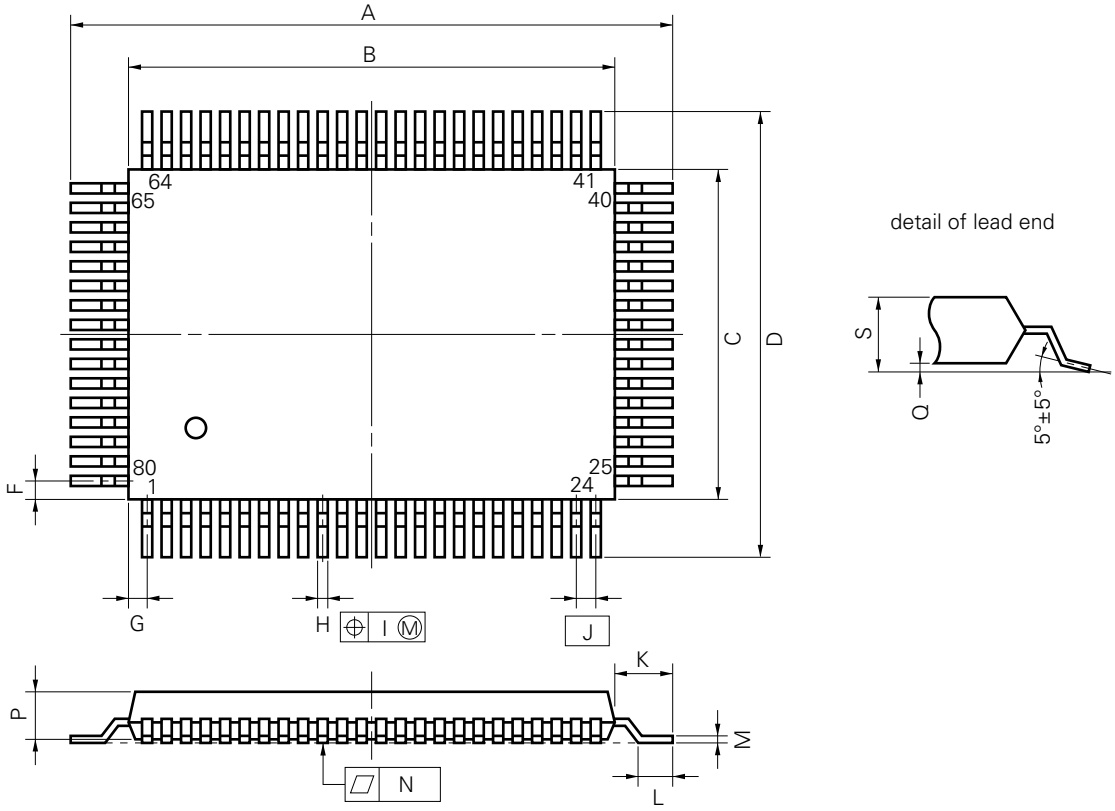


Program Memory Read Timing



6. PACKAGE INFORMATION

80 PIN PLASTIC QFP (14×20)



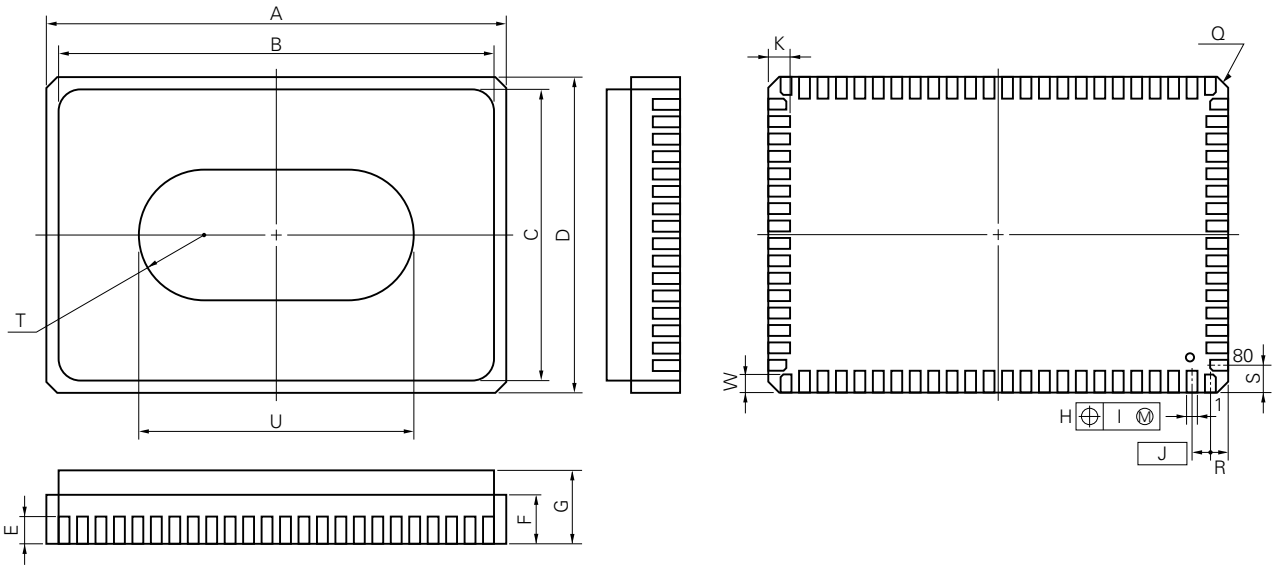
P80GF-80-3B9-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	0.8	0.031
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

80 PIN CERAMIC WQFN



X80KW-80A-1

NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	20.0±0.4	$0.787^{+0.017}_{-0.016}$
B	19.0	0.748
C	13.2	0.520
D	14.2±0.4	0.559±0.016
E	1.64	0.065
F	2.14	0.084
G	4.064 MAX.	0.160 MAX.
H	0.51±0.10	0.020±0.004
I	0.08	0.003
J	0.8 (T.P.)	0.031 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
Q	C 0.5	C 0.020
R	0.8	0.031
S	1.1	0.043
T	R 3.0	R 0.118
U	12.0	0.472
W	0.75±0.2	$0.030^{+0.008}_{-0.009}$

7. RECOMMENDED SOLDERING CONDITIONS

The μPD75P316A should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document "**Semiconductor Device Mount Manual**" (IEI-1207).

For soldering methods and conditions other than those recommended below, contact our salesman.

Table 7-1 Surface Mounting Type Soldering Conditions

μPD75P316AGF-3B9 : 80-pin plastic QFP (14 × 20 mm)

Solderring Method	Solderring Conditions	Recommended Condition Symbol
Wave soldering	Solder bath temperature: 260 °C or below. , Duration: 10 sec. max. Number of times: Once, Time limit: 7 days*(thereafter 20 hours prebaking required at 125 °C)	WS60-207-1
Infrared reflow	Package peak temperature: 230 °C, Duration: 30 sec. max. (at 210 °C or above), Number of times: Once, Time limit: 7 days*(thereafter 20 hours prebaking required at 125 °C)	IR30-207-1
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above), Number of times: Once, Time limit: 7 days* (thereafter 20 hours prebaking required at 125 °C)	VP15-207-1
Pin part heating	Pin part temperature: 300 °C or below , Duration: 3 sec. max. (per device side)	——

***** For the storage period after dry-pack decapsulation, storage conditions are max. 25 °C, 65 % RH.

Note Use more than one soldering method should be avoided (except in the case of pin part heating).

For Your Information

Products to improve the recommended soldering conditions are available.
(Improvements : Extension of the infrared reflow peak temperature to 235 °C, doubled frequency, increased life, etc.)
For further details, consult our sales personnel.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD75P316A.

Hardware	IE-75000-R***1** IE-75001-R		In-circuit emulator for use with the 75X series
	IE-75000-R-EM***2**		Emulation board for use with the IE-75000-R and the IE-75001-R
	EP-75308GF-R	EV-9200G-80	Emulation probe for use with the μPD75P308GF 80-pin conversion socket EV-9200G-80 included
	PG-1500		PROM programmer
	PA-75P308GF		Connect to PG-1500 with PROM programmer adapter for use with the μPD75P308GF
	PA-75P308K		Connect to PG-1500 with PROM programmer adapter for use wtih the μPD75P308K
Software	IE-control program		Host machine • PC-9800 series (MS-DOS™ Ver. 3.30 to Ver.5.00A ***3**) • IBM PC/AT™ (PC DOS™ Ver. 3.1)
	PG-1500 controller		
	RA75X relocatable assembler		

* **1.** Maintenance product
2. Not a built-in component in the IE-75001-R
3. Ver. 5.00/5.00A has a task swaping function, which cannot be used with this software.

Remarks Refer to the **75X Series Selection Guide (IF-151)** for third-party development tools.

APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name	Document Number
User's Manual	IEM-5016
Instruction Application Table	IEM-994
75X Series Selection Guide	IF-151

Development Tools Documents

	Document Name		Document Number
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-846
	IE-75000-R-EM User's Manual		EEU-673
	EP-75308GF-R User's Manual		EEU-689
	PG-1500 User's Manual		EEU-651
Software	RA75X Assembler Package User's Manual	Operation Volume	EEU-731
		Language Volume	EEU-730
	PG-1500 Controller User's Manual		EEU-704

Other Documents

Document Name	Document Number
Package Manual	IEI-635
Surface Mount Technology Manual	IEI-1207
Quality Grade on NEC Semiconductor Devices	IEI-1209
NEC Semiconductor Device Reliability & Quality Control	IEM-5068
Electrostatic Discharge (ESD) Test	MEM-539
Semiconductor Devices Quality Guide Guarantee Guide	MEI-603
Microcomputer Related Products Guide Other Other Manufacturers Volume	MEI-604

Note The information in these related documents is subject to change without notice. For design purpose, etc., check if your documents are the latest ones and be sure to use the latest ones.

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