HIGH PERFORMANCE CURRENT MODE PWM CONTROLLER

NOT FOR NEW DESIGN

1 FEATURES

- TRIMMED OSCILLATOR DISCHARGE CURRENT
- CURRENT MODE OPERATION TO 500kHz AUTOMATIC FEED FORWARD COMPENSATION
- LATCHING PWM FOR CYCLE-BY-CYCLE CURRENT LIMITING
- INTERNALLY TRIMMED REFERENCE WITH UNDERVOLTAGE LOCKOUT
- HIGH CURRENT TOTEM POLE OUTPUT UNDERVOLTAGE LOCKOUT WITH HYSTERESIS
- LOW START-UP CURRENT (< 0.5mA) DOUBLE PULSE SUPPRESSION

2 DESCRIPTION

The UC384xA family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include a trimmed oscillator for precise DUTY CYCLE CONTROL under voltage lockout featuring start-up current less than 0.5mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off-state.

Figure 1. Package



DIP-8



SO-8

Table 1. Order Codes

Part Number	Package
UC2842AD1; UC3842AD1; UC2843AD1; UC3843AD1; UC2844AD1; UC3844AD1; UC2845AD1; UC3845AD1	SO-8
UC2842AN; UC3842AN; UC2843AN; UC3843AN; UC2844AN; UC3844AN; UC2845AN; UC3845AN	DIP-8

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC3842A and UC3844A have UVLO thresholds of 16V (on) and 10V (off), ideally suited off-line applications The corresponding thresholds for the UC3843A and UC3845A are 8.5 V and 7.9V. The UC3842A and UC3843A can operate to duty cycles approaching 100%. A range of the zero to < 50 % is obtained by the UC3844A and UC3845A by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

Figure 2. Block Diagram (toggle flip flop used only in UC3844A and UC3845A)

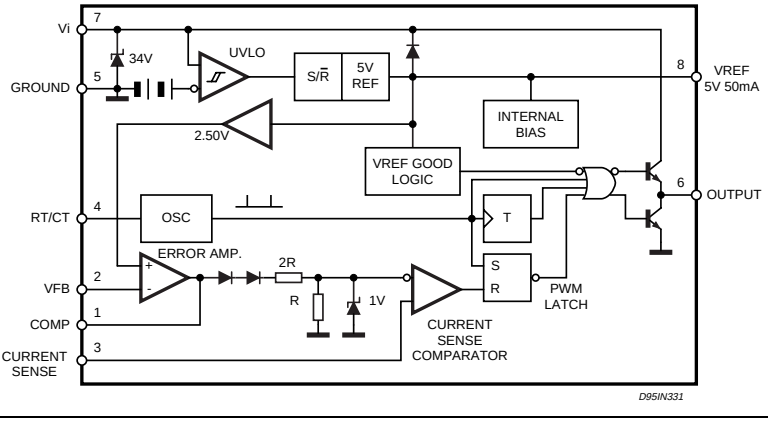
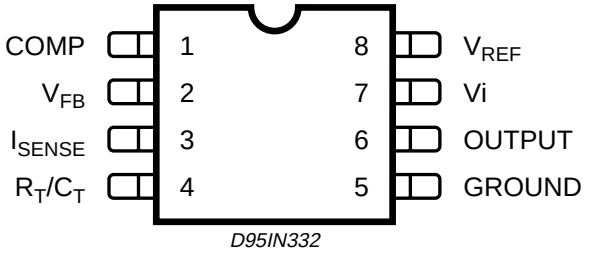


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_i	Supply Voltage (low impedance source)	30	V
V_i	Supply Voltage (Ii < 30mA)	Self Limiting	
I_O	Output Current	±1	A
E_O	Output Energy (capacitive load)	5	µJ
	Analog Inputs (pins 2, 3)	– 0.3 to 5.5	V
	Error Amplifier Output Sink Current	10	mA
P_{tot}	Power Dissipation at $T_{amb} \leq 25$ °C (DIP-8)	1.25	W
P_{tot}	Power Dissipation at $T_{amb} \leq 25$ °C (SO-8)	800	mW
T_{stg}	Storage Temperature Range	– 65 to 150	°C
T_J	Junction Operating Temperature	– 40 to 150	°C
T_L	Lead Temperature (soldering 10s)	300	°C

* All voltages are with respect to pin 5, all currents are positive into the specified terminal.

Figure 3. DIP-8/SO-8 Pin Connection (Top view)



D95IN332

Table 3. Pin Description

N°	Pin	Function
1	COMP	This pin is the Error Amplifier output and is made available for loop compensation.
2	V_{FB}	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	I_{SENSE}	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R_T/C_T	The oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and cpacitor C_T to ground. Operation to 500kHz is possible.
5	GROUND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sunk by this pin.
7	V_{CC}	This pin is the positive supply of the control IC.
8	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.

Table 4. Thermal Data

Symbol	Parameter		DIP-8	SO-8	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	100	150	°C/W

Table 5. Electrical Characteristcs

([note 1] Unless otherwise stated, these specifications apply for -25 < T_{amb} < 85°C for UC284XA; 0 < T_{amb} < 70°C for UC384XA; V_i = 15V (note 5); R_T = 10K; C_T = 3.3nF)

Symbol	Parameter	Test Condition	UC284XA			UC384XA			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V_{REF}	Output Voltage	T_j = 25°C I_o= 1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
ΔV_{REF}	Line Regulation	12V ≤ V_i ≤ 25V		2	20		2	20	mV
ΔV_{REF}	Load Regulation	1 ≤ I_o ≤ 20mA		3	25		3	25	mV
$\Delta V_{REF}/\Delta T$	Temperature Stability	(Note 2)		0.2			0.2		mV/°C
	Total Output Variation	Line, Load, Temperature	4.9		5.1	4.82		5.18	V
e_N	Output Noise Voltage	10Hz ≤ f ≤ 10KHz T_j = 25°C (note 2)		50			50		µV
	Long Term Stability	T_{amb} = 125°C, 1000Hrs (note 2)		5	25		5	25	mV
I_{SC}	Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
OSCILLATOR SECTION									
f_{OSC}	Frequency	T_j = 25°C	47	52	57	47	52	57	KHz
$\Delta f_{OSC}/\Delta V$	Frequency Change with Volt.	V_{CC} = 12V to 25V	–	0.2	1	–	0.2	1	%
$\Delta V_{REF}/\Delta T$	Frequency Change with Temp.	T_A = T_{low} to T_{high}	–	5	–	–	5	–	%
V_{OSC}	Oscillator Voltage Swing	(peak to peak)	–	1.6	–	–	1.6	–	V
I_{dischg}	Discharge Current (V_{OSC} =2V)	T_J = 25°C	7.8	8.3	8.8	7.8	8.3	8.8	mA
ERROR AMP SECTION									
V_2	Input Voltage	V_{PIN1} = 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
I_b	Input Bias Current	V_{FB} = 5V		-0.1	-1		-0.1	-2	µA
	A_{VOL}	2V ≤ V_o ≤ 4V	65	90		65	90		dB
BW	Unity Gain Bandwidth	T_J = 25°C	0.7	1		0.7	1		MHz
PSRR	Power Supply Rejec. Ratio	12V ≤ V_i ≤ 25V	60	70		60	70		dB
I_o	Output Sink Current	V_{PIN2} = 2.7V V_{PIN1}= 1.1V	2	12		2	12		mA
I_o	Output Source Current	V_{PIN2} = 2.3V V_{PIN1} = 5V	-0.5	-1		-0.5	-1		mA
	V_{OUT} High	V_{PIN2} = 2.3V;R_L = 15KΩ to Ground	5	6.2		5	6.2		V
	V_{OUT} Low	V_{PIN2} = 2.7V;R_L = 15KΩ to Pin 8		0.8	1.1		0.8	1.1	V
CURRENT SENSE SECTION									
G_V	Gain	(note 3 & 4)	2.85	3	3.15	2.85	3	3.15	V/V
V_3	Maximum Input Signal	V_{PIN1} = 5V (note 3)	0.9	1	1.1	0.9	1	1.1	V
SVR	Supply Voltage Rejection	12 ≤ V_i ≤ 25V (note 3)		70			70		dB
I_b	Input Bias Current			-2	-10		-2	-10	µA
	Delay to Output			150	300		150	300	ns

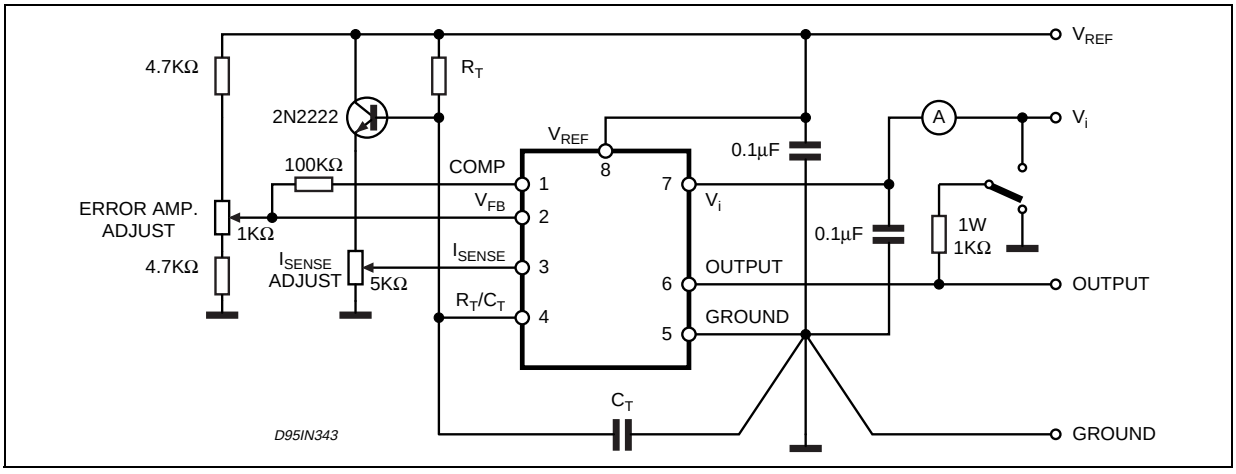
Table 5. Electrical Characteristcs (continued)

([note 1] Unless otherwise stated, these specifications apply for -25 < T_{amb} < 85°C for UC284XA; 0 < T_{amb} < 70°C for UC384XA; V_i = 15V (note 5); R_T = 10K; C_T = 3.3nF)

Symbol	Parameter	Test Condition	UC284XA			UC384XA			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
OUTPUT SECTION									
V_{OL}	Output Low Level	I_{SINK} = 20mA		0.1	0.4		0.1	0.4	V
		I_{SINK} = 200mA		1.6	2.2		1.6	2.2	V
V_{OH}	Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
		I_{SOURCE} = 200mA	12	13.5		12	13.5		V
V_{OLS}	UVLO Saturation	V_{CC} = 6V; I $_{SINK}$ = 1mA		0.7	1.2		0.7	1.2	V
t_r	Rise Time	T_j = 25°C C_L = 1nF (2)		50	150		50	150	ns
t_f	Fall Time	T_j = 25°C C_L = 1nF (2)		50	150		50	150	ns
UNDER-VOLTAGE LOCKOUT SECTION									
	Start Threshold	X842A/4A	15	16	17	14.5	16	17.5	V
		X843A/5A	7.8	8.4	9.0	7.8	8.4	9.0	V
	Min Operating Voltage After Turn-on	X842A/4A	9	10	11	8.5	10	11.5	V
PWM SECTION									
	Maximum Duty Cycle	X842A/3A	94	96	100	94	96	100	%
		X844A/5A	47	48	50	47	48	50	%
	Minimum Duty Cycle				0			0	%
TOTAL STANDBY CURRENT									
I_{st}	Start-up Current	V_i = 6.5V for UCX843A/ 45A		0.3	0.5		0.3	0.5	mA
		V_i = 14V for UCX842A/44A		0.3	0.5		0.3	0.5	mA
I_i	Operating Supply Current	V_{PIN2} = V_{PIN3} = 0V		12	17		12	17	mA
V_{iz}	Zener Voltage	I_i = 25mA	30	36		30	36		V

Notes: 1. Max package power dissipation limits must be respected; low duty cycle pulse techniques are used during test maintain T_j as close to T_{amb} as possible.
2. These parameters, although guaranteed, are not 100% tested in production.
3. Parameter measured at trip point of latch with V_{PIN2} = 0.
4. Gain defined as : A = $\Delta V_{PIN1}/\Delta V_{PIN3}$; 0 ≤ V_{PIN3} ≤ 0.8V
5. Adjust V_i above the start threshold before setting at 15 V.

Figure 4. Open Loop Test Circuit.



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5 KΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 5. Oscillator Frequency vs Timing Resistance

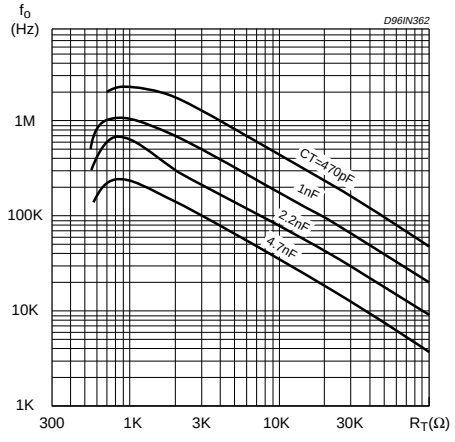


Figure 6. Maximum Duty Cycle vs Timing Resistor

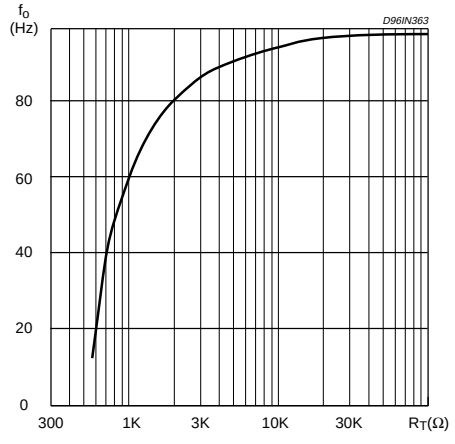


Figure 7. Oscillator Discharge Current vs. Temperature.

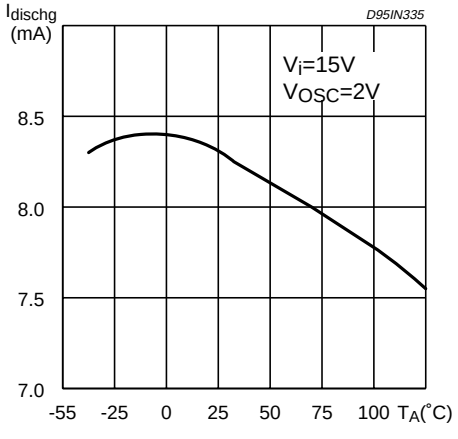


Figure 8. Error Amp Open-Loop Gain and Phase vs. Frequency.

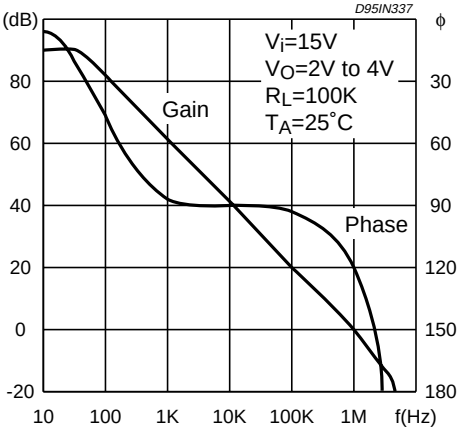


Figure 9. Current Sense Input Threshold vs. Error Amp Output Voltage.

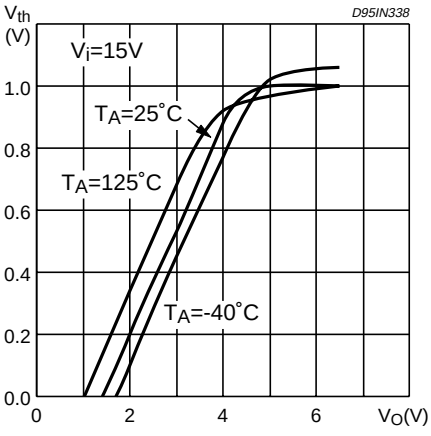


Figure 10. Reference Voltage Change vs. Source Current..

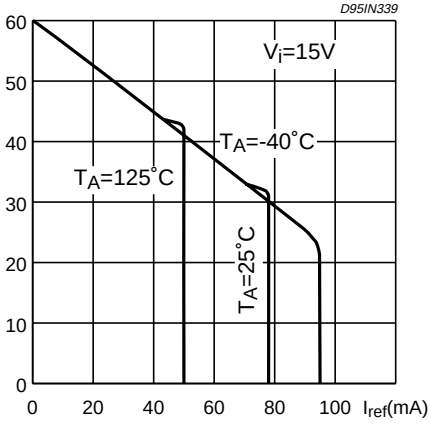


Figure 11. Reference Short Circuit Current vs. Temperature..

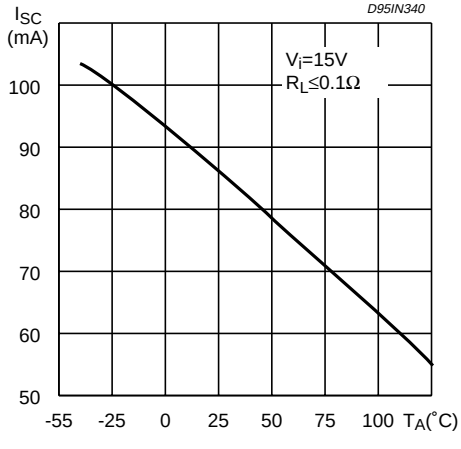


Figure 12. Output Saturation Voltage vs. Load Current.

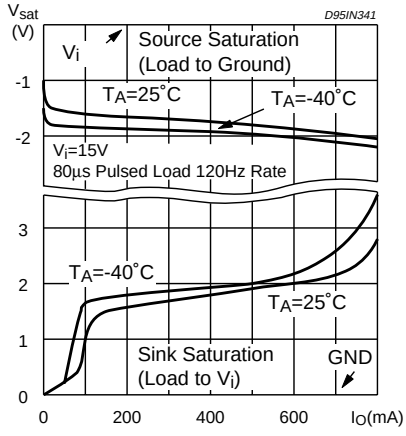


Figure 13. Supply Current vs. Supply Voltage.

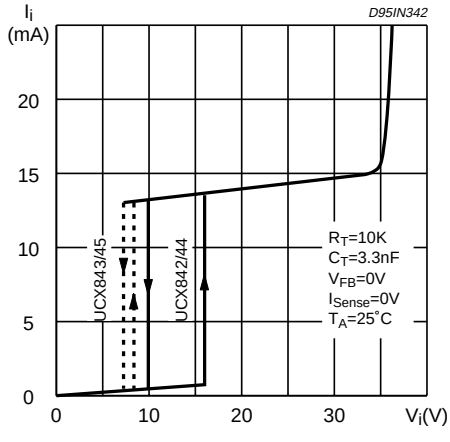


Figure 14. Output Waveform.

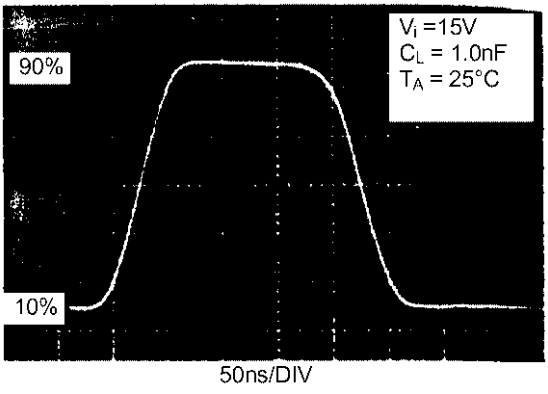


Figure 15. Output Cross Conduction

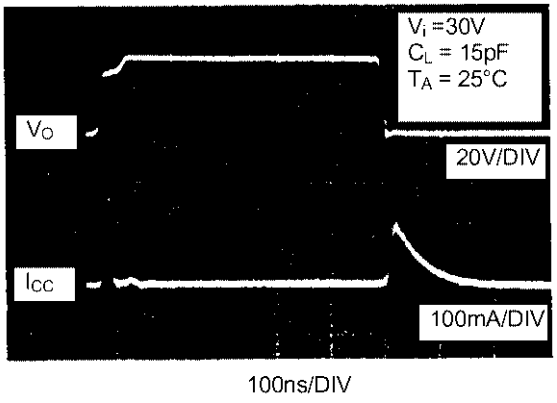


Figure 16. Oscillator and Output Waveforms.

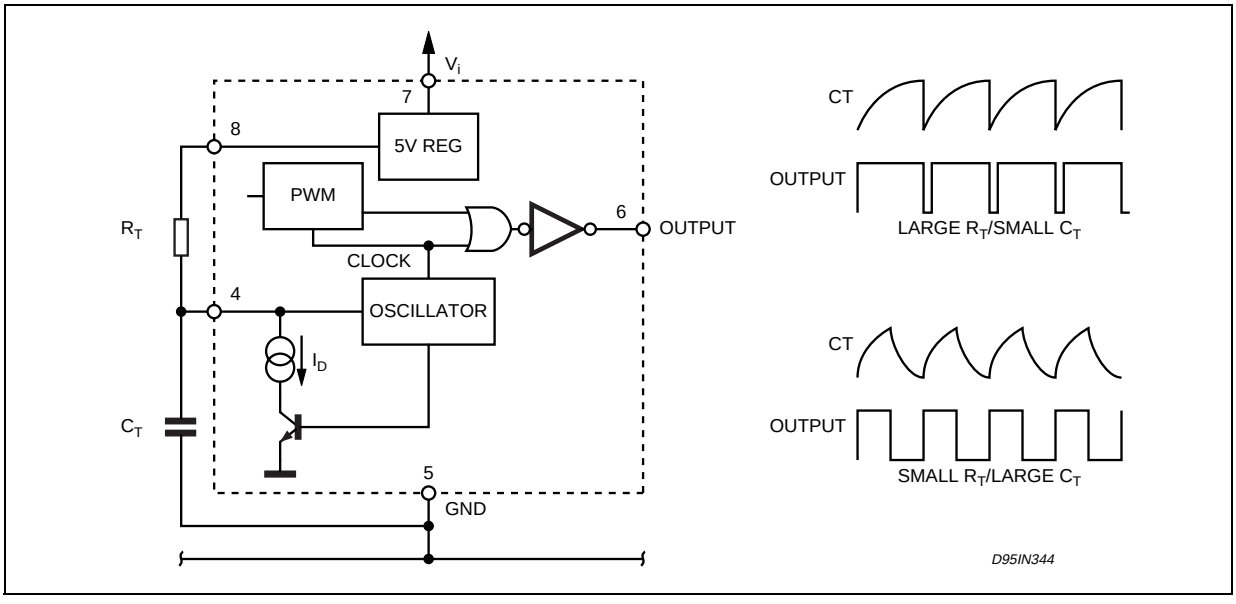


Figure 17. Error Amp Configuration.

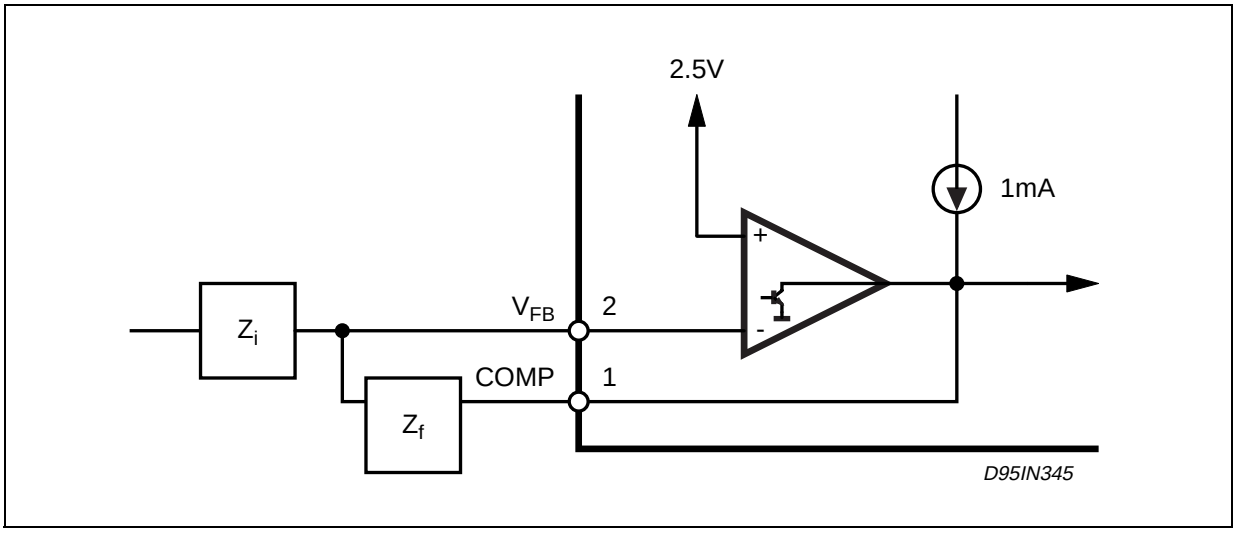


Figure 18. Under Voltage Lockout.

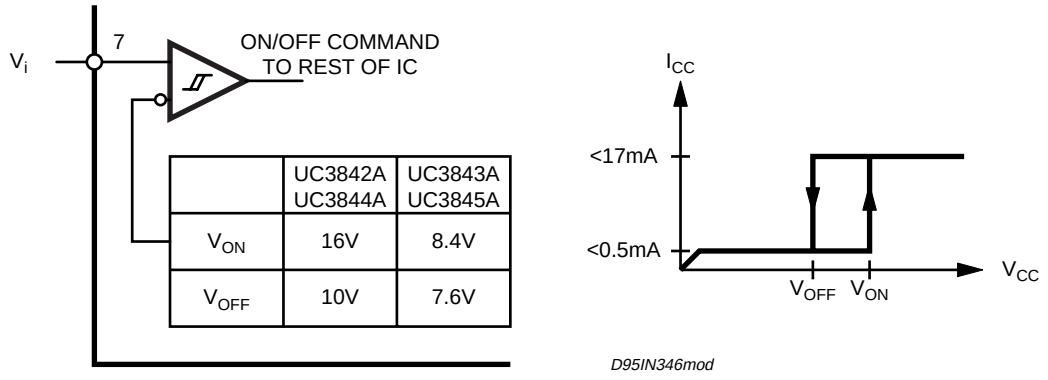
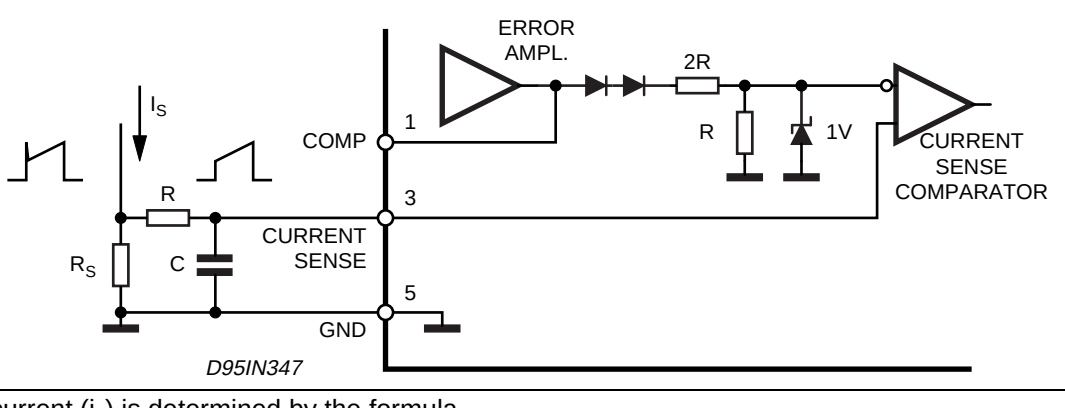


Figure 19. Current Sense Circuit.



Peak current (i_S) is determined by the formula

$$I_{Smax} \approx \frac{1.0V}{R_S}$$

A small RC filter may be required to suppress switch transients.

Figure 20. Slope Compensation Techniques.

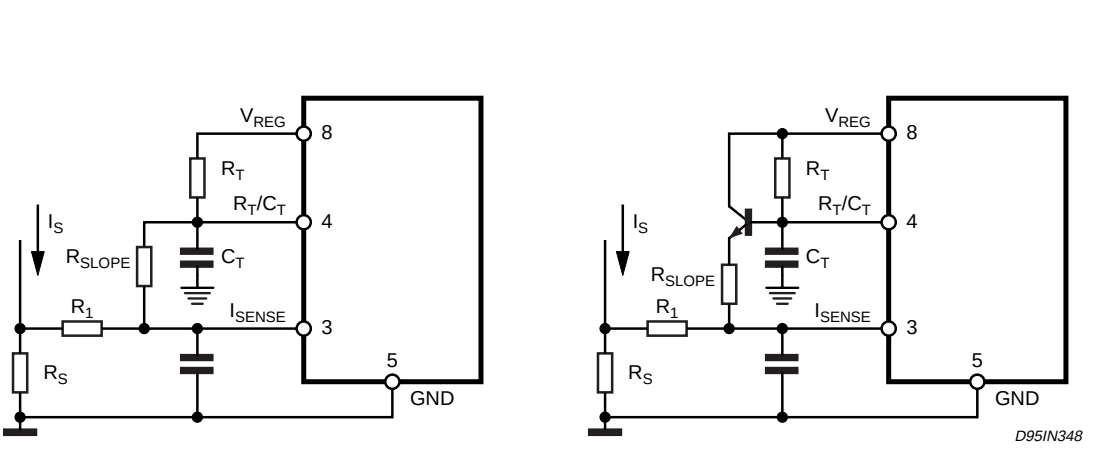


Figure 21. Isolated MOSFET Drive and Current Transformer Sensing.

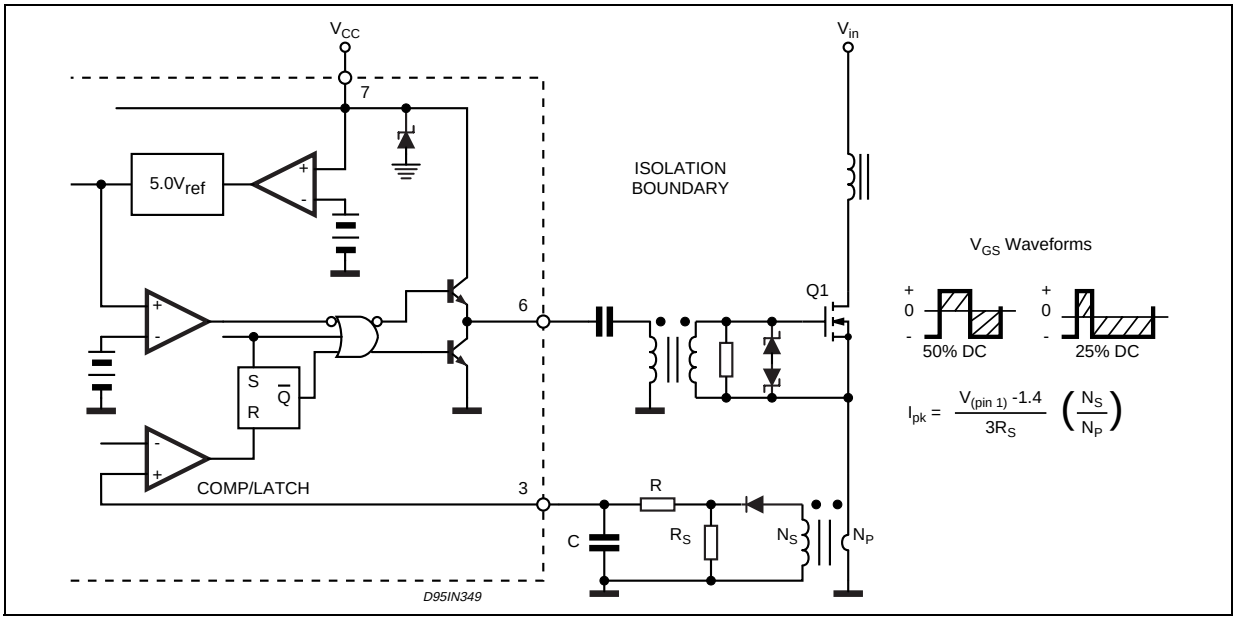
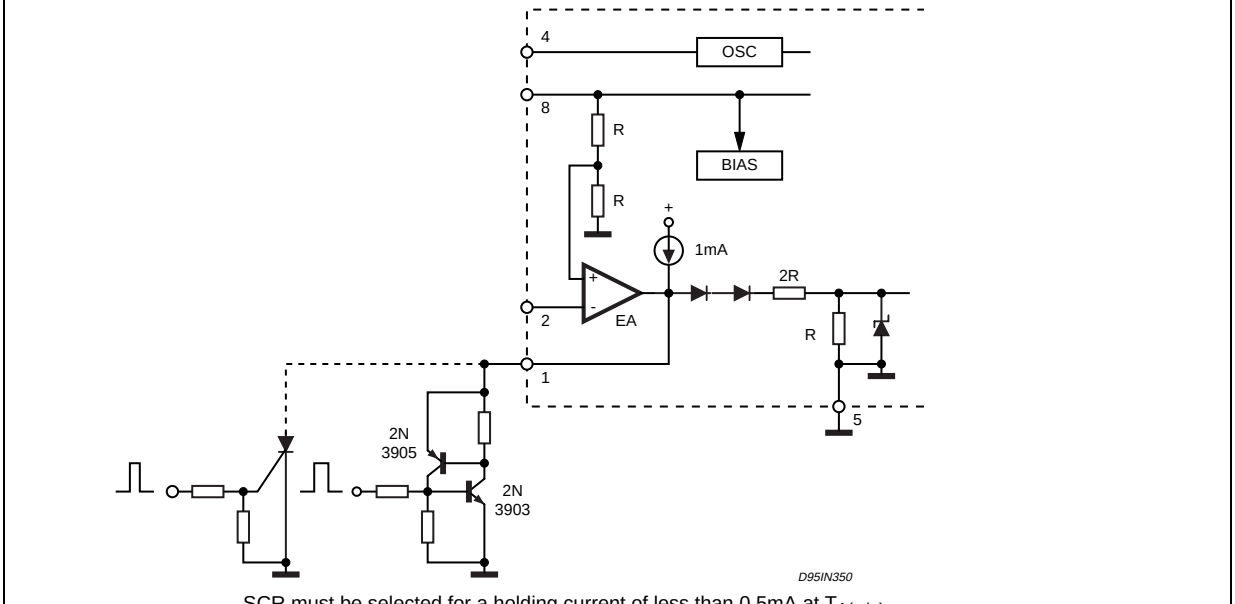
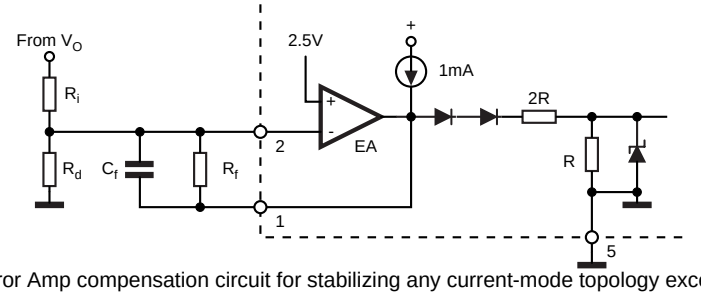


Figure 22. Latched Shutdown.

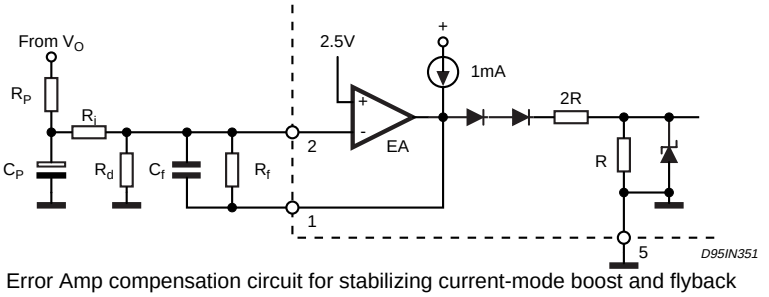


SCR must be selected for a holding current of less than 0.5mA at $T_{A(min)}$.
The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10K.

Figure 23. Error Amplifier Compensation

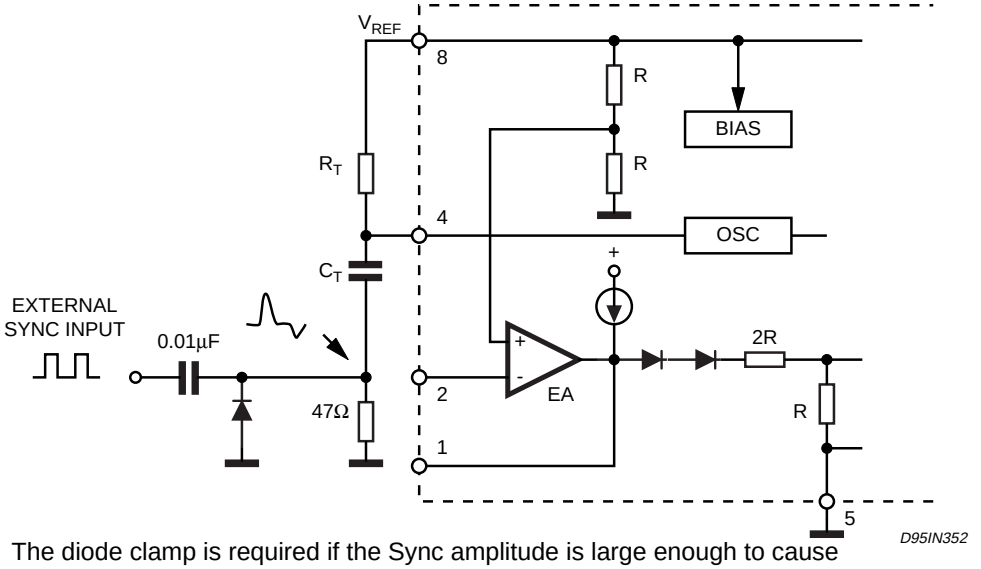


Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

Figure 24. External Clock Synchronization.



The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300mV below ground

Figure 25. External Duty Cycle Clamp and Multi Unit Synchronization.

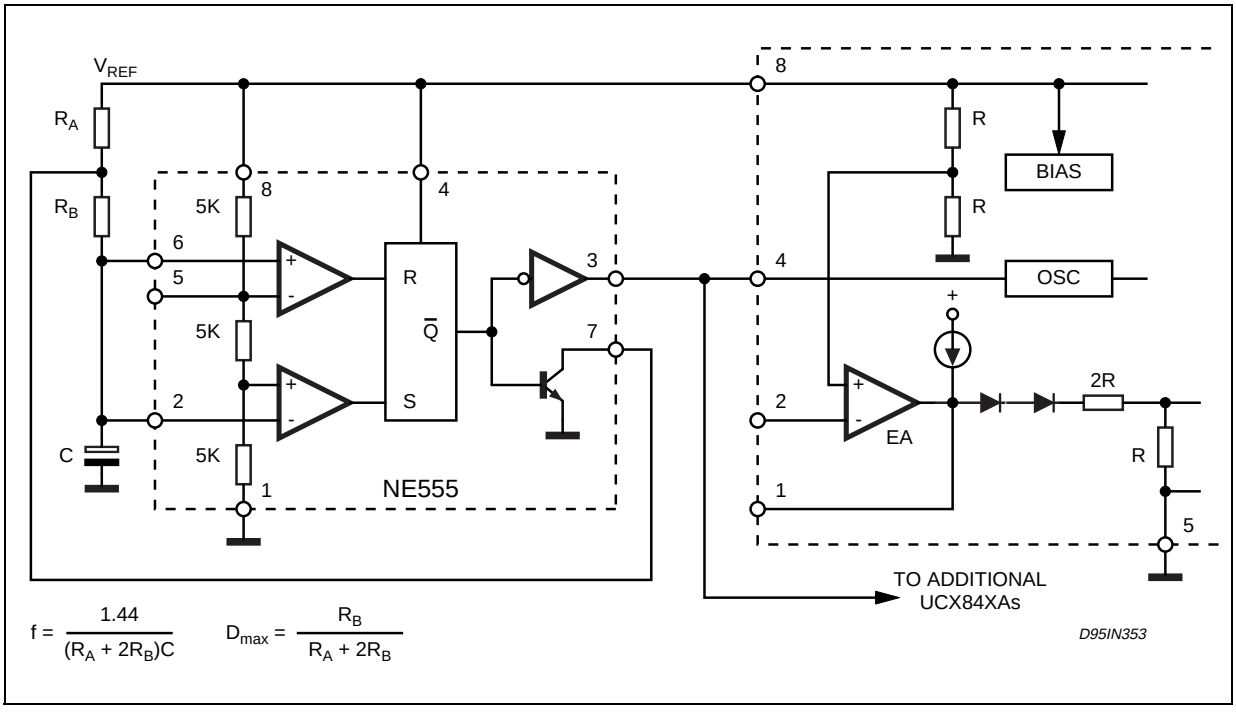


Figure 26. Soft-Start Circuit

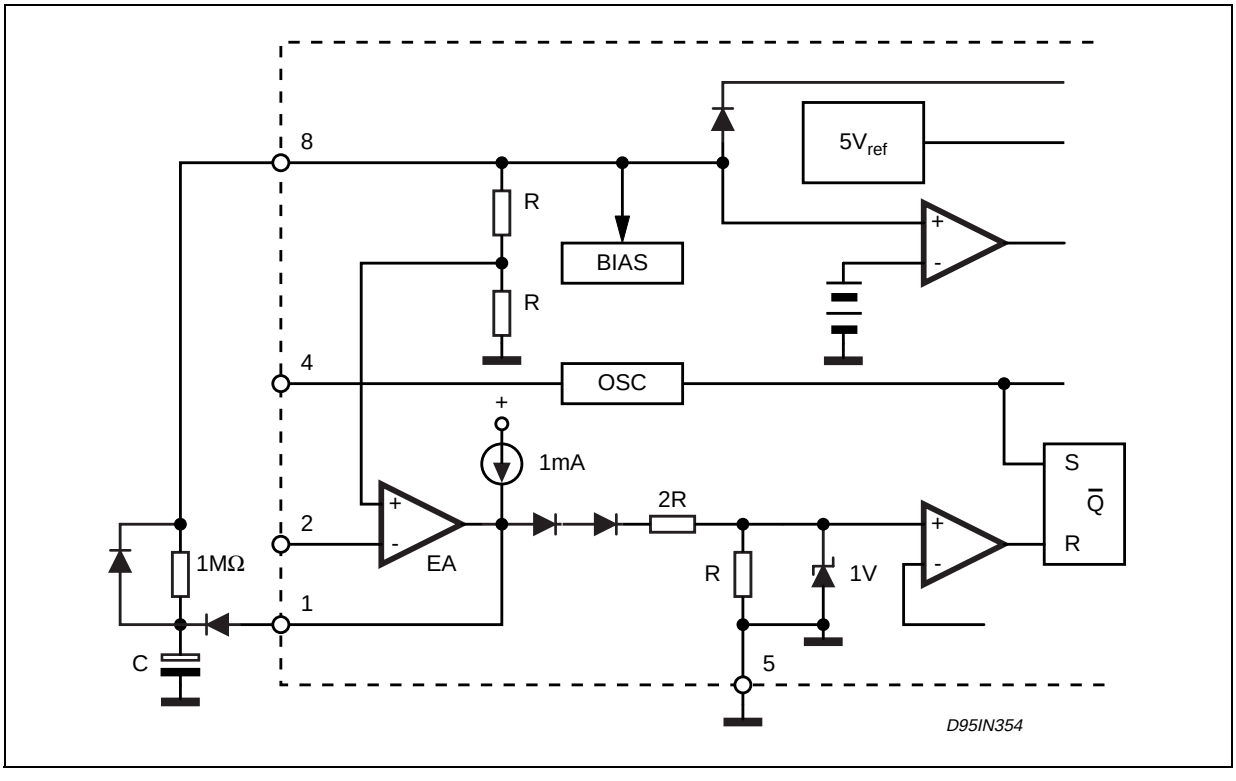


Figure 27. Soft-Start and Error Amplifier Output Duty Cycle Clamp.

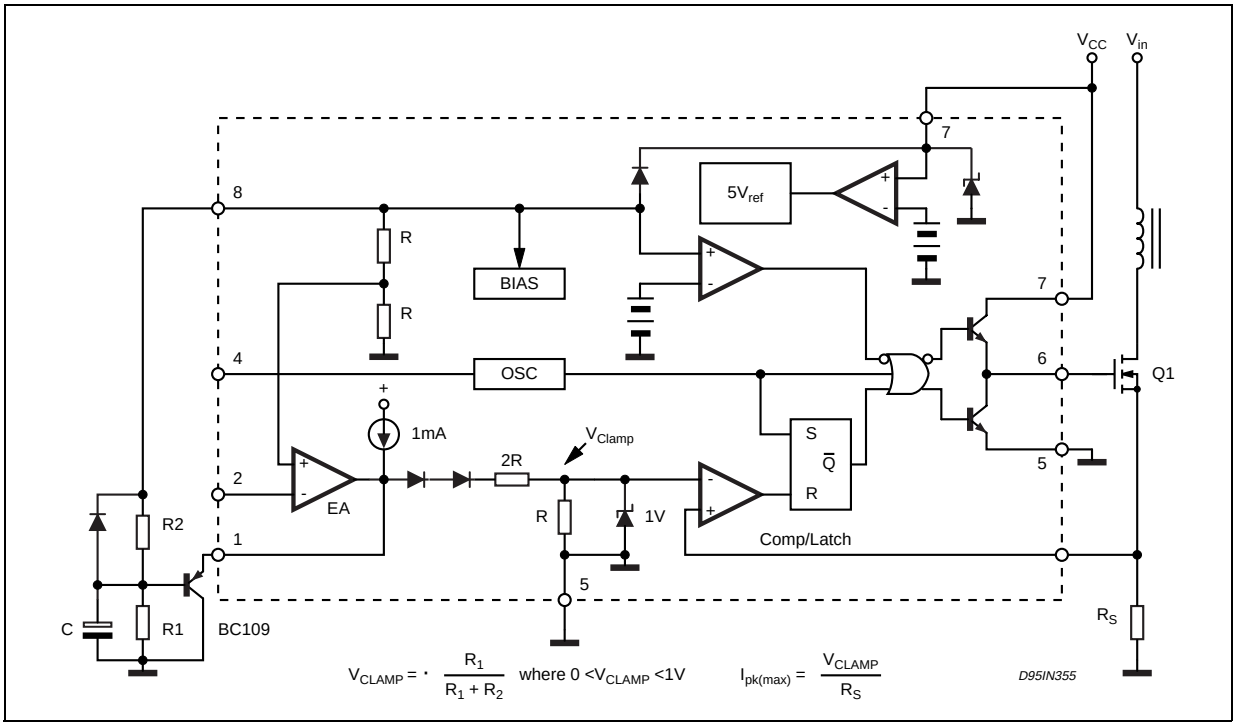
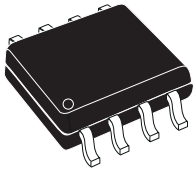


Figure 28. SO-8 Mechanical Data & Package Dimensions

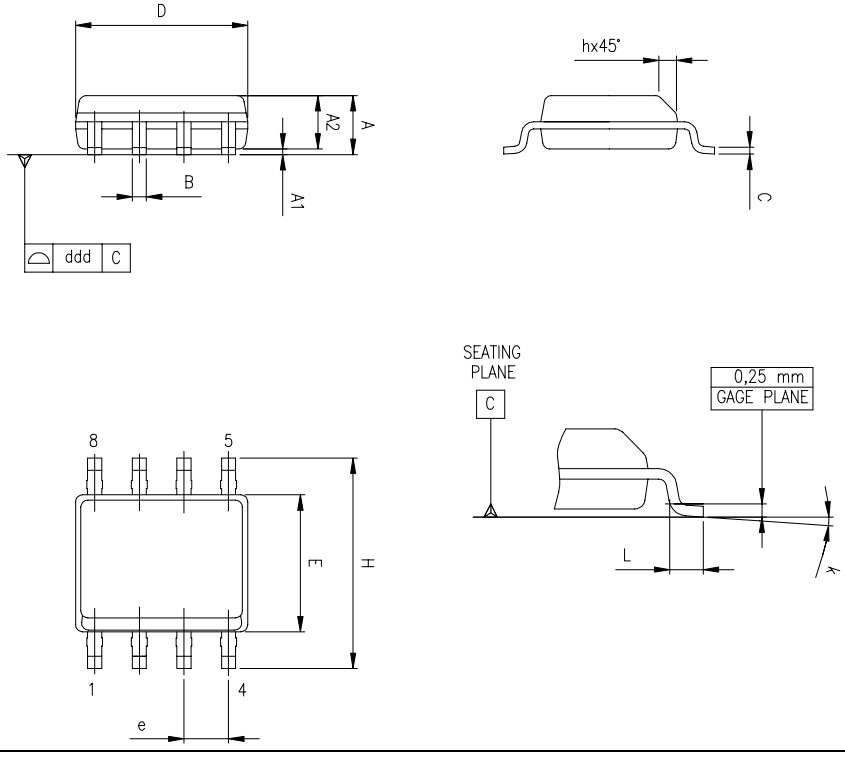
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

Note: (1) Dimensions D does not include mold flash, protrusions or gate burrs.
Mold flash, potrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

OUTLINE AND MECHANICAL DATA



SO-8

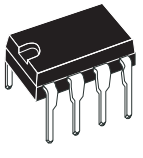


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Figure 29. DIP-8 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

OUTLINE AND MECHANICAL DATA



DIP-8

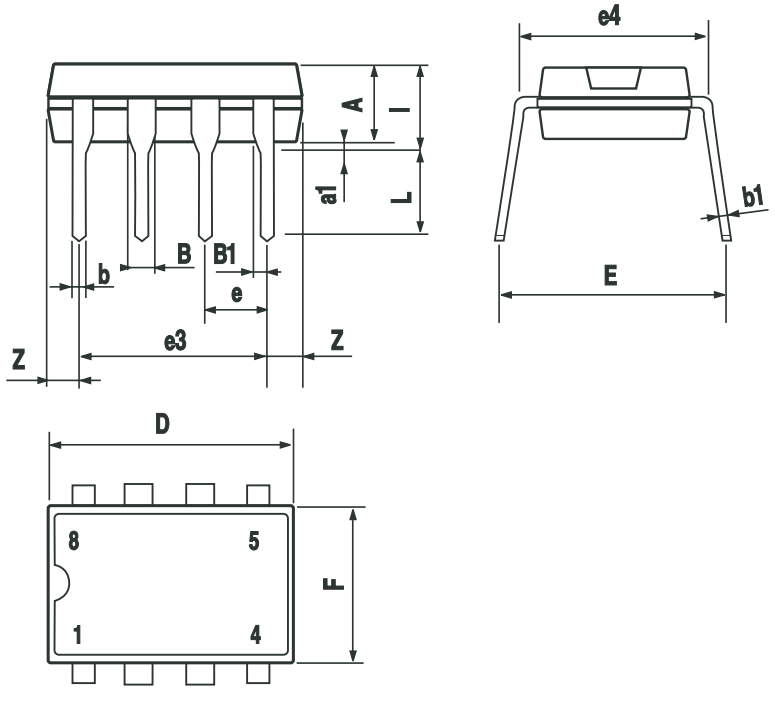


Table 6. Revision History

Date	Revision	Description of Changes
March 1999	4	First Issue in EDOCS
May 2004	5	NOT FOR NEW DESIGN

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