MP7611

Octal 14-Bit DAC Array™ D/A Converter with Output Amplifier and Parallel Data/Address μP Control Logic

June 1998-3

FEATURES

- Eight Independent Channel 14-Bit DACs with Output Amplifiers
- Low Power 320 mW (typ.)
- Parallel Digital Data and Address Port
- Double Buffered Data Interface
- Readback of DAC Latches
- Zero Volt Output Preset (Data = 10 .. 00)
- 14-Bit Resolution, 12-Bit Accuracy
- Extremely Well Matched DACs
- Extremely Low Analog Ground Current (<60μA/Channel)
- ±10 V Output Swing with ±11.4 V Supplies
- Rugged Construction – Latch-Up Free
- Serial Version: MP7610

APPLICATIONS

- Data Acquisition Systems
- ATE
- Process Control
- Self-Diagnostic Systems
- Logic Analyzers
- Digital Storage Scopes
- PC Based Controller/DAS

GENERAL DESCRIPTION

The MP7611 provides eight independent 14-bit resolution Digital-to-Analog Converters with voltage output amplifiers and a parallel digital address and data port.

Built using an advanced linear BiCMOS, these devices offer rugged solutions that are latch-up free, and take advantage of EXAR s patented thin-film resistor process which exhibits excellent long term stability and reliability.

A standard μ-processor and TTL/CMOS compatible 14-bit input data port loads the data into the pre-selected DACS.

This device can easily be interfaced to a data bus, and digital readback of each channel is available.

Typical DAC matching for C grade versions is 1.5 LSB across all codes. The output amplifier is capable of sinking and sourcing 5mA, and the output voltage settles to 12-bits in less than 30μs (typ.).

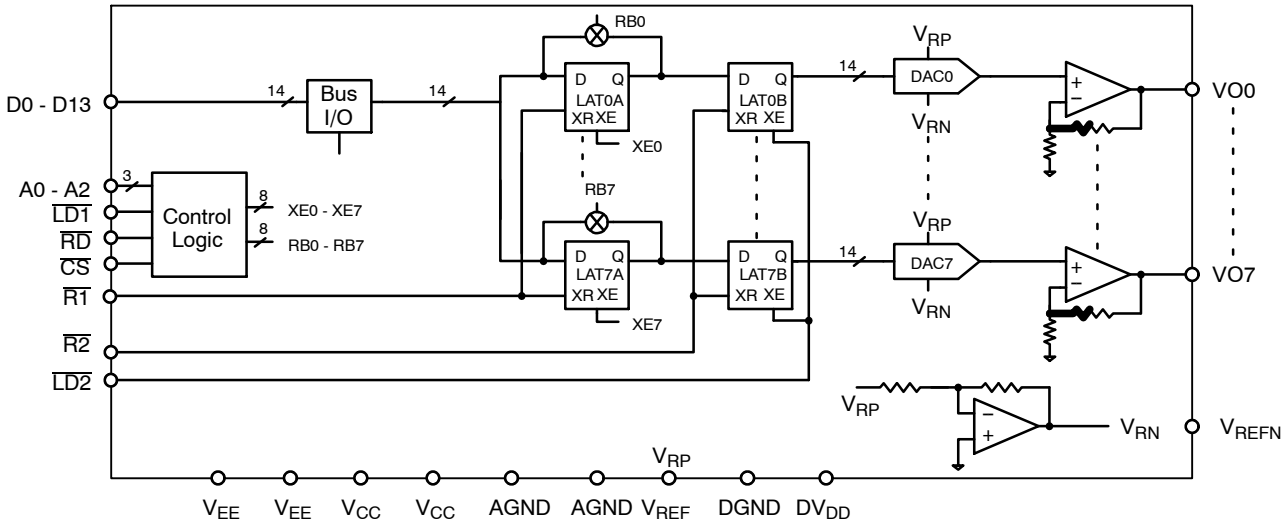
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	Res. (Bits)	INL (LSB)	DNL (LSB)	FSE (LSB)
PQFP	0 to +70°C	MP7611CE	14	±2	±2	±16
PQFP	–40 to +85°C	MP7611BE	14	±4	±3	±24
PQFP	–40 to +85°C	MP7611AE	14	±8	±4	±32
PLCC	0 to +70°C	MP7611CP	14	±2	±2	±16
PLCC	–40 to +85°C	MP7611BP	14	±4	±3	±24
PLCC	–40 to +85°C	MP7611AP	14	±8	±4	±32

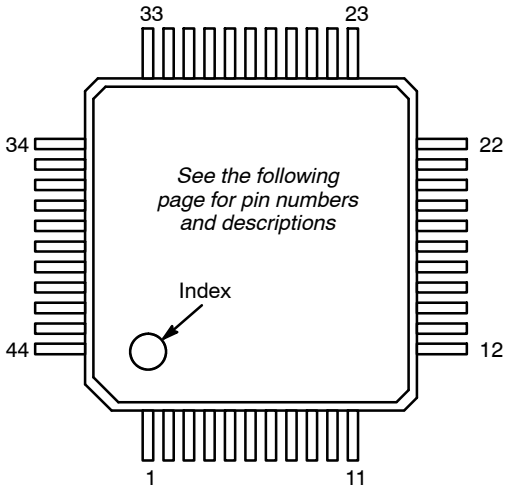
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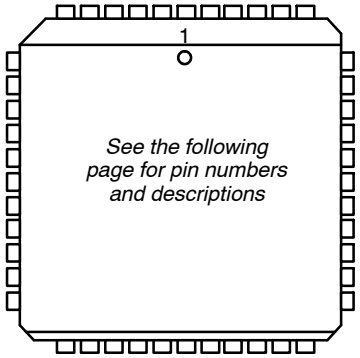
SIMPLIFIED BLOCK DIAGRAM



PIN CONFIGURATIONS



44-Pin PQFP (14 mm x 14 mm)



44-Pin PLCC

PIN OUT DEFINITIONS

PLCC PIN NO.	PQFP PIN NO.	NAME	DESCRIPTION
29	1	N/C	No Connection
30	2	VO3	DAC 3 Output
31	3	V_{EE}	Analog Negative Power Supply (–12 V)
32	4	V_{CC}	Analog Positive Power Supply (+12 V)
33	5	N/C	No Connection or DV_{DD}
34	6	V_{REF}	Analog Voltage Reference Input (+5 V)
35	7	V_{REFN}	Analog Negative Voltage Reference Output (–2.5 V)
36	8	V_{CC}	Analog Positive Power Supply (+12 V)
37	9	V_{EE}	Analog Negative Power Supply (–12 V)
38	10	VO4	DAC 4 Output
39	11	N/C	No Connection
40	12	VO5	DAC 5 Output
41	13	VO6	DAC 6 Output
42	14	VO7	DAC 7 Output
43	15	AGND	Analog Ground (0 V)
44	16	$\overline{CS}$	Chip Select Enable
1	17	$\overline{RD}$	Read Back Enable
2	18	$\overline{R2}$	Second–Latch-Bank Reset Enable
3	19	$\overline{R1}$	First–Latch-Bank Reset Enable
4	20	$\overline{LD2}$	Second–Latch-Bank Load Enable
5	21	$\overline{LD1}$	First–Latch-Bank Load Enable
6	22	A2	Digital Address Bit 2
7	23	A1	Digital Address Bit 1
8	24	A0	Digital Address Bit 0
9	25	DB0	Digital Input Data Bit 0
10	26	DB1	Digital Input Data Bit 1
11	27	DB2	Digital Input Data Bit 2
12	28	DB3	Digital Input Data Bit 3
13	29	DB4	Digital Input Data Bit 4
14	30	DB5	Digital Input Data Bit 5
15	31	DB6	Digital Input Data Bit 6
16	32	DB7	Digital Input Data Bit 7
17	33	DB8	Digital Input Data Bit 8
18	34	DB9	Digital Input Data Bit 9
19	35	DB10	Digital Input Data Bit 10
20	36	DB11	Digital Input Data Bit 11
21	37	DB12	Digital Input Data Bit 12
22	38	DB13	Digital Input Data Bit 13 (MSB)
23	39	DV_{DD}	Digital Positive Power Supply (+5 V)
24	40	DGND	Digital Ground (0 V)
25	41	AGND	Analog Ground (0 V)
26	42	VO0	DAC 0 Output
27	43	VO1	DAC 1 Output
28	44	VO2	DAC 2 Output

ELECTRICAL CHARACTERISTICS

V_{CC} = +12 V, V_{EE} = −12 V, V_{REF} = 5 V, DV_{DD} = 5.0 V, T = 25°C, Output Load = 5kΩ (unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE								
Resolution (All Grades)	N	14					Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity Spec
A				±8		±8		
B				±4		±4		
C				±2		±2.5		
Differential Non-Linearity	DNL						LSB	
A				±4		±4		
B				±3		±3		
C				±2		±2.5		
Positive Full Scale Error	+FSE						LSB	
A			24	±32		±32		
B			16	±24		±24		
C			12	±16		±16		
Positive Full Scale Error Temperature Coefficient	Δ+FSE/ ΔT		4				ppm/°C	0°C to 85°C
Negative Full Scale Error	−FSE						LSB	
A			24	±32		±32		
B			16	±24		±24		
C			12	±16		±16		
Negative Full Scale Error Temperature Coefficient	Δ−FSE/ ΔT		4				ppm/°C	0°C to 85°C
Bipolar Zero Offset	ZOFS						LSB	
A				±16		±16		
B				±12		±12		
C				±12		±12		
Bipolar Zero Offset Temperature Coefficient	ΔZOFS/ ΔT		2				ppm/°C	0°C to 85°C
INL Matching	ΔINL						LSB	
A				±8		±8		
B				±6		±6		
C				±6		±6		
All Channels Maximum Error with DAC 0 adjusted to minimum error	ME						LSB	
A				±16		±16		
B				±8		±8		
C				±6		±6		
Bipolar Zero Matching	ΔZOFS						LSB	
A				±16		±16		
B				±12		±12		
C				±12		±12		
Full Scale Error Matching	ΔFSE						LSB	
A				±16		±16		
B				±12		±12		
C				±12		±12		

ELECTRICAL CHARACTERISTICS (CONT D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE								
Voltage Settling from $\overline{LD}$ to VDAC Out[1]	t_{sd}		30	50		50	µs	ZS to FS (20 V Step) 5k, 50pF load
Channel-to-Channel Crosstalk[6]	CT		0.04				LSB	DC
Digital Feedthrough[1, 6]	Q		–70				dB	CLK and Data to V_{OUTi}
Power Supply Rejection Ratio	PSRR		5				ppm/%	ΔV_{EE} & ΔV_{CC} = ±5%, ppm of FS
REFERENCE INPUTS								
Impedance of V_{REF}	REF	350	700	1.05k	350	1.05k	Ω	See Application Hints for driving the reference input
V_{REF} Voltage1, [2]	V_{REF}	3.5		6			V	
DIGITAL INPUTS[3]								
Logic High	V_{IH}	2.4					V	
Logic Low	V_{IL}			0.8			V	
Input Current	I_L			±10			µA	
Input Capacitance[1]	C_L			8			pF	
ANALOG OUTPUTS								
Output Swing		$-V_{EE}$ +1.4	V_{CC} –1.4				V	
Output Drive Current		–5		5			mA	
V_{REFN} Output Drive Current		–10		+10			µA	For test purposes only
Output Impedance	R_O		1				Ω	
Output Short Circuit Current	I_{SC}		25				mA	+FS to AGND
			30				mA	+FS to V_{EE}
			40				mA	–FS to AGND
			55				mA	–FS to V_{CC}
DIGITAL OUTPUTS								
Output High Voltage	V_{OH}		4.5				V	
Output Low Voltage	V_{OL}		0.5				V	
POWER SUPPLIES								
V_{CC} Voltage[5]	V_{CC}	V_{REF}+1.5	12	12.75	V_{REF}+1.5	12.75	V	
V_{EE} Voltage[5]	V_{EE}	–12.75	–12	–5	–12.75	–5	V	
DV_{DD} Voltage	DV_{DD}	4.5	5	5.5	4.5	5.5	V	
Positive Supply Current	I_{CC}		8	10		10	mA	Bipolar zero
Negative Supply Current	I_{EE}		15	20		20	mA	Bipolar zero
Digital Supply Current	I_{DD}			2		2	mA	Bipolar zero
Power Dissipation	PD_{ISS}		320	420		450	mW	Bipolar zero
ANALOG GROUND CURRENT								
Per Channel[1]	I_{AGND}		±60				µA	See Application Notes
DIGITAL TIMING SPECIFICATIONS[1,4]								V_{IL} = 0 V, V_{IH} = 5 V, C_L = 20 pF
Data Setup Time	t_{DS}	20					ns	
Data Hold Time	t_{DH}	20					ns	
Address Set-up Time	t_{AS}	100					ns	
Address Hold Time	t_{AH}	0					ns	
Chip Select to $\overline{LD1}$ Set-up Time	t_{CS1}	6					ns	
Chip Select to $\overline{LD1}$ Hold Time	t_{CH1}	0					ns	
$\overline{LD1}$ Pulse Width	t_{LD1W}	50					ns	
$\overline{LD1}$ Negative Edge to $\overline{LD2}$ Positive Edge	t_{LD1LD2}	60					ns	
$\overline{LD2}$ Pulse Width	t_{LD2W}	60					ns	
Chip Select to $\overline{RD}$ Set-Up Time	t_{CS2}	6					ns	
Chip Select to $\overline{RD}$ Hold Time	t_{CH2}	0					ns	

ELECTRICAL CHARACTERISTICS (CONT D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL TIMING SPECIFICATIONS[1, 4] (CONT D)								
$\overline{RD}$ Pulse Width	t_{RD}	600					ns	
High Z to Data Valid for Readback	t_{DA}	600					ns	
Data Valid for Readback to High Z	t_{DR}	200					ns	
$\overline{R1}$ Pulse Width	t_{R1W}	100					ns	
$\overline{R2}$ Pulse Width	t_{R2W}	100					ns	

NOTES:

1 Guaranteed; not tested.

2 Specified values guarantee functionality.

3 Digital inputs should not go below digital GND or exceed DV_{DD} supply voltage.

4 *See Figures 1, 2 and 3*. All digital input signals are specified with $t_R = t_F = 10$ ns 10% to 90% and timed from a 50% voltage level.

5 For power supply values < $\pm 2 * V_{REF}$, the output swing is limited as specified in Analog Outputs.

6 Digital feedthrough and channel-to-channel crosstalk are heavily dependent on the board layout and environment.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)[1, 2]

V_{CC} to AGND ..... +16.5 V
V_{EE} to AGND ..... −16.5 V
DV_{DD} to DGND ..... +6.5 V
VREF to DGND ..... +7.0 V
Analog Outputs & Inputs
Infinite Shorts to V_{CC}, V_{EE}, DV_{DD}, AGND and DGND (provided that power dissipation of the package spec is not exceeded)
AGND to DGND ..... ±1 V
(Functionality guaranteed for ±0.5 V only)
Digital Input & Digital Output Voltage to:
DV_{DD} ..... +.5 V
DGND ..... −.5 V
Operating Temperature Range
Extended Industrial ..... −40°C to +85°C
Military ..... −55°C to +125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation Rating to 75°C
PQFP, PGA, PLCC 800mW
Derates above 75°C ..... 11mW/°C

NOTES:

1 Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

APPLICATION NOTES

NOTE: When using these DACs to drive remote devices, the accuracy of the output can be improved by utilizing a remote analog ground connection. The difference between the DGND and AGND should be limited to ±300 mV to assure normal operation. If there is any chance that the AGND to DGND can be greater than ±1 V, we recommend two back-to-back diodes be used between DGND and AGND to clamp the voltage and prevent damage to the DAC. Using a buffer between the remote ground location and AGND may help reduce noise induced from long lead or trace lengths.

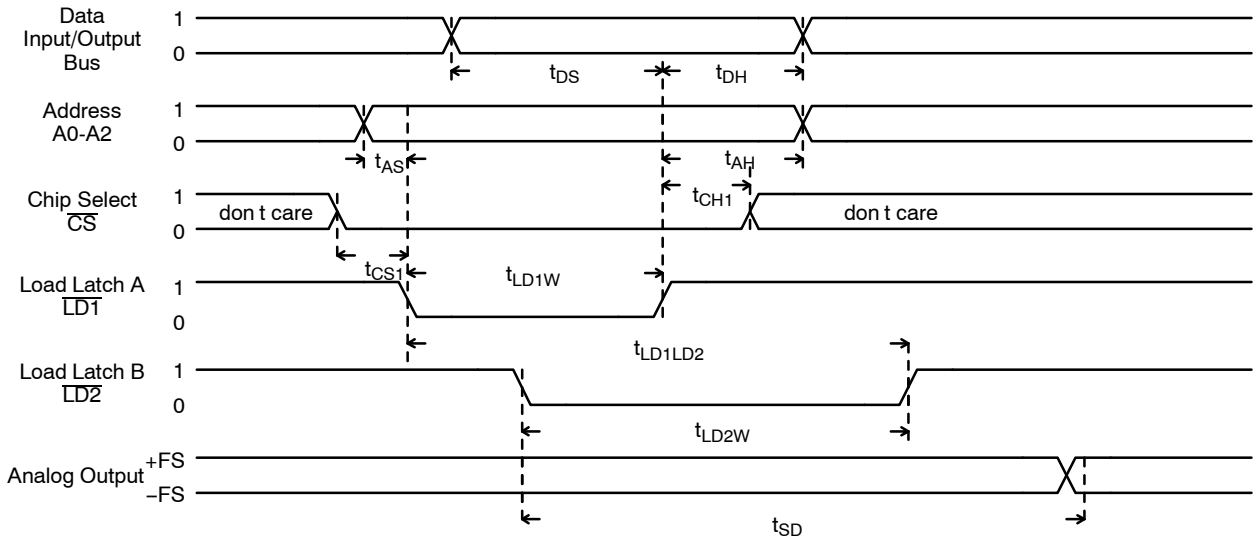


Figure 1. Loading Latch A and Updating Latch B

Notes:
(1) Chip Select ($\overline{CS}$) and Load LATCHA ($\overline{LD1}$) Signals follow the same timing constraints and are interchangeable in the above diagram.
(2) $\overline{R1}$ = $\overline{R2}$ = 1.
(3) For the case where $\overline{LD2}$ is in the low state, analog output would respond to the falling edge of $\overline{LD1}$ (transparent mode).

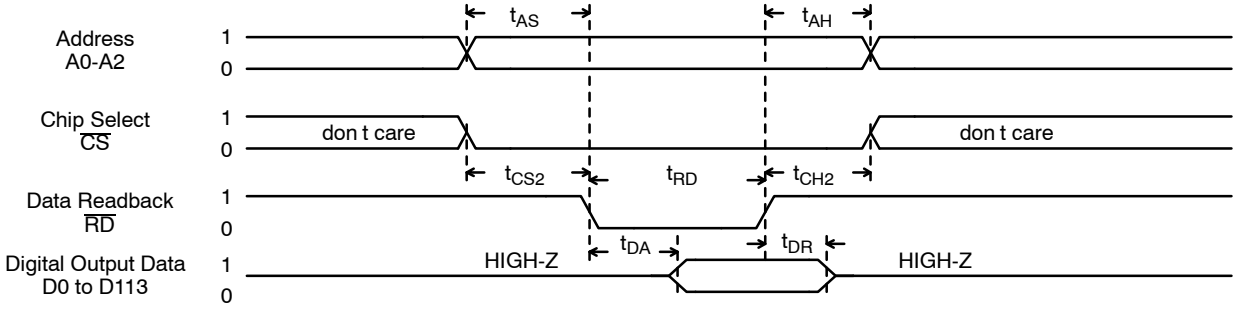


Figure 2. Read Back First Latch Bank of One DAC

Notes:
(1) Chip Select ($\overline{CS}$) and Data Readback ($\overline{RD}$) Signals follow the same timing constraints and are interchangeable in the above diagram.
(2) $\overline{R1}$ = $\overline{R2}$ = 1.

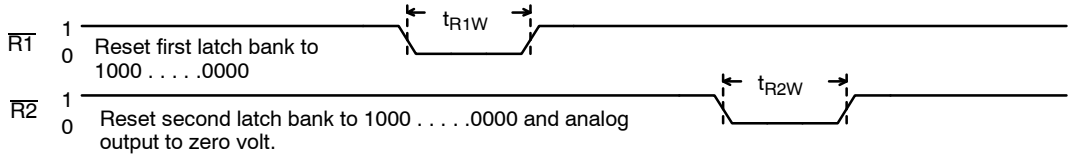


Figure 3. Reset Operations

A standard μ-processor and TTL/CMOS compatible input data port loads the data into the pre-selected DACS. If $\overline{CS}$ = 0, the chip accesses digital data on the bus. Then address bits A0 to A2 select the appropriate DAC and $\overline{LD1}$ loads the data into the first-latch-bank. When all 8-channels first-latch-banks are loaded, then $\overline{LD2}$ enables the second-latch-bank and updates all 8-channels simultaneously. The selected DAC becomes transparent (activity on the digital inputs appear at the analog output) when both $\overline{LD1}$ = $\overline{LD2}$ = 0.

$\overline{R1}$ = 0 resets the first-latch-bank. $\overline{R2}$ = 0 resets the second-latch-bank which sets the analog output to zero volts (data = 100...00), regardless of digital inputs.

Function	A2	A1	A0	$\overline{RD}$	$\overline{LD1}$	$\overline{LD2}$	$\overline{CS}$	$\overline{R1}$	$\overline{R2}$
Load Latch 1 of DAC1	0	0	0	1	0→1	1	0	1	1
Load Latch 1 of DAC2	0	0	1	1	0→1	1	0	1	1
Load Latch 1 of DAC3	0	1	0	1	0→1	1	0	1	1
Load Latch 1 of DAC4	0	1	1	1	0→1	1	0	1	1
Load Latch 1 of DAC5	1	0	0	1	0→1	1	0	1	1
Load Latch 1 of DAC6	1	0	1	1	0→1	1	0	1	1
Load Latch 1 of DAC7	1	1	0	1	0→1	1	0	1	1
Load Latch 1 of DAC8	1	1	1	1	0→1	1	0	1	1
Load Latch 2 of DAC1→8	X	X	X	1	1	0→1	X	1	1
Read Latch 1 of DAC1	0	0	0	0	1	1	0	1	1
Read Latch 1 of DAC2	0	0	1	0	1	1	0	1	1
Read Latch 1 of DAC3	0	1	0	0	1	1	0	1	1
Read Latch 1 of DAC4	0	1	1	0	1	1	0	1	1
Read Latch 1 of DAC5	1	0	0	0	1	1	0	1	1
Read Latch 1 of DAC6	1	0	1	0	1	1	0	1	1
Read Latch 1 of DAC7	1	1	0	0	1	1	0	1	1
Read Latch 1 of DAC8	1	1	1	0	1	1	0	1	1
Reset Latch 1 of DAC1→8	X	X	X	X	X	X	X	0	1
Reset Latch 2 of DAC1→8	X	X	X	X	X	X	X	1	0

Note: 1: High, 0: Low, X: Don t Care

Table 1. Octal Parallel Data Input 14-Bit DAC Truth Table

Note: *For timing information see Electrical Characteristics*

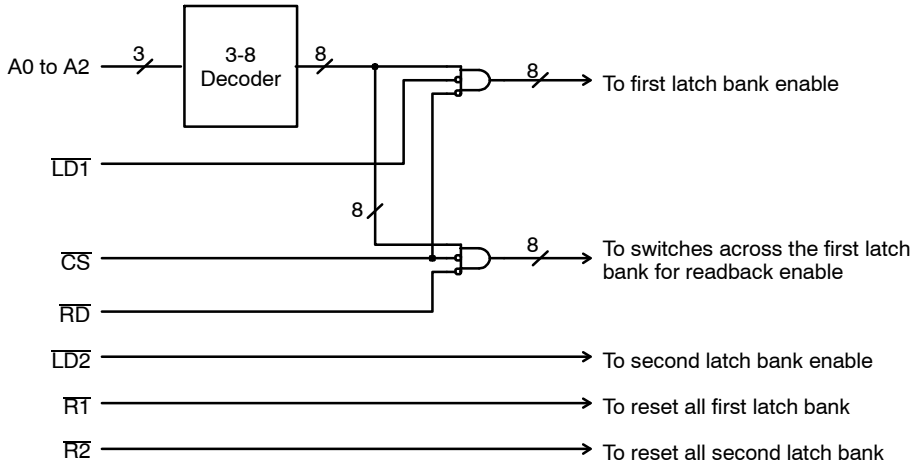


Figure 4. Simplified Parallel Logic Port

Hex Code	Binary Code	Output Voltage = 2 • Vr (–1 + $\frac{2 \bullet D}{16384}$) (Vr = +5 V)
O O O O	00000000000000	10 • (–1 + 0) = –10
⋮	⋮	⋮
1 F F F	01111111111111	10 • (–1 + $\frac{16382}{16384}$) = –1.22 mV
2 O O O	10000000000000	10 • (–1 + $\frac{16384}{16384}$) = 0
2 O O 1	10000000000001	10 • (–1 + $\frac{16386}{16384}$) = 1.22 mV
⋮	⋮	⋮
3 F F F	11111111111111	10 • (–1 + $\frac{32766}{16384}$) = 9.99878

Table 2. MP7611
Ideal DAC Output vs. Input Code

Note: *See Electrical Characteristics for real system accuracy*

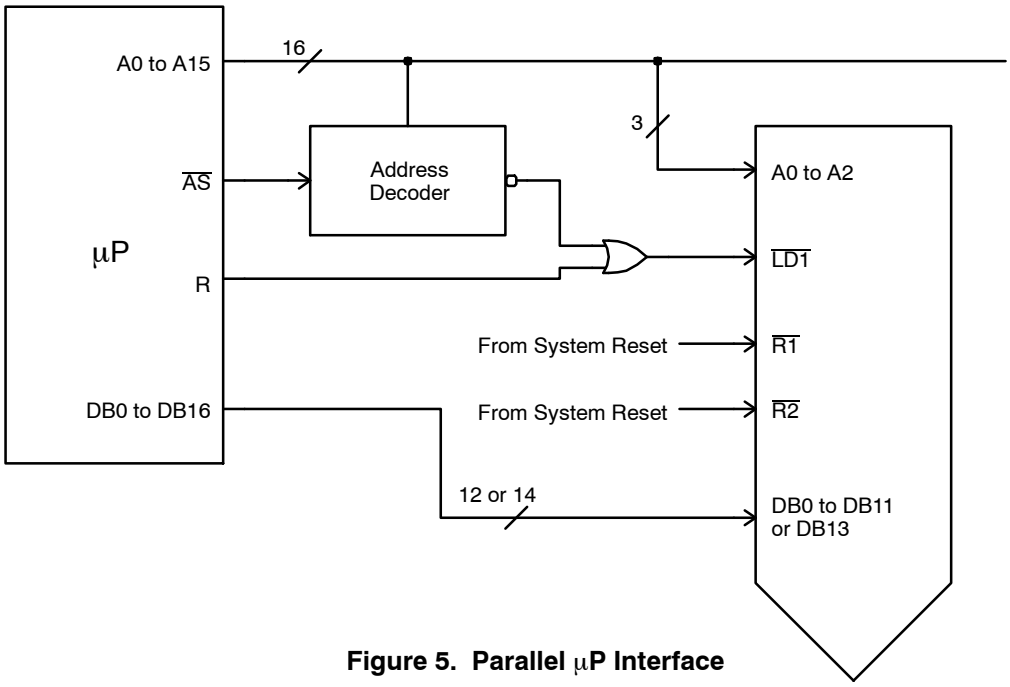
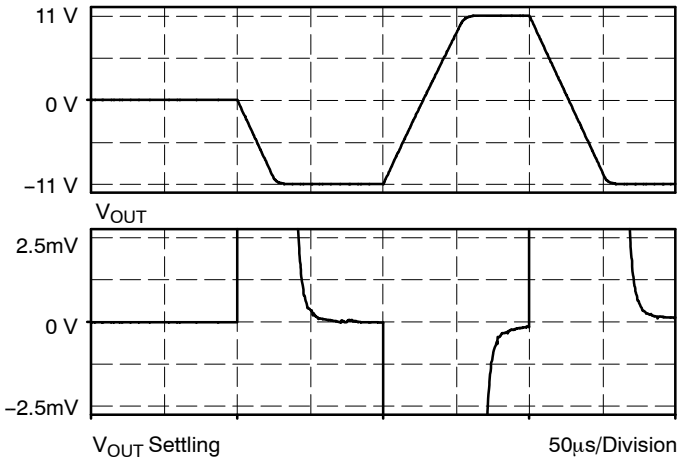


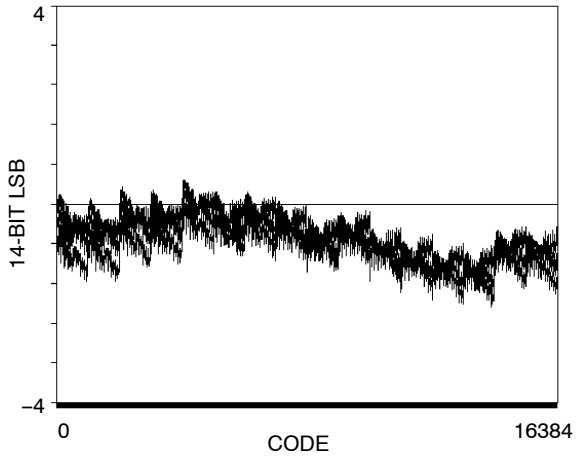
Figure 5. Parallel μP Interface

PERFORMANCE CHARACTERISTICS

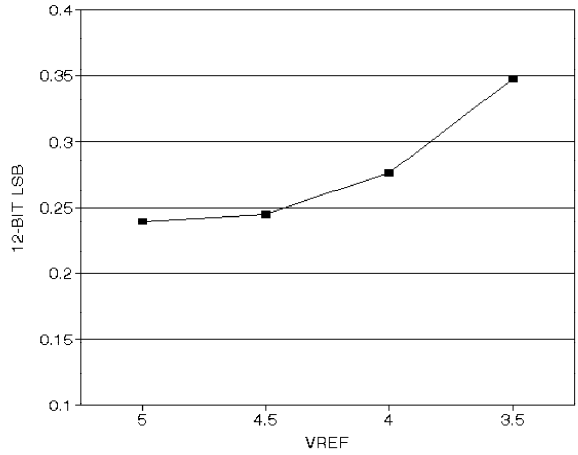


Graph 1. Typical Output Settling Characteristic
V_{REF} = 5 V, R_L = 5K, C_L = 500pF

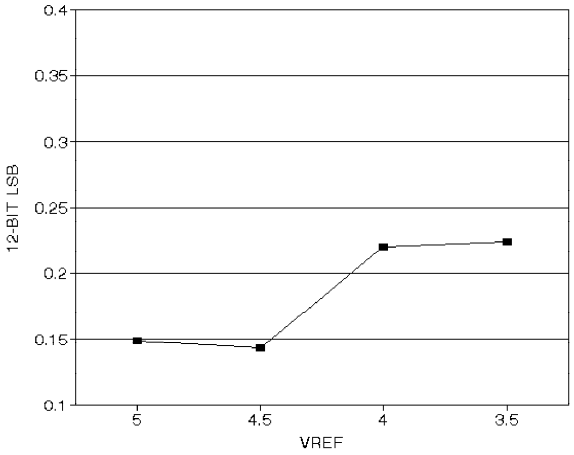
Graph 1 shows the typical output settling characteristic of the MP7610 Family for a RESET →ZS→FS→ZS series of code transitions. The top graph shows the output voltage transients, while the bottom graph shows the difference between the output and the ideal output.



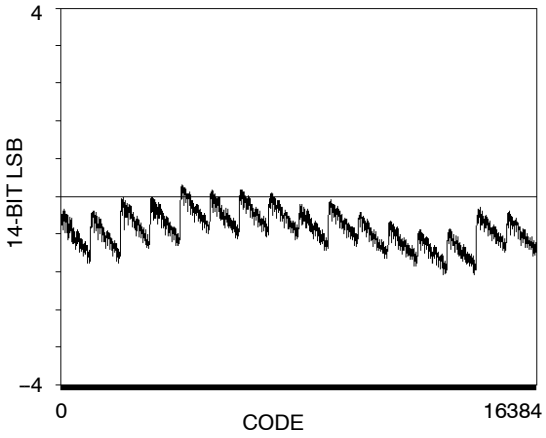
Graph 2. Linearity with
V_{REF} = 5 V, All DACs, All Codes



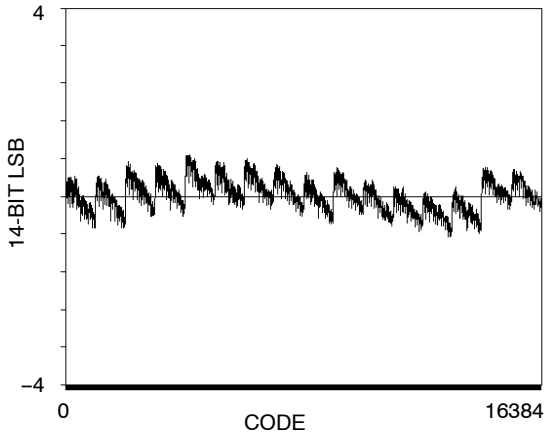
Graph 3. DAC 0 INL vs. V_{REF}



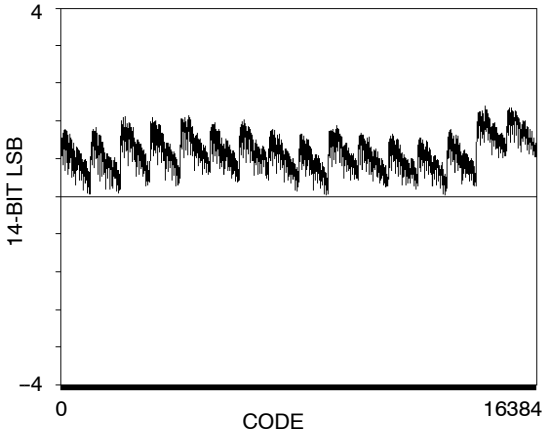
Graph 4. DAC 0 DNL vs. V_{REF}



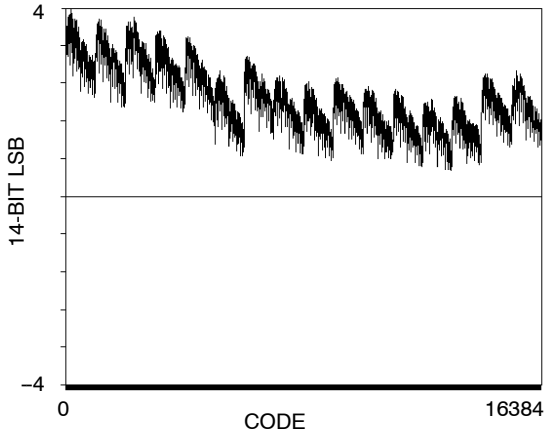
Graph 5. DAC 0 Linearity with V_{REF} = 5 V, V_{OUT} = ±10



Graph 6. DAC 0 Linearity with V_{REF} = 4.5 V, V_{OUT} = ±9



Graph 7. DAC 0 Linearity with V_{REF} = 4 V, V_{OUT} = ±8



Graph 8. DAC 0 Linearity with V_{REF} = 3.5 V, V_{OUT} = ±7

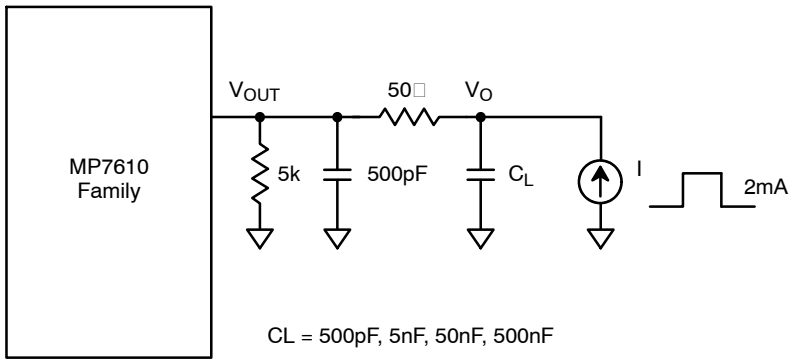
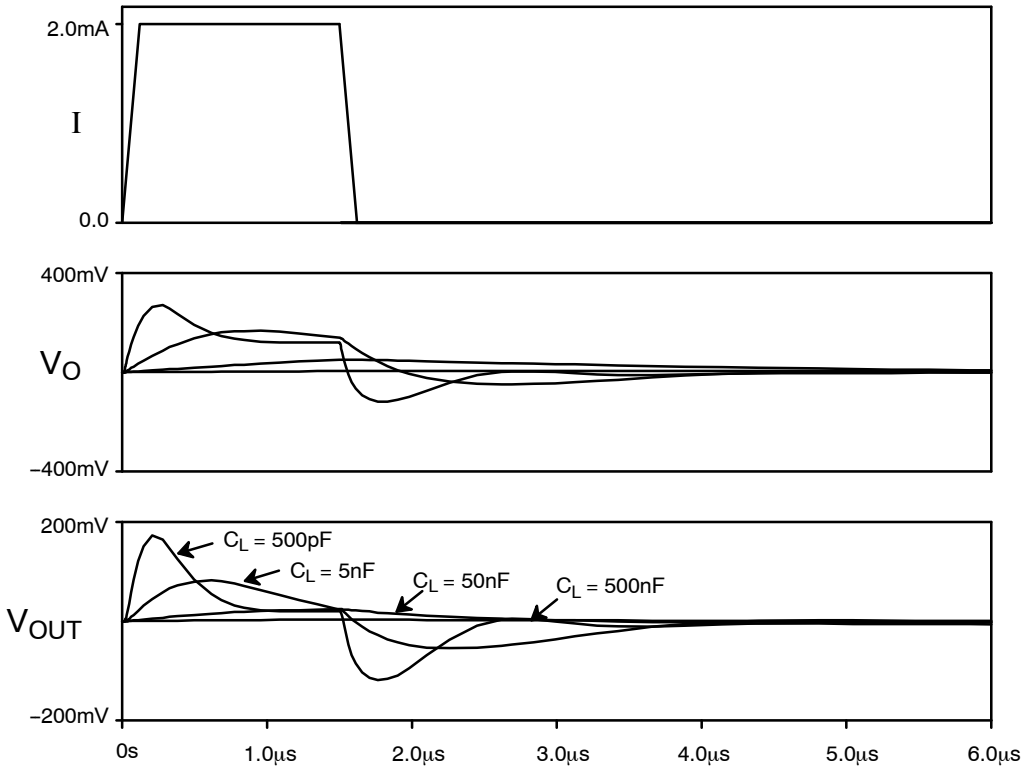


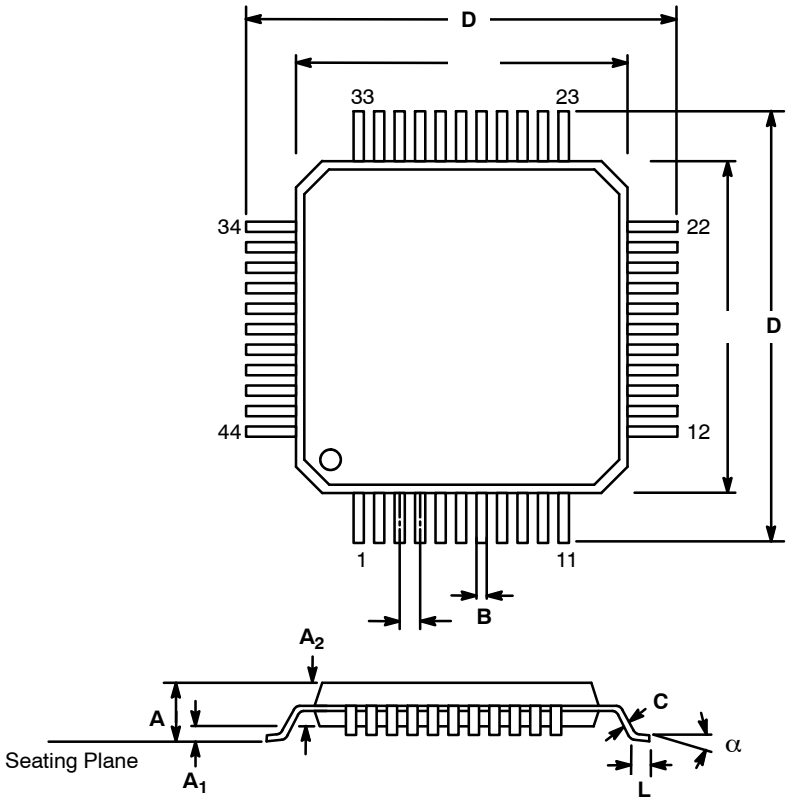
Figure 6. Circuit for Determining Typical Analog Output Pulse Response



Graph 9. Typical Response of the MP7610 Family Analog Output to a Current Pulse with CL=500pF, 5nF, 50nF, 500nF (*See Figure 9. above*)

44 LEAD PLASTIC QUAD FLAT PACK
(14 mm x 14 mm QFP)

Rev. 1.00

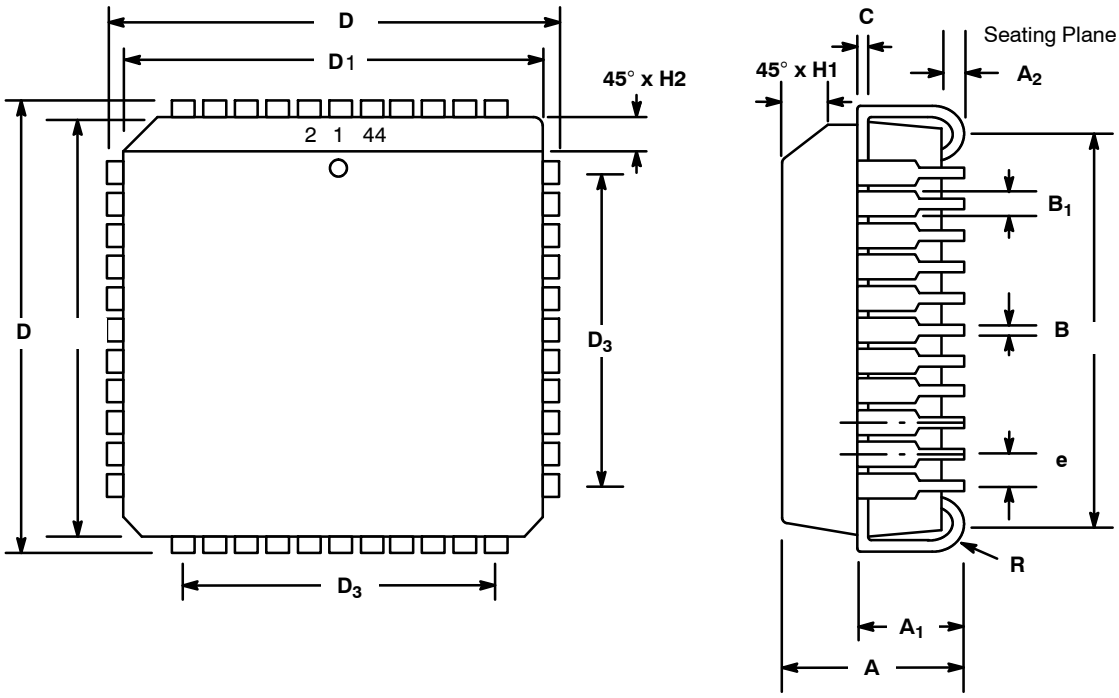


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.110	0.134	2.80	3.40
A_1	0.010	0.014	0.25	0.35
A_2	0.100	0.120	2.55	3.05
B	0.014	0.020	0.35	0.50
C	0.005	0.009	0.13	0.23
D	0.667	0.687	16.95	17.45
D_1	0.547	0.555	13.90	14.10
e	0.039 BSC		1.00 BSC	
L	0.026	0.37	0.65	0.95
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

44 LEAD PLASTIC LEADED CHIP CARRIER (PLCC)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A_1	0.090	0.120	2.29	3.05
A_2	0.020	–––.	0.51	–––
B	0.013	0.021	0.33	0.53
B_1	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.685	0.695	17.40	17.65
D_1	0.650	0.656	16.51	16.66
D_2	0.590	0.630	14.99	16.00
D_3	0.500 typ.		12.70 typ.	
e	0.050 BSC		1.27 BSC	
H1	0.042	0.056	1.07	1.42
H2	0.042	0.048	1.07	1.22
R	0.025	0.045	0.64	1.14

Note: The control dimension is the inch column

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