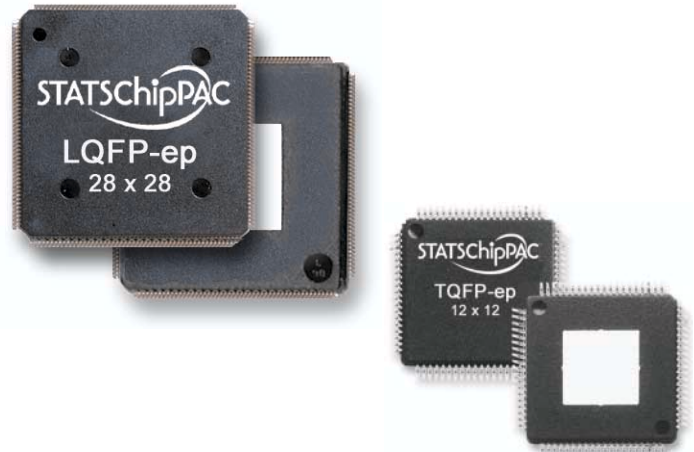


QFP-ep

Exposed Pad Quad Flat Pack

- 7 x 7mm to 24 x 24mm body sizes
- 32 to 216 lead count
- Lead pitch range from 0.80mm to 0.40mm



FEATURES

- Body Sizes: 7 x 7mm to 24 x 24mm
- Package Height: 1.0mm (TQFP-ep) and 1.4mm (LQFP-ep)
- Lead Counts: 32L to 216L
- Lead Pitch: 0.40mm to 0.80mm
- Wide range of open tool leadframe and die pad sizes available
- JEDEC standard compliant
- Lead-free and Green material sets available

APPLICATIONS

- ASIC
- DSP
- Gate Array
- Logic, Microprocessors/Controllers
- Multimedia, PC Chipsets, Others

DESCRIPTION

STATS ChipPAC's Exposed Pad Quad Flat Pack (QFP-ep) is a thermally enhanced version of the QFP package. Thermal enhancement is achieved by means of an exposed die pad, which can be soldered to a mother PC board for effective heat removal and grounding. STATS ChipPAC's QFP-ep family includes the Exposed Pad-Low Profile QFP (LQFP-ep) and the Exposed Pad-Thin QFP (TQFP-ep). These enhanced thermal packages are made possible by deep downset die pad leadframe design combined with well controlled low loop wirebonding and package warpage control during the molding process.

QFP-ep

Exposed Pad Quad Flat Pack

SPECIFICATIONS

| | |
|-----------------|--|
| Die Thickness | 304-482 μ m (12-19mils) range preferred |
| Gold Wire | 25/30 μ m (1.0/1.2mils) diameter, 99.999% Au |
| Lead Finish | 85/15 Sn/Pb or Matte Tin |
| Marking | Laser/ink |
| Packing Options | JEDEC tray/tape and reel |

RELIABILITY

| | |
|----------------------------|----------------------------------|
| Moisture Sensitivity Level | JEDEC Level 3 |
| Temperature Cycling | -65°C/150°C, 1000 cycles |
| High Temperature Storage | 150°C, 500 hrs |
| Pressure Cooker Test | 121°C 100% RH, 2 atm, 168 hrs |
| Liquid Thermal Shock (opt) | -55°C/125°C, 1000 cycles |

THERMAL PERFORMANCE, θ_{ja} (°C/W)

| Package | Body Size (mm) | Pad Size (mm) | Die Size (mm) | PCB Vias | Thermal Performance, θ_{ja} (°C/W) |
|---------|----------------|---------------|---------------|----------|---|
| 48L | 7 x 7 x 1.0 | 5.5 x 5.5 | 5.3 x 5.3 | 25 | 26.9 |
| 64L | 10 x 10 x 1.0 | 6.5 x 6.5 | 6.0 x 6.0 | 36 | 24.0 |
| 80L | 12 x 12 x 1.0 | 7.2 x 7.2 | 6.0 x 6.0 | 36 | 23.0 |

Note: Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-7) under natural convection as defined in JESD51-2.

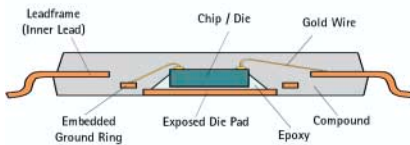
ELECTRICAL PERFORMANCE

Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. Data below is for a frequency of 100MHz and assumes 1.0 mil gold bonding wire.

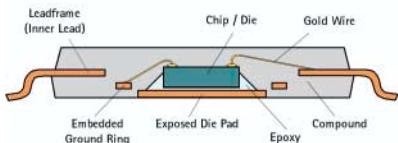
| Conductor Component | Length (mm) | Resistance (mOhms) | Inductance (nH) | Inductance Mutual (nH) | Capacitance (pF) | Capacitance Mutual (pF) |
|-------------------------|-------------|--------------------|-----------------|------------------------|------------------|-------------------------|
| Wire | 2 | 120 | 1.65 | 0.45 - 0.85 | 0.10 | 0.01 - 0.02 |
| Lead (14 x 14mm, 100L) | 4.4 - 5.9 | 30.5 - 41.4 | 1.52 - 2.07 | 0.70 - 0.93 | 0.70 - 0.95 | 0.39 - 0.52 |
| Total (14 x 14mm, 100L) | | 150.5 - 161.4 | 3.17 - 3.72 | 1.15 - 1.78 | 0.8 - 1.05 | 0.4 - 0.54 |
| Wire | 2 | 120 | 1.65 | 0.45 - 0.85 | 0.10 | 0.01 - 0.02 |
| Lead (20 x 20mm, 144L) | 4.2 - 6.1 | 29.3 - 42.8 | 1.47 - 2.14 | 0.68 - 0.98 | 0.75 - 1.10 | 0.44 - 0.65 |
| Total (20 x 20mm, 144L) | | 149.3 - 162.8 | 3.12 - 3.79 | 1.13 - 1.83 | 0.85 - 1.20 | 0.45 - 0.67 |

CROSS-SECTION

TQFP-ep



LQFP-ep



PACKAGE CONFIGURATIONS

| | Package Size | Lead Count | | | |
|---------|---------------|------------|--------|--------|--------|
| | | 0.80mm | 0.65mm | 0.50mm | 0.40mm |
| TQFP-ep | 7 x 7 x 1.0 | 32 | - | 48 | - |
| | 10 x 10 x 1.0 | 44, 48 | 52 | 64 | - |
| | 12 x 12 x 1.0 | 52 | 64 | 80 | 100 |
| | 14 x 14 x 1.0 | 64 | 80 | 100 | - |
| LQFP-ep | 10 x 10 x 1.4 | - | - | 64 | - |
| | 14 x 14 x 1.4 | 64 | 80 | 100 | - |
| | 20 x 20 x 1.4 | 96 | 128 | 144 | 164 |
| | 24 x 24 x 1.4 | - | - | - | 216 |

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